ESS Technology, Inc.

ES3210
Video CD Processor
Product Brief

DESCRIPTION

The ES3210 Video CD processor is a highly integrated, high quality and cost-effective single-chip solution for Video CD players. Based upon ESS's Programmable Multimedia Processor (PMP) architecture, the ES3210 integrates MPEG1 video and audio processing and a full MPEG system stream parser. The ES3210 is fully programmable and incorporates a RISC-based 32-bit processor as an on-chip video controller (VC) and a supporting 64-bit processor core that functions as an on-chip video processor (VP).

The VC module can be used as a microcontroller to provide system and user interface controls, while also being able to support embedded systems applications. The VP module performs MPEG audio and video processing operations such as arbitrary scaling, video standards conversion and video filtering. The MPEG1 system layer bitstream is decoded at up to 9 Mb/s at Standard Intermediate Format (SIF) resolution with a picture rate of 30 f/s. Two channels of MPEG layer 1 or audio layer 2 are decoded simultaneously.

The ES3210 includes SmartScale™ technology for advanced scaling techniques, SmartStream™ technology for video error concealment, and SmartZoom™ technology for enabling in/out zooming of a particular area of a still picture. Additional features include DiscScan, TrackScan, QuickScan, On-Screen-Display (OSD), Karaoke, Playback Control (PBC) for Video CD 2.0, Smart Art and entertainment game software.

The incoming MPEG1 bit stream from a video CD is passed to the ES3210 through its five-wire TDM serial bus, parses the system layer and demultiplexes the video and audio channels. Video is decoded and output as YUV or RGB digital pixels to an NTSC or PAL video DAC/encoder, then to the screen. Audio is decoded and passed to the speakers via the audio serial bus, then to an audio DAC. The ES3210 also has general-purpose auxiliary pins and an integrated audio Digital-to-Analog Converter (DAC) interface to reduce the need for external audio glue logic.

When coupled with the ES3207 Video CD Companion Chip, echo cancellation and vocal reverb are also supported. The echo cancellation feature removes unwanted acoustic reflection from the audio output, while the vocal reverb feature simulates a theater acoustic environment.

The ES3210 is available in an industry-standard 100-pin Thin Quad Flat Pack (TQFP) device package.

FEATURES

- Single-chip Video CD processor in a 100-pin TQFP package.
- Programmable Multimedia Processor (PMP) architecture.
- MPEG1 video/audio decoder and system parser.
- Video CD 1.1 and 2.0, and Audio CD compatible.
- On-chip video interlacing hardware incorporated.
- Color Space Conversion (CSC) function supported.
- STC interpretation and video/audio Phase-lock Loop (PLL)
- Power management
- 3.3V power supply with 5V tolerant I/Os.
- 8- and 16-bit YUV output supported.
- On-chip On Screen Display (OSD) controller supports karaoke lyric and subtitle text display functions.

Video

- Playback Control (PBC) for Video CD 2.0 supported.
- Trick mode functions such as Repeat, Goto, and Set A-B supported.
- SmartScale™ for NTSC to PAL conversion and vice versa supported.
- SmartZoom™ for motion zoom and pan supported.
- SmartStream™ for video error concealment supported.
- Video Fader for fading video image in and out supported.

Audio

- CD block decoder functions supported.
- 256/384 frame sync audio system clocks supported.
- Programmable master clock for external audio DAC.
- Independent bit clock for audio transmit and receive.
- 3DSound and surround sound supported.

Software Support

- Software stack support for the TCP/IP protocols defined by RFC 791 and RFC 793.
- Software stack support for the POP3, SMTP and SNMP Internet e-mail protocols defined by RFC 821, RFC 1157and RFC 2449.
- Software stack support provided for the HTTP Web browsing protocol defined by RFC 1945, RFC 2068 and RFC2616.
- Software stack support provided for RTP payload format for MPEG-1/2 and H.261 video streaming protocols defined by Character generation and software support for English, Big 5/GB Chinese and Japanese fonts.
- Software support for infrared remote control and wireless keyboard.

ES3210 PINOUT

Figure 1 shows the ES3210 device pinout.

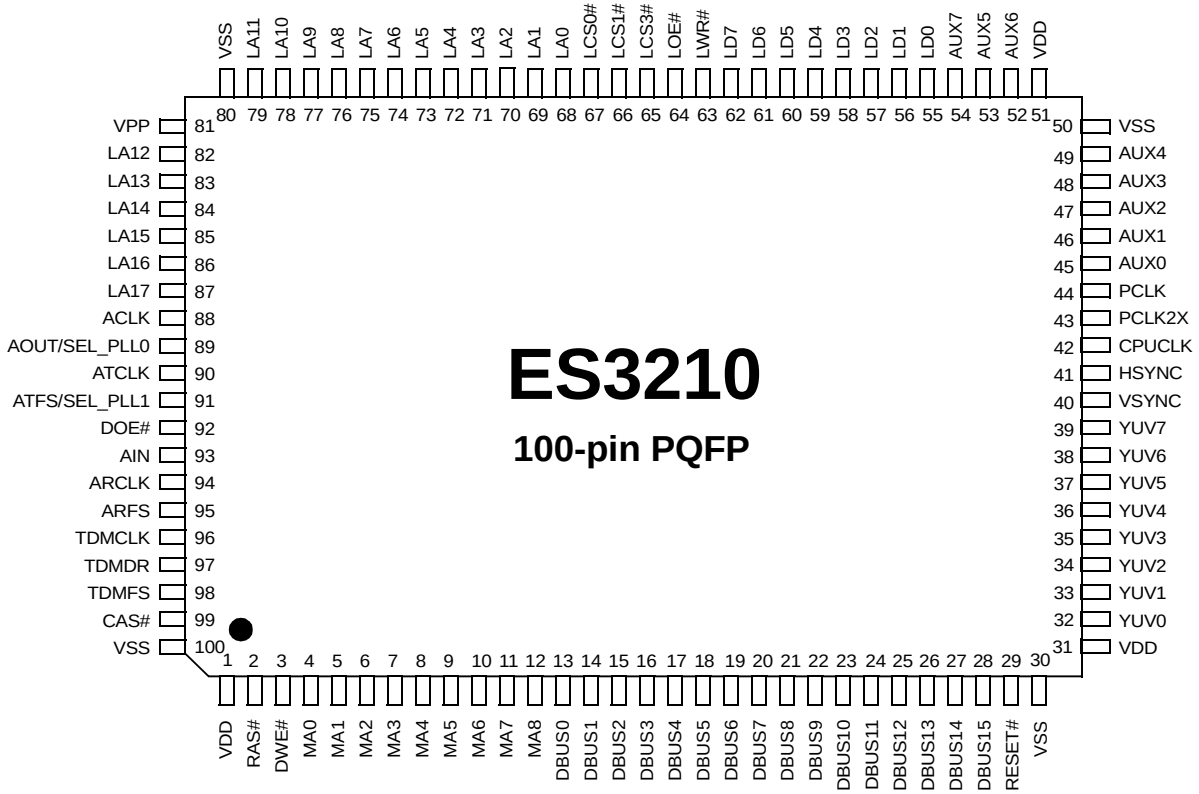


Figure 1 ES3210 Pinout Diagram

ES3210 PIN DESCRIPTION

Table 1 lists the ES3210 pin descriptions.

Table 1 ES3210 Pin Description

Name	Number	I/O	Definition
VDD	1, 31, 51	I	Voltage supply for 3.3V.
RAS#	2	O	DRAM row address strobe (active low).
DWE#	3	O	DRAM write enable (active low).
MA[8:0]	12:4	O	DRAM multiplexed row and column address bus.
DBUS[15:0]	28:13	I/O	DRAM data bus I/O [15:0].
RESET#	29	I	System reset (active low).
VSS	30, 50, 80, 100	I	Ground.
YUV[7:0]	39:32	O	YUV[7:0] pixel output data.
VSYNC	40	I/O	Vertical sync for screen video interface, programmable for rising or falling edge.
HSYNC	41	I/O	Horizontal sync for screen video interface, programmable for rising or falling edge.
CPUCLK	42	I	RISC and system clock input. CPUCLK is used only if SEL_PLL[1:0] = 00.
PCLK2X	43	I/O	Pixel clock; two times the actual pixel clock for screen video interface.

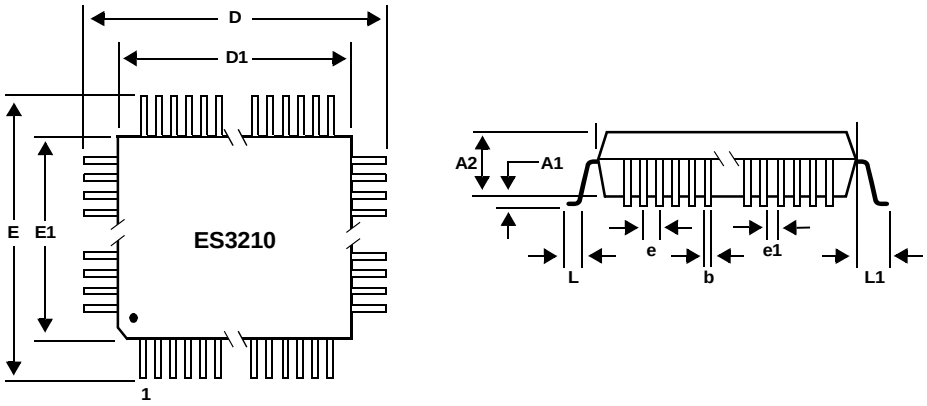
Table 1 ES3210 Pin Description (Continued)

Name	Number	I/O	Definition
PCLK	44	I/O	Pixel clock qualifier in for screen video interface.
AUX[7:0]	54:52, 49:45	I/O	Auxiliary control pins (AUX0 and AUX1 are open collectors).
LD[7:0]	62:55	I/O	RISC interface data bus.
LWR#	63	O	RISC interface write enable (active low).
LOE#	64	O	RISC interface output enable (active low).
LCS[3,1,0]#	65:67	O	RISC interface chip select (active low).
LA[17:0]	87:82, 79:68	O	RISC interface address bus.
VPP	81	I	Digital supply voltage for 5V.
ACLK	88	I/O	Master clock for external audio DAC (8.192 MHz, 11.2896 MHz, 12.288 MHz, 16.9344 MHz, and 18.432 MHz).
AOUT/	89	O	Dual-purpose pin. AOUT is the audio interface serial data output
SEL_PLL0		I	Select PLL[0] input. The matrix below lists the available clock frequencies and their respective PLL bit settings.
ATCLK	90	I/O	Audio transmit bit clock.
ATFS	91	O	Audio transmit frame sync.
SEL_PLL1		I	Refer to the description and matrix for SEL_PLL0 pin 89.
DOE#	92	O	DRAM output enable (active low).
AIN	93	I	Audio serial data input.
ARCLK	94	I	Audio receive bit clock.
ARFS	95	I	Audio receive frame sync.
TDMCLK	96	I	TDM interface serial clock.
TDMDR	97	I	TDM interface serial data receive.
TDMFS	98	I	TDM interface frame sync.
CAS#	99	O	DRAM column address strobe bank 0 (active low).

SEL_PLL1	SEL_PLL0	Clock Output
0	0	Bypass PLL
0	1	54.0 MHz
1	0	67.5 MHz
1	1	81.0 MHz

MECHANICAL DIMENSIONS

Figure 2 shows the mechanical dimensions of the ES3210 package.



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	23.65	23.90	24.15
D1	Package's outside, X-axis	19.90	20.00	20.10
E	Lead to lead, Y-axis	17.65	17.90	18.15
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.10	0.25	0.36
A2	Package thickness	2.57	2.71	2.87
b	Lead width	0.20	0.30	0.40
e	Lead pitch	-	0.65	-
e1	Lead gap	0.24	-	-
L	Foot length	0.65	0.80	0.95
L1	Lead length	1.88	1.95	2.02
-	Foot angle	0°	-	7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	30	-
-	Leads in Y-axis	-	20	-
-	Total leads	-	100	-
-	Package type	-	PQFP	-

Figure 2 ES3210 Mechanical Dimensions

ORDERING INFORMATION

Part Number	Description	Package
ES3210	Video CD processor	100-pin PQFP

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