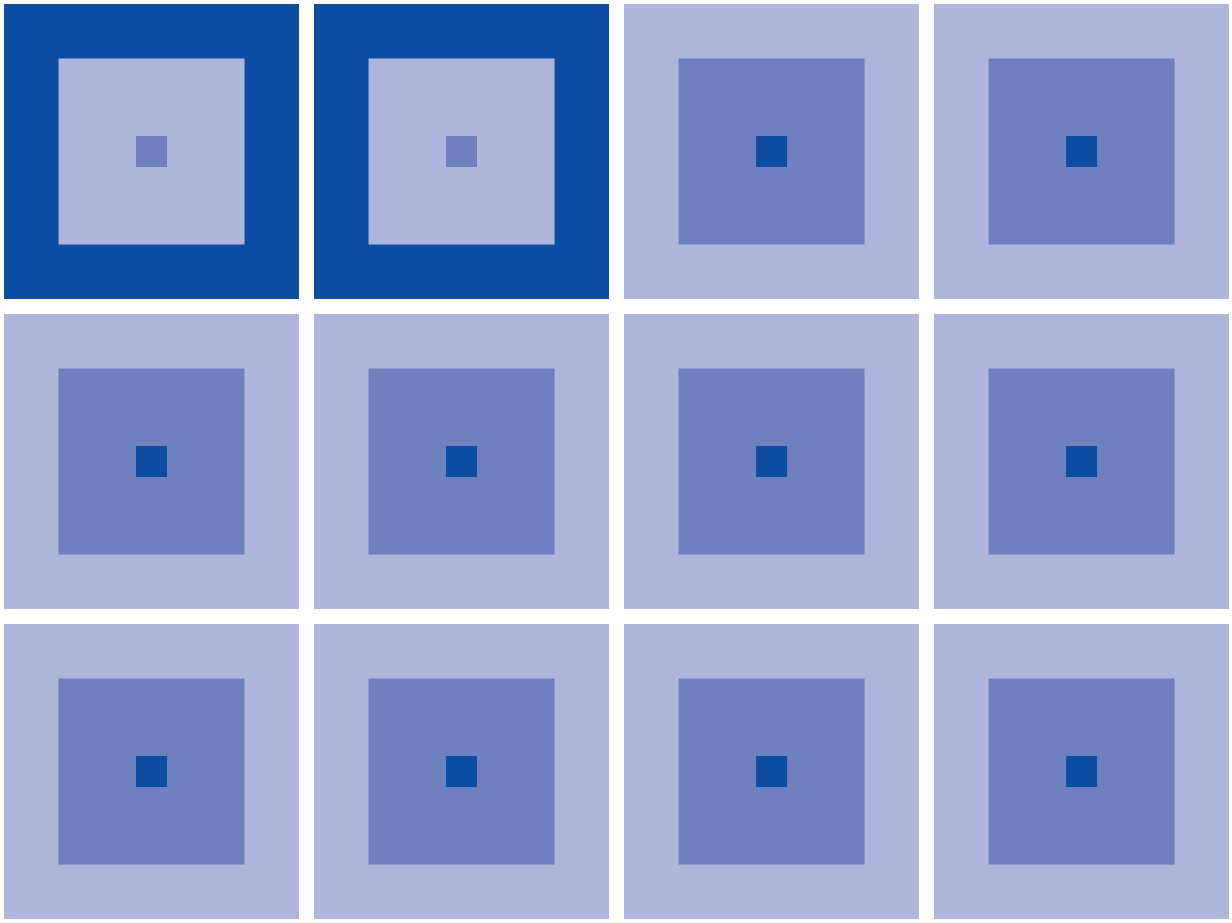
MF652-07

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C62440/624A0/624C0/62480 Technical Manual

S1C62440/624A0/624C0/62480 Technical Hardware
S1C62440/624A0/624C0/62480 Technical Software



SEIKO EPSON CORPORATION

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PREFACE

This manual is individualy described about the hardware and the software of the S1C62440/624A0/624C0/62480.

I. S1C62440/624A0/624C0/62480 Technical Hardware

This part explains the function of the S1C62440/624A0/624C0/62480, the circuit configurations, and details the controlling method.

II. S1C62440/624A0/624C0/62480 Technical Software

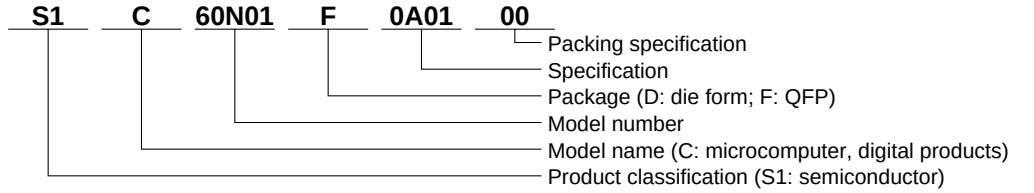
This part explains the programming method of the S1C62440/624A0/624C0/62480.

The information of the product number change

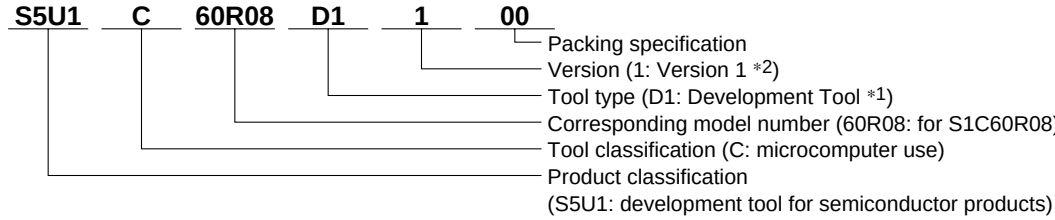
Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices



Development tools



*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.
E0C621A	S1C621A0
E0C6215	S1C62150
E0C621C	S1C621C0
E0C6S27	S1C6S2N7
E0C6S37	S1C6S3N7
E0C623A	S1C6N3A0
E0C623E	S1C6N3E0
E0C6S32	S1C6S3N2
E0C6233	S1C62N33
E0C6235	S1C62N35
E0C623B	S1C6N3B0
E0C6244	S1C62440
E0C624A	S1C624A0
E0C6S46	S1C6S460

Previous No.	New No.
E0C6247	S1C62470
E0C6248	S1C62480
E0C6S48	S1C6S480
E0C624C	S1C624C0
E0C6251	S1C62N51
E0C6256	S1C62560
E0C6292	S1C62920
E0C6262	S1C62N62
E0C6266	S1C62660
E0C6274	S1C62740
E0C6281	S1C62N81
E0C6282	S1C62N82
E0C62M2	S1C62M20
E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.
ASM62	S5U1C62000A
DEV6001	S5U1C60N01D
DEV6002	S5U1C60N02D
DEV6003	S5U1C60N03D
DEV6004	S5U1C60N04D
DEV6005	S5U1C60N05D
DEV6006	S5U1C60N06D
DEV6007	S5U1C60N07D
DEV6008	S5U1C60N08D
DEV6009	S5U1C60N09D
DEV6011	S5U1C60N11D
DEV60R08	S5U1C60R08D
DEV621A	S5U1C621A0D
DEV621C	S5U1C621C0D
DEV623B	S5U1C623B0D
DEV6244	S5U1C62440D
DEV624A	S5U1C624A0D
DEV624C	S5U1C624C0D
DEV6248	S5U1C62480D
DEV6247	S5U1C62470D

Previous No.	New No.
DEV6262	S5U1C62620D
DEV6266	S5U1C62660D
DEV6274	S5U1C62740D
DEV6292	S5U1C62920D
DEV62M2	S5U1C62M20D
DEV6233	S5U1C62N33D
DEV6235	S5U1C62N35D
DEV6251	S5U1C62N51D
DEV6256	S5U1C62560D
DEV6281	S5U1C62N81D
DEV6282	S5U1C62N82D
DEV6S27	S5U1C6S2N7D
DEV6S32	S5U1C6S3N2D
DEV6S37	S5U1C6S3N7D
EVA6008	S5U1C60N08E
EVA6011	S5U1C60N11E
EVA621AR	S5U1C621A0E2
EVA621C	S5U1C621C0E
EVA6237	S5U1C62N37E
EVA623A	S5U1C623A0E

Previous No.	New No.
EVA623B	S5U1C623B0E
EVA623E	S5U1C623E0E
EVA6247	S5U1C62470E
EVA6248	S5U1C62480E
EVA6251R	S5U1C62N51E1
EVA6256	S5U1C62N56E
EVA6262	S5U1C62620E
EVA6266	S5U1C62660E
EVA6274	S5U1C62740E
EVA6281	S5U1C62N81E
EVA6282	S5U1C62N82E
EVA62M1	S5U1C62M10E
EVA62T3	S5U1C62T30E
EVA6S27	S5U1C6S2N7E
EVA6S32R	S5U1C6S3N2E2
ICE62R	S5U1C62000H
KIT6003	S5U1C60N03K
KIT6004	S5U1C60N04K
KIT6007	S5U1C60N07K

I. S1C62440/624A0/624C0/62480 Technical Hardware

CONTENTS

Hardware

CHAPTER 1 INTRODUCTION

The S1C62440/4A0/4C0/480 are a microcomputer with a C-MOS 4-bit core CPU S1C6200 as main component, and ROM, RAM, dot matrix LCD driver, time base counter, clock synchronous serial interface, etc. built-in.
Moreover, in the S1C624A0/4C0/480 external memory device control is possible, and are most suitable for applications with equipment requiring large memory and dot matrix display functions such as a highly functional electronic pocketbook.

Table 1.1 Configuration of the S1C62440/4A0/4C0/480

Model	ROM capacity	RAM capacity	Number of segment pins	External memory control
S1C62440	4,096 words	384 words	40	Not used
S1C624A0	6,144 words	640 words	40	Used
S1C624C0	5,120 words	1,152 words	51	Used
S1C62480	8,192 words	768 words	51	Used

1.1 Features

Table 1.1.1 Features

		S1C62480	S1C624C0	S1C624A0	S1C62440H
Power voltage		2.2 to 5.5 V (Min. 1.8 V, when OSC3 oscillation circuit is not used)			
Built-in oscillation circuit	OSC1 oscillation circuit:	Crystal or CR oscillation (*1) 32,768 Hz (Typ.)	Crystal or CR oscillation (*1) 32,768 Hz (Typ.)	Crystal oscillation 32,768 Hz (Typ.)	Crystal or CR oscillation (*1) 32,768 Hz (Typ.)
	OSC3 oscillation circuit:	CR or ceramic oscillation (*1) 2 MHz (Max.)			
Instruction set		108 types			
Program memory (ROM) capacity		8,192 words × 12 bits	5,120 words × 12 bits	6,144 words × 12 bits	4,096 words × 12 bits
Data memory (RAM) capacity	RAM:	768 words × 4 bits	1,152 words × 4 bits	640 words × 4 bits	384 words × 4 bits
	Segment data memory:	204 words × 4 bits	204 words × 4 bits	160 words × 4 bits	160 words × 4 bits
External memory capacity		Read/write capacity: max. 64K bits × 4 (*2) Read-only capacity: max. 128K bits × 4 (*2)			———
Input ports		8 bits (pull up resistors may be supplemented *1)			
Output ports		Max. 20 bits (*3, *5)			12 bits (*5)
Input/output ports		Max. 16 bits (*4)			12 bits
Serial interface		1 port (8 bits serial, synchronous type clock)			
Dot matrix LCD driver		51 segments × 16 common duty (or 8 common duty)		40 segments × 16 common duty (or 8 common duty)	
Time base counter		3 systems (clock timer / stopwatch timer / programmable timer)			
Watchdog timer		built-in			
Sound generator		8 programmable sounds (8 types of frequency); built-in digital envelope 1-shot output function			
Supply voltage detection (SVD)		-2.2 / -2.5 / -3.1 / -4.2 V, programmable (V_{DD} reference voltage)			
Interrupt	External interrupt:	Input port interrupt 2 systems			
	Internal interrupt:	Time base counter interrupt 3 systems Serial interface interrupt 1 system			
Consumed current (Typ.)	CLK = 32,768 Hz (During HALT)	2.5 µA (Typ.)	2.5 µA (Typ.)	2.5 µA (Typ.)	2.5 µA (Typ.)
	CLK = 32,768 Hz (During operation)	6.5 µA (Typ.)	6.5 µA (Typ.)	6.5 µA (Typ.)	6.5 µA (Typ.)
	CLK = 2 MHz (During operation)	1 mA (Typ.)	1 mA (Typ.)	1 mA (Typ.)	1 mA (Typ.)
Supply form		144-pin QFP (plastic) or chip		128-pin QFP (plastic) or chip	

*1: May be selected with mask option

*2: When the output port and input/output port are set through mask option selection as external memory access

*3: Maximum number that may be set as output port (when external memory is not used)

*4: Maximum number that may be set as input/output port (when external memory is not used)

*5: BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, $\overline{SRDY}$, PTCLK, CL, and FR outputs are possible through mask option selections

1.2 Block Diagram

The S1C62440/4A0/4C0/480 block diagrams are shown in Figures 1.2.1–1.2.4.

S1C62440

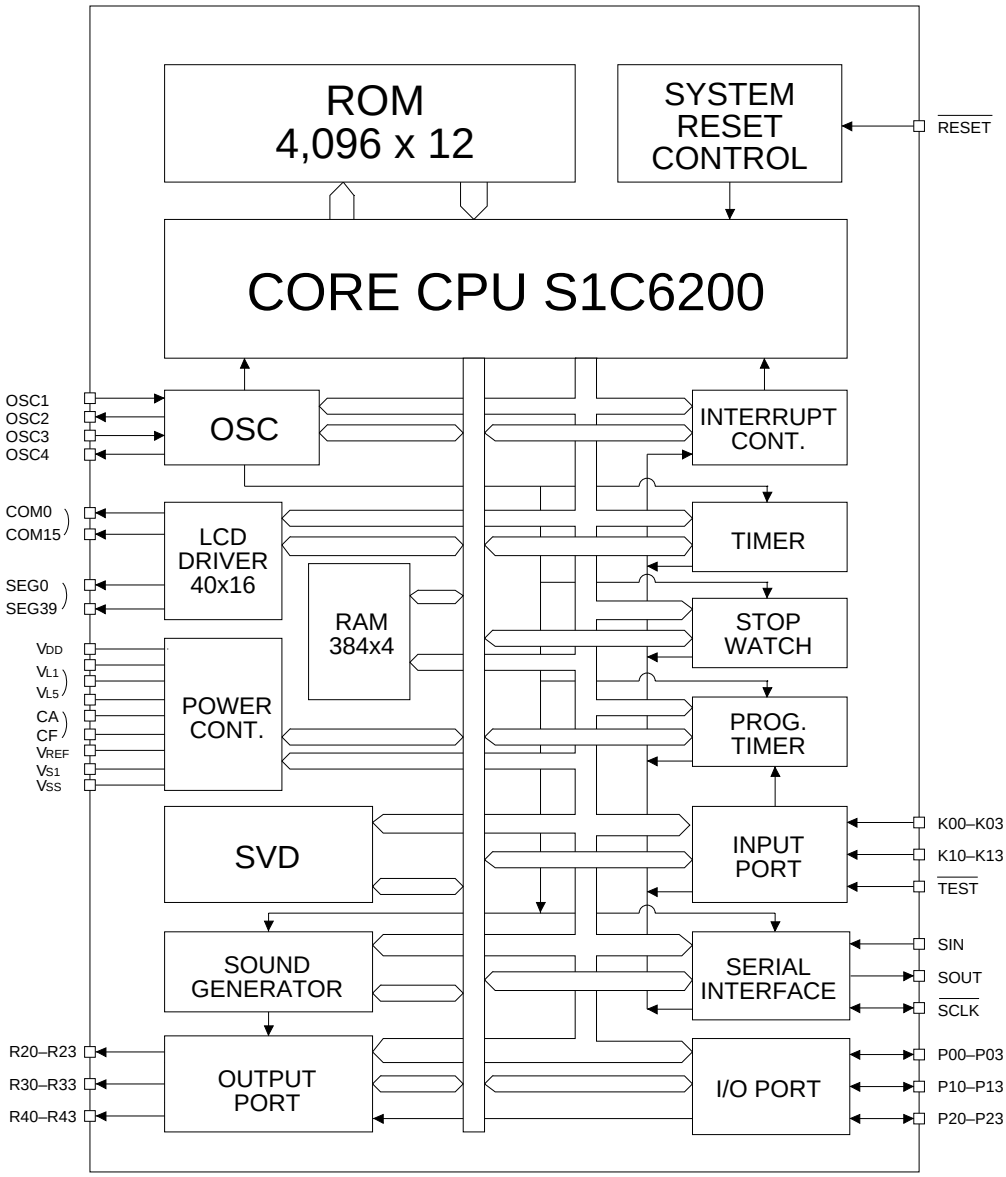


Fig. 1.2.1
S1C62440 block diagram

S1C624A0

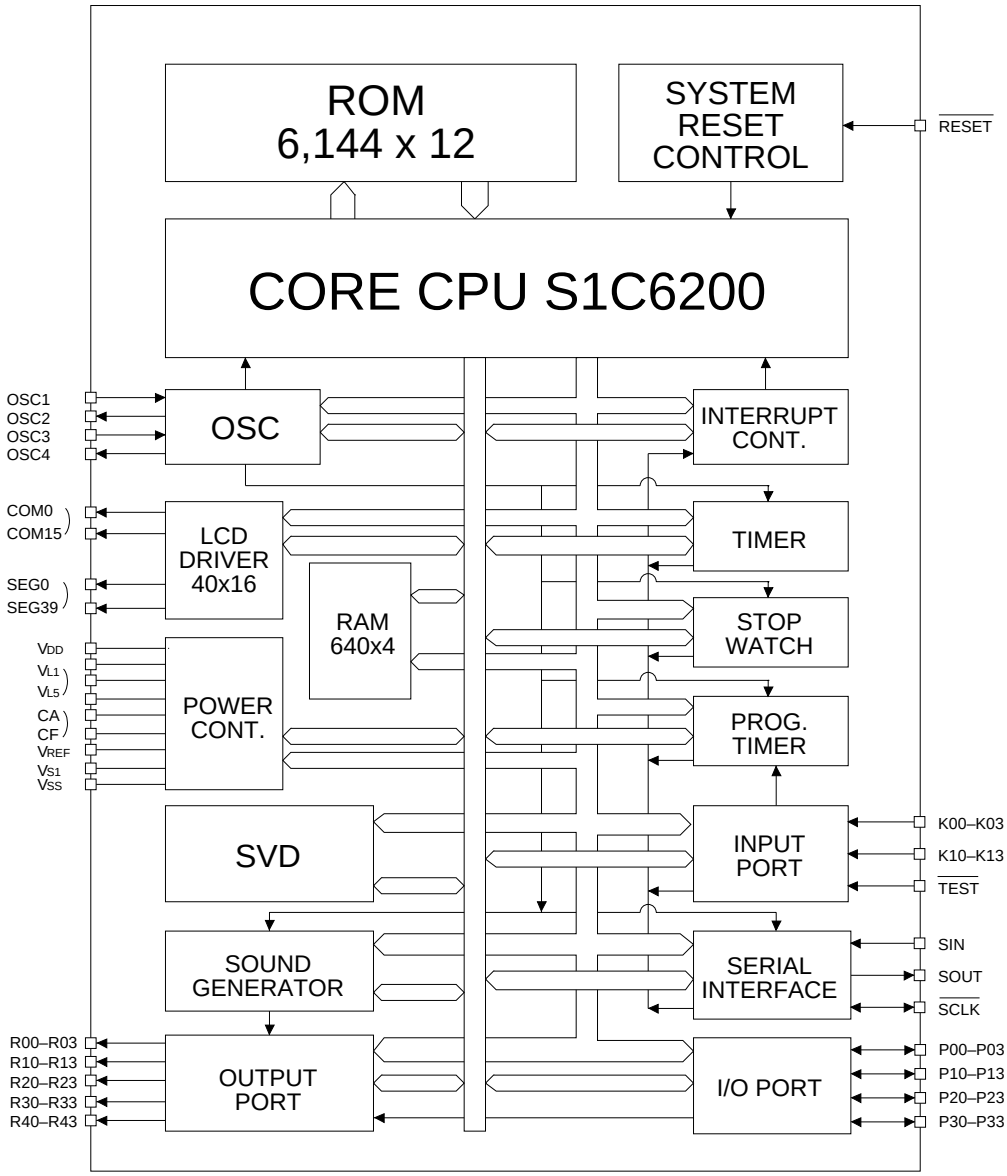


Fig. 1.2.2
S1C624A0 block diagram

S1C624C0

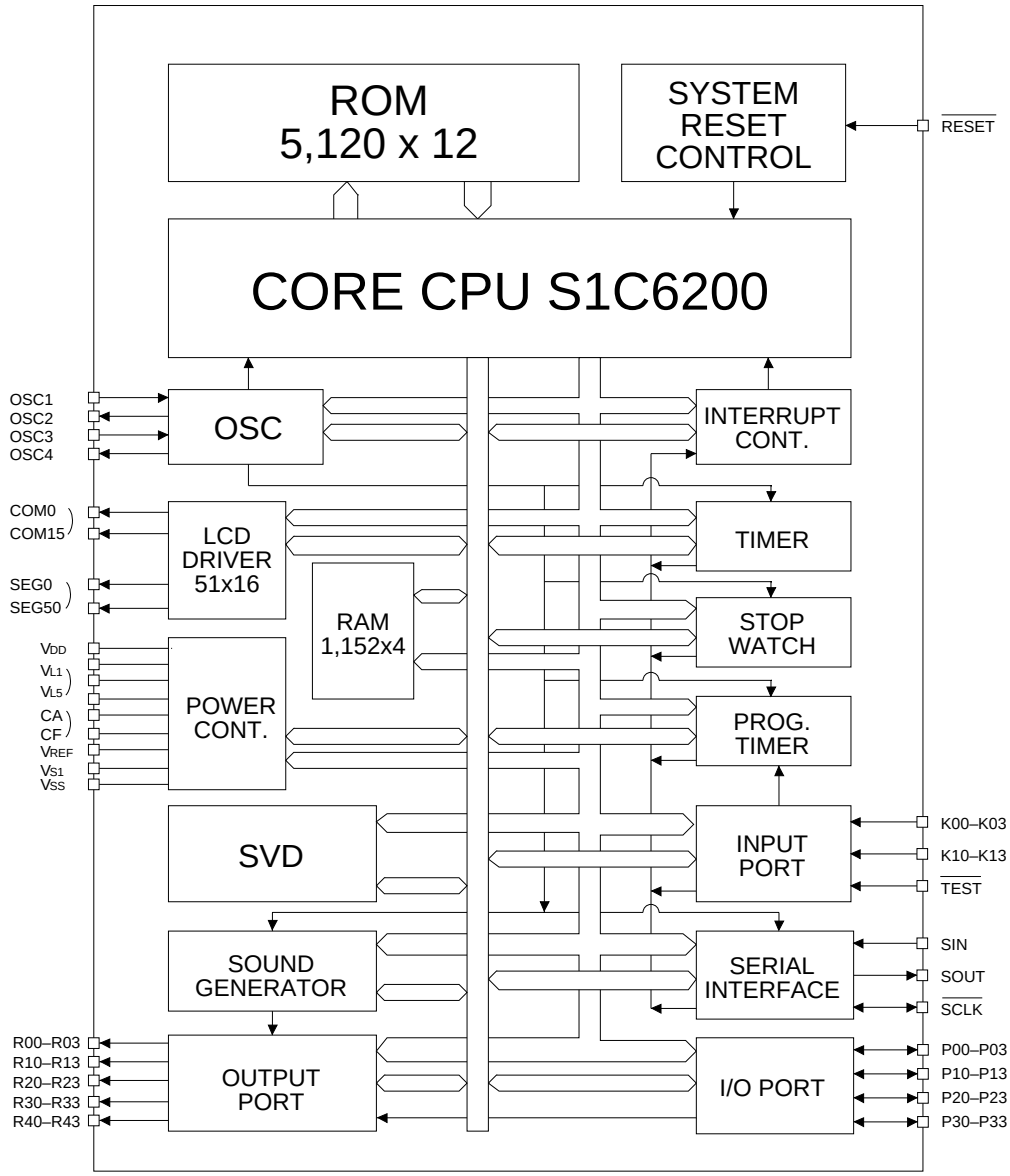


Fig. 1.2.3
S1C624C0 block diagram

S1C62480

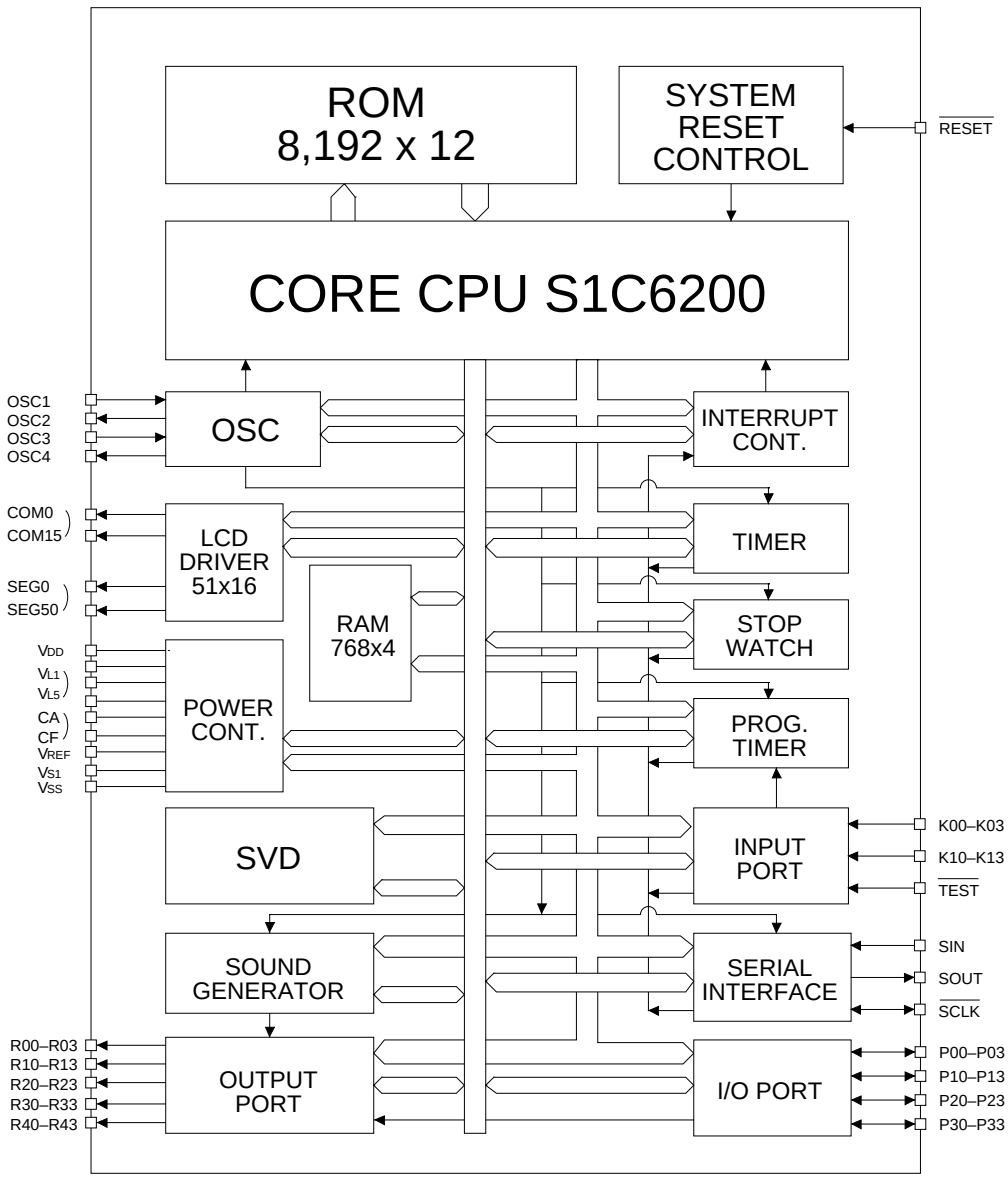
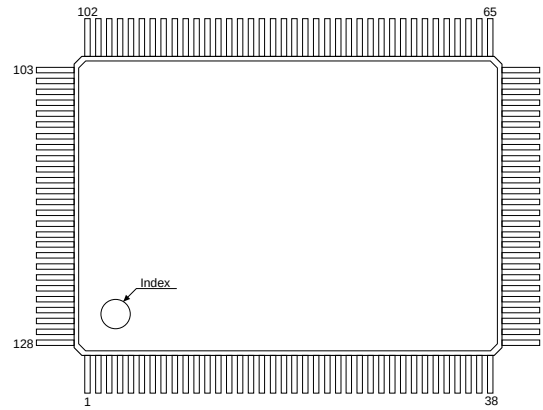


Fig. 1.2.4
S1C62480 block diagram

1.3 Pin Layout Diagram

S1C62440

QFP5-128 pin

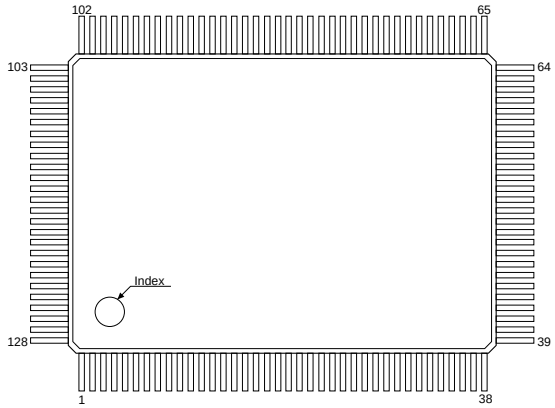


Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	N.C.	33	SEG30	65	SEG1	97	R40
2	CC	34	SEG29	66	N.C.	98	N.C.
3	N.C.	35	N.C.	67	SEG0	99	N.C.
4	CB	36	SEG28	68	N.C.	100	N.C.
5	CA	37	N.C.	69	N.C.	101	R33
6	N.C.	38	SEG27	70	$\overline{\text{SCLK}}$	102	R32
7	COM0	39	N.C.	71	SOUT	103	R31
8	COM1	40	SEG26	72	SIN	104	R30
9	COM2	41	SEG25	73	K13	105	R23
10	COM3	42	SEG24	74	K12	106	R22
11	COM4	43	SEG23	75	K11	107	R21
12	COM5	44	SEG22	76	K10	108	R20
13	COM6	45	SEG21	77	K03	109	V_{SS}
14	COM7	46	SEG20	78	K02	110	$\overline{\text{RESET}}$
15	COM8	47	SEG19	79	K01	111	$\overline{\text{TEST}}$
16	COM9	48	SEG18	80	K00	112	OSC4
17	COM10	49	SEG17	81	P23	113	OSC3
18	COM11	50	SEG16	82	P22	114	N.C.
19	COM12	51	SEG15	83	P21	115	V_{S1}
20	COM13	52	SEG14	84	P20	116	OSC2
21	COM14	53	SEG13	85	P13	117	OSC1
22	COM15	54	SEG12	86	P12	118	N.C.
23	N.C.	55	SEG11	87	P11	119	V_{DD}
24	SEG39	56	SEG10	88	P10	120	V_{REF}
25	SEG38	57	SEG9	89	P03	121	V_{L1}
26	SEG37	58	SEG8	90	P02	122	V_{L2}
27	SEG36	59	SEG7	91	P01	123	V_{L3}
28	SEG35	60	SEG6	92	P00	124	V_{L4}
29	SEG34	61	SEG5	93	R43	125	V_{L5}
30	SEG33	62	SEG4	94	R42	126	CF
31	SEG32	63	SEG3	95	N.C.	127	CE
32	SEG31	64	SEG2	96	R41	128	CD

Fig. 1.3.1
S1C62440 pin assignment

S1C624A0

QFP5-128 pin

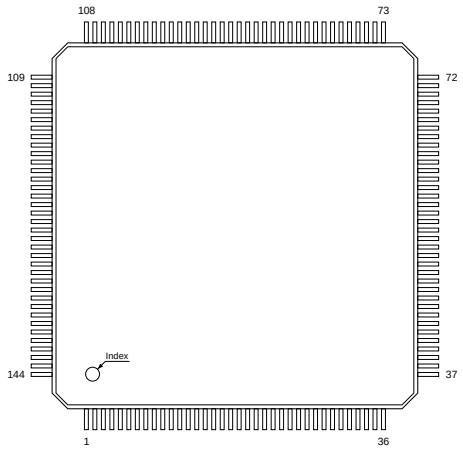


Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	V_{L3}	33	SEG33	65	SEG2	97	R42
2	V_{L4}	34	N.C.	66	SEG1	98	N.C.
3	V_{L5}	35	SEG32	67	SEG0	99	R41
4	CF	36	SEG31	68	$\overline{SCLK}$	100	R40
5	N.C.	37	SEG30	69	N.C.	101	R33
6	CE	38	SEG29	70	SOUT	102	R32
7	CD	39	SEG28	71	SIN	103	R31
8	CC	40	SEG27	72	K13	104	R30
9	CB	41	SEG26	73	K12	105	R23
10	CA	42	SEG25	74	K11	106	R22
11	COM0	43	SEG24	75	K10	107	R21
12	COM1	44	SEG23	76	K03	108	R20
13	COM2	45	SEG22	77	K02	109	R13
14	COM3	46	SEG21	78	K01	110	R12
15	COM4	47	SEG20	79	K00	111	R11
16	COM5	48	SEG19	80	P33	112	R10
17	COM6	49	SEG18	81	P32	113	R03
18	COM7	50	SEG17	82	P31	114	R02
19	COM8	51	SEG16	83	P30	115	R01
20	COM9	52	SEG15	84	P23	116	R00
21	COM10	53	SEG14	85	P22	117	V_{SS}
22	COM11	54	SEG13	86	P21	118	$\overline{RESET}$
23	COM12	55	SEG12	87	P20	119	$\overline{TEST}$
24	COM13	56	SEG11	88	P13	120	OSC4
25	COM14	57	SEG10	89	P12	121	OSC3
26	COM15	58	SEG9	90	P11	122	V_{S1}
27	SEG39	59	SEG8	91	P10	123	OSC2
28	SEG38	60	SEG7	92	P03	124	OSC1
29	SEG37	61	SEG6	93	P02	125	V_{DD}
30	SEG36	62	SEG5	94	P01	126	V_{REF}
31	SEG35	63	SEG4	95	P00	127	V_{L1}
32	SEG34	64	SEG3	96	R43	128	V_{L2}

Fig. 1.3.2
S1C624A0 pin assignment

S1C624C0/480

QFP8-144 pin



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	CB	37	SEG36	73	SEG1	109	R33
2	CA	38	SEG35	74	SEG0	110	R32
3	N.C.	39	SEG34	75	N.C.	111	R31
4	COM0	40	SEG33	76	$\overline{\text{SCLK}}$	112	R30
5	COM1	41	SEG32	77	SOUT	113	R23
6	COM2	42	SEG31	78	SIN	114	R22
7	COM3	43	SEG30	79	K13	115	R21
8	COM4	44	SEG29	80	K12	116	R20
9	COM5	45	SEG28	81	K11	117	R13
10	COM6	46	SEG27	82	K10	118	R12
11	COM7	47	SEG26	83	K03	119	R11
12	COM8	48	SEG25	84	N.C.	120	R10
13	COM9	49	SEG24	85	K02	121	R03
14	COM10	50	N.C.	86	K01	122	R02
15	COM11	51	SEG23	87	K00	123	R01
16	COM12	52	SEG22	88	P33	124	R00
17	COM13	53	SEG21	89	P32	125	V_{SS}
18	COM14	54	SEG20	90	P31	126	$\overline{\text{RESET}}$
19	N.C.	55	SEG19	91	P30	127	$\overline{\text{TEST}}$
20	COM15	56	SEG18	92	P23	128	OSC4
21	SEG50	57	SEG17	93	P22	129	OSC3
22	SEG49	58	SEG16	94	P21	130	V_{S1}
23	SEG48	59	SEG15	95	P20	131	OSC2
24	SEG47	60	SEG14	96	P13	132	OSC1
25	SEG46	61	SEG13	97	N.C.	133	N.C.
26	SEG45	62	SEG12	98	P12	134	V_{DD}
27	SEG44	63	SEG11	99	P11	135	V_{REF}
28	SEG43	64	SEG10	100	P10	136	V_{L1}
29	SEG42	65	SEG9	101	P03	137	V_{L2}
30	SEG41	66	SEG8	102	P02	138	V_{L3}
31	SEG40	67	SEG7	103	P01	139	V_{L4}
32	SEG39	68	SEG6	104	P00	140	V_{L5}
33	SEG38	69	SEG5	105	R43	141	CF
34	SEG37	70	SEG4	106	R42	142	CE
35	N.C.	71	SEG3	107	R41	143	CD
36	N.C.	72	SEG2	108	R40	144	CC

Fig. 1.3.3
S1C624C0/480 pin assignment

1.4 Pin Description

Table 1.4.1 Pin description

Pin Name	Pin No			In/Out	Function
	S1C62440	S1C624A0	S1C624C0/480		
V_{DD}	119	125	134	I	Power (+)
V_{SS}	109	117	125	I	Power (-)
V_{S1}	115	122	130	–	Internal logic system/oscillation system regulated voltage
V_{L1} –V_{L5}	121–125	127, 128 1–3	136–140	–	LCD system power 1/4 bias generated internally 1/5 bias generated externally (selected by mask option)
CA–CF	5, 4, 2 128–126	10–6, 4	2, 1 144–141	–	LCD system voltage booster condenser connecting terminal
OSC1	117	124	132	I	Crystal or CR (selected by mask option only for S1C62440/4C0/480) oscillator input terminal
OSC2	116	123	131	O	Crystal or CR (selected by mask option only for S1C62440/4C0/480) oscillator output terminal (C_D built-in)
OSC3	113	121	129	I	CR or ceramic oscillator input terminal (selected by mask option)
OSC4	112	120	128	O	CR or ceramic oscillator output terminal (selected by mask option)
COM0–15	7–22	11–26	4–18 20	O	LCD common output (1/8 duty or 1/16 duty is selected on software)
SEG0–39	67, 65–40 38, 36 34–24	67–35 33–27	74–51 49–37 34–32	O	LCD segment output
SEG40–50	–	–	31–21		
$\overline{\text{RESET}}$	110	118	126	I	Initial reset input terminal
$\overline{\text{TEST}}$	111	119	127	I	Testing input terminal
V_{REF}	120	126	135	O	LCD system power test terminal
K00–K03	80–77	79–76	87–85, 83	I	Input ports
K10–K13	76–73	75–72	82–79		(Use of pull up resistor is selected with mask option)
P00–P03	92–89	95–92	104–101	I/O	Input/Output ports
P10–P13	88–85	91–88	100–98, 96		(Complementary output or Nch open drain output,
P20–P23	84–81	87–84	95–92		and DC output or external data bus output are selected
P30–P33	–	83–80	91–88		with mask option)
R00–R03	–	116–113	124–121	O	Output ports
R10–R13	–	112–109	120–117		(Complementary output or Nch open drain output,
R20–R23	108–105	108–105	116–113		and DC output or external address bus output,
R30–R33	104–101	104–101	112–109		buzzer output, FOUT output, $\overline{\text{SRDY}}$ output, CL output,
R40–R43	97, 96, 94, 93	100, 99, 97, 96	108–105		and FR output are selected by mask option)
SIN	72	71	78	I	Serial interface data input terminal
SOUT	71	70	77	O	Serial interface data output terminal
$\overline{\text{SCLK}}$	70	68	76	I/O	Serial interface clock input/output terminal

* The $\overline{\text{TEST}}$ (test terminal) is used when the IC load is being detected.
  During ordinary operation be certain to connect this pin to V_{DD}.
* Leave the V_{REF} terminal unconnected (N.C.).

CHAPTER 2 CPU AND BUILT-IN MEMORY

2.1 CPU and Instruction Set

S1C62440/4A0/4C0/480 use the 4-bit core CPU S1C6200 for its CPU. It have almost the same register configurations, instructions, and other features as the other family devices which use S1C6200, allowing full use of software assets. The instruction set of S1C62440/4A0/4C0/480 have 108 types of commands, all consisting of one word (12 bits).

For detailed information on the CPU and the instruction set, refer to the "S1C6200/6200A Core CPU Manual".
Note, however, that because S1C62440/4A0/4C0/480 do not assume SLEEP operation, SLP command is not available in the S1C6200 instruction set.

The instruction set list is shown in Tables 2.1.1(a)–(c).
The list of operands is shown in Table 2.1.2.
Common examples of operation are shown in Table 2.1.3.

Table 2.1.1(a) Instruction sets (1)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
	SLP *		1	1	1	1	1	1	1	1	1	0	0	1					5	SLEEP (stop oscillation)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

* Not in S1C62440/4A0/4C0/480

Table 2.1.1(b) Instruction sets (2)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

Table 2.1.1(c) Instruction sets (3)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP ← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F ← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH ← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r ← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r ← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r ← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r ← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r ← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r ← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r ← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∧i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r ← r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r ← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r ← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r ← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r ← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C ← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C ← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r ← $\overline{r}$

Table 2.1.2 List of operands

Signal	Explanation
P	5-bit immediate data or label (00H–1FH)
S	8-bit immediate data or label (00H–FFH)
I	8-bit immediate data (00H–FFH)
i	4-bit immediate data (0H–FH)
r, q	2-bit immediate data (showing four kinds of registers) A when (r1, r0)=(q1, q0)=(0, 0) B when (r1, r0)=(q1, q0)=(0, 1) MX when (r1, r0)=(q1, q0)=(1, 0) MY when (r1, r0)=(q1, q0)=(1, 1)
A	A register (4 bits)
B	B register (4 bits)
X	XHL register (8 low-order bits of index register IX)
Y	YHL register (8 low-order bits of index register IY)
XH	XH register (4 high-order bits of XHL register)
XL	XL register (4 low-order bits of XHL register)
YH	YH register (4 high-order bits of YHL register)
YL	YL register (4 low-order bits of YHL register)
XP	XP register (4 high-order bits of index register IX)
YP	YP register (4 high-order bits of index register IY)
SP	Stack pointer (8 bits)
SPH	4 high-order bits of stack pointer (SP)
SPL	4 low-order bits of stack pointer (SP)
F	Flag group (IF, DF, ZF, CF)
MX	Data memory addressable with index register IX (4 bits)
MY	Data memory addressable with index register IY (4 bits)
Mn	Data memory addressable with immediate data n (0H–FH) (4 bits)

Table 2.1.3 Common examples of operation

Signal	General explanation
NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	4 high-order bits of PCS
PCSL	4 low-order bits of PCS
A	A register
B	B register
M(X)	Data memory whose address can be specified with index register IX
M(Y)	Data memory whose address can be specified with index register IY
M(SP)	Data memory whose address can be specified with stack pointer SP
M(n3–0)	Data memory of address 00nH (nH = n3n2n1n0B)
r	A, B, M(X) or M(Y)
XP	4 high-order bits (page portion) of index register IX
X	8 low-order bits of index register IX
XH	4 high-order bits of X
XL	4 low-order bits of X
YP	4 high-order bits (page portion) of index register IY
Y	8 low-order bits of index register IY
YH	4 high-order bits of Y
YL	4 low-order bits of Y
SP	Stack pointer
SPH	4 high-order bits of SP
SPL	4 low-order bits of SP
+	Add
-	Subtract
∧	AND
∨	OR
∀	Exclusive-OR
↓	Flag reset
↑	Flag set
↕	Flag set/reset
★	Instruction to add or subtract in decimals when D flag is set

2.2 Program Memory (ROM)

The S1C62440/4A0/4C0/480 have a built-in mask ROM with the following capacity for program storage.

Model	ROM capacity	Configuration
S1C62440	4,096 steps × 12 bits	0000H–0FFFH (bank 0: 16 page, bank 1: non)
S1C624A0	6,144 steps × 12 bits	0000H–17FFH (bank 0: 16 page, bank 1: 8 page)
S1C624C0	5,120 steps × 12 bits	0000H–13FFH (bank 0: 16 page, bank 1: 4 page)
S1C62480	8,192 steps × 12 bits	0000H–1FFFH (bank 0: 16 page, bank 1: 16 page)

* One page is composed of 256 steps.

After initial reset, the program beginning address is bank 0, page 1, step 00H. The interrupt vector is allocated to each page 1, steps 02H–0CH.
The configuration of the ROM is as shown in Figures 2.2.1(a)–(d).

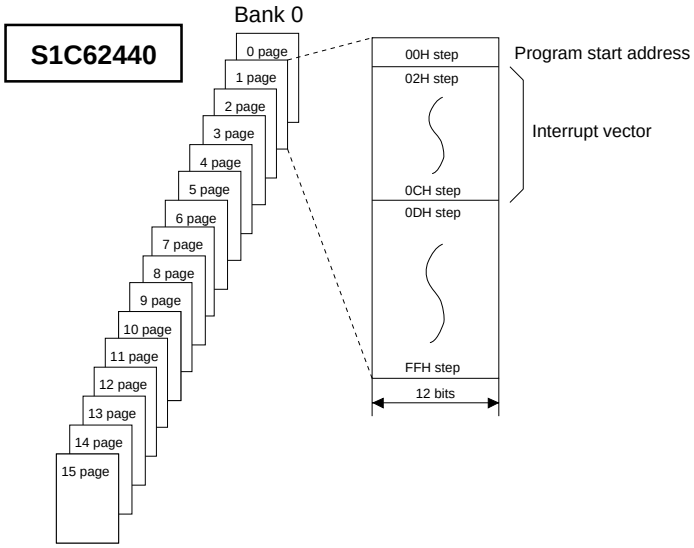


Fig. 2.2.1(a)
Configuration of
the built-in ROM (S1C62440)

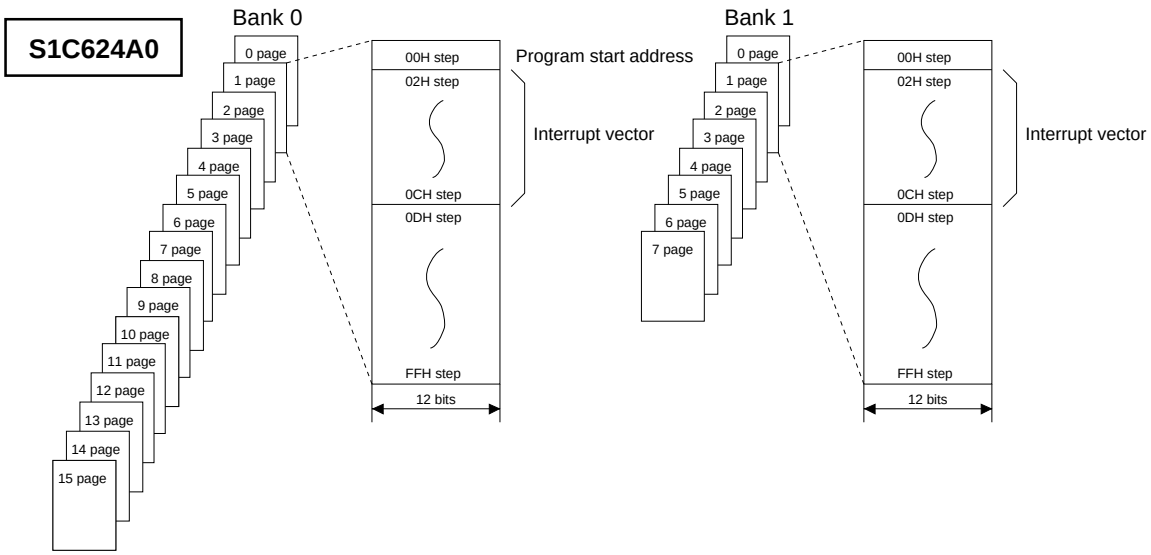


Fig. 2.2.1(b)
Configuration of
the built-in ROM (S1C624A0)

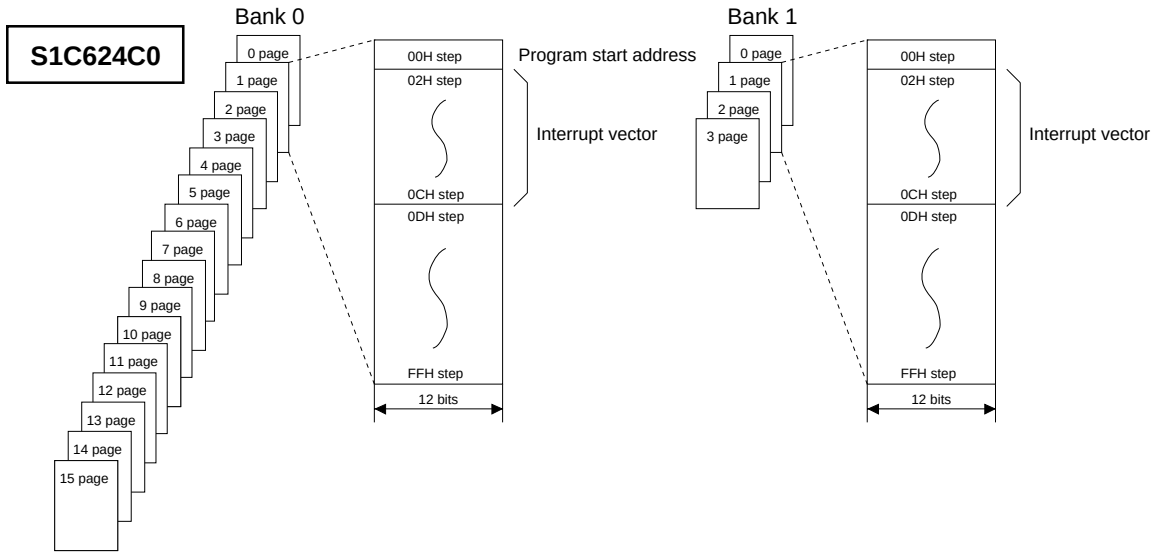


Fig. 2.2.1(c)
Configuration of
the built-in ROM (S1C624C0)

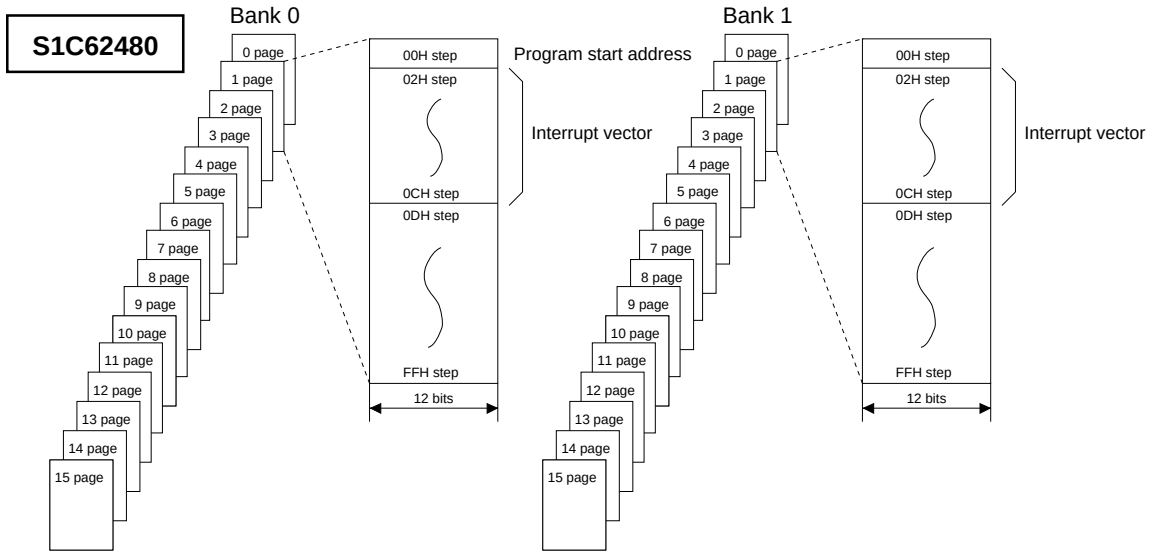


Fig. 2.2.1(d)
Configuration of
the built-in ROM (S1C62480)

2.3 Data Memory (RAM)

The S1C62440/4A0/4C0/480 built-in data memorys are configured a general-purpose RAM, display data memory of the LCD, and I/O data memory which controls the peripheral circuit.

Table 2.3.1 Data memory capacity

Model	RAM capacity	Display data memory
S1C62440	384 words × 4 bits (000H–17FH)	160 words × 4 bits (E00H–E4FH, E80H–ECFH)
S1C624A0	640 words × 4 bits (000H–27FH)	160 words × 4 bits (E00H–E4FH)
S1C624C0	1,152 words × 4 bits (000H–47FH)	204 words × 4 bits (E00H–E65H, E80H–EF5H)
S1C62480	768 words × 4 bits (000H–2FFH)	204 words × 4 bits (E00H–E65H, E80H–EF5H)

During programming, take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

Furthermore, when external memory access function is selected by mask option of S1C624A0/4C0/480, maximum 4-RAM of 8K bytes (64K bits SRAM) may be expanded externally. Refer to Chapter 13 for further information on external memory.

The memory map of the built-in data memory (RAM) and details of the I/O data memory map are shown in Figures 2.3.1(a)–(d) and Tables 2.3.2(a)–(f), respectively.

Note *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

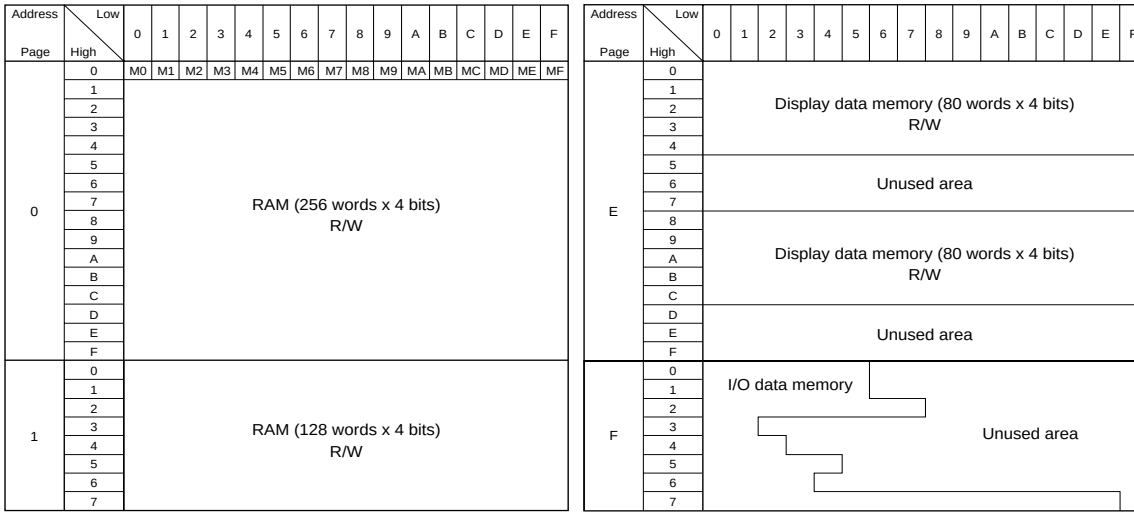


Fig. 2.3.1(a) Memory map (S1C62440)

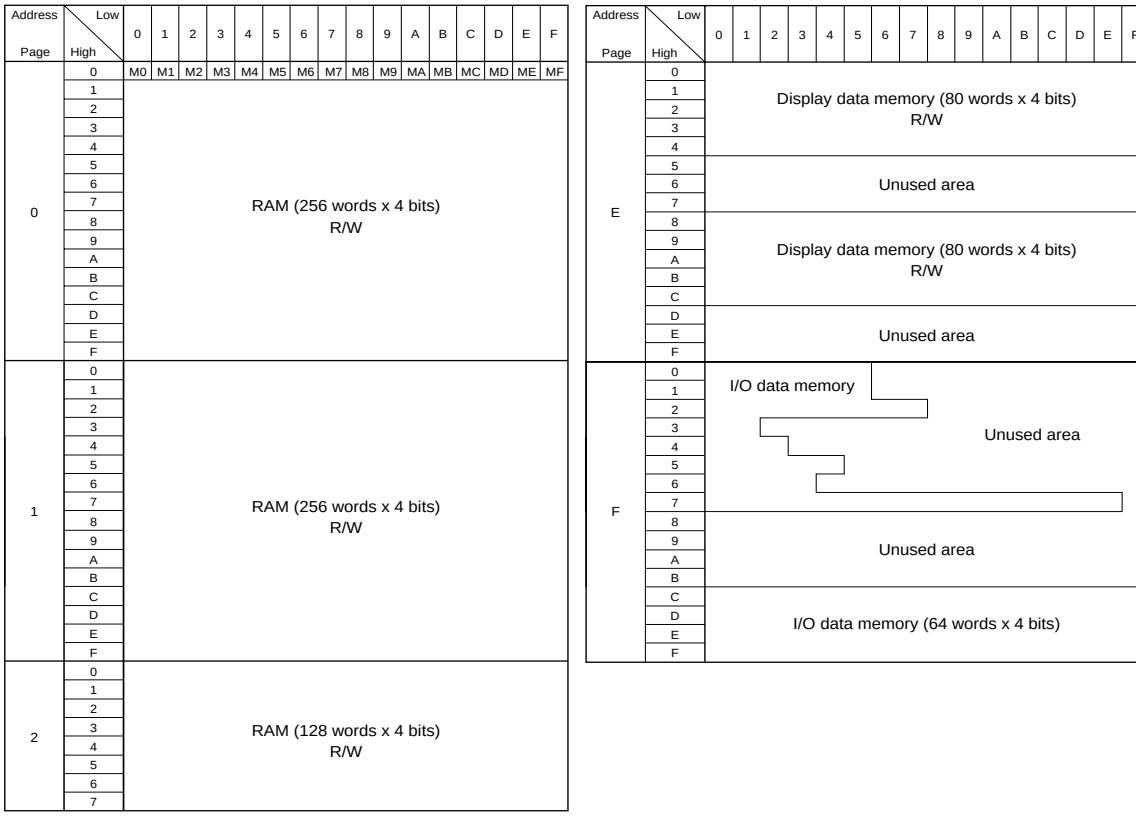


Fig. 2.3.1(b) Memory map (S1C624A0)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
0	1–F	RAM (256 words x 4 bits) R/W															
1	0–F	RAM (256 words x 4 bits) R/W															
2	0–F	RAM (256 words x 4 bits) R/W															
3	0–F	RAM (256 words x 4 bits) R/W															
4	0–7	RAM (128 words x 4 bits) R/W															

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0–6	Display data memory (102 words x 4 bits) R/W															
	7	Unused area															
	8–E	Display data memory (102 words x 4 bits) R/W															
	F	Unused area															
F	0–2	I/O data memory															
	3–7	Unused area															
	8–B	Unused area															
	C–F	I/O data memory (64 words x 4 bits)															

Fig. 2.3.1(c) Memory map (S1C624C0)

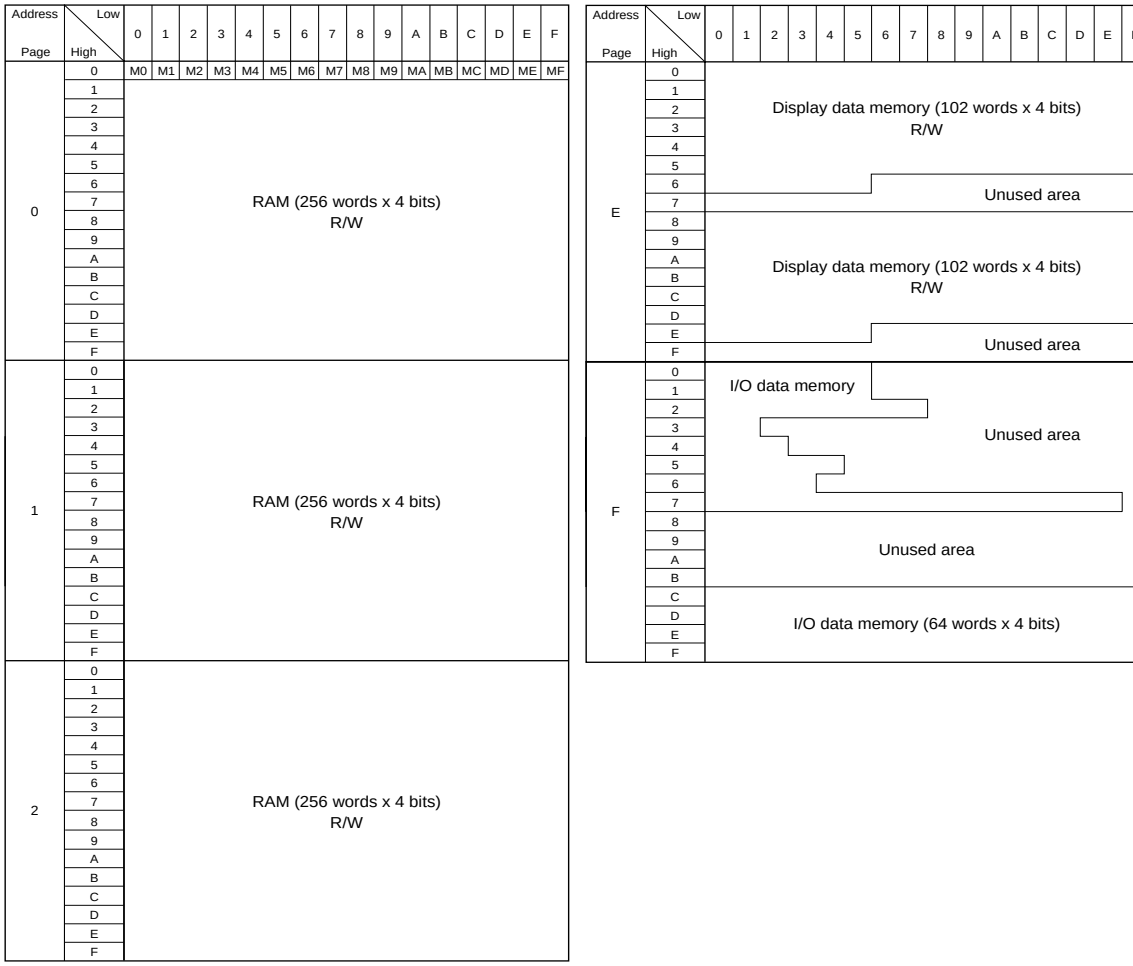


Fig. 2.3.1(d) Memory map (S1C62480)

Table 2.3.2(a) I/O data memory map (F00H–F05H, F10H–F15H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1 *3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F03H	0	0	0	ISIO	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					ISIO *3	0	Yes	No	Interrupt factor flag (serial interface)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0 *3	– *2			
					0 *3	– *2			
	R				0 *3	– *2			
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *3	– *2			
					0 *3	– *2			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F13H	0	0	0	EISIO	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Reset (0) immediately after being read
*4 Always "0" when being read

Table 2.3.2(b) I/O data memory map (F20H–F27H, F30H, F31H, F40H–F42H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB Stopwatch timer
					SWL2	0			1/100 sec data (BCD)
	R				SWL1	0			
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB Stopwatch timer
					SWH2	0			1/10 sec data (BCD)
	R				SWH1	0			
					SWH0	0			LSB
F24H	PT3	PT2	PT1	PT0	PT3	X *3			MSB Programmable timer data (low-order)
					PT2	X *3			
	R				PT1	X *3			
					PT0	X *3			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X *3			MSB Programmable timer data (high-order)
					PT6	X *3			
	R				PT5	X *3			
					PT4	X *3			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X *3			MSB Programmable timer
					RD2	X *3			reload data (low-order)
	R/W				RD1	X *3			
					RD0	X *3			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X *3			MSB Programmable timer
					RD6	X *3			reload data (high-order)
	R/W				RD5	X *3			
					RD4	X *3			LSB
F30H	SD3	SD2	SD1	SD0	SD3	X *3			MSB Serial interface
					SD2	X *3			data register (low-order)
	R/W				SD1	X *3			
					SD0	X *3			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X *3			MSB Serial interface
					SD6	X *3			data register (high-order)
	R/W				SD5	X *3			
					SD4	X *3			LSB
F40H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
					DFK02	1	↓	↑	
	R/W				DFK01	1	↓	↑	
					DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined

Table 2.3.2(c) I/O data memory map (F50H–F54H, F60H–F63H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F50H *6	R03	R02	R01	R00	R03	X *2	High	Low	Output port (R03) / External memory address (A3)
					R02	X *2	High	Low	Output port (R02) / External memory address (A2)
	R/W				R01	X *2	High	Low	Output port (R01) / External memory address (A1)
					R00	X *2	High	Low	Output port (R00) / External memory address (A0)
F51H *6	R13	R12	R11	R10	R13	X *2	High	Low	Output port (R13) / External memory address (A7)
					R12	X *2	High	Low	Output port (R12) / External memory address (A6)
	R/W				R11	X *2	High	Low	Output port (R11) / External memory address (A5)
					R10	X *2	High	Low	Output port (R10) / External memory address (A4)
F52H	R23	R22	R21	R20	R23	X *2	High	Low	Output port (R23) / External memory address (A11) *4
					R22	X *2	High	Low	Output port (R22) / External memory address (A10) *4
	R/W				R21	X *2	High	Low	Output port (R21) / External memory address (A9) *4
					R20	X *2	High	Low	Output port (R20) / External memory address (A8) *4
F53H	R33	R32	R31	R30	R33	X *2	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						*3	*3	[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X *2	High	Low	Output port (R32)
							*3	*3	[External memory read ($\overline{\text{RD}}$)] *4
					R31	X *2	High	Low	Output port (R31) / External memory address (A13) *4
							*3	*3	[External memory write ($\overline{\text{WR}}$)] *4
					R30	X *2	High	Low	Output port (R30) / External memory address (A12) *4
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
							*3	*3	[Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
							Off	On	LCD synchronous signal (CL)
F60H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data (D3) *5
					P02	X *2	High	Low	I/O port (P02) / External memory data (D2) *5
	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data (D1) *5
					P00	X *2	High	Low	I/O port (P00) / External memory data (D0) *5
F61H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data (D7) *5
					P12	X *2	High	Low	I/O port (P12) / External memory data (D6) *5
	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data (D5) *5
					P10	X *2	High	Low	I/O port (P10) / External memory data (D4) *5
F62H	P23	P22	P21	P20	P23	X *2	High	Low	I/O port (P23) / External memory CS ($\overline{\text{CS3}}$) *5
					P22	X *2	High	Low	I/O port (P22) / External memory CS ($\overline{\text{CS2}}$) *5
	R/W				P21	X *2	High	Low	I/O port (P21) / External memory CS ($\overline{\text{CS1}}$) *5
	W				P20	X *2	High	Low	I/O port (P20) / External memory CS ($\overline{\text{CS0}}$) *5
F63H *6	P33	P32	P31	P30	P33	X *2	High	Low	I/O port / Dedicated output port (P33)
					P32	X *2	High	Low	I/O port / Dedicated output port (P32)
	R/W				P31	X *2	High	Low	I/O port / Dedicated output port (P31)
					P30	X *2	High	Low	I/O port / Dedicated output port (P30)

*1 Initial value following initial reset
*2 Undefined
*3 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs
*4 In the S1C62440, it can be used only as a port for output
*5 In the S1C62440, it can be used only as a port for I/O port
*6 In the S1C62440, the F50H, F51H and F63H cannot be used

Table 2.3.2(d) I/O data memory map (F70H–F79H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X *4			LCD contrast adjustment
					LC2	X *4			LC3–LC0 = 0 light
	R/W				LC1	X *4			:
					LC0	X *4			LC3–LC0 = 15 dark
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1 *5	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X *4			SVD criteria voltage setting
					SVC0	X *4			
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			Buzzer frequency selection
	R/W				BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
	W	W	R/W		ENVRST	RESET	Reset	–	Envelope reset
	R				ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *3	– *2			
					0 *3	– *2			
	R		W		TMRST *3	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	SWRST *3	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
F78H	0	0	PTRST	PTRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	PTRST *3	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			Programmable timer input clock selection
	R/W				PTC1	0			
					PTC0	0			

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 Undefined
*5 When SVD is off, "1" is read out

Table 2.3.2(e) I/O data memory map (F7AH–F7EH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					SEN	0	↓	↑	Serial interface clock edge selection
	W	R/W			SCS1	0			Serial interface clock mode selection
					SCS0	0			
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3*3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1*6	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0*6	0	Output	High-Z	R00–R03 output high-impedance control
F7CH	0	HZCS	ADINC	PICON	0 *3, *5, 7	– *2			
					HZCS *3, 4, 6	0	Output	High-Z	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
	R	R/W	W	R/W	ADINC *4, 7	– *2	Increment	–	External memory address increment (A0–A13)
					PICON	0	Auto Inc.	Normal	External memory address auto increment mode
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3*6	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
	R/W				IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3*6	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
	R/W				PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 These control bits are only valid during selection of external memory/address output as output port option
*5 These control bits are only valid during selection of external memory/chip select output as I/O port option
*6 In the S1C62440, it is a register that becomes invalid and during reading it is always "0"
*7 In the S1C62440, it is used as a general purpose register that does not have a function

Table 2.3.2(f) I/O data memory map (FC0H–FFFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FC0H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data bus (D3)
					P02	X *2	High	Low	I/O port (P02) / External memory data bus (D2)
FFEH (even)*3	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data bus (D1)
					P00	X *2	High	Low	I/O port (P00) / External memory data bus (D0)
FC1H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data bus (D7)
					P12	X *2	High	Low	I/O port (P12) / External memory data bus (D6)
FFFH (odd)*3	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data bus (D5)
					P10	X *2	High	Low	I/O port (P10) / External memory data bus (D4)

*1 Initial value following initial reset
*2 Undefined
*3 Image area of I/O ports (P00–P03, P10–P13) .... S1C624A0/4C0/480 only
See Chapter 13, "EXTERNAL MEMORY ACCESS (S1C624A0/4C0/480)"

CHAPTER 3 POWER SOURCE

3.1 Power Supply System

The S1C62440/4A0/4C0/480 operating power voltage is as follows:

2.2 V–5.5 V (Min. 1.8 V, when OSC3 oscillation circuit is not used)

The S1C62440/4A0/4C0/480 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. Even if the voltage is not within the above range necessary for the internal circuits, the IC itself can generate the following built-in power circuits.

Table 3.1.1 Power supply circuits

Circuit	Power supply circuit	Output voltage
Oscillation circuit and internal circuit	Regulated voltage circuit	V_{S1}
LCD driver	LCD system voltage circuit	V_{L1}–V_{L5}

Note
- *V_{L3} is used only when the driving voltage of the LCD system will be supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), it is shorted with V_{L2}.*
  V_{L1}, V_{L2}, V_{L4} and V_{L5} can only supply voltage for external LCD driver expansion.
- *See "17 ELECTRICAL CHARACTERISTICS" for voltage values.*

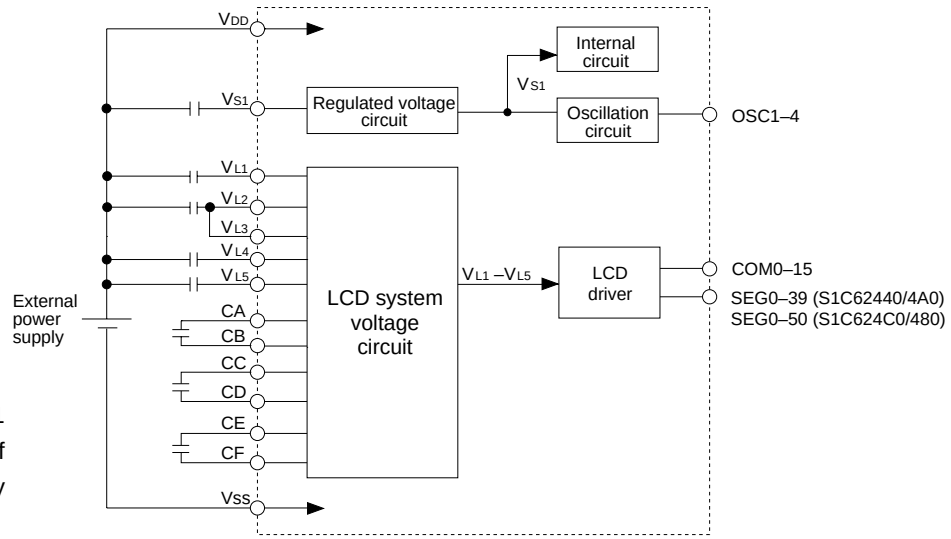


Fig. 3.1.1 Configuration of power supply

3.2 SVD (Supply Voltage Detection) Circuit

Configuration of SVD circuit

The S1C62440/4A0/4C0/480 have a built-in SVD (supply voltage detection) circuit which allows detection of power voltage drop through software.
Turning the SVD operation on and off can be controlled through the software. Because the IC consumes a large amount of current during SVD operation, it is recommended that the SVD operation be kept OFF unless it is otherwise necessary.
Also, the SVD criteria voltage can be set by software. The criteria voltage can be set by matching to one of the 4 types of batteries below that can be used.

-2.2 / -2.5 / -3.1 / -4.2V (V_{DD} reference voltage)

See "17 ELECTRICAL CHARACTERISTICS" for the precision of the criteria voltage.

Figure 3.2.1 shows the configuration of the SVD circuit.

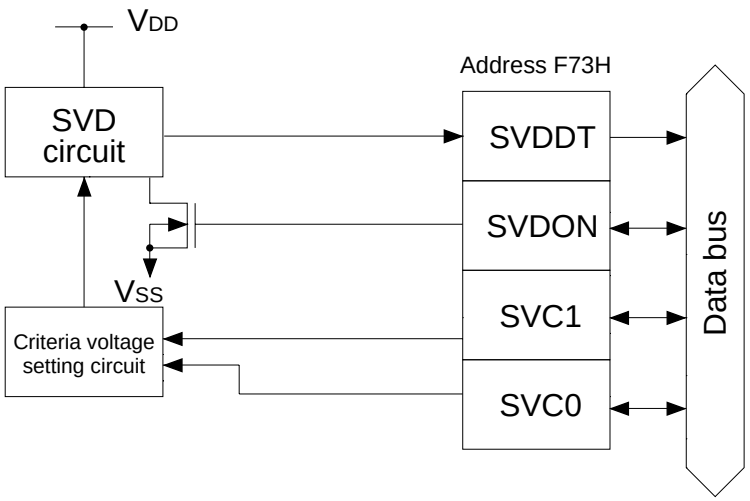


Fig. 3.2.1
Configuration of SVD circuit

Control of SVD circuit

The SVD operation control registers are explained below.

Table 3.2.1 Control registers of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1	Low	Normal	SVD evaluation data
	R	R/W			SVDON	0	On	Off	SVD circuit On/Off
					SVC1	X			SVD criteria voltage setting
					SVC0	X			

SVC0 and SVC1 (F73H [D0 and D1], R/W)

Criteria voltage for supply voltage detection is set as shown in Table 3.2.2.

Table 3.2.2 Criteria voltage for SVD circuit

SVC1	SVC0	Criteria voltage
0	0	-2.2 V
0	1	-2.5 V
1	0	-3.1 V
1	1	-4.2 V

The V_{DD} reference voltage is used as the criteria voltage.
At initial reset, this register becomes undefined.

SVDON (F73H [D2], R/W)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

By writing "1" to the SVDON, the SVD circuit is turned ON, and determination of supply voltage is initiated. Likewise, by writing "0", it is turned OFF.
At initial reset, it is set to "0" (OFF).

Note *The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.*

SVDDT (F73H [D3], R) This is the result of supply voltage determination.

When "0" is read: Criteria voltage ≤ Source voltage (V_{DD}–V_{SS})
When "1" is read: Criteria voltage > Source voltage (V_{DD}–V_{SS})
Writing: Invalid

If the SVD circuit is ON, when the voltage of the battery is detected to be lower than the criteria voltage set at SVC0 and SVC1, SVDDT is "1". If it is more than the criteria voltage, it is "0".
The SVDDT reading is valid when SVDON is "1" and is always "1" when SVDON is "0".

Note *To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.*

Programming notes

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

3.3 Heavy Load Protection Mode

Because the load of the battery in the S1C62440/4A0/4C0/480 becomes heavy due to the buzzer, lamp, and other features, it has been equipped with heavy load protection function in case of power voltage drop. This functions works in the heavy load protection mode.
Based on the workings of the heavy load protection function, the S1C62440/4A0/4C0/480 realizes operation at 2.2 V (Min. 1.8 V, when OSC3 oscillation circuit is not used) source voltage.

During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode.
At the normal mode, the LCD system regulated voltage is created with V_{L2}; V_{L1} is 1/2 reduced V_{L2} voltage while V_{L4} and V_{L5} are created by boosting to 1.5 and 2 times voltages, respectively. On the other hand, at the heavy load protection mode, the regulated voltage is V_{L1}; V_{L2}, V_{L4}, and V_{L5} are created by boosting to 2, 3 and 4 times voltages. Because of this, the consumed current becomes greater than that in the normal mode, be careful not to set the heavy load protection unless necessary.
The LCD system voltage modes are shown in Table 3.3.1.

Table 3.3.1
LCD system voltage for SVD circuit mode

Terminal	Operation mode	
	Normal mode	Heavy load protection mode
V_{L1}	1/2 V_{L2}	V_{L1} regulated voltage
V_{L2}	V_{L2} regulated voltage	2V_{L1}
V_{L4}	3/2 V_{L2}	3V_{L1}
V_{L5}	4/2 V_{L2}	4V_{L1}

Control of heavy load protection mode

The control register for the heavy load protection mode are explained below.

Table 3.3.2 Control register for heavy load protection mode

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
	R/W				ALON	0	All on	Normal	All LCD dots displayed control
					LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode

HLMOD (F71H [D0], R/W)

Controls the heavy load protection mode.

When "1" is written: Heavy load protection mode is set
When "0" is written: Heavy load protection mode is released
Reading: Valid

Conversion to heavy load protection mode is done by writing "1" to HLMOD while cancellation of this mode is done by writing "0".
During initial reset, the mode is set at "0" (heavy load protection mode cancellation).

Programming notes

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.1.)

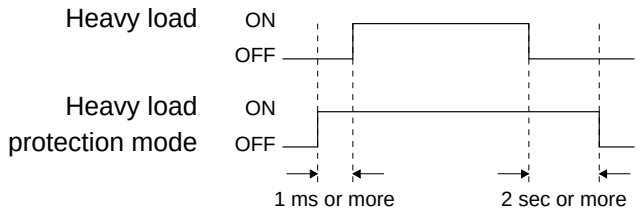


Fig. 3.3.1
Control timing for
heavy load protection mode

3.4 CPU Operating Voltage Change

During operation, S1C62440/4A0/4C0/480 can change OSC1 and OSC3 system clocks through the software, and operation at clock mode or high-speed mode is then possible. In this case, to obtain stable operating, operating voltage V_{S1} of the internal circuit is changed through the software. For details, see Chapter 5, "OSCILLATION CIRCUIT".

CHAPTER 4 WATCHDOG TIMER AND INITIAL RESET

4.1 Watchdog Timer

Configuration of watchdog timer

S1C62440/4A0/4C0/480 have a built-in watchdog timer with OSC1 (clock timer 1 Hz signal) basic oscillation. The watchdog timer needs to be reset periodically through the software, and if not reset within 3–4 seconds, it automatically generates initial reset signal to the CPU.
Figure 4.1.1 shows the configuration of the watchdog timer.

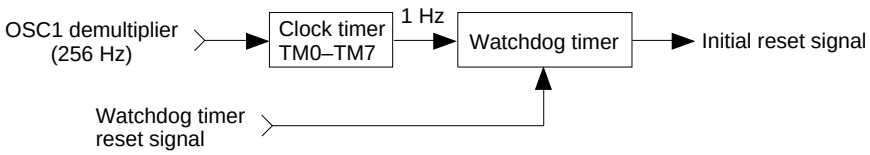


Fig. 4.1.1 Configuration of watchdog timer

By resetting the watchdog timer during the program's main routine, program runaways which do not pass the watchdog timer processing during main routine can be detected.
Note, however, that the watchdog timer operates even during HALT such that if the HALT condition continues for 3–4 seconds, it is re-initiated through initial resetting.

Control of watchdog timer

The control register of the watchdog timer is explained below.

Table 4.1.1 Control register of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F76H	0	0	TMRST	WDRST	0	–			
	R		W		0	–		–	
					TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

WDRST (F76H [D0], W)

This bit resets the watchdog timer.

When "1" is written: Watchdog timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on WDRST, the watchdog timer is reset, after which it is immediately restarted. Writing "0" will mean no operation.
Because this bit is only for writing, it is always set to "0" during reading.

Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST←"1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

4.2 Initial Reset

S1C62440/4A0/4C0/480 require initial reset function to initialize the circuits.
There are four types of initial reset factors:

(1) External reset through LOW level input to the $\overline{\text{RESET}}$ terminal

(2) External initial reset by simultaneous L level input of K00–K03 terminals (mask option)

(3) Initial reset by oscillation detector

(4) Initial reset by watchdog timer

Figure 4.2.1 shows the configuration of the initial reset circuit.

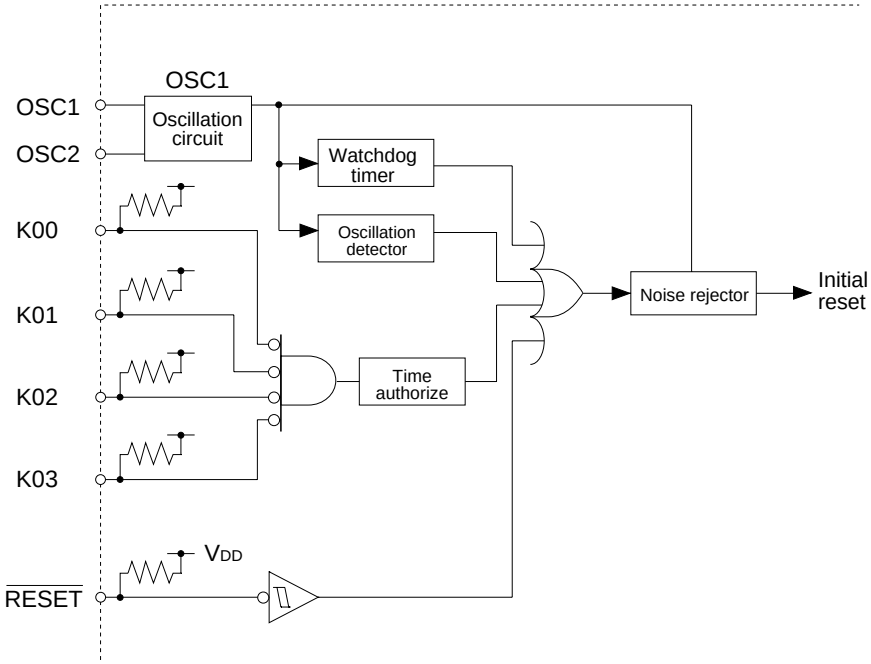


Fig. 4.2.1
Configuration of initial reset circuit

External initial reset by the $\overline{\text{RESET}}$ terminal

Initial resetting can be done externally by placing the reset terminal at Low level. Because the initial reset circuit has noise rejector built-in, keep it at Low level for at least 2 ms (in case oscillation frequency f_{OSC1} = 32,768 Hz). When the reset terminal goes High, the CPU will start operating.

External initial reset by simultaneous L level input of K00–K03 terminals (mask option)

Initial reset may be done by simultaneously providing Low level input externally to the input port (K00–K03) selected by mask option. Because the initial reset circuit has time authorize circuit built-in, keep the specified input port terminal at Low level for at least 2 seconds (in case oscillation frequency f_{OSC1} = 32,768 Hz). The input port combination which can be selected from the mask option are as follows:

– Not use
– K00*K01
– K00*K01*K02
– K00*K01*K02*K03

Initial reset by oscillation detector

The oscillation detector generates initial reset frequency until the crystal oscillation circuit (OSC1) starts oscillation during power charge.
However, depending on the power-on sequence (voltage rise timing), the circuit may not work properly. Therefore, use the reset terminal or reset by simultaneous low input to the input port (K00–K03) for initial reset after turning power on.

Initial reset by watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See "4.1 Watchdog Timer" for details.

Internal register at initial resetting

The CPU is initialized by initial resetting as follows:

Table 4.2.1 Initial values

CPU core			
Name	Symbol	Bit length	Setting value
Program counter, step	PCS	8	00H
Program counter, page	PCP	4	1H
Program counter, bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register • IX	IX	12	Undefined
Index register • IY	IY	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register	A	4	Undefined
General-purpose register	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuit		
Name	Bit length	Setting value
RAM	4	Undefined
Segment data memory	4	Undefined
Other peripheral circuits	4	*

* See Tables 2.3.2(a)–(f).

CHAPTER 5 OSCILLATION CIRCUIT

5.1 OSC1 Oscillation Circuit

S1C62440/4A0/4C0/480 have a built-in crystal oscillation circuit (OSC1 oscillation circuit).
Figure 5.1.1 shows the configuration of the OSC1 crystal oscillation circuit.

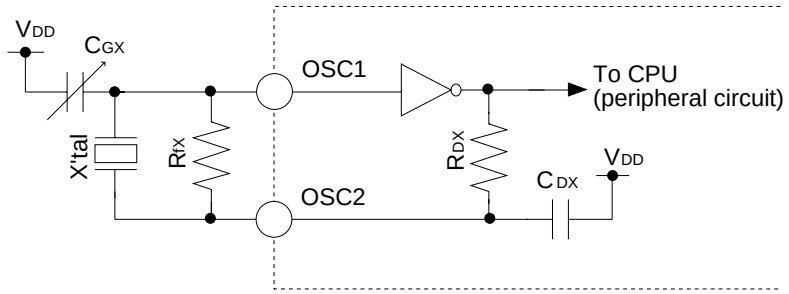


Fig. 5.1.1
Configuration of
OSC1 crystal oscillation circuit

As Figure 5.1.1 indicates, the crystal oscillation circuit can be configured simply by connecting the crystal X'tal (Typ. 32,768 Hz) and feedback resistor Rfx (10 MΩ) between pins OSC1 and OSC2 to the trimmer capacitor CGX (5–25 pF) between pins OSC1 and VDD.

For the S1C62440/4C0/480, CR oscillation circuit may also be selected by a mask option. Figure 5.1.2 is the configuration of the OSC1 CR oscillation circuit.

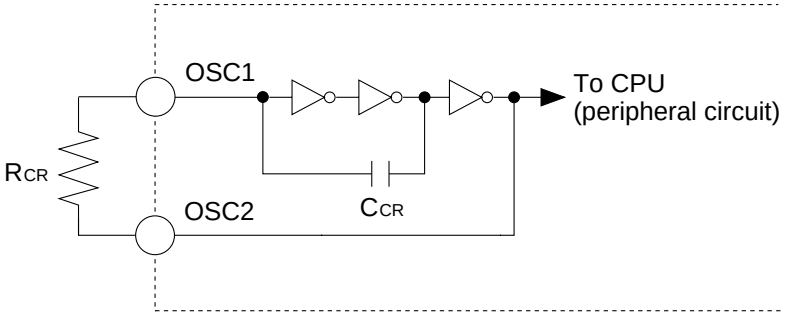


Fig. 5.1.2
Configuration of
OSC1 CR oscillation circuit
(S1C62440/4C0/480)

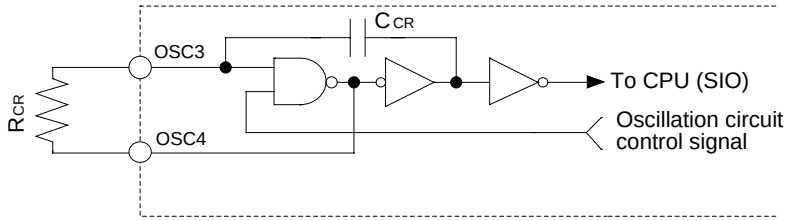
As indicated in Figure 5.1.2, the CR oscillation circuit can be configured simply by connecting the resistor (R_{CR}) between terminals OSC1 and OSC2 when CR oscillation is selected.
When 1.6 MΩ is used for R_{CR}, the oscillation frequency is about 32 kHz (V_{S1} = -2.1 V) / about 34 kHz (V_{S1} = -3.0 V).

Note – CR oscillation increases current consumption more than the crystal oscillation.

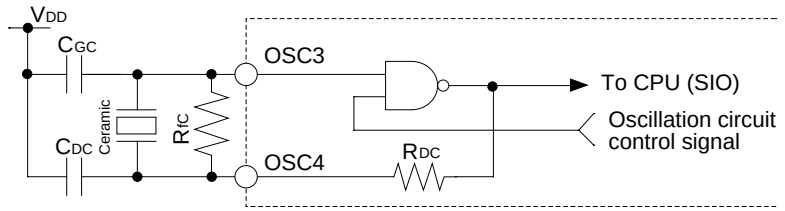
– Be aware that the frequency of the CR oscillation is uneven. In particular, pay attention to the time base counter (time lag), the LCD frame frequency (change of the display quality, flicker in low frequency, etc.) and the sound generator (change of sound quality).

5.2 OSC3 Oscillation Circuit

The S1C62440/4A0/4C0/480 have a built-in OSC3 oscillation circuit that enables the high-speed operation of 2 MHz oscillation frequency.
Either the CR oscillation circuit or the ceramic oscillation circuit can be selected by a mask option.
Figure 5.2.1 shows the configuration of the OSC3 oscillation circuit.



(a) OSC3 CR oscillation circuit



(b) OSC3 ceramic oscillation circuit

Fig. 5.2.1
Configuration of
OSC3 oscillation circuit

When CR oscillation circuit is selected by mask option, resistor RCR is connected between OSC3 and OSC4 terminals. When almost 20 kΩ is used for RCR, the oscillation frequency will be about 1.7 MHz (VS1 = -3.0 V).
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic and feedback resistor Rfc (≈ 1 MΩ) between pins OSC3 and OSC4 to the capacitors CGC and CDC located between pins OSC3 and VDD, OSC4 and VDD. For both CGC and CDC, connect capacitors that are about 100 pF.

Either the OSC3 oscillation circuit or the OSC1 crystal oscillation circuit output clock can be selected with the software for use as the CPU system clock.
When OSC1 is selected as the system clock, OSC3 oscillation can be halted with the software so as to lower the current consumption.

When the OSC3 oscillation circuit is not used, connect the OSC3 terminal to V_{S1}.
The connection diagram in this case is shown in Figure 5.2.2.

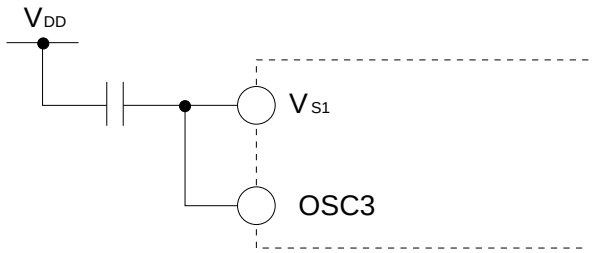


Fig. 5.2.2
Connection diagram when the OSC3 oscillation circuit is unused

5.3 Operating Voltage Change

S1C62440/4A0/4C0/480 can change OSC1 and OSC3 system clocks through the software. In this case, to obtain stable operation, operating voltage V_{S1} of the internal circuit is changed through the software.
Likewise, when selecting OSC1 as the system clock, there is need to change operating voltage V_{S1} according to the value of the power voltage (V_{DD}–V_{SS}).
Oscillation frequency and the corresponding operating voltage V_{S1} are shown in Table 5.3.1.

Table 5.3.1
Oscillation frequency and operating voltage

Oscillation frequency	Oscillation circuit	Operating voltage V_{S1}
32,768 Hz	OSC1	-1.2 V or -2.1 V
1 MHz	OSC3	-2.1 V
2 MHz	OSC3	-3.0 V

The V_{DD} reference voltage is used as the operating voltage V_{S1}.
When OSC3 is to be used as the CPU system clock, change the operating voltage V_{S1} accordingly through the software and then turn the OSC3 oscillation ON and switch the clock frequency.
If the OSC3 oscillation frequency is to be fixed around 1 MHz, set the operating voltage to -2.1 V; at 2 MHz, set the operating voltage to -3.0 V.
Moreover, when the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). However, it can be used fixed at -1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

Note *Switching V_{S1} when the power source voltage is lower than the set voltage may cause misoperation. Perform the operating voltage only after making sure that power voltage by SVD is more than the V_{S1} setting voltage (absolute value).*

5.4 Clock Frequency and Instruction Execution Time

Table 5.4.1 shows the instruction execution time according to each frequency of the system clock.

Table 5.4.1
Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µs)		
	5-clock instruction	7-clock instruction	12-clock instruction
32,768 Hz	152.6	213.6	366.2
1 MHz	5.0	7.0	12.0
2 MHz	2.5	3.5	6.0

5.5 Control of Oscillation Circuit

The control registers for the oscillation circuit are explained below.

Table 5.5.1 Control registers of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock change
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					VSC1	0			CPU operating voltage switch
					VSC0	0			

VSC0 and VSC1 (F70H [D0 and D1], R/W)

Switches the operating voltage of the internal circuit in accordance to the oscillation frequency and power source voltage.
The corresponding setting description is shown in Table 5.5.2.

Table 5.5.2 Corresponding between oscillation frequency, power source voltage, and operating voltage (V_{S1})

VSC1	VSC0	V_{S1}	Oscillation circuit	Oscillation frequency	Power source voltage (V_{DD}–V_{SS})
0	0	-1.2 V	OSC1	32,768 Hz	Under 3.1 V
0	1	-2.1 V	OSC1	32,768 Hz	3.1 V or more (*)
0	1	-2.1 V	OSC3	1 MHz	2.2 V or more
1	×	-3.0 V	OSC3	2 MHz	3.1 V or more

The V_{DD} reference voltage is used as the operating voltage V_{S1}.
There is no need to set the (*) state with regards to power whose initial value is 3.6 V or less as in lithium batteries.
VSC1 and VSC0 are set to "0" at initial reset.

Note – When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)
= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

– In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option as OSC1, V_{S1} becomes -2.1 V even when VSC1 = VSC0 = 0 and will never become -1.2 V. In addition, since the current consumption is great for CR oscillation compared with the quartz crystal oscillation, when low power consumption is required, you should select quartz crystal oscillation as OSC1.

OSCC (F70H [D2], R/W) Controls the oscillation of the OSC3 oscillation circuit.

When "1" is written:	OSC3 oscillation ON
When "0" is written:	OSC3 oscillation OFF
Reading:	Valid

When high-speed operation of the CPU is required, OSCC is set to "1"; otherwise, set it to "0" to minimize power current consumption.
At initial reset, OSCC is set to "0".

Note It takes 5 ms for the OSC3 oscillation circuit to stabilize after oscillation turns ON. Since oscillation stabilization time differs according to external oscillation terminal and usage conditions, set the stand-by time with enough allowance when switching the clock frequency.

CLKCHG (F70H [D3], R/W) Selects the CPU operating clock.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When assigning OSC3 as the CPU operating clock, set CLKCHG to "1"; when assigning OSC1, set it to "0".
At initial reset, CLKCHG is set to "0".

Note *When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.5.1 and then proceed with software processing.*

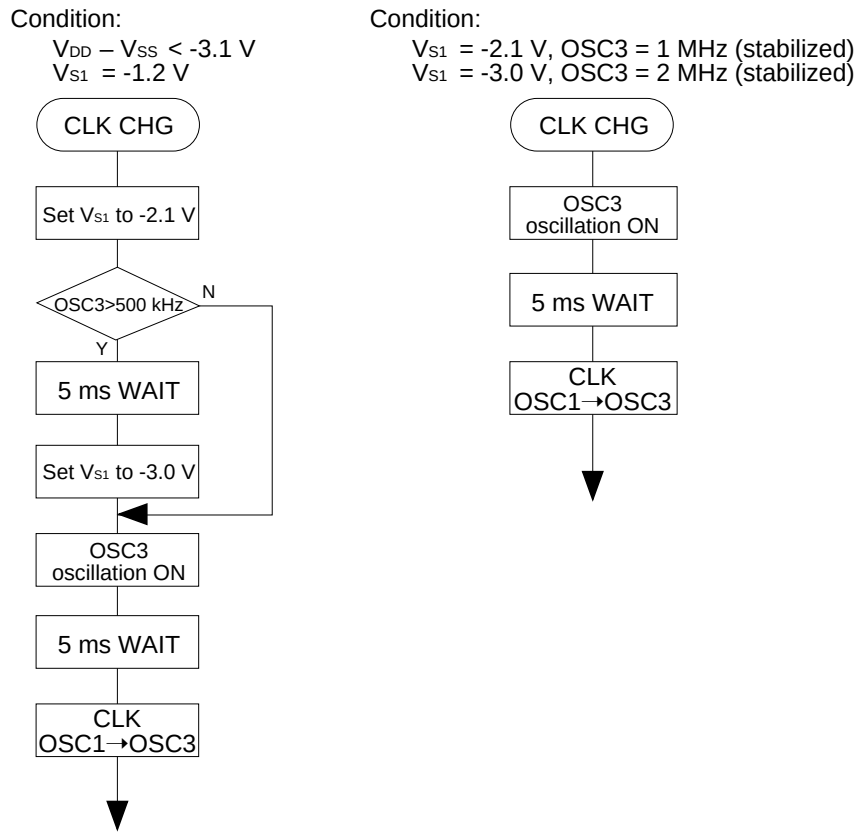


Fig. 5.5.1
CPU operating clock control flow

5.6 Programming Notes

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0)→ (0, 1)→ 5 ms WAIT → (1, ×)
= (1, ×)→ (0, 1)→ 5 ms WAIT → (0, 0)

= (0, 0)→ (1, ×) is prohibited
= (1, ×)→ (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.5.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

CHAPTER 6 INPUT PORTS (Kxx)

6.1 Configuration of Input Ports

The S1C62440/4A0/4C0/480 have 8 bits (4 bits × 2, K00–K03, K10–K13) general input ports built-in.
Figure 6.1.1 shows the configuration of the input port.

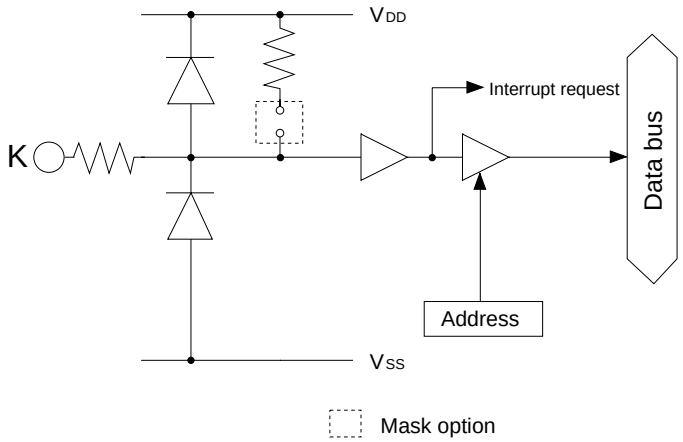


Fig. 6.1.1
Configuration of input port

The input port pin K03 is used as the clock input pins for the programmable timer. See "10.3 Programmable Timer" for details.

6.2 Mask Option

The input ports (K00–K03 and K10–K13) are provided with built-in pull up resistor the use of which may be selected for every bit with the mask option.

Selection of "Pull up resistor enable" with the mask option suits input from the push switch, key matrix, and so forth. When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

When "Pull up resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that floating state does not occur.

6.3 Interrupt Function

All eight bits of the input ports K00–K03 and K10–K13 provide the interrupt function.
Whether to mask the interrupt function can be selected individually for all eight bits by the software.

Input interrupt (K00–K03) and input relation registers

The input ports K00–K03 are equipped with input relation registers. The condition for issuing an interrupt can be set by the software.
Figure 6.3.1 shows the configuration of the input (K00–K03) interrupt circuit.

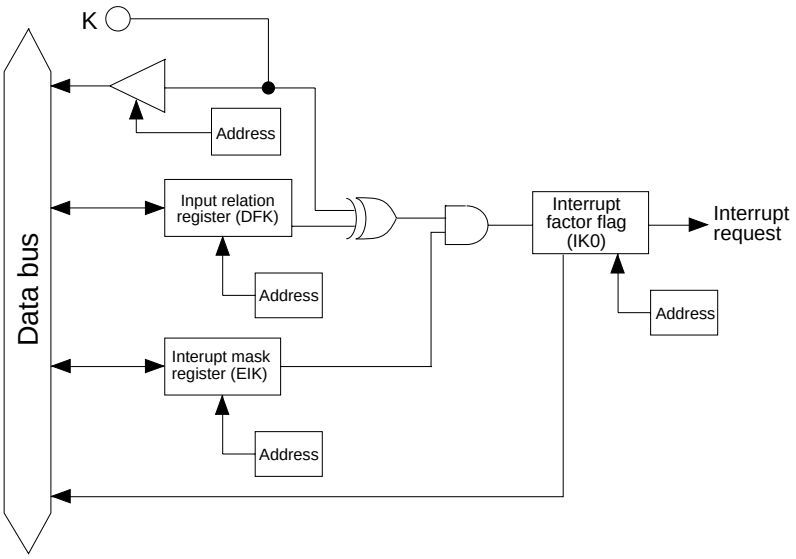


Fig. 6.3.1
Configuration of input (K00–K03) interrupt circuit

The input interrupt timing of K00–K03 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input relation registers DFK00–DFK03. Moreover, masking can be set individually to the interrupt of K00–K03. However, if the interrupt of any one of K00–K03 is enabled, interrupt will be generated when the content change from matched to no matched with the input relation register.
When interrupt is generated, the interrupt factor flag IK0 is set to "1".
Figure 6.3.2 shows an example of an interrupt for K00–K03.

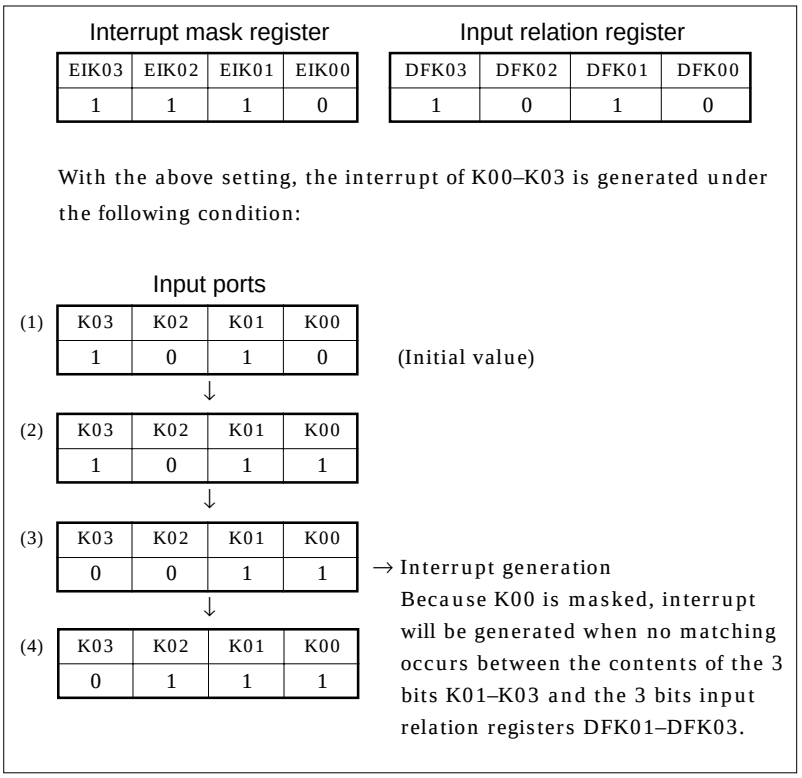


Fig. 6.3.2
Example of an interrupt for K00–K03

Because K00 is masked by an interrupt mask register (EIK00), interrupt will not be generated at the above step (2). Next, since K03 becomes "0" at step (3), interrupt is generated due to the no matching of the data of the terminal whose interrupt is enabled and the data of the input relation registers. No interrupt is generated from a no matched state to another no matched state as in step (4) because the condition for interrupt generation, as has been previously stated, is that the port data and the contents of the input relation registers must change from a matched state to a no matched one. Moreover, a terminal whose interrupt is masked will not affect the condition for interrupt generation.

Input interrupt (K10–K13)

Figure 6.3.3 shows the configuration of the input (K10–K13) interrupt circuit.

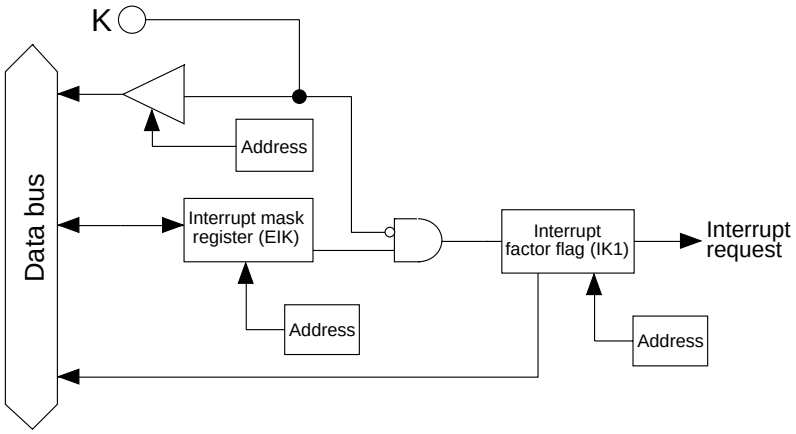


Fig. 6.3.3
Configuration of the input (K10–K13) interrupt circuit

There is no input relation registers for K10–K13, and interrupt is fixed to occur at the falling edge of input. The interrupt mask can be selected for each of the four pins with the interrupt mask register EIK10–EIK13. When all the enabled pins are "1", interrupt occurs when one or more of the pins changes to "0".

When interrupt is generated, the interrupt factor flag IK1 is set to "1".

Figure 6.3.4 shows an example of an interrupt for K10–K13.

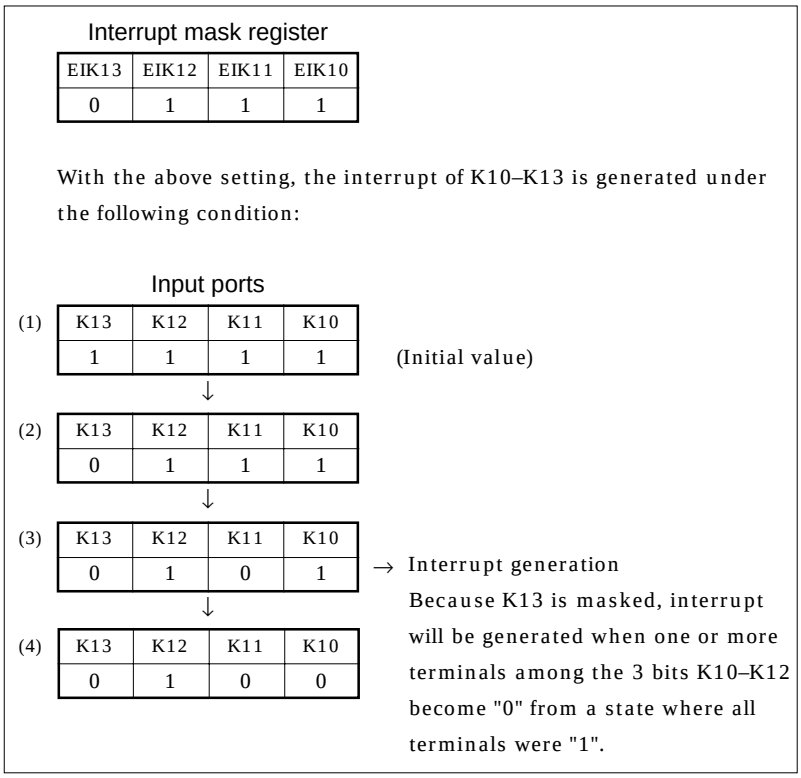


Fig. 6.3.4
Example of an interrupt for K10–K13

The mask register (EIK13) masks the interrupt of K13, so an interrupt does not occur at (2). At (3), K11 becomes "0", so that an interrupt occurs if the interrupt enabled pins were all "1" and at least one pin then changes to "0". At (4), the conditions for interrupt are not established, so an interrupt does not occur. Further, pins that have been masked for interrupt do not affect the conditions for interrupt generation.

6.4 Control of Input Ports

The control registers for the input ports are explained below.

Table 6.4.1(a) Control registers of input ports (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F04H	0	0	0	IK0	0	–			
	R				0	–			
					0	–			
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0	–			
	R				0	–			
					0	–			
					IK1	0	Yes	No	Interrupt factor flag (K10–K13)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
	R/W				EIK12	0	Enable	Mask	Interrupt mask register (K12)
					EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)

Table 6.4.1(b) Control registers of input ports (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F40H	K03	K02	K01	K00	K03	–	High	Low	Input port (K00–K03)
	R				K02	–	High	Low	
					K01	–	High	Low	
					K00	–	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	
					DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	–	High	Low	Input port (K10–K13)
	R				K12	–	High	Low	
					K11	–	High	Low	
					K10	–	High	Low	

K00–K03, K10–K13 (F04H, F42H, R) Input data of the input port terminal may be read out with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The terminal voltage of 8 bits input ports (K00–K03 and K10–K13) are each reading as "1" and "0" at high (V_{DD}) level and low (V_{SS}) level, respectively.
When these bits are used for reading only, writing operation becomes invalid.

DFK00–DFK03 (F41H, R/W)

These input relation registers which set the interrupt generating conditions of K00–K03.

When "1" is written:	Falling edge
When "0" is written:	Rising edge
Reading:	Valid

When DFK0x is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". DFK0x respectively correspond to input ports K0x and may be set in units of 1 bit.
At initial reset, these registers are all set to "1".

EIK00–EIK03,EIK10–EIK13 (F14H, F15H, R/W)

These are interrupt mask registers of the input ports.

When "1" is written:	Enable
When "0" is written:	Mask
Reading:	Valid

EIK0x corresponds to input port K0x, and EIK1x corresponds to input port K1x. Whether to mask the interrupt function can be set in units of 1 bit.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IK0, IK1 (F04H [D0], F05H [D0], R)

These are interrupt factor flags of the input ports.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

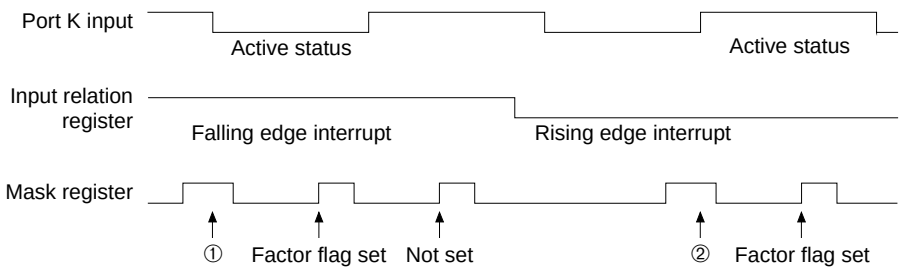
The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectivery. From the status of these flags, the software can decide whether an input interrupt has occurred.

These flags will not be set even if the input conditions are established if, for every terminal series, the interrupt mask registers (EIKxx) are all set to "0" (i.e., EIK00–EIK03, or EIK10–EIK13 are all set to "0", or all are individually set to "0").
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

6.5 Programming Notes

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

(2) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 6.5.1
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = Low status, when the falling edge interrupt is effected and

input terminal = High status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 6.5.1. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 6.5.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.

In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 7 OUTPUT PORTS (Rxx)

7.1 Configuration of Output Ports

The S1C624A0/4C0/480 have 20 bits (4 bits × 5, R00–R03, R10–R13, R20–R23, R30–R33, and R40–R43), and S1C62440 has 12 bits (4 bits × 3, R20–R23, R30–R33, and R40–R43) general output ports built-in.
Figure 7.1.1 shows the configuration of the output port.

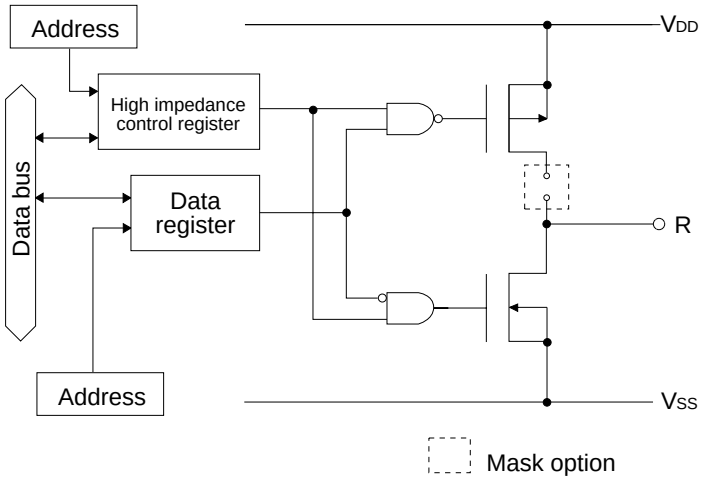


Fig. 7.1.1
Configuration of output port

7.2 Mask Option

The output ports may be selected for the following by mask option.

(1) Output specification of output ports

The output specification of the output ports may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

R00–R03: Complementary or Nch open drain (selected with the 4 bits group) *1
R10–R13: Complementary or Nch open drain (selected with the 4 bits group) *1
R20–R22: Complementary or Nch open drain (selected with the 3 bits group) *2
R23: Complementary or Nch open drain *2
R30–R33: Complementary or Nch open drain (select in units of 1 bit)
R40–R43: Complementary or Nch open drain (select in units of 1 bit)

*1 R00–R03 and R10–R13 are not set for the S1C62440.
*2 In the S1C62440 it selects as a four bit group of R20–R23.

(2) External memory access

In the S1C624A0/4C0/480 aside from DC output, output ports R00–R03, R10–R13, R20–R23, and R30–R32 may also be set with the mask option as external memory access port as follows:

R00–R03: External memory address (A0–A3)
(selected with the 4 bits group)
R10–R13: External memory address (A4–A7)
(selected with the 4 bits group)
R20–R22: External memory address (A8–A10)
(selected with the 3 bits group)
R23: External memory address (A11)
R30: External memory address (A12)
R31: External memory address (A13)
or external memory write ($\overline{WR}$)
R32: External memory read ($\overline{RD}$)

The control of external memory access is explained in Chapter 13.

(3) Special output

Output ports R33 and R40–R43 may be selected, in addition to DC output, as special output port as follows:

R33: SIO Ready ($\overline{SRDY}$) or programmable timer operating clock output (PTCLK)
R40: Clock inverted output ($\overline{FOUT}$)
or LCD synchronous signal (CL)
R41: LCD frame signal (FR)
R42: Buzzer inverted output ($\overline{BZ}$)
or clock output (FOUT)
R43: Buzzer output (BZ)

Buzzer outputs BZ (R43) and $\overline{BZ}$ (R42)

Through mask option selection, R43 and R42 may be assigned as buzzer outputs. BZ and $\overline{BZ}$ are buzzer signal outputs for driving piezo-electric buzzers, the buzzer signal being created by the division of f_{OSC1}. Moreover, digital envelope may be added to the buzzer signal.
See Chapter 12, "SOUND GENERATOR" for details.

Buzzer output BZ and $\overline{BZ}$ can be controlled simultaneously by register R43. Note, however, that register R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (output from the R42 terminal).

Note – The BZ and $\overline{BZ}$ output signals could generate hazards during ON/OFF switching.
– When output port R43 is set to DC output, output port R42 may not be set to $\overline{BZ}$ output.

Figure 7.2.1 shows the output waveform of BZ and $\overline{BZ}$.

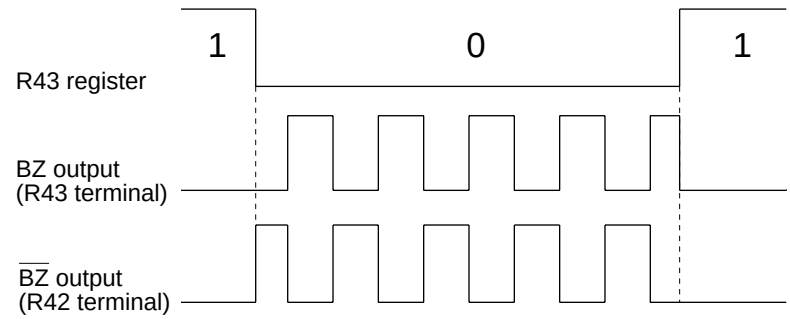


Fig. 7.2.1
Output waveform of BZ and $\overline{BZ}$

SIO Ready $\overline{SRDY}$ (R33)

When output port R33 is selected as $\overline{SRDY}$ output, it will generate a Ready signal which will indicate whether the serial interface is available to transmit or receive signals.
See Chapter 11, "SERIAL INTERFACE" for details.

PTCLK (R33)

The operating clock for the programmable timer is outputed externally from this port. In this case, the clock output ON or OFF may be controlled from the R33 register by setting PTCOUT (F79H [D3]) to "1". The clock frequency is selected by the 3 bits register of PTC0–PTC2.
Moreover, when PTCOUT is set to "0", output port R33 becomes DC output.
Because of the above functions, PTCLK output and DC output belong to a common option selection item.
Refer to "10.3 Programmable Timer" regarding selection of clock frequency.

Control of R33 output

3 states output or 2 states output for output port R33 may be selected with the mask option.
When $\overline{\text{SRDY}}$ is selected for R33, 2 states output is ordinarily selected in compliance with it.
Moreover, although 2 states output may be selected even during the selection of DC output and PTCLK output, caution is required as output becomes undefined (i.e., it will not be initially reset) when power is supplied.

Clock outputs FOUT (R42)
$\overline{\text{FOUT}}$ (R40)

When R40 and R42 are selected to clock output, it outputs the clock of f_{OSC3}, f_{OSC1} or the demultiplied f_{OSC1}. The clock frequency is selectable with the mask options, from the frequencies listed in Table 7.2.1.

Table 7.2.1
FOUT clock frequency

Setting	Clock frequency (Hz)
f_{OSC3}	OSC3 oscillation frequency
f_{OSC1} / 1	32,768
f_{OSC1} / 2	16,384
f_{OSC1} / 4	8,192
f_{OSC1} / 8	4,096
f_{OSC1} / 16	2,048
f_{OSC1} / 32	1,024
f_{OSC1} / 64	512
f_{OSC1} / 128	256

R40 ($\overline{FOUT}$) output generates an antiphase clock in relation to R42 (FOUT).
Figure 7.2.2 shows the output waveform of FOUT and $\overline{FOUT}$.

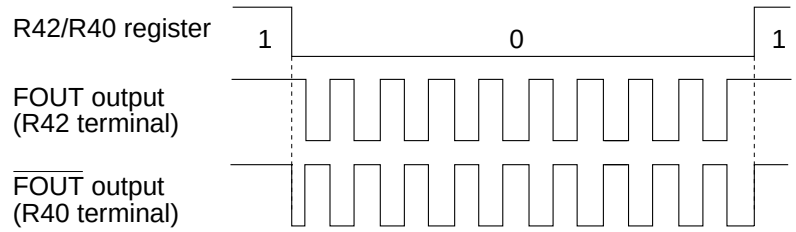


Fig. 7.2.2
Output waveform of FOUT and $\overline{FOUT}$

Note *Clock output signal could generate hazards during ON/OFF switching.*

LCD synchronous signal CL (R40) and LCD frame signal FR (R41)

S1C62440/4A0/4C0/480 are able to generate LCD synchronous signal and LCD frame signal to provide for cases when expansion LCD driver (S1D15201F10A∗) is externally connected.
By setting the R40 and R41 registers individually to "0", CL signal and FR signal are generated from the R40 and R41 terminals, respectively.
The CL signal can select from one of two types, the CL-16 for 1/16 duty or the CL-8 for 1/8 duty.
The respective frequency of CL-16 signal, CL-8 signal and FR signal are 1,024 Hz, 512 Hz and 32 Hz; FR signal synchronizes with the rising edge of CL signal and changes.
The output waveforms of CL and FR signals are shown in Figures 7.2.3(a) and (b).

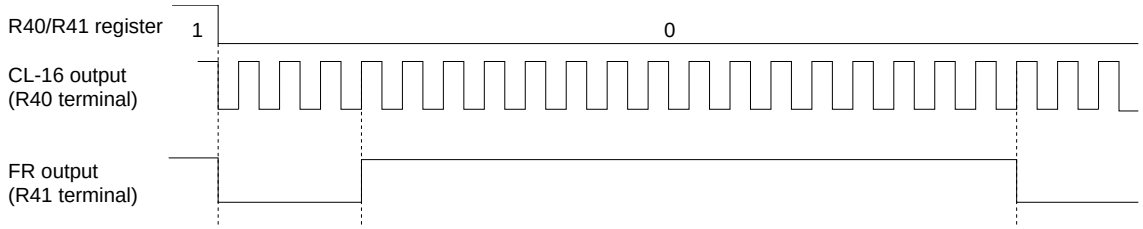


Fig. 7.2.3(a)
Output waveform of CL-16, FR

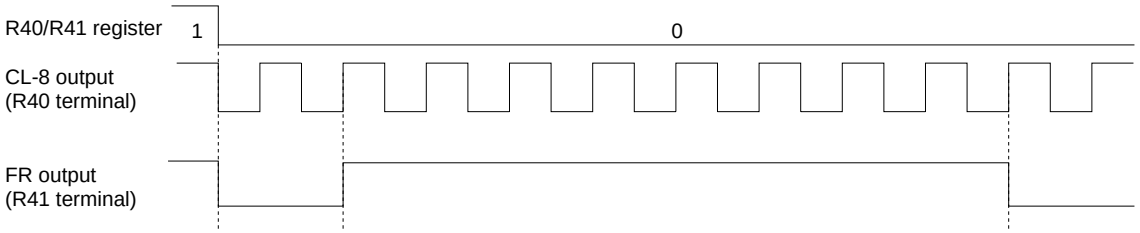


Fig. 7.2.3(b)
Output waveform of CL-8, FR

*Note Do not use the CL and FR signals for purposes other than to supply signal to the expansion LCD driver (*S1D15201F10A∗*).*

7.3 Control of Output Ports

High impedance control

The terminal output state of output ports R00–R03, R10–R13, R20–R23, and R30–R33, may be selected for high impedance state through the software in 4 bits groups. Control is done with the high impedance control registers (HZR0–HZR3).
In the case of the S1C62440, the output ports R20–R23 and R30–R33 can effect high impedance control by HZR2 and HZR3.

Control registers of output ports

The control registers for the output ports are explained below.

Table 7.3.1(a) Control registers of output ports (1)

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F50H *2	R03	R02	R01	R00	R03	X	High	Low	Output port (R03)
							High	Low	External memory address (A3)
	R/W				R02	X	High	Low	Output port (R02)
							High	Low	External memory address (A2)
					R01	X	High	Low	Output port (R01)
							High	Low	External memory address (A1)
					R00	X	High	Low	Output port (R00)
							High	Low	External memory address (A0)
F51H *2	R13	R12	R11	R10	R13	X	High	Low	Output port (R13)
							High	Low	External memory address (A7)
	R/W				R12	X	High	Low	Output port (R12)
							High	Low	External memory address (A6)
					R11	X	High	Low	Output port (R11)
							High	Low	External memory address (A5)
					R10	X	High	Low	Output port (R10)
							High	Low	External memory address (A4)
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R23)
							High	Low	External memory address (A11) *1
	R/W				R22	X	High	Low	Output port (R22)
							High	Low	External memory address (A10) *1
					R21	X	High	Low	Output port (R21)
							High	Low	External memory address (A9) *1
					R20	X	High	Low	Output port (R20)
							High	Low	External memory address (A8) *1
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W								[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X	High	Low	Output port (R32)
									[External memory read ($\overline{\text{RD}}$)] *1
					R31	X	High	Low	Output port (R31)
							High	Low	External memory address (A13) *1
									[External memory write ($\overline{\text{WR}}$)] *1
					R30	X	High	Low	Output port (R30)
							High	Low	External memory address (A12) *1

Table 7.3.1(b) Control registers of output ports (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output (BZ)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output (FOUT)
							Off	On	LCD synchronous signal (CL)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
	R/W				HZR2	0	Output	High-Z	R20–R23 output high-impedance control
					HZR1	0	Output	High-Z	R10–R13 output high-impedance control *3
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control *3

*1 In the S1C62440, it can be used only as a port for output
*2 In the S1C62440, the F50H and F51H cannot be used
*3 In the S1C62440, it is a register that becomes invalid and during reading it is always "0"

HZR0–HZR3 (F7BH, R/W) Controls high impedance loading to output ports R00–R03, R10–13, R20–R23 and R30–R33 in units of 4 bits groups.

When "1" is written: Data output
When "0" is written: High impedance
Reading: Valid

By writing "1" in the control registers (HZR0–HZR3) corresponding to the groups, the output register data is generated in the terminal; writing "0" will generate high impednce state.
During initial reset, these registers are set to "0" and the ports acquire high impedance state.
In the S1C62440 HZR0 and HZR1 become invalid and always become "0" during reading.

When DC output

R00–R03, R10–R13, R20–R23, R30–R33, R40–R43 (F50H, F51H, F52H, F53H, F54H, R/W)

When DC output is selected

Sets the output data for the output ports.

When "1" is written:	High level
When "0" is written:	Low level
Reading:	Valid

Output port terminals will generate the data written into the corresponding registers (R00–R03, .. R40–R43) as it is. The output port terminal goes high (V_{DD}) when "1" is written to the register, and goes low (V_{SS}) when "0" is written.
At initial reset, only R40–R43 are set to "1" and the other output registers become undefined.
The output ports R00–R03 and R10–R13 are not set for the S1C62440.

When special output

R43 (F54H [D3], R/W)

When BZ and $\overline{BZ}$ output is selected

Performs the output control of buzzer signal (BZ, $\overline{BZ}$).

When "0" is written:	Buzzer signal output
When "1" is written:	Low level (DC)
Reading:	Valid

When "0" is set on R43, BZ signal is generated from R43 terminal; at the same time, $\overline{BZ}$ signal (BZ inverted signal) is generated from R42 terminal if R42 is set to $\overline{BZ}$ output.
When "1" is set on R43, R43 terminal (and R42 terminal too, when $\overline{BZ}$ output is selected) output goes low (V_{SS}).
Note, however, that R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (R42 terminal output).
At initial reset, R43 and R42 are set to "1".

R33 (F53H [D3], R/W)

When PTCLK (DC) output is selected

Controls the output of the programmable timer operating clock (PTCLK).

When "0" is written:	Clock output
When "1" is written:	High level (DC)
Reading:	Valid

With "1" written on PTCOUT (F79H [D3]), the operating clock of the programmable timer may be generated externally by writing "0" on R33 register. Moreover, the output will go high (V_{DD}) by writing "1".
However, when PTCOUT is "0", the output becomes regular DC output.
Because this register is not initialized during initial reset, R33 terminal becomes undefined when 2 states output is selected with mask option.

R40, R42 (F54H [D0, D2], R/W)

When FOUT and $\overline{FOUT}$ output is selected

Controls the $\overline{FOUT}$ and FOUT (clock) output.

When "0" is written:	Clock output
When "1" is written:	High level (DC)
Reading:	Valid

When R42 is set to FOUT output, clock with the specified frequency is generated from R42 terminal by writing "0" on R42 register.
By writing "1", the R42 terminal will go high (V_{DD}).
The same applies to R40. The clock phase when $\overline{FOUT}$ signal is output from R40 is antiphase to that of R42.
At initial reset, R40 and R42 are set to "1".

R40, R41 When CL and FR output is selected
(F54H [D0, D1], R/W)

Controls the output of the LCD synchronous signal and frame signal.

When "0" is written:	Synchronous signal and frame signal output
When "1" is written:	High level (DC)
Reading:	Valid

By setting R40 and R41 registers to "0", LCD synchronous signal (CL) and LCD frame signal (FR) can be generated from R40 and R41 terminals, respectively, making it possible to drive the expansion LCD driver (S1D15201F10A*) externally. At initial reset, R40 and R41 registers are set to "1".

7.4 Programming Notes

(1) When BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

CHAPTER 8 I/O PORTS (Pxx)

8.1 Configuration of I/O Ports

The S1C624A0/4C0/480 have 16 bits (4 bits × 4, P00–P03, P10–P13, P20–P23, and P30–P33), and S1C62440 has 12 bits (4 bits × 3, P00–P03, P10–P13 and P20–P23) general I/O ports built-in.

Figure 8.1.1 shows the configuration of the I/O port.

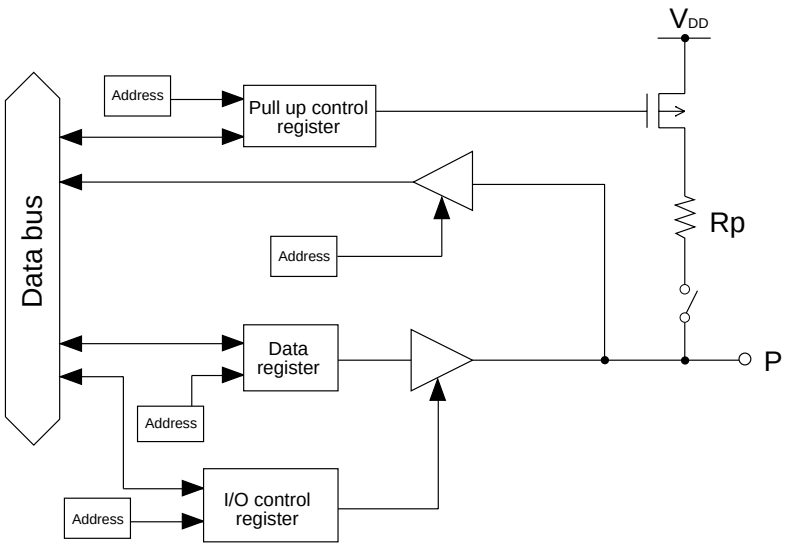


Fig. 8.1.1
Configuration of I/O port

8.2 Mask Option

The I/O ports P00–P33 may be selected for the following by mask option.

(1) Output specification during output mode

Output specification (during output) for each I/O port may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

P00–P03: Complementary or Nch open drain
(selected with the 4 bits group)
P10–P13: Complementary or Nch open drain
(selected with the 4 bits group)
P20–P22: Complementary or Nch open drain
(select in units of 1 bit)
P30–P33: Complementary or Nch open drain
(select in units of 1 bit) *

* Only for S1C624A0/4C0/480.

(2) External memory access

In the S1C624A0/4C0/480 I/O ports P00–P03, P10–P13, and P20–P23 may be set with the mask option as external memory access as follows:

P00–P03: External memory data (D0–D3)
P10–P13: External memory data (D4–D7)
(selected with the 8 bits group P00–P13)
P20–P23: External memory chip select ($\overline{CS0}$–$\overline{CS3}$)
(select in units of 1 bit)

The control of memory access is explained in Chapter 13.

(3) Dedicated output port

I/O ports P30–P33 of S1C624A0/4C0/480 may be set with the mask option as dedicated output ports.
This selection may be conducted by 1 bit.

8.3 Control of I/O Ports

I/O control register and input/output mode

When using an I/O port as Pxx (x = 0 to 3), input/output direction may be set by group, with 4 bits each of Px0 to Px3 (x = 0 to 3) considered as one group. Modes can be set by writing input/output direction data to the I/O control register corresponding I/O port group.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance state and works as an input port.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the data of output register is "1", and a low level (V_{SS}) when the data of output register is "0".

Setting of the I/O control register is not effective for external memory access through the mask option or for ports set as dedicated output.

Pull up resistor

The common input/output ports can be selected through the software to apply pull up resistor in 4 bits groups. Selection of pull up resistor application is done by writing data to the pull up resistor control registers (PUP0–PUP3).

Control register of I/O ports

The control registers for the I/O ports are explained below.

Table 8.3.1 Control register of I/O ports

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P03)
							High	Low	External memory data (D3) *1
	R/W				P02	X	High	Low	I/O port (P02)
							High	Low	External memory data (D2) *1
					P01	X	High	Low	I/O port (P01)
							High	Low	External memory data (D1) *1
					P00	X	High	Low	I/O port (P00)
							High	Low	External memory data (D0) *1
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P13)
							High	Low	External memory data (D7) *1
	R/W				P12	X	High	Low	I/O port (P12)
							High	Low	External memory data (D6) *1
					P11	X	High	Low	I/O port (P11)
							High	Low	External memory data (D5) *1
					P10	X	High	Low	I/O port (P10)
							High	Low	External memory data (D4) *1
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P23)
							High	Low	External memory chip select ($\overline{CS3}$) *1
	R/W W				P22	X	High	Low	I/O port (P22)
							High	Low	External memory chip select ($\overline{CS2}$) *1
					P21	X	High	Low	I/O port (P21)
							High	Low	External memory chip select ($\overline{CS1}$) *1
					P20	X	High	Low	I/O port (P20)
							High	Low	External memory chip select ($\overline{CS0}$) *1
F63H *2	P33	P32	P31	P30	P33	X	High	Low	I/O port (P33)
							High	Low	Dedicated output port (P33)
	R/W				P32	X	High	Low	I/O port (P32)
							High	Low	Dedicated output port (P32)
					P31	X	High	Low	I/O port (P31)
							High	Low	Dedicated output port (P31)
					P30	X	High	Low	I/O port (P30)
							High	Low	Dedicated output port (P30)
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33) *3
	R/W				IOC2	0	Output	Input	I/O control (P20–P23)
					IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33) *3
	R/W				PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
					PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 In the S1C62440, it can be used only as a port for I/O port
*2 In the S1C62440, the F63H cannot be used
*3 In the S1C62440 it is a register that becomes invalid and during reading it is always "0"

IOC0, IOC1, IOC2, IOC3 (F7DH, R/W)

Input/output direction of I/O ports are set in units of 4 bits groups.

When "1" is written:	Output mode
When "0" is written:	Input mode
Reading:	Valid

IOCx (I/O control register) and port group correspondence are as follows:

IOC0:	P00–P03
IOC1:	P10–P13
IOC2:	P20–P23
IOC3:	P30–P33

By writing "1" to IOCx (x = 0 to 3), the I/O ports in the corresponding group are placed in the output mode, while writing "0" place them in the input mode.
At initial reset, IOCx are set to "0" and the I/O ports are all in the input mode.
In the S1C62440 IOC3 become invalid and always become "0" during reading.

PUP0, PUP1, PUP2, PUP3 (F7EH, R/W)

Whether the I/O ports will be pulled up or not is set in units of 4 bits groups.

When "0" is written:	Pull up ON
When "1" is written:	Pull up OFF
Reading:	Valid

PUPx and port group correspondence are the same as that of the IOCx.
By writing "0" to PUPx (x = 0 to 3), the I/O ports in the corresponding group are pulled up, while writing "1" turns the pull up function OFF.
At initial reset, PUPx are set at "0", and all I/O ports are pulled up.
In the S1C62440 PUP3 become invalid and always become "0" during reading.

P00–P03, P10–P13, P20–P23, P30–P33 (F60H, F61H, F62H, F63H, R/W)

• During writing operation

When "1" is written: High level
When "0" is written: Low level

When the I/O port is set at output port, the data written is generated on the I/O port terminal as it is. When "1" is written as port data, the port terminal goes high (V_{DD}) and goes low (V_{SS}) when "0" is written.
This is the same when P30–P33 are set as dedicated output ports through the mask option.
Note, however, that even at input mode, port data writing is also possible.

• During reading operation

When "1" is read: High level
When "0" is read: Low level

Reading the I/O port terminal voltage level. When the I/O port is at input mode, voltage level input of the port terminal is read; when set at output mode, output voltage level is read. When the terminal voltage is at High (V_{DD}) level, port data reading is "1"; at Low (V_{SS}) level, it is "0".

P30–P33 are not set for the S1C62440.

8.4 Programming Notes

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
– The input/output mode is set at output mode
– Output specification is set at Nch open drain
– The content of the data register is "1"
– The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

CHAPTER 9 LCD DRIVER

The S1C62440/4A0 have 16 common terminals and 40 segment terminals and can drive a maximum of 640 (40 × 16) dots (8 characters × 2 lines) LCD.
The S1C624C0/480 can be expanded to 51 segment terminals and can drive a maximum 816 (51 × 16) dots (10 characters × 2 lines) LCD.
This LCD driver performs the following control through the software.

– Drive duty can be set to 1/16 or 1/8 duty.

– LCD contrast can be adjusted through a 16 steps range.

– All dots of the LCD panel can be switched ON and OFF.

9.1 Drive Duty

Because the power for LCD driving is generated by the internal circuit of the CPU, there is no need to provide for it externally. Driving is done by 1/16 duty or 1/8 duty dynamic drive through 4 electric potentials (1/4 bias) : V_{L1}, V_{L2}, V_{L4}, and V_{L5}. The 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set.
Drive duty may be selected from the software. Dot number differences due to the selected duty are shown in Table 9.1.1.

Table 9.1.1 Differences due to selected duty

Duty	Common terminal in use	Maximum dot number	Frame frequency *
1/16	COM0–15	640 dots (S1C62440/4A0) 816 dots (S1C624C0/480)	32 Hz
1/8	COM0–7	320 dots (S1C62440/4A0) 408 dots (S1C624C0/480)	32 Hz

* Frame frequency = f_{OSC1}/1,024

Figure 9.1.1 shows the drive waveform for 1/16 duty (1/5 bias), and Figure 9.1.2 shows the drive waveform for 1/8 duty (1/4 bias).

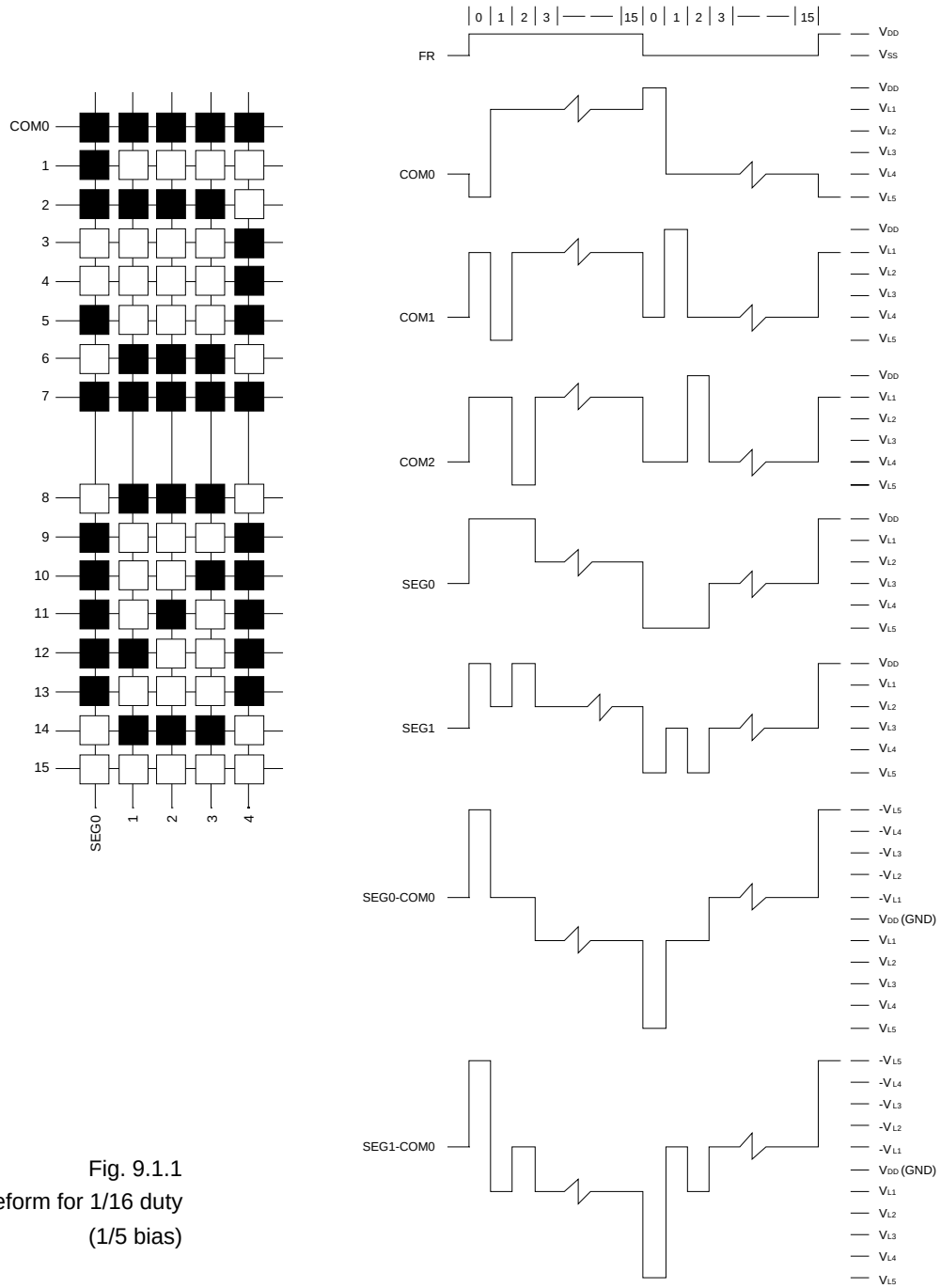


Fig. 9.1.1
Drive waveform for 1/16 duty
(1/5 bias)

Note *1/5 bias may only be utilized when power for LCD driving is supplied externally; when internal power circuit is used, 1/4 bias is utilized.*

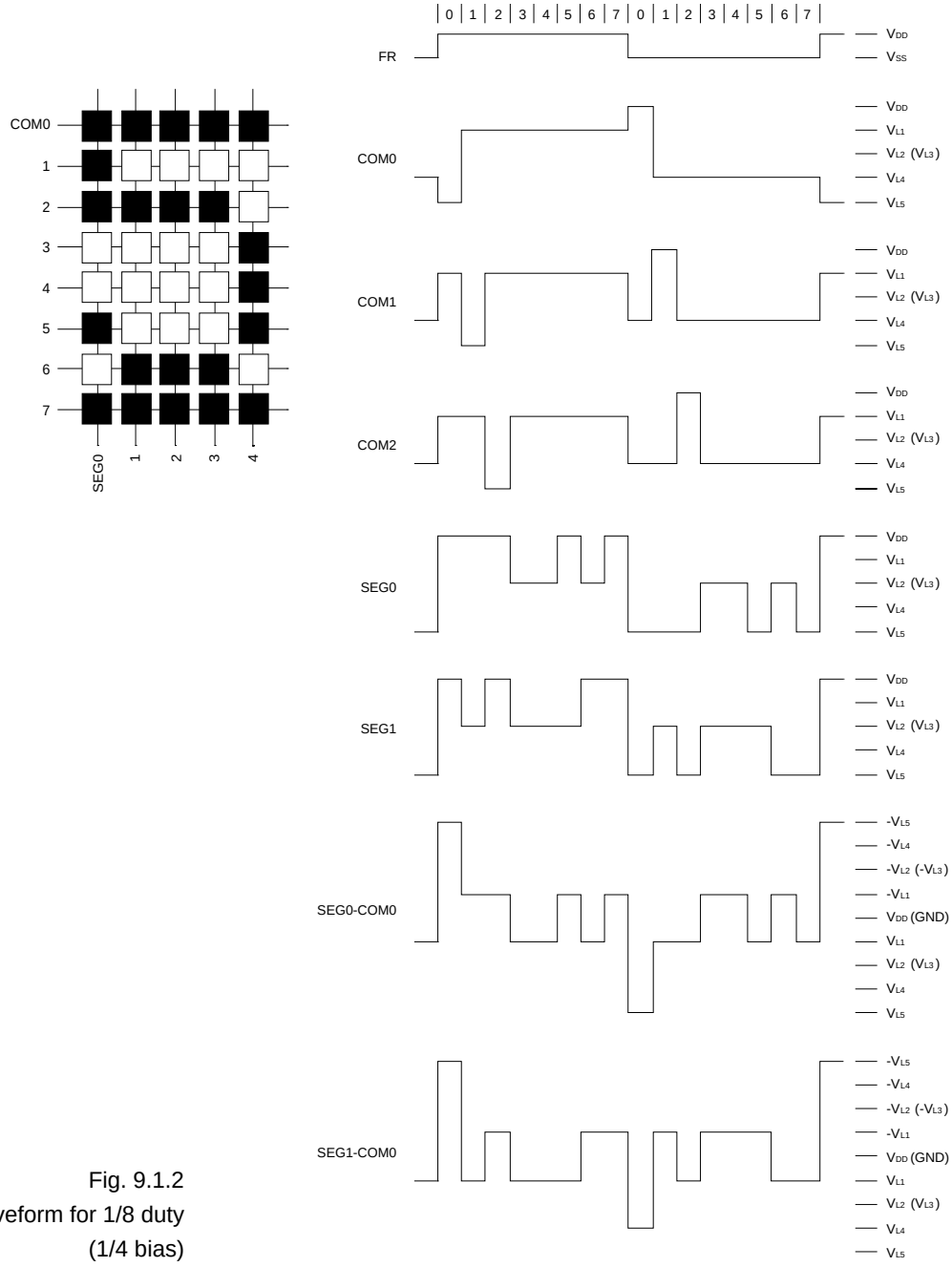


Fig. 9.1.2
Drive waveform for 1/8 duty
(1/4 bias)

9.2 Mask Option

Disconnecting the internal power for LCD driving will enable electric potentials to be supplied externally. In such case, the 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.
Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 9.2.1.

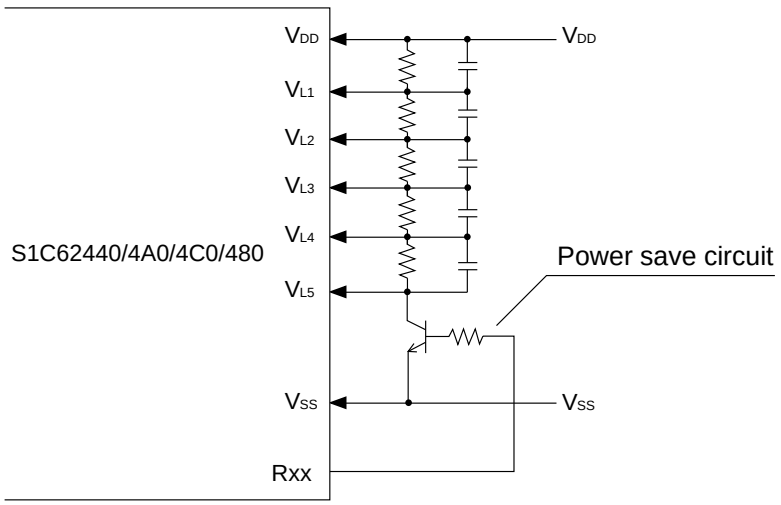


Fig. 9.2.1
A sample circuit of external power for LCD driving when power is supplied externally

9.3 Segment Data Memory

The segment data memory of S1C62440/4A0 is allocated to the built-in RAM addresses E00H–E4FH and E80H–ECFH, and S1C624C0/480 is allocated to the built-in RAM addresses E00H–E65H and E80H–EF5H.
Figures 9.3.1(a) and (b) show the correspondence between the segment data memory and the LCD dot matrix.

S1C62440/4A0

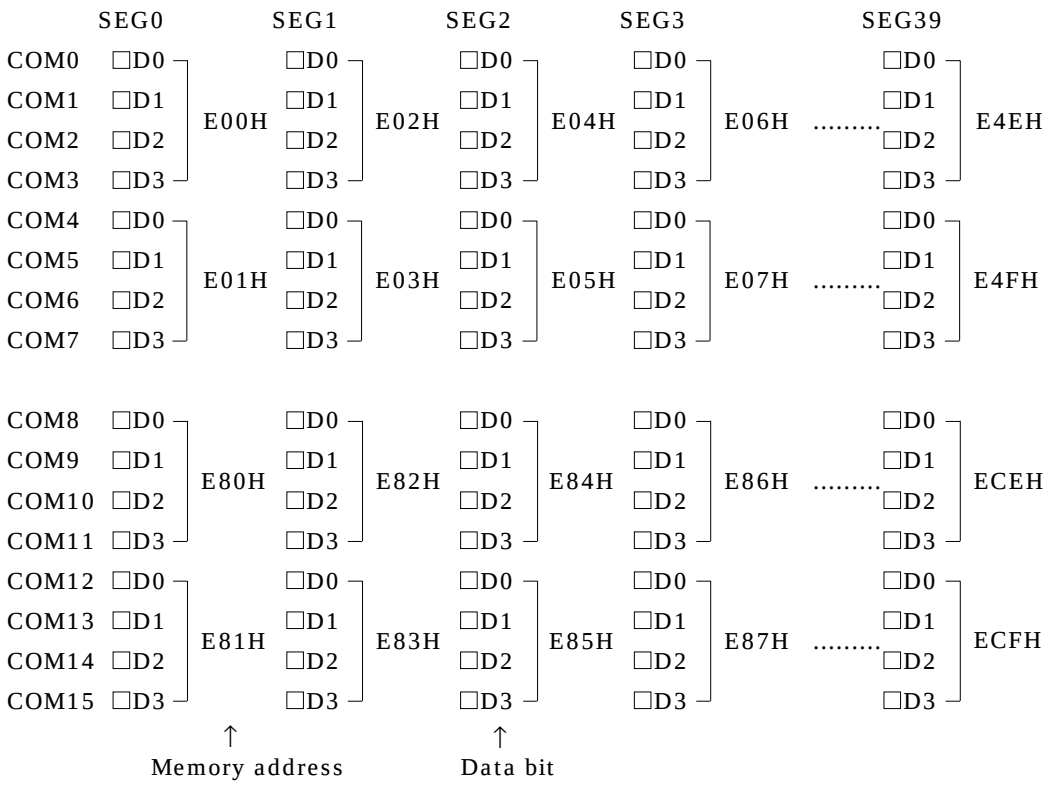


Fig. 9.3.1(a)
LCD dot matrix and segment memory correspondence (S1C62440/4A0)

S1C624C0/480

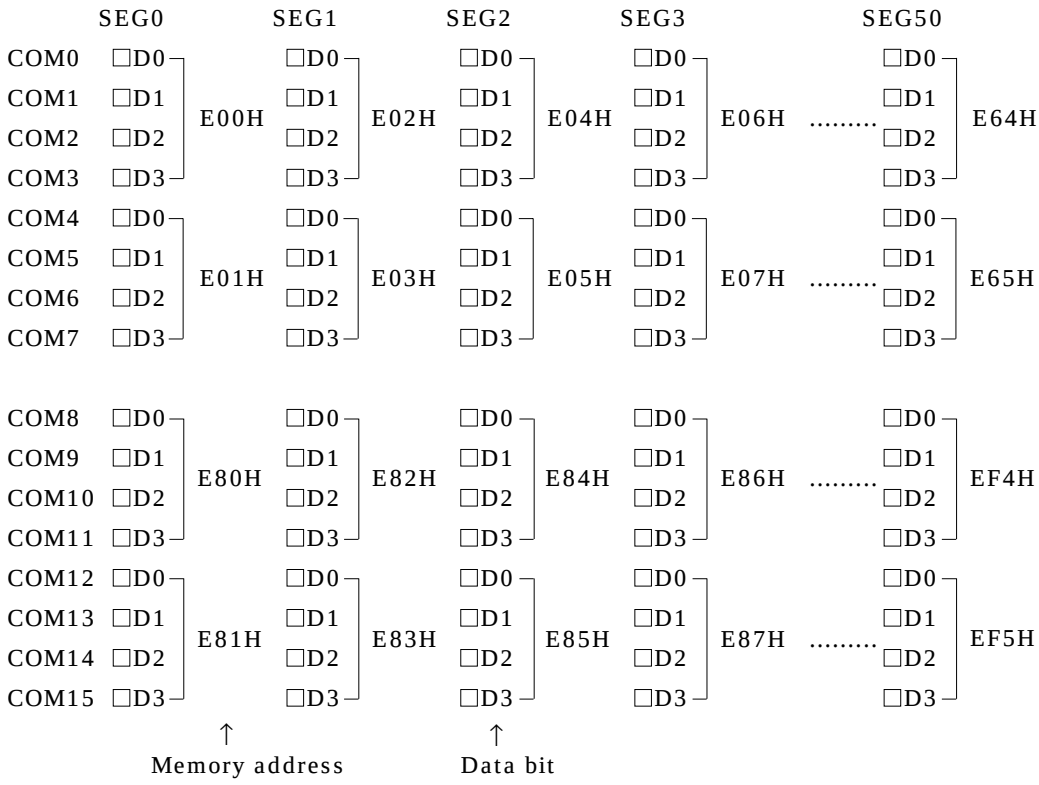


Fig. 9.3.1(b)
LCD dot matrix and segment memory correspondence (S1C624C0/480)

When the segment memory bit is assigned as "1", the corresponding LCD dot lights up, and when assigned as "0", the dot dies out.
At 1/16 duty drive and 1/8 duty drive, COM0 to COM15 lines and COM0 to COM7 lines light up, respectively.
At initial reset, the segment data memory content becomes undefined and hence, there is need to initialize by software.

9.4 Control of LCD Driver

The control registers for the LCD driver are explained below.

Table 9.4.1 Control registers of LCD driver

Address	Register				Name	SR	1	0	Comment
	D3	D2	D1	D0					
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
	R/W				ALON	0	All on	Normal	All LCD dots displayed control
					LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
	R/W				LC2	X			
					LC1	X			
					LC0	X			

LDUTY (F71H [D1], R/W) Sets the LCD drive duty.

When "1" is written: 1/8 duty
When "0" is written: 1/16 duty
Reading: Valid

Writing "1" or "0" on LDUTY will set is to 1/8 duty or 1/16 duty, respectively.
At initial reset, LDUTY is set at "0".

ALON (F71H [D2], R/W)

Displays the all LCD dots on.

When "1" is written:	All LCD dots displayed
When "0" is written:	Normal operation
Reading:	Valid

Writing "1" to ALON will display all the LCD dots on; writing "0" will set the LCD display back to normal. LCD panel testing may be conducted with this function.
Total LCD displaying at ALON = "1" is a static operation and does not affect the content of the segment data memory.
ALON precedes ALOFF.
At initial reset, ALON is set at "0".

ALOFF (F71H [D3], R/W)

Fade outs the all LCD dots.

When "1" is written:	All LCD dots fade out
When "0" is written:	Normal operation
Reading:	Valid

When "1" is written on ALOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at ALOFF = "1" is due to light out signals and does not affect the content of the segment data memory.
Flashing of the entire LCD panel is performed by this function.
At initial reset, ALOFF is set to "1".

LC0, LC1, LC2, LC3 (F72H, R/W) Will adjust the LCD contrast. Contrast may be adjusted to 16 levels as shown in Table 9.4.2.

Table 9.4.2 LCD contrast

	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
A	1	0	1	0	
B	1	0	1	1	
C	1	1	0	0	
D	1	1	0	1	
E	1	1	1	0	↓
F	1	1	1	1	dark

At room temperature, use setting number 7 or 8 as standard. Moreover, because the voltage of the LCD system power terminals V_{L1}, V_{L2}, V_{L4} and V_{L5} changes through this function, the contrast of the external expansion LCD driver may be adjusted in the same manner.
Because at initial reset, the contents of LC0–LC3 are undefined, initialize it by the software.

9.5 Programming Note

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

CHAPTER 10 TIME BASE COUNTER

10.1 Clock Timer

Configuration of clock timer

The S1C62440/4A0/4C0/480 have a clock timer with OSC1 (crystal oscillation) as basic oscillation built-in. The clock timer is configured with an 8 bits binary counter with 256 Hz signal divided from OSC1 as input clock, allowing 128 Hz–1 Hz of data to be read by the software.
Figure 10.1.1 shows the configuration of the clock timer.

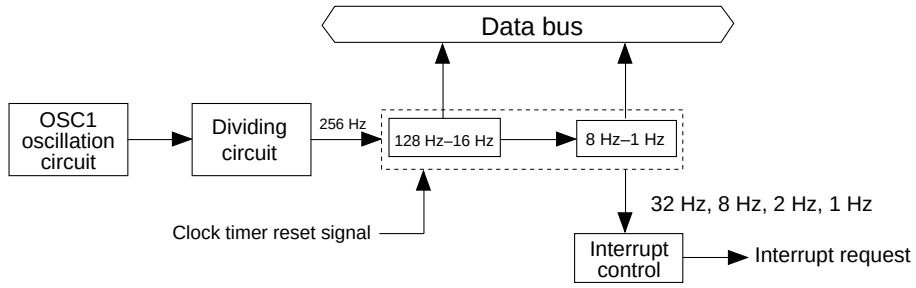


Fig. 10.1.1 Configuration of clock timer

Interrupt function

The clock timer has interrupt capability, and interrupt is generated by the falling edge of 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals.
Figure 10.1.2 shows the timing chart of the clock timer.

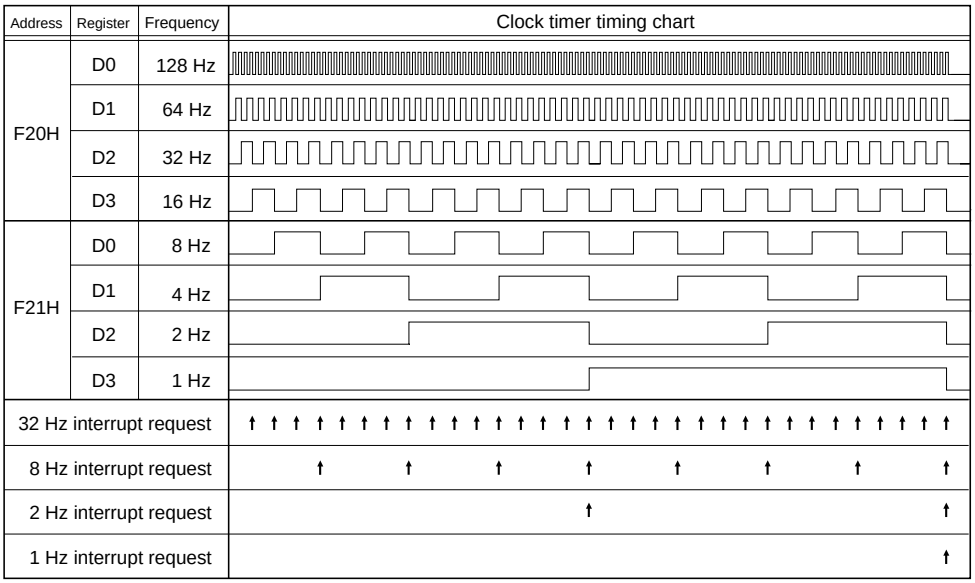


Fig. 10.1.2 Timing chart of clock timer

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT8, IT2, and IT1) is set to "1".
Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT8, EIT2, and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

Control of clock timer

The control registers for the clock timer are explained below.

Table 10.1.1 Control registers of clock timer

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F00H	IT1	IT2	IT8	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
	R				TM2	0			Clock timer data (32 Hz)
					TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
	R				TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F76H	0	0	TMRST	WDRST	0	–			
	R		W		0	–			
					TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

TMRST (F76H [D1], W)

This bit resets the clock timer.

When "1" is written:	Clock timer reset
When "0" is written:	No operation
Reading:	Always "0"

By writing "1" on TMRST, the clock timer is reset and all timer data are set to "0".
Because this bit is only for writing, it is always "0" during reading.

TM0–TM7 (F20H, F21H, R)

Will read the data of the clock timer.
TMx (x = 0–7) and frequency correspondence are as follows:

F20H		F21H	
TM0:	128 Hz	TM4:	8 Hz
TM1:	64 Hz	TM5:	4 Hz
TM2:	32 Hz	TM6:	2 Hz
TM3:	16 Hz	TM7:	1 Hz

The above 8 bits are only for reading and render writing operation invalid.
At initial reset, timer data is initialized to "0".

EIT32, EIT8, EIT2, EIT1 (F10H, R/W)

There are the interrupt mask registers of the clock timer.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

EIT32, EIT8, EIT2, and EIT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IT32, IT8, IT2, IT1 (F00H, R)

There are the interrupt factor flags of the clock timer.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

IT32, IT8, IT2, and IT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
The occurence of clock timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" due to the falling edge of the corresponding signal.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

10.2 Stopwatch Timer

Configuration of stopwatch timer

The S1C62440/4A0/4C0/480 have 1/100 sec unit (SWL) and 1/10 sec unit (SWH) stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4 bits BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software.
Figure 10.2.1 shows the configuration of the stopwatch timer.

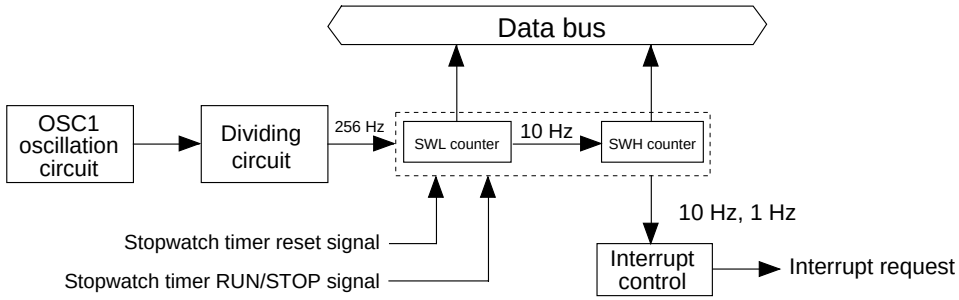


Fig. 10.2.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

Count-up pattern

The stopwatch timer is configured of 4 bits BCD counters SWL and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.
Figure 10.2.2 shows the count-up pattern of the stopwatch timer.

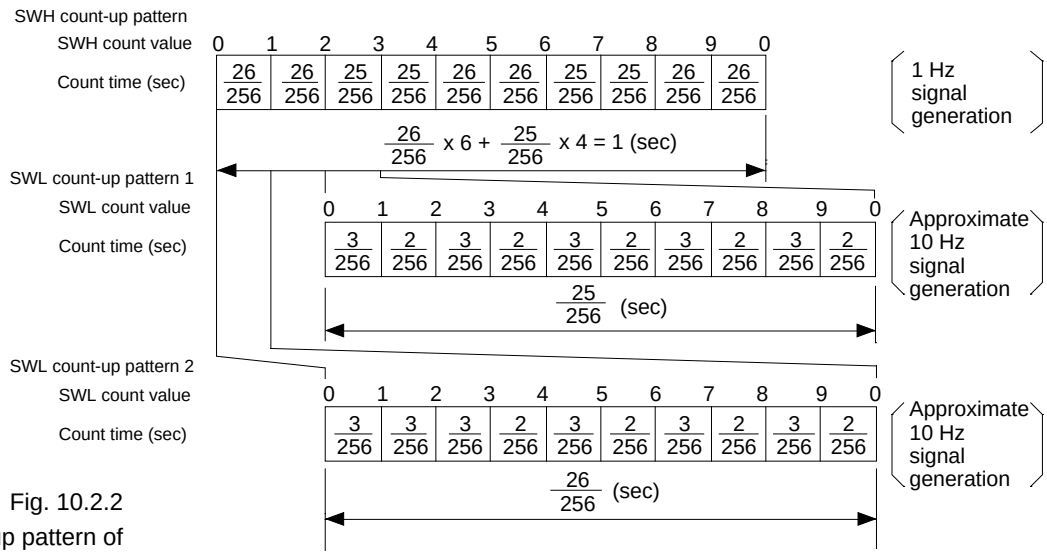


Fig. 10.2.2
Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

Interrupt function

Stopwatch timers SWL and SWH, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.
Figure 10.2.3 shows the timing chart for the stopwatch timer.

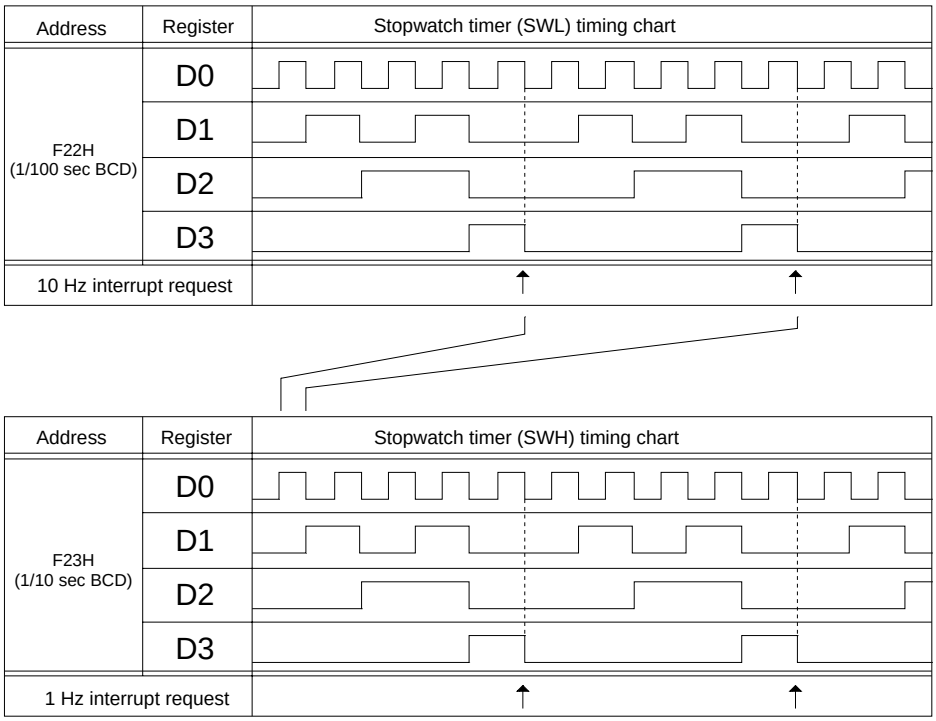


Fig. 10.2.3
Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWL and SWH (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW0 and ISW1) are set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EISW0 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

Control of stopwatch timer

The control registers for the stopwatch timer are explained below.

Table 10.2.1 Control registers of stopwatch timer

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F01H	0	0	ISW1	ISW0	0	–			
	R				0	–			
					ISW1	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F11H	0	0	EISW1	EISW0	0	–			
	R		R/W		0	–			
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec data (BCD)
					SWL1	0			
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec data (BCD)
					SWH1	0			
					SWH0	0			LSB
F77H	0	0	SWRST	SWRUN	0	–			
	R		W	R/W	0	–			
					SWRST	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

SWRST (F77H [D1], W)

This bit resets the stopwatch timer.

When "1" is written:	Stopwatch timer reset
When "0" is written:	No operation
Reading:	Always "0"

By writing "1" on SWRST, the stopwatch timer is reset. All timer data is set to "0".
When the stopwatch timer is reset in the RUN mode, it will re-start counting immediately after the reset and at STOP mode, the reset data is maintained.
Because this bit is for writing only, it is always "0" during reading.

SWRUN (F77H [D0], R/W)

This register controls RUN/STOP of the stopwatch timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

By writing "1" on SWRUN, the stopwatch timer performs counting operation. Writing "0" will make the stopwatch stop counting.
Even if the stopwatch is stopped, the timer data at that point is kept.
When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWL) into high-order digits (SWH) (i.e., in case SWL and SWH reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).
At initial reset, SWRUN is set to "0".

SWL0–SWL3 (F22H, R)
Will read the stopwatch timer data to the 1/100 sec digits (BCD).
Since these bits are for reading only, writing operation is invalidated.
At initial reset, timer data is set to "0".

SWH0–SWH3 (F23H, R)
Will read the stopwatch timer data to the 1/10 sec digits (BCD).
Since these bits are for reading only, writing operation is invalidated.
At initial reset, timer data is set to "0".

EISW0, EISW1 (F11H [D0, D1], R/W)
There are the interrupt mask registers of the stopwatch timer.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

EISW0 and EISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

ISW0, ISW1 (F01H [D0, D1], R)

There are the interrupt factor flags of the stopwatch timer.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

ISW0 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.
The occurence of stopwatch timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" by the overflow of the corresponding counters.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

(2) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

10.3 Programmable Timer

Configuration of programmable timer

The S1C62440/4A0/4C0/480 have a programmable timer with OSC1 (crystal oscillation) as basic oscillation built-in. The programmable timer is configured with an 8 bits pre-settable down counter and it has been down-count at initial value by 256 Hz–8,192 Hz signal or by the input signal of input port K03.
The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.
The down-counter data may be read through the software. Moreover, the input clock being selected may be generated to output port R33.
Figure 10.3.1 shows the configuration of the programmable timer.

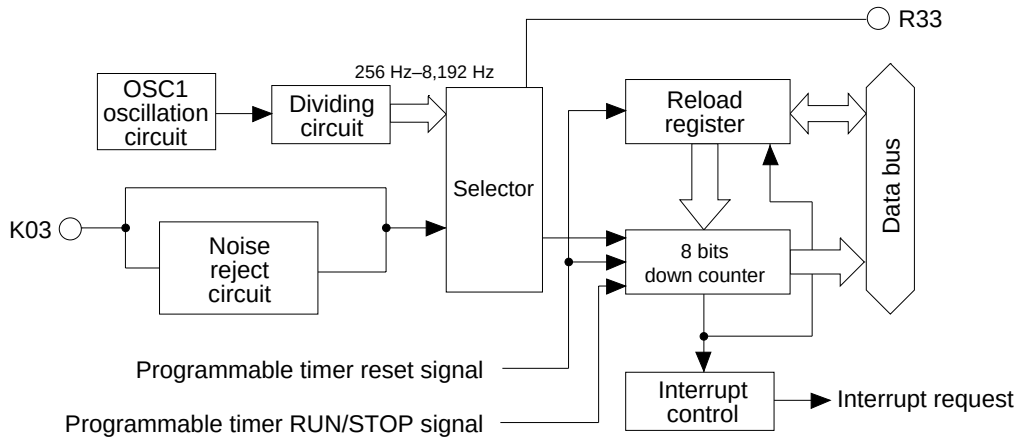


Fig. 10.3.1
Configuration of programmable timer

One input clock may be selected by software from any of the following 8 types:

(1) K03 input (with noise rejector) ┐ external clock
(2) K03 input (direct) ┘
(3) 256 Hz ┐
(4) 512 Hz │
(5) 1,024 Hz │ internal clock
(6) 2,048 Hz │
(7) 4,096 Hz │
(8) 8,192 Hz ┘

Note, however, that down-count is done at falling edges of the input signal as shown in Figure10.3.2.

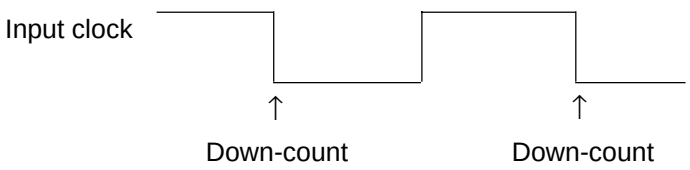


Fig. 10.3.2
Timing of down-counts

Type (1) K03 input (with noise rejector) is for counting by key entry, the input signal from which passes the 256 Hz sampling noise reject circuit. With this, no more than 2 ms of chattering is purged, and at least 4 ms signal is received.

Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.
After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.
Figure 10.3.3 shows the timing chart of the programmable timer.

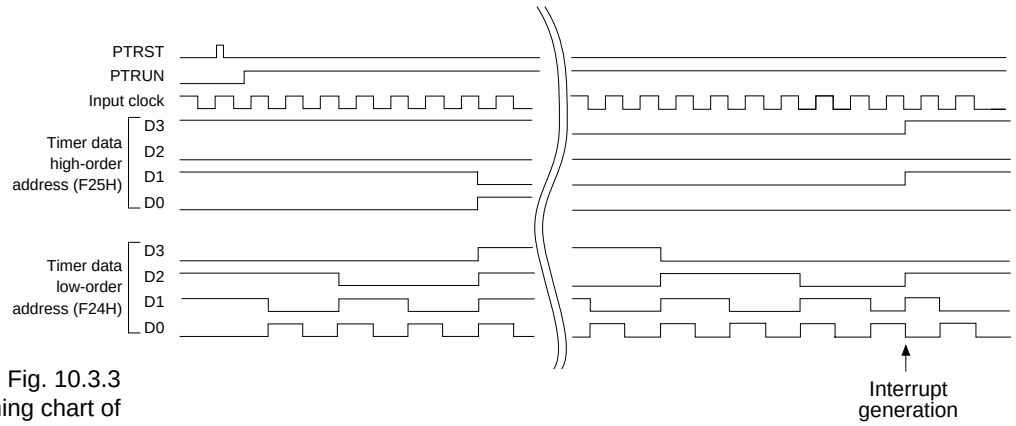


Fig. 10.3.3
Timing chart of programmable timer

Note: When "A6H" is set into reload register

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

Control of programmable timer

The control registers for the programmable timer are explained below.

Table 10.3.1(a) Control registers of programmable timer (1)

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F02H	0	0	0	IPT	0	–			
	R				0	–			
					0	–			
					IPT	0	Yes	No	Interrupt factor flag (programmable timer)
F12H	0	0	0	EIPT	0	–			
	R			R/W	0	–			
					0	–			
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F24H	PT3	PT2	PT1	PT0	PT3	X			MSB
	R				PT2	X			
					PT1	X			Programmable timer data (low-order)
					PT0	X			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X			MSB
	R				PT6	X			
					PT5	X			Programmable timer data (high-order)
					PT4	X			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X			MSB
	R/W				RD2	X			Programmable timer reload data (low-order)
					RD1	X			
					RD0	X			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X			MSB
	R/W				RD6	X			Programmable timer reload data (high-order)
					RD5	X			
					RD4	X			LSB

Table 10.3.1(b) Control registers of programmable timer (2)

Address	Register				Name	SR	1	0	Comment
	D3	D2	D1	D0					
F78H	0	0	PTRST	PTRUN	0	–			
	R		W	R/W	0	–			
					PTRST	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0			Programmable timer clock output
	R/W				PTC2	0			Programmable timer input clock selection
					PTC1	0			
					PTC0	0			

PTC0, PTC1, PTC2 (F79H [D0–D2], R/W) Selects the input clock. The PTC0–PTC2 setting and input clock correspondence is shown in Table 10.3.2.

Table 10.3.2 Input clock setting

PTC2	PTC1	PTC0	Input Clock
0	0	0	K03 input (with noise rejector)
0	0	1	K03 input (direct)
0	1	0	256 Hz
0	1	1	512 Hz
1	0	0	1,024 Hz
1	0	1	2,048 Hz
1	1	0	4,096 Hz
1	1	1	8,192 Hz

PTCOUT (F79H [D3], R/W) Generates the input clock being selected to output port R33. Refer to Chapter 7, "OUTPUT PORTS" regarding control methods.

RD0–RD3, RD4–RD7 (F26H, F27H, R/W)

These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is 00H.
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, this register will be undefined.

PTRST (F78H [D1], W)

This bit resets the programmable timer.

When "1" is written:	Programmable timer reset
When "0" is written:	No operation
Reading:	Always "0"

By writing "1" on PTRST, the programmable timer is reset. The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN (F78H [D0], R/W)

This register controls RUN/STOP of the programmable timer.

When "1" is written:	RUN
When "0" is written:	STOP
Reading:	Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
When data of the counter is read at the RUN mode, proper reading may not be obtained due to the carry from the low-order digits (PT0–PT3) into the high-order digits (PT4–PT7) (when the reading of the low-order digits and high-order digits span the timing of the carry). To avoid this occurence, perform the reading after suspending the programmable timer once, and set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty).
At initial reset, PTRUN is set to "0".

PT0–PT3, PT4–PT7 (F24H, F25H, R)

Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
At initial reset, timer data will be undefined.

EIPT (F12H [D0], R/W) This is the interrupt mask register of the programmable timer.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

IPT (F02H [D0], R) This is the interrupt factor flag of the programmable timer.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

Programming notes

(1) When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than a 256 Hz, high speed processing by OSC3 is required.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 11 SERIAL INTERFACE (SIN, SOUT, and $\overline{\text{SCLK}}$)

11.1 Configuration of Serial Interface

The S1C62440/4A0/4C0/480 have a synchronous clock type 8 bits serial interface built-in.

The configuration of the serial interface is shown in Figure 11.1.1.

The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal.

The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the S1C62440/4A0/4C0/480 are to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C62440/4A0/4C0/480 are to be the slave for serial input/output).

Also, when the serial interface is used at slave mode, $\overline{\text{SRDY}}$ (SIO READY) signal which indicates whether or not the serial interface is available to transmit or receive can be output to output port R33 by mask option.

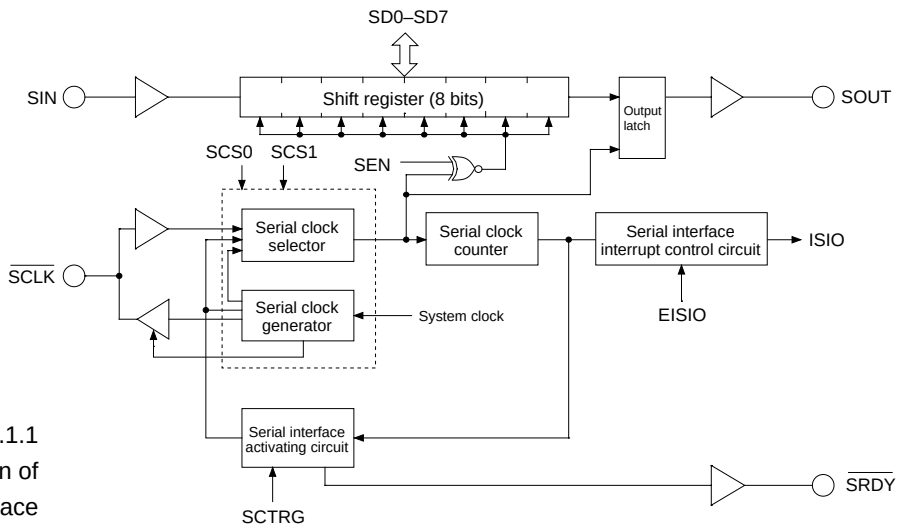


Fig. 11.1.1 Configuration of serial interface

11.2 Mask Option

The serial interface may be selected for the following by mask option.

(1) Whether or not the SIN terminal will use built-in pull up resistor may be selected.
If the use of no pull up resistor is selected, take care that floating state does not occur at the SIN terminal.

(2) Either complementary output or N channel (Nch) open drain as output specification for the SOUT terminal may be selected.
However, even if Nch open drain has been selected, application of voltage exceeding power source voltage to the SOUT terminal will be prohibited.

(3) Whether or not the $\overline{\text{SCLK}}$ terminal will use pull up resistor which is turned ON during input mode (external clock) may be selected.
If the use of no pull up resistor is selected, take care that floating state does not occur at the $\overline{\text{SCLK}}$ terminal during input mode.
Normally, the use of pull up resistor should be selected.

(4) As output specification during output mode, either complementary output or N channel (Nch) open drain output may be selected for the $\overline{\text{SCLK}}$ terminal. However, even if the same Nch open drain as that of the SOUT terminal is selected, application of voltage exceeding the power current voltage is not permitted.

(5) LSB first or MSB first as input/output permutation of serial data may be selected.

(6) Output port R33 may be assigned as $\overline{\text{SRDY}}$ output terminal which will indicate whether the serial interface is available to transmit or receive signals.

11.3 Master Mode and Slave Mode of Serial Interface

The serial interface of the S1C62440/4A0/4C0/480 have two types of operation mode: master mode and slave mode. In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the $\overline{SCLK}$ terminal and controls the external (slave side) serial interface.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{SCLK}$ terminal and uses it as the synchronous clock to the built-in shift register.
The master mode and slave mode are selected through registers SCS0 and SCS1; when the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 11.3.1.

Table 11.3.1
Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

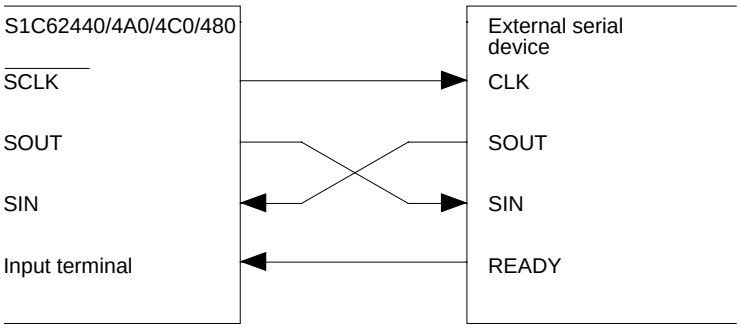
At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input /output of the 8 bits serial data, is controlled as follows:

– At master mode, after output of 8 clocks from the $\overline{SCLK}$ terminal, clock output is automatically suspended and $\overline{SCLK}$ terminal is fixed at high level.

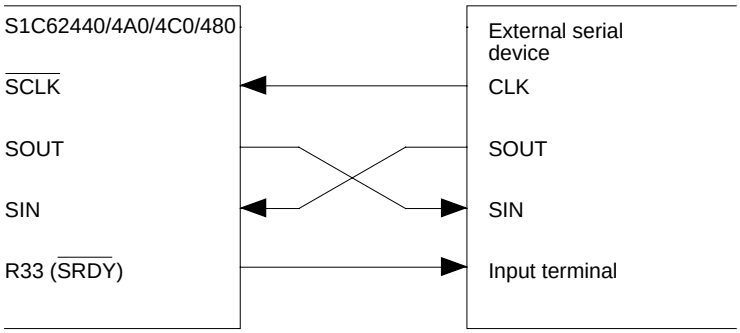
– At slave mode, after input of 8 clocks to the $\overline{SCLK}$ terminal, subsequent clock inputs are masked.

Note *When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.*

A sample basic serial input/output portion connection is shown in Figure 11.3.1.



a. Master mode



b. Slave mode

Fig. 11.3.1
Sample basic connection of serial input/output section

11.4 Data Input/Output and Interrupt Function

The serial interface of S1C62440/4A0/4C0/480 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from $\overline{SCLK}$ terminal (master mode), or the synchronous clock input to $\overline{SCLK}$ (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock ($\overline{SCLK}$); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure

The S1C62440/4A0/4C0/480 serial interface is capable of outputting parallel data as serial data, in units of 8 bits.
By setting the parallel data to data registers SD0–SD3 and SD4–SD7 individually and writing "1" to SCTRG (F7AH[D3]), it synchronizes with the synchronous clock and serial data is output at the SOUT terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ terminal. The serial output of the SOUT terminal changes with the falling edge of the clock that is input or output from the $\overline{SCLK}$ terminal.

When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8 bits data.

(2) Serial data input procedure

The S1C62440/4A0/4C0/480 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. By writing "1" to SCTRG, the serial data is input from the SIN terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ terminal. The serial data to the built-in shift register is read with the falling edge of the $\overline{\text{SCLK}}$ signal when SEN bit is "1" and is read with the rising edge of the $\overline{\text{SCLK}}$ signal when SEN bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

Also, the data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The S1C62440/4A0/4C0/480 allow the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 11.4.1.

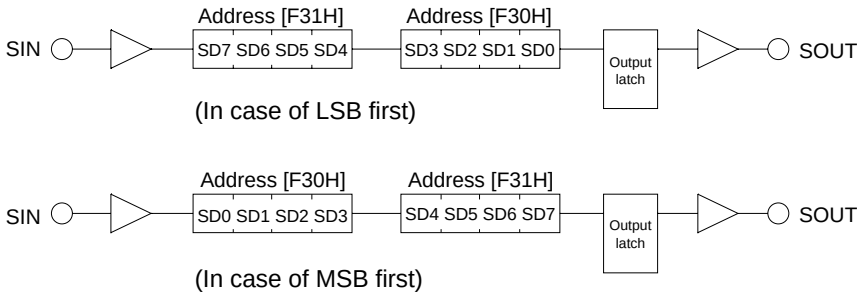


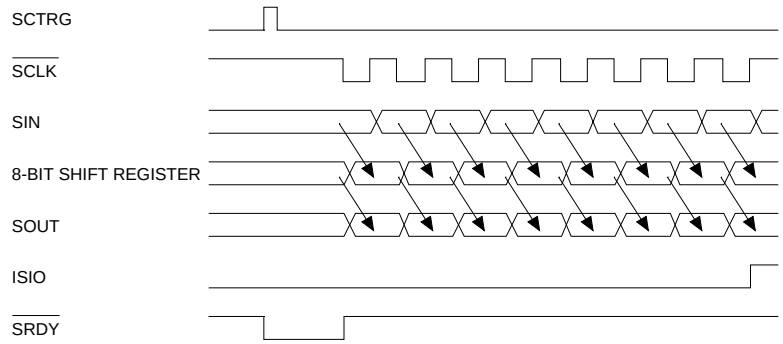
Fig. 11.4.1
Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

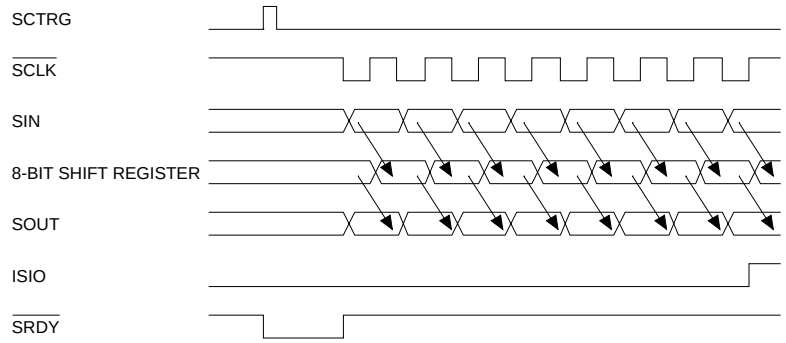
When the S1C62440/4A0/4C0/480 serial interface are used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is generated from output port R33 by mask option.
$\overline{\text{SRDY}}$ signal becomes "0" (low) when the S1C62440/4A0/4C0/480 serial interface become available to transmit or receive data; normally, it is at "1" (high).
$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to $\overline{\text{SCLK}}$ terminal (i.e., when the serial input/output begins transmitting or receiving data).
Moreover, when data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".
Moreover, the operating state (wait state or transmitting/receiving state) of the serial interface may be checked by connecting output port R33 ($\overline{\text{SRDY}}$) to input port (Kxx) or I/O port (Pxx) and performing reading.

(5) Timing chart

The S1C62440/4A0/4C0/480 serial interface timing chart is shown in Figure 11.4.2.



a. Timing chart, SEN = "1"



b. Timing chart, SEN = "0"

Fig. 11.4.2
Serial interface timing chart

11.5 Control of Serial Interface

The control registers for the serial interface are explained below.

Table 11.5.1 Control registers of serial interface

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F03H	0	0	0	ISIO	0	–			
	R				0	–			
					0	–			
					ISIO	0	Yes	No	Interrupt factor flag (serial interface)
F13H	0	0	0	EISIO	0	–			
	R			R/W	0	–			
					0	–			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F30H	SD3	SD2	SD1	SD0	SD3	X			MSB
	R/W				SD2	X			Serial interface data register (low-order)
					SD1	X			
					SD0	X			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X			MSB
	R/W				SD6	X			Serial interface data register (high-order)
					SD5	X			
					SD4	X			LSB
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG	–	Trigger		Serial interface clock trigger
	W	R/W			SEN	0	⌐	⌐	Serial interface clock edge selection
					SCS1	0			Serial interface clock mode selection
					SCS0	0			

SD0–SD3, SD4–SD7 (F30H, F31H, R/W)

This is the data register of the serial interface.

• During writing operation

When "1" is written: High level
When "0" is written: Low level

Writes serial data will be output to SOUT terminal. From the SOUT terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".
Perform data writing only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

• During reading operation

When "1" is read: High level
When "0" is read: Low level

The serial data input from the SIN terminal can be read by this register.
The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN terminal.
Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

SCS1, SCS0 (F7AH [D1, D0], R/W)

Selects the synchronous clock for the serial interface ($\overline{SCLK}$).

Table 11.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous Clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

Synchronous clock ($\overline{SCLK}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

SEN (F7AH [D2], R/W)

Selects the timing for reading in the serial data input.

When "1" is written:	Falling edge of $\overline{SCLK}$
When "0" is written:	Rising edge of $\overline{SCLK}$
Reading:	Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the falling edge (at "1" writing) or rising edge (at "0" writing) of the $\overline{SCLK}$ signal.
The input data fetching timing may be selected but output timing for output data is fixed at $\overline{SCLK}$ falling edge.
At initial reset, rising edge of $\overline{SCLK}$ (SEN = "0") is selected.

SCTRG (F7AH [D3], W)

This is a trigger to start input/output of synchronous clock.

When "1" is written:	Trigger
When "0" is written:	No operation
Reading:	Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{SCLK}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state.
Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

EISIO (F13H [D0], R/W) This is the interrupt mask register of the serial interface.

When "1" is written:	Enabled
When "0" is written:	Masked
Reading:	Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

ISIO (F03H [D0], R) This is the interrupt factor flag of the serial interface.

When "1" is read:	Interrupt has occurred
When "0" is read:	Interrupt has not occurred
Writing:	Invalid

From the status of this flag, the software can decide whether the serial interface interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.

Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

11.6 Programming Notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 12 SOUND GENERATOR

12.1 Configuration of Sound Generator

The S1C62440/4A0/4C0/480 are capable of generating buzzer signals ($\overline{BZ}$ and BZ) to drive a piezo-electric buzzer. The buzzer signal frequency may be selected by software from 8 types of signal divided from f_{OSC1} (32,768 Hz). Also, digital envelope which is duty ratio controlled may be added to the buzzer signal.
In addition, 1-shot output circuit is built-in to output key operation check sound, and the like.
Figure 12.1.1 shows the sound generator configuration.
Figure 12.1.2 shows the sound generator timing chart.

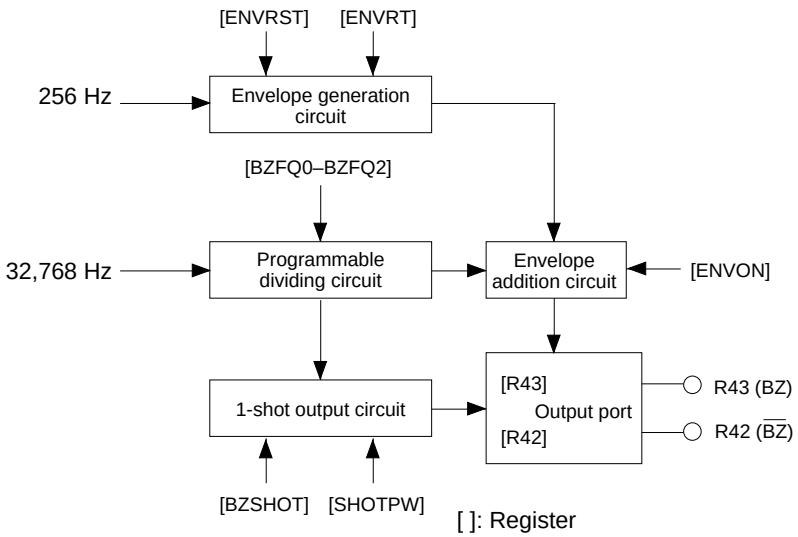


Fig. 12.1.1 Configuration of sound generator

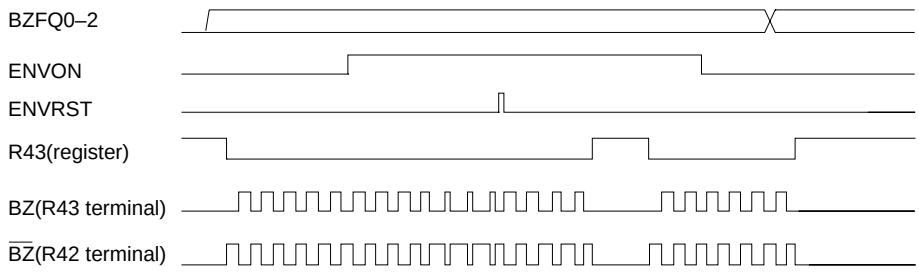


Fig. 12.1.2 Timing chart of sound generator

12.2 Mask Option

(1) Selection can be made whether to output the BZ signal from the R43 terminal.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R42 terminal.
However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

See Chapter 7, "OUTPUT PORTS" for details of the above mask option.

12.3 Frequency Setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2.
Table 12.3.1 lists the register setting values and the frequencies that can be set.

Table 12.3.1
Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

Note *A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when switchs the buzzer frequency while the BZ and $\overline{BZ}$ signals being output.*

12.4 Digital Envelope

A duty ratio control data envelope (with duty ratio change in 8 steps) can be added to the buzzer signal (BZ, $\overline{BZ}$).
Duty ratio refers to the ratio of pulse width to the pulse cycle; given that high level output time is TH, and low level output time is TL, BZ output becomes TH/(TH+TL).
$\overline{BZ}$ output becomes TL/(TH+TL) owing to the inverted output of the BZ output. Moreover, care is necessary as the duty ratio differs according to the buzzer frequency.
Envelope addition is performed by writing "1" to ENVON; when "0" is written, the duty ratio is fixed at the maximum (1/2 duty). Moreover, when envelope is added, writing "1" to ENVRST will cause the BZ signal duty ratio to be returned to maximum.
The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 ms (16 Hz) when "0" is written, and 125 ms (8 Hz) when "1" is written. However, a maximum difference of 4 ms is taken from envelope-ON until the first change.
Table 12.4.1 lists the duty ratio and buzzer frequencies.
Figure 12.4.1 shows the digital envelope timing chart.

Table 12.4.1 Duty ratio and buzzer frequencies

Duty ratio	Buzzer frequencies			
	4,096.6	3,276.8	2,730.7	2,340.6
	2,048.0	1,638.4	1,365.3	1,170.3
Level 1 (maximum)	8/16	8/20	12/24	12/28
Level 2	7/16	7/20	11/24	11/28
Level 3	6/16	6/20	10/24	10/28
Level 4	5/16	5/20	9/24	9/28
Level 5	4/16	4/20	8/24	8/28
Level 6	3/16	3/20	7/24	7/28
Level 7	2/16	2/20	6/24	6/28
Level 8 (minimum)	1/16	1/20	5/24	5/28

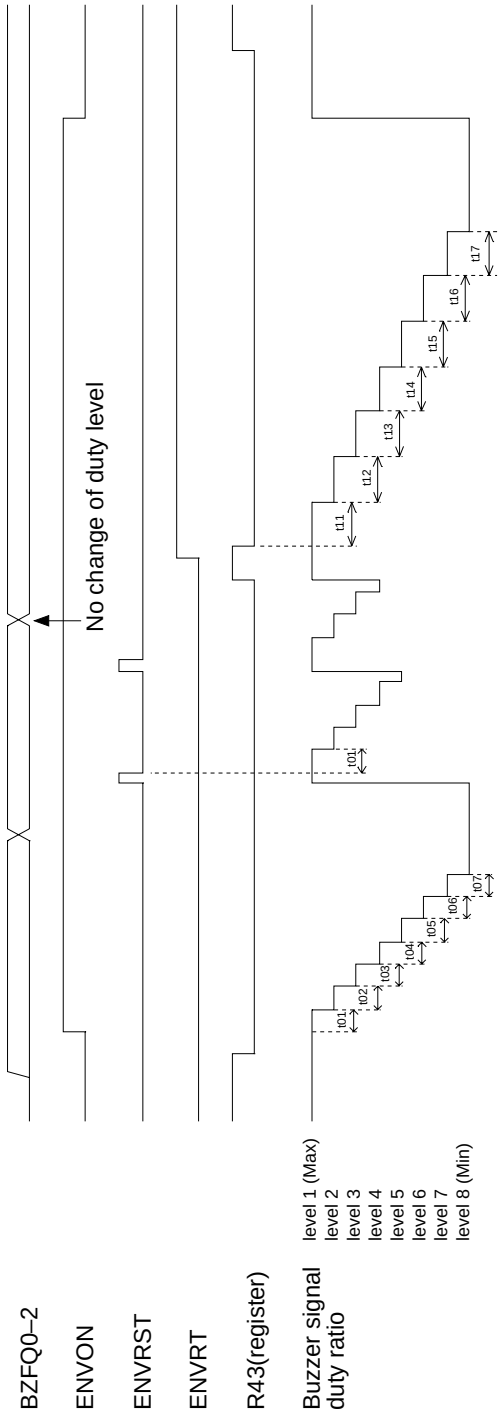


Fig. 12.4.1 Digital envelop timing chart

12.5 1-shot Output

In order to cause the buzzer to ring in a short period of time as in the case of key operation check sound, 1-shot output function is built-in. The time duration for buzzer signal to be output (BZ and $\overline{BZ}$) may be selected by SHOTPW; when "0" is written on SHOTPW, it is set to 31.25 ms and to 62.5 ms when "1" written.
Actual output operation is performed by writing "1" on BZSHOT; after performing the previously described writing operation, it synchronizes with the internal 256 Hz signal and buzzer signal is output in output port R43 (R42). Moreover, after the set time has lapsed, it synchronizes with the same 256 Hz previously described and the buzzer signal is automatically turned off. Also, by reading BZSHOT, whether the 1-shot circuit is in operation or not may be determined with the software.

Figure 12.5.1 shows the timing chart of the 1-shot output.

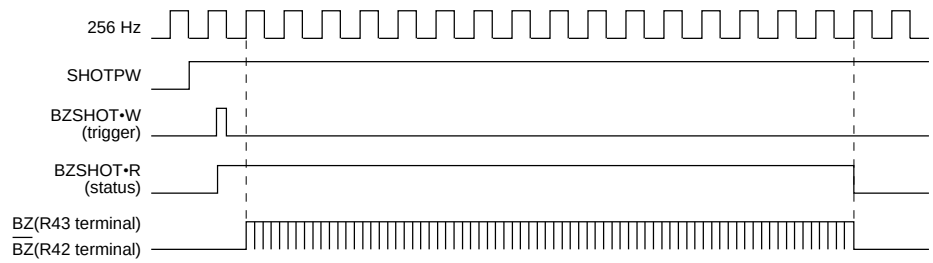


Fig. 12.5.1
Timing chart of
1-shot output

12.6 Control of Sound Generator

The control registers for the sound generator are explained below.

Table 12.6.1 Control registers of sound generator

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output ($\overline{BZ}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{FOUT}$)
							Off	On	LCD synchronous signal(CL)
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
	R/W				BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger
							BUSY	READY	Status
	W/R	W	R/W		ENVRST	Reset	Reset	–	Envelope reset
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off

BZFQ0–BZFQ2 (F74H [D0, D1, D2], R/W)

Will select the buzzer signal frequency.

Table 12.6.2 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4096.0
0	0	1	3276.8
0	1	0	2730.7
0	1	1	2340.6
1	0	0	2048.0
1	0	1	1638.4
1	1	0	1365.3
1	1	1	1170.3

At initial reset, 4,096 Hz is selected.

ENVRST (F75H [D2], W)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written: Reset input
When "0" is written: No operation
Reading: Always "0"

When envelope is added to the buzzer signal, by writing "1" on ENVRST, the envelope is reset and duty ratio becomes maximum. When envelope is not added, or when buzzer signal is not being output, reset operation is ineffective.

ENVON (F75H [D0], R/W)

This controls adding the envelope to the buzzer signal.

When "1" is written: Envelope added (ON)
When "0" is written: No envelope (OFF)
Reading: Valid

By writing "1" on ENVON, envelope is added to the buzzer signal. Writing "0" means envelope will not be added.
At initial reset, ENVON is set to "0" and envelope OFF will be selected.

ENVRT (F75H [D1], R/W)

Selects the attenuation time of the envelope added to the buzzer signal.

When "1" is written:	1.0 sec (125 ms × 7 = 875 ms)
When "0" is written:	0.5 sec (62.5 ms × 7 = 437.5 ms)
Reading:	Valid

The attenuation time of digital envelopes is determined by the time change for duty ratio. When "1" is written on ENVRT, attenuation time is set in 125 ms (8 Hz) units (125 ms × 7 = 875 ms), and in 62.5 ms (16 Hz) unit (62.5 ms × 7 = 437.5 ms) when "0" is written.
However, there is a maximum error of 4 ms from envelope ON to the first change in both cases.

R43, R42 (F54H [D3, D2], R/W)

R43 Controls the output of the buzzer signals (BZ, $\overline{BZ}$).

When "0" is written:	Buzzer signal output
When "1" is written:	Low level (DC)
Reading:	Valid

When "0" is set on R43, BZ signal is generated from R43 terminal, and if R42 is set to $\overline{BZ}$ output, $\overline{BZ}$ signal (inverted signal of BZ) is generated at the same time.
When "1" is set on R43, R43 terminal (R42 to, if $\overline{BZ}$ output is selected) becomes of low (V_{SS}) level output.
However, R42 with $\overline{BZ}$ output selected, may be used as a 1-bit general register capable of read/write function, the data of which register does not affect $\overline{BZ}$ (R42 terminal output).
At initial reset, both R43 and R42 are set to "1".

Note *BZ and $\overline{BZ}$ output signals may produce hazards during ON/OFF switching.*

SHOTPW (F74H [D3], R/W)

Sets the output time duration of the 1-shot buzzer.

When "1" is written:	62.5 ms
When "0" is written:	31.25 ms
Reading:	Valid

Output time duration is set to 62.5 ms or 31.25 ms by writing "1" or "0", respectively, on SHOTPW.
At initial reset, SHOTPW is set to "0".

BZSHOT (F75H [D3], W, R)

Controls the output of the 1-shot buzzer.

• During writing operation

When "1" is written:	Trigger
When "0" is written:	No operation

When "1" is written on BZSHOT, the 1-shot circuit operates and the buzzer signal (BZ and $\overline{BZ}$) is output.
The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

• During reading operation

When "1" is read:	Busy
When "0" is read:	Ready

The BZSHOT reads "1" when the 1-shot buzzer is ringing and "0" when it is not ringing. The period of "1" is from the time of the trigger until the buzzer output is turned OFF.
At initial reset, "0" is read.

12.7 Programming Notes

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

CHAPTER 13 EXTERNAL MEMORY ACCESS (S1C624A0/4C0/480)

To control external devices such as expansion LCD driver (S1D15201F10A*) and static RAM, the S1C624A0/4C0/480 can be set by mask option using output port and I/O port as external memory access ports.
Figure 13.1 shows the External memory block diagram.

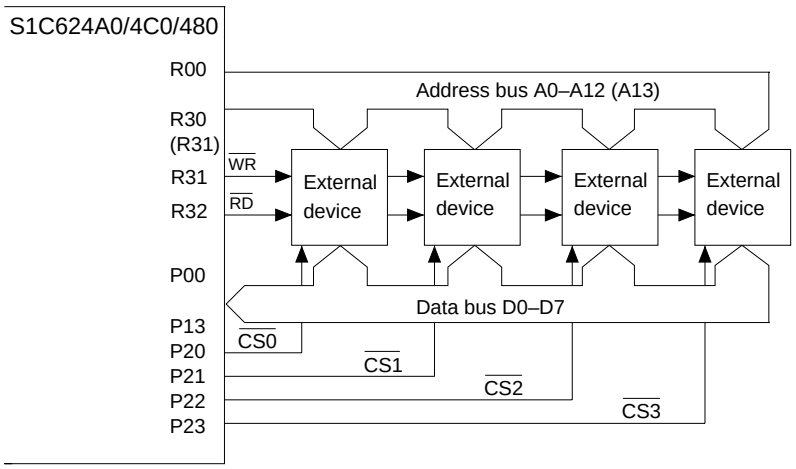


Fig. 13.1
External memory
block diagram

Note *The S1C62440 does not have an external memory access function.*

13.1 Address Bus

The address bus may be set to a maximum of 14 bits (A0–A13) in case of read-only devices, and to a maximum of 13 bits (A0–A12) in case of read/write devices.
Address buses are allocated to the following ports and by writing address data to each register, external memory address may be set.

Table 13.1.1
Output ports and address bus

Output port	Address bus
R00–R03	A0–A3 (select in units of 4 bits)
R10–R13	A4–A7 (select in units of 4 bits)
R20–R22	A8–A10 (select in units of 3 bits)
R23	A11 (select in units of 1bit)
R30	A12 (select in units of 1 bit)
R31	A13 (read-only device only)

The above address signals may be selected by mask option as shown in the table and therefore, unneeded address lines may used as regular output ports.

Moreover, address bus perform the following control functions by software:

– Can perform high impedance control.

– Address incrementing may be automatically accomplished through software and data read/write.

13.2 Data Bus

The data bus consists of 8 bits (D0–D7) and are allocated to the input/output ports indicated in Table 13.2.1.

Table 13.2.1
I/O ports and data bus

I/O port	Data bus
P00–P03	D0–D3
P10–P13	D4–D7

Data is written and read in the order of low-order bits (D0–D3) then high-order bits (D4–D7). Through writing/read operation to this register, the write signal ($\overline{WR}$) and read signal ($\overline{RD}$) to the external memory are automatically output.

• Consecutive access of data and virtual data register

Output or input of external memory data to the external data bus is done by accessing registers P00–P03 and P10–P13. It requires access of low order data and high order data, and is related to the increase of program steps. Hence, the S1C624A0/4C0/480 allows even and odd number addresses in the RAM addresses (FC0H–FFFH) to be logically allocated to P00–P03 and P10–P13, respectively, as virtual data; S1C624A0/4C0/480 also makes consecutive access by LBPX and RETD instructions possible.
The memory map of this logical space is shown on Figure 13.2.1.

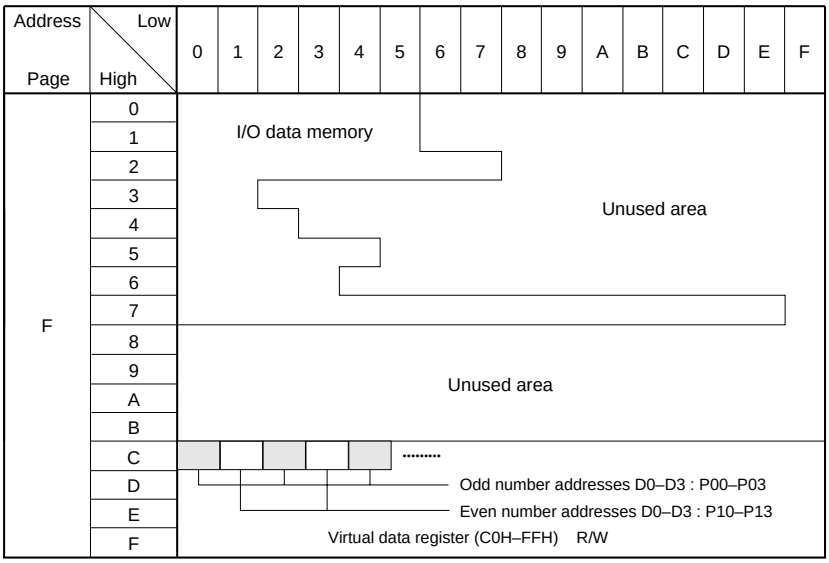


Fig. 13.2.1
Memory map
(virtual data registers)

Note *The virtual data register is a logical space and no memory is physically allocated. The actual writing/reading through access of this space is done for registers P00–P03, and P10–P13.*

13.3 Write Signal ($\overline{WR}$) and Read Signal ($\overline{RD}$)

Write signal ($\overline{WR}$) and read signal ($\overline{RD}$) for the external memory are automatically generated according to data writing/reading from R31 terminal and R32 terminal, respectively.

$\overline{WR}$ and $\overline{RD}$ signals can perform high impedance control by software.

Refer to "13.5 External Memory Read/Write Sequence" for the data writing/reading timing.

13.4 Chip Select Signal

External device selection requires no external address (S1C624A0/4C0/480) decoder, and maximum 4 chips select signal may be generated.
Chip select signals are allocated to the following I/O ports:

Table 13.4.1
I/O ports and
chip selector signal

I/O port	Chip selector signal
P20	$\overline{CS0}$
P21	$\overline{CS1}$
P22	$\overline{CS2}$
P23	$\overline{CS3}$

By writing "0" on P2x, the $\overline{CSx}$ signal becomes active (low level setting); writing "1" will make it normal (high level setting).

By setting the chip select register (P20–P23) corresponding to the device desired to be accessed to "0" and then performing data reading/writing, the $\overline{CSx}$ terminal which selects the active signal will be automatically set to low level, in the same manner as $\overline{RD}$ and $\overline{WR}$ signals. Moreover, after the access, it is automatically set to high level.

Because of the write-only (W/O) function, the chip select register may not be re-written by logical arithmetic instructions.

$\overline{CS}$ signal can perform high impedance control by software. Note, however, that the pull up resistor is turned on to prevent misoperation of external devices.

13.5 External Memory Read/Write Sequence

Reading and writing of external memory data is done by the following steps:

(1) Write the address data to R00–R30 (R31).

(2) Write "0" on the chip select register corresponding to the external device which will be read or written.

Note: Do not generate multiple $\overline{CS}$ signals at one time.

(3) Perform data reading/writing.
When address auto increment function is set to valid, the address is incremented (+1) after completion of reading/writing operation.

- Data reading

Data register is read in the order of: low order 4 bits first, then high order 4 bits.
$\overline{RD}$ signal and $\overline{CS}$ signal are automatically generated at the point where the low order 4 bits are read.
Data can be read from P00–P03 (low order) and P10–P13 (high order) addresses, or from the even address (low order) and odd address (high order) of the FC0H–FFFH addresses.

- Data writing

Data register is written in the order of: low order 4 bits first, then high order 4 bits.
$\overline{WR}$ signal and $\overline{CS}$ signal are automatically generated at the point where the high order 4 bits are written.
Data can be written to P00–P03 (low order) and P10–P13 (high order) addresses, or to the even address (low order) and odd address (high order) of the FC0H–FFFH addresses.
When address auto increment function is set to be valid, consecutive writing is possible from FC0H–FFFH addresses through the LBPX and RETD instructions.

(4) Write "1" on the chip select register.

With register to high impedance control, follow the requirements of the external circuit.

Figure 13.5.1 shows the timing chart of external memory access.

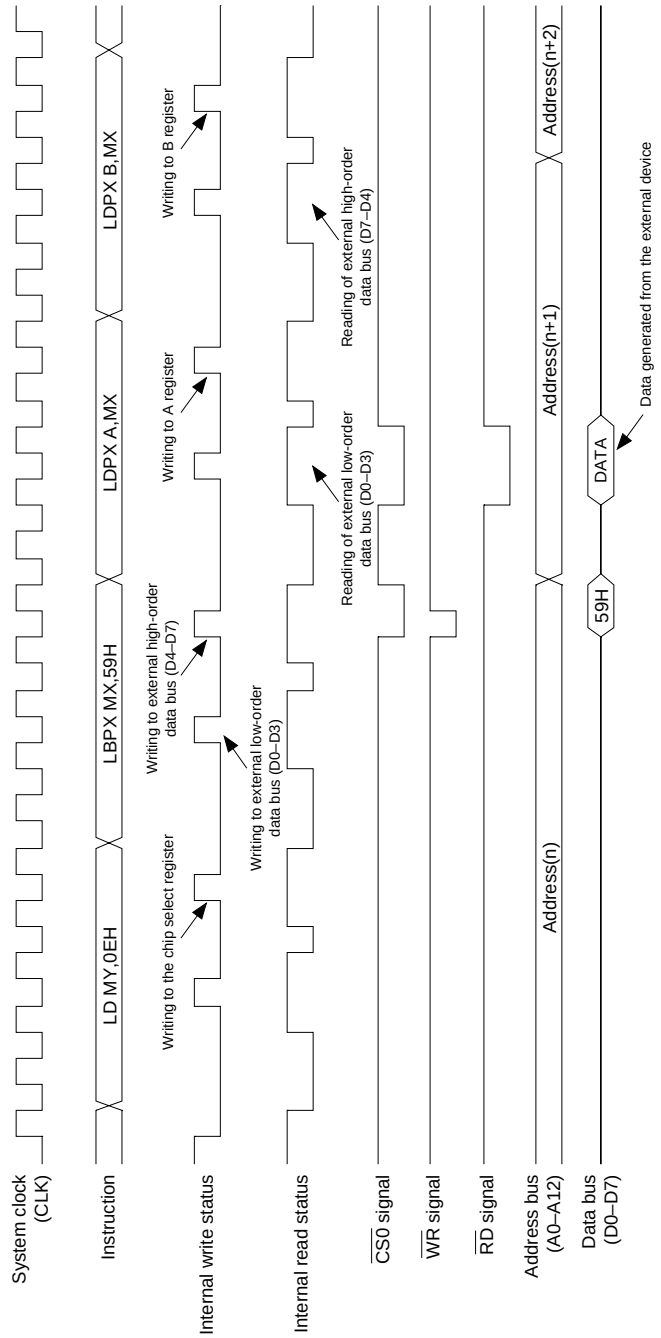


Fig. 13.5.1 Timing chart of external memory access

13.6 Control of External Memory

The control registers for external memory are explained below.

Table 13.6.1(a) Control registers of external memory (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F50H	R03	R02	R01	R00	R03	X	High	Low	Output port (R03)
							High	Low	External memory address (A3)
	R/W				R02	X	High	Low	Output port (R02)
							High	Low	External memory address (A2)
					R01	X	High	Low	Output port (R01)
							High	Low	External memory address (A1)
					R00	X	High	Low	Output port (R00)
							High	Low	External memory address (A0)
F51H	R13	R12	R11	R10	R13	X	High	Low	Output port (R13)
							High	Low	External memory address (A7)
	R/W				R12	X	High	Low	Output port (R12)
							High	Low	External memory address (A6)
					R11	X	High	Low	Output port (R11)
							High	Low	External memory address (A5)
					R10	X	High	Low	Output port (R10)
							High	Low	External memory address (A4)
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R23)
							High	Low	External memory address (A11)
	R/W				R22	X	High	Low	Output port (R22)
							High	Low	External memory address (A10)
					R21	X	High	Low	Output port (R21)
							High	Low	External memory address (A9)
					R20	X	High	Low	Output port (R20)
							High	Low	External memory address (A8)
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						BUSY	READY	[SRDY (SIO READY)]
					R32	X	High	Low	Output port (R32)
									[External memory read ($\overline{RD}$)]
					R31	X	High	Low	Output port (R31)
							High	Low	External memory address (A13)
									[External memory write ($\overline{WR}$)]
					R30	X	High	Low	Output port (R30)
							High	Low	External memory address (A12)

Table 13.6.1(b) Control registers of external memory (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P03)
							High	Low	External memory data (D3)
	R/W				P02	X	High	Low	I/O port (P02)
							High	Low	External memory data (D2)
					P01	X	High	Low	I/O port (P01)
							High	Low	External memory data (D1)
					P00	X	High	Low	I/O port (P00)
							High	Low	External memory data (D0)
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P13)
							High	Low	External memory data (D7)
	R/W				P12	X	High	Low	I/O port (P12)
							High	Low	External memory data (D6)
					P11	X	High	Low	I/O port (P11)
							High	Low	External memory data (D5)
					P10	X	High	Low	I/O port (P10)
							High	Low	External memory data (D4)
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P23)
							High	Low	External memory chip select ($\overline{CS3}$)
	R/W W				P22	X	High	Low	I/O port (P22)
							High	Low	External memory chip select ($\overline{CS2}$)
					P21	X	High	Low	I/O port (P21)
							High	Low	External memory chip select ($\overline{CS1}$)
					P20	X	High	Low	I/O port (P20)
							High	Low	External memory chip select ($\overline{CS0}$)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
	R/W				HZR2	0	Output	High-Z	R20–R23 output high-impedance control
					HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control
F7CH	0	HZCS	ADINC	PICON	0	–			
	R	R/W	W	R/W	HZCS	0	Output	High-Z	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					ADINC	–	Increment	–	External memory address increment (A0–A13)
					PICON	0	Auto Inc.	Normal	External memory address auto increment mode

R00–R03, R10–R13, R20–R23, R30, R31 (F50H, F51H, F52H, F53H [D0, D1], R/W)

These registers set the external memory address.

When "1" is written:	Address bit high level
When "0" is written:	Address bit low level
Reading:	Valid

By writing "1" on Rxx register, the corresponding address bit is generated as high level on the address bus; by writing "0", it is generated as low level on the address bus.

Table 13.6.2 Relationships of Rxx registers and address bits

Address	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Register	R31	R30	R23	R22	R21	R20	R13	R12	R11	R10	R03	R02	R01	R00

Note *When a read-write device is connected to external memory, R31 become the $\overline{WR}$ output, and the A13 signal cannot be output.*

At initial reset, the above registers will be undefined.

P00–P03, P10–P13 (F60H,F61H, ODD, EVEN address of FC0H–FFFH, R/W)

These registers perform reading/writing for external memory data.

When "1" is written:	Data bit high level
When "0" is written:	Data bit low level
When "1" is read:	Data bit high level
When "0" is read:	Data bit low level

• During writing operation

By writing "1" on Pxx register, the corresponding data bit is generated as high level on the data bus; by writing "0", it is generated as low level on the data bus.
$\overline{WR}$ signal is automatically generated from R31 terminal, and from the $\overline{CSx}$ terminal if $\overline{CSx}$ signal were set active.

• During readting operation

The data of the data bus is read from the corresponding register Pxx with the high level as "1" and the low level as "0".
$\overline{RD}$ signal is automatically generated from R32 terminal, and from the $\overline{CSx}$ terminal if $\overline{CSx}$ signal were set active.

Table 13.6.3 Relationships of registers Pxx and data bits

Data	D7	D6	D5	D4	D3	D2	D1	D0
Register	P13	P12	P11	P10	P03	P02	P01	P00

Note *The data is written and read in the order of low-order bits (D0–D3) then high-order bits (D4–D7).*

At initial reset, the above registers will be undefined.

P20–P23 (F62H, W)

Output the chip select signal.

When "0" is written:	Active standby
When "1" is written:	Normal (high level)
Reading:	Always "1"

By writing "0" on P2x, $\overline{CSx}$ signal becomes valid; during read/write operation of the external memory device, it goes low.
The $\overline{CSx}$ signal is fixed at high level by writing "1".
Because of the write-only (W/O) function, these registers may not be re-written by logical arithmetic instruction.
Correspondence between P2x and $\overline{CSx}$ is as follows:

P20: $\overline{CS0}$
P21: $\overline{CS1}$
P22: $\overline{CS2}$
P23: $\overline{CS3}$

R31 (F53H [D1], R/W)

When R31 is selected to $\overline{WR}$ output, the $\overline{WR}$ output control is performed through the hardware, and register R31 can be used as a 1 bit read/write general register.
When a read-only device is only connected, R31 can be used as address A13.

R32 (F53H [D2], R/W)

The read signal $\overline{RD}$ is output from the output R32. Output control is performed through the hardware, and register R32 can be used as a 1 bit read/write general register.

ADINC (F7CH [D1], W)

Increment the address.

When "1" is written:	Address incremented (+1)
When "0" is written:	No operation
Reading:	Always "0"

When "1" is written to ADINC the external memory address A0–A12 (A13) will be incremented (+1).

PICON (F7CH [D0], R/W) Sets the address auto increment function.

When "1" is written:	Auto increment ON
When "0" is written:	Auto increment OFF
Reading:	Valid

When "1" is written to PICON, the auto increment function of the external memory address A0–A12 (A13) becomes effective. In auto increment mode the address is automatically incremented (+1) after high-order data (D4–D7) is written or read. For timing of writing/reading and address increment, see Figure 13.5.1.
When "0" is written to PICON, auto increment is not possible.
At initial reset, PICON is set to "0", and the auto increment function is invalidated.

HZR0–HZR3 (F7BH, R/W) Performs the high-impedance control of the Rxx (x = 0–3) terminals.

When "0" is written:	High impedance
When "1" is written:	Signal output
Reading:	Valid

Controls the output of Rxx (x = 0–3) in units of 4 bits.
When "1" is written to HZRx, the specified signal is output from the corresponding terminals Rx0–Rx3. When "0" is written the output becomes high impedance.
HZRx and Rxx correspondence are as follows:

HZR0:	R00–R03
HZR1:	R10–R13
HZR2:	R20–R23
HZR3:	R30–R33

At initial reset, all HZRx are set to "0" and output becomes high impedance.
With this function, the external device may be communally used with other CPUs through a common bus line.

HZCS (F7CH [D2], R/W) Controls the high impedance of the $\overline{CSx}$ (x = 0–3) terminals.

When "0" is written:	High impedance
When "1" is written:	Signal output
Reading:	Valid

When "1" is written to HZCS, $\overline{CSx}$ signals are output from pins P20–P23. When "0" is written, the output becomes high impedance (pulled up).
At initial reset, HZCS is set to "0" and the output becomes high impedance (pulled up).
Moreover, P2x port which will not be used as $\overline{CS}$ will not gain high impedance even if HZCS is set to "0".
With this function, the external device may be communally used with other CPUs through a common bus line.

13.7 Programming Notes

(1) Be sure to data writing/reading for external memory in the order of low-order bits (D0–D3) then high-order bits (D4–D7).

(2) Because of the write-only (W/O) function, the chip select register (P20–P23) may not be re-written by logical arithmetic instruction.

CHAPTER 14 INTERRUPT AND HALT

The S1C62440/4A0/4C0/480 have the following interrupt functions built-in, and masking is possible for each one.

External interrupt
- Input interrupt (2 systems)

Internal interrupt
- Clock timer interrupt (3 systems)
- Stopwatch timer interrupt (2 systems)
- Programmable timer interrupt (1 system)
- Serial interface interrupt (1 system)

To allow the interrupt to function, it is necessary that the interrupt mask register of the required system be set to "1" (enable) and, at the same time, the interrupt flag be set to "1" (EI).
When interrupt occurs, the interrupt flag is automatically reset to "0" (DI), prohibiting the any consequent interrupts.

The CPU stops the operating clock when a HALT instruction is executed and then enters the HALT state.
Re-running the CPU from the HALT state requires issuance of interrupt request.
If return through interrupt request is not effective, return is effected from initial reset by the watchdog timer.

Figure 14.1 shows the configuration of the interrupt circuit.

See the explanations of the relevant circuits for interrupt details.

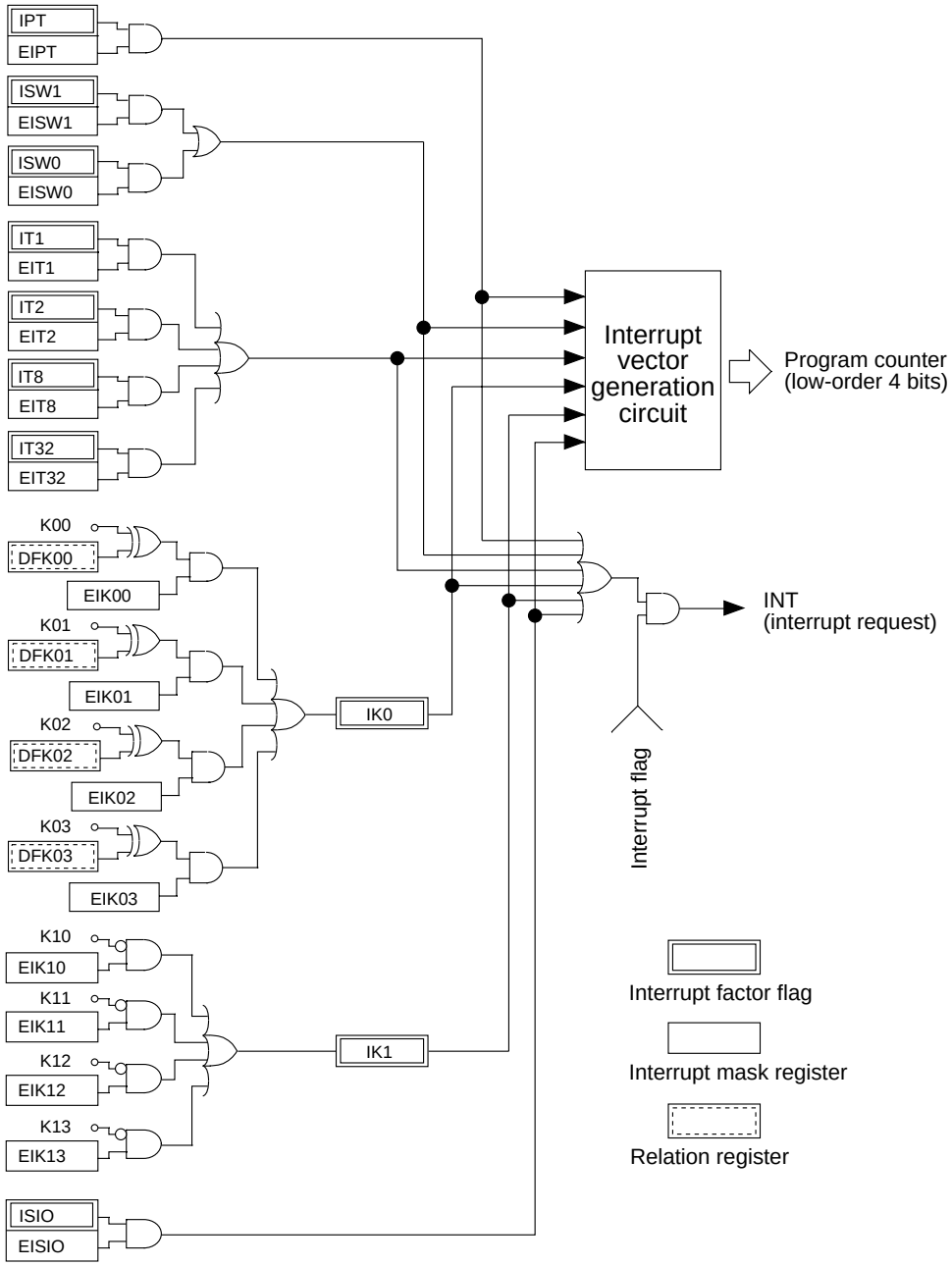


Fig. 14.1
Configuration of interrupt circuit

14.1 Interrupt Factor Flag and Interrupt Mask

The corresponding interrupt factor flag is set to "1" with the individual interrupt element.
If the following conditions exist, interrupt for the CPU occurs when the interrupt factor flag is set to "1".

- The corresponding interrupt mask register is set at "1" (enable).
- The interrupt flag is set at "1" (EI).

The interrupt factor flag is reset to "0" at the read-only register by reading the data.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt factor flag is reset to "0".

The interrupt can be masked by the corresponding interrupt mask register.
The interrupt mask register is a register capable of read/write operation; by writing "1", it is enabled (interrupt is allowed) and by writing "0", it is masked (interrupt is prohibited).
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt mask register is set to "0".

The interrupt factor flag is set to "1" by interrupt factor even if the interrupt is masked. (The input interrupt factor flags IK0 and IK1 will be eliminated.)

Table 14.1.1 shows the correspondence between interrupt factor flags and interrupt mask registers.

Table 14.1.1 Interrupt factor flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1 (F00H [D3])	EIT1 (F10H [D3])
Falling edge of clock timer (2 Hz)	IT2 (F00H [D2])	EIT2 (F10H [D2])
Falling edge of clock timer (8 Hz)	IT8 (F00H [D1])	EIT8 (F10H [D1])
Falling edge of clock timer (32 Hz)	IT32 (F00H [D0])	EIT32 (F10H [D0])
Overflow of stopwatch timer (SWH) (1 Hz)	ISW1 (F01H [D1])	EISW1 (F11H [D1])
Overflow of stopwatch timer (SWL) (10 Hz)	ISW0 (F01H [D0])	EISW0 (F11H [D0])
No matching between input ports (K00–K03) and input relation registers (DFK00–DFK03)	IK0 (F04H [D0])	EIK03 (F14H [D3]) EIK02 (F14H [D2]) EIK01 (F14H [D1]) EIK00 (F14H [D0])
Falling edge of input ports (K10–K13)	IK1 (F05H [D0])	EIK13 (F15H [D3]) EIK12 (F15H [D2]) EIK11 (F15H [D1]) EIK10 (F15H [D0])
Data (8 bits) input/output of serial interface has completed	ISIO (F03H [D0])	EISIO (F13H [D0])
Counter value of programmable timer = 00H	IPT (F02H [D0])	EIPT (F12H [D0])

14.2 Interrupt Vector

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

① The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

② The vector address (1 page 02H–0CH) for each interrupt request is set to the program counter.

③ Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Note *Time equivalent to 12 cycles of CPU system clock is required for steps ① and ②.*

The interrupt request and interrupt vector correspondence is shown in Table 14.2.1.

Table 14.2.1 Interrupt request and interrupt vectors

Interrupt vector (PCS and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Serial interface interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

14.3 Programming Notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(5) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.
Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.
Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.
If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.
When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER 15 SUMMARY OF NOTES

15.1 Notes for Low Current Consumption

The S1C62440/4A0/4C0/480 contain control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 15.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (Chapter 17)
CPU operation frequency	CLKCHG, OSCC	See electrical characteristics (Chapter 17)
Internal regulated voltage	VSC0, VSC1	See electrical characteristics (Chapter 17)
Heavy load protection mode	HLMOD	See electrical characteristics (Chapter 17)
SVD circuit	SVDON	Several tens µA

Below are the circuit statuses at initial reset.

CPU:	Operating
CPU operating frequency:	OSC1 side (CLKCHG = "0"), OSC3 oscillation circuit stoped (OSCC = "0")
Internal regulated voltage:	-1.2 V (VSC0, VSC1 = "0") In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V.
Heavy load protection mode:	Normal operating mode (HLMOD = "0")
SVD circuit:	OFF (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

15.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mined when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

SVD (Supply voltage detection) circuit

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

Heavy load protection mode

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.1.)

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST←"1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

Oscillation circuit

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1)→ 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1)→ 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.5.1 and then proceed with software processing.

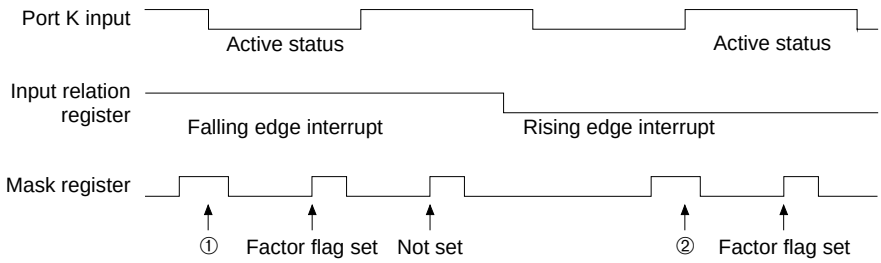
(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

(6) In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V and will never become -1.2 V.

Input port (Kxx)

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

(2) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 15.2.1
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = Low status, when the falling edge interrupt is effected and

input terminal = High status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 15.2.1. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case.

When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 15.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.
In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

Output port (Rxx)

(1) When BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

I/O port (Pxx)

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
– The input/output mode is set at output mode
– Output specification is set at Nch open drain
– The content of the data register is "1"
– The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

LCD driver

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

Stopwatch timer

When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

Programmable timer

(1) When initiating programmable timer count, perform programming by the following steps:
1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than 256 Hz, high speed processing by OSC3 is required.

Serial interface (SIN, SOUT, and $\overline{SCLK}$)

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

Sound generator

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

External memory access

(1) Be sure to data writing/reading for external memory in the order of low-order bits (D0–D3) then high-order bits (D4–D7).

(2) Because of the write-only (W/O) function, the chip select register (P20–P23) may not be re-written by logical arithmetic instruction.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

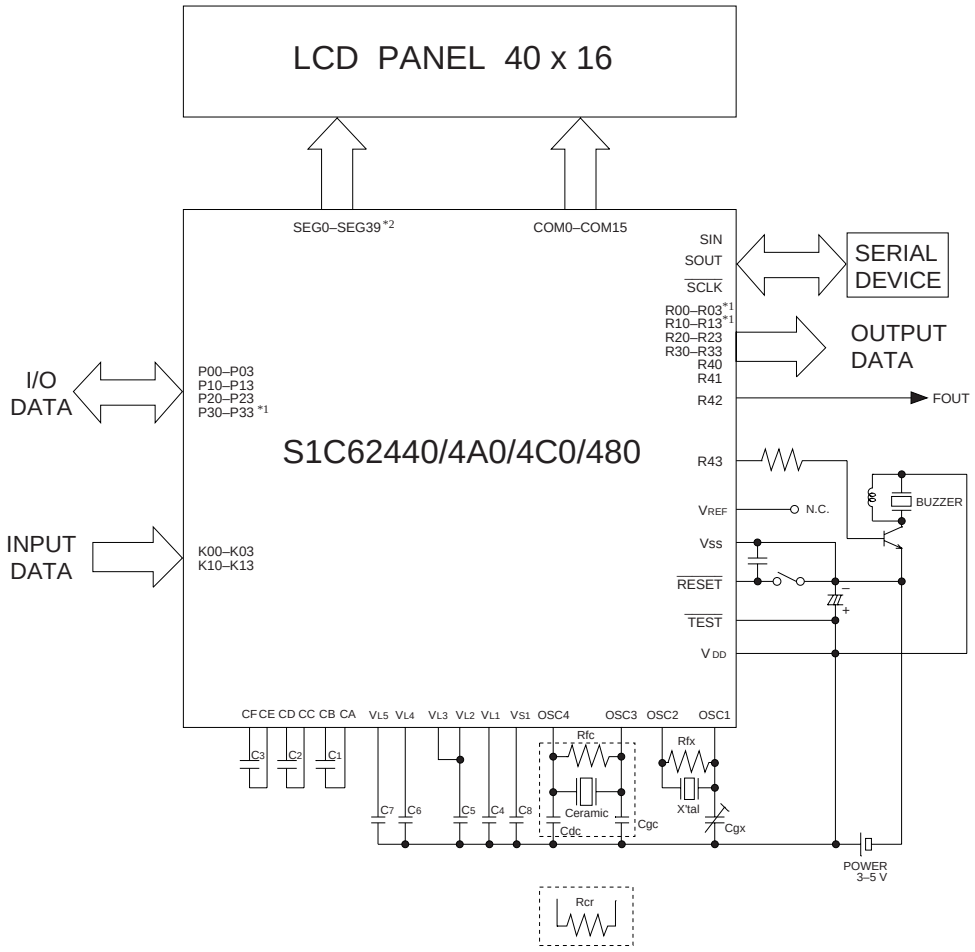
(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(5) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.
Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.
Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.
If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.
When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER 16 BASIC EXTERNAL CONNECTION DIAGRAM

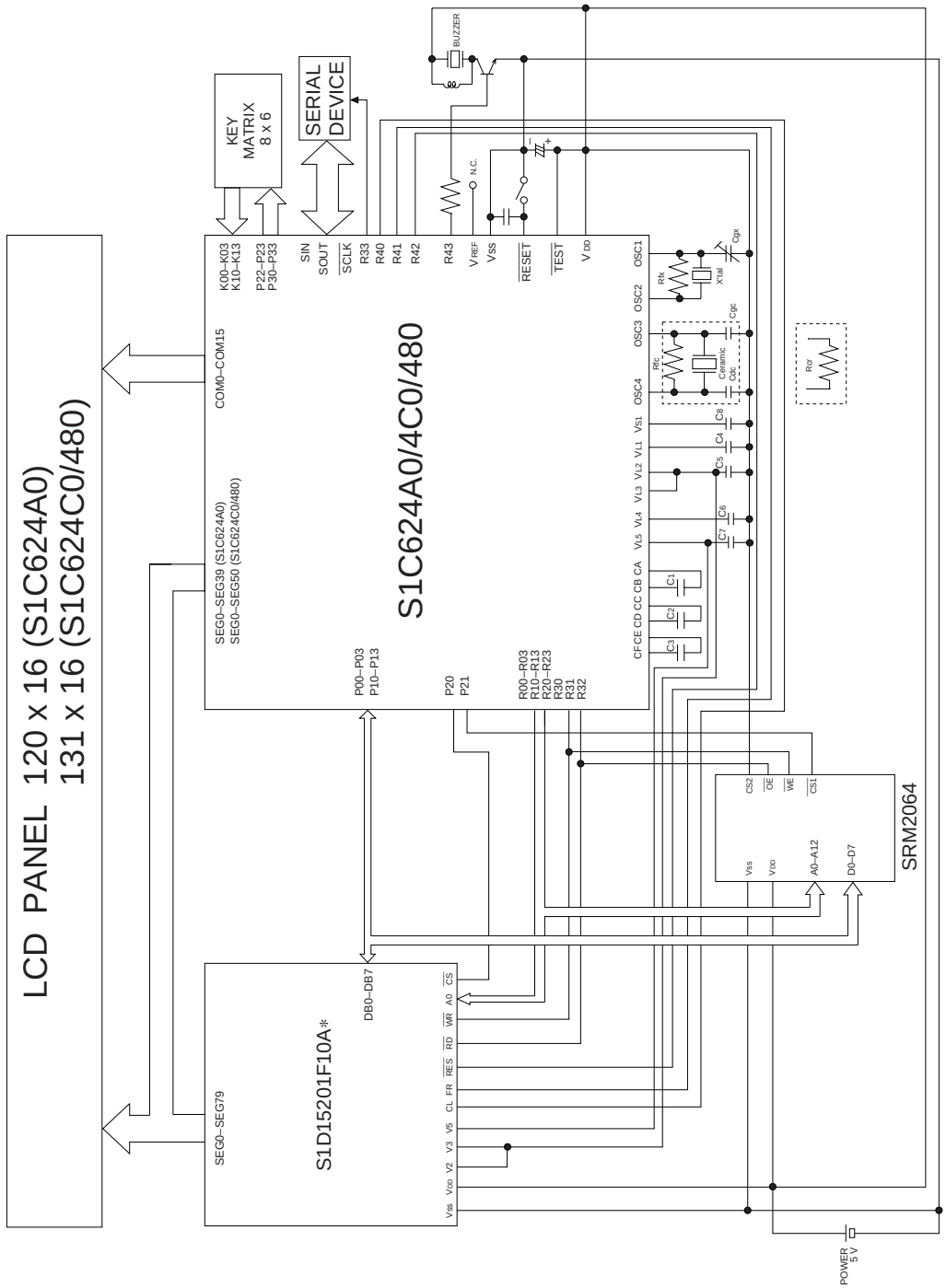
16.1 Connection Diagram on S1C62440/4A0/4C0/480 only



*1 S1C624A0/4C0/480 only

*2 The S1C624C0/480 can be used up to SEG50

16.2 Connection Diagram when External Device is Connected



16.3 Recommended Values for External Parts

Table 16.3.1 Recommended values for external parts

X'tal	Crystal oscillator	32,768 Hz, CI (MAX)=35 kΩ
Rfx	Feedback resistor	10 MΩ
Cgx	Trimmer capacitor	5–25 pF
Ceramic	Ceramic oscillator	500 kHz–2 MHz
Rfc	Feedback resistor	1 MΩ
Cgc	Gate capacitance	100 pF
Cdc	Drain capacitance	100 pF
Rcr	Resistance for CR oscillation	20 kΩ–100 kΩ
C_1	Voltage booster capacitor (1)	0.1 µF *1
C_2	Voltage booster capacitor (2)	0.1 µF *1
C_3	Voltage booster capacitor (3)	0.1 µF *1
C_4	Capacitor between V_{DD} and V_{L1}	0.1 µF *1
C_5	Capacitor between V_{DD} and V_{L2}	0.1 µF *1
C_6	Capacitor between V_{DD} and V_{L4}	0.1 µF *1
C_7	Capacitor between V_{DD} and V_{L5}	0.1 µF *1
C_8	Capacitor between V_{DD} and V_{S1}	0.1 µF

*1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C_1–C_3) and the capacitors between V_{DD} and liquid crystal system power (C_4–C_7).

CHAPTER 17 ELECTRICAL CHARACTERISTICS

17.1 Absolute Maximum Rating

(V_{DD} = 0V)

Item	Code	Rated Value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS}-0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1}-0.3 to 0.5	V
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldered temperature, time	Tsol	260°C, 10 sec (lead section)	–
Permitted loss *1	P_D	250	mW

*1 For 128-pin and 144-pin plastic package

17.2 Recommended Operating Conditions

(Ta = -20 to 70°C)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD} = 0V	VSC = "0"	-3.8	-3.0	-1.8	V
			VSC = "1"	-5.5	-3.0	-2.2	V
			VSC = "2"	-5.5	-5.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC = "1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC = "2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C_1				0.1		µF
Voltage booster capacitor (2)	C_2				0.1		µF
Voltage booster capacitor (3)	C_3				0.1		µF
Capacitor between V_{DD} and V_{L1}	C_4				0.1		µF
Capacitor between V_{DD} and V_{L2}	C_5				0.1		µF
Capacitor between V_{DD} and V_{L4}	C_6				0.1		µF
Capacitor between V_{DD} and V_{L5}	C_7				0.1		µF
Capacitor between V_{DD} and V_{S1}	C_8				0.1		µF

17.3 DC Characteristics

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Unless otherwise specified, the values listed below are standard values under the following conditions:

(V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32,768Hz, f_{OSC3}=1MHz, Ta=25°C, C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8=0.047µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03·10–13 P00–03·10–13	0.2· V_{SS}		0	V
Low-level input voltage	V_{LIN}		P20–23 SIN, $\overline{SCLK}$	V_{SS}		0.8· V_{SS}	V
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage	V_{LIN}			V_{SS}		V_{SS} +0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03·10–13 P00–03·10–13 P20–23 SIN, $\overline{SCLK}$, $\overline{RESET}$	0		0.5	µA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} Has pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23 SIN, $\overline{SCLK}$, $\overline{RESET}$	-45		-15	µA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23 SIN, $\overline{SCLK}$, $\overline{RESET}$	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03·10–13 P20–23 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03·10–13 P20–23 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$	4.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42·43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL2}=V_{SS}+0.5V	R42·43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

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Unless otherwise specified, the values listed below are standard values under the following conditions:

(V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32,768Hz, f_{OSC3}=1MHz, Ta=25°C, C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8=0.047µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03·10–13 P00–03·10–13	0.2·V_{SS}		0	V
Low-level input voltage	V_{LIN}		P20–23·30–33 SIN, $\overline{SCLK}$	V_{SS}		0.8·V_{SS}	V
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage	V_{LIN}			V_{SS}		V_{SS} +0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	0		0.5	µA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} Has pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-45		-15	µA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$	4.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42·43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL2}=V_{SS}+0.5V	R42·43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

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Unless otherwise specified, the values listed below are standard values under the following conditions:

(V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32,768Hz, f_{OSC3}=1MHz, Ta=25°C, C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8=0.047µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03·10–13 P00–03·10–13	0.2·V_{SS}		0	V
Low-level input voltage	V_{LIN}		P20–23·30–33 SIN, $\overline{SCLK}$	V_{SS}		0.8·V_{SS}	V
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage	V_{LIN}			V_{SS}		V_{SS} +0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	0		0.5	µA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} Has pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-45		-15	µA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$	4.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42·43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL2}=V_{SS}+0.5V	R42·43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–50			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

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Unless otherwise specified, the values listed below are standard values under the following conditions:

(V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32,768Hz, f_{OSC3}=1MHz, Ta=25°C, C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8=0.047µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03·10–13 P00–03·10–13	0.2·V_{SS}		0	V
Low-level input voltage	V_{LIN}		P20–23·30–33 SIN, $\overline{SCLK}$	V_{SS}		0.8·V_{SS}	V
High-level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage	V_{LIN}			V_{SS}		V_{SS} +0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	0		0.5	µA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} Has pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-45		-15	µA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistance	K00–03·10–13 P00–03·10–13 P20–23·30–33 SIN, $\overline{SCLK}$, $\overline{RESET}$	-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03·10–13 P20–23·30–33 R00–03·10–13 R20–23·30–33 R40·41 SOUT, $\overline{SCLK}$	4.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42·43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL2}=V_{SS}+0.5V	R42·43	8.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–50			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

17.4 Analog Circuit Characteristics and Consumed Current

Unless otherwise specified, the values listed below are standard values under the following conditions:

(V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32,768Hz, f_{OSC3}=1MHz, Ta=25°C, C_1=C_2=C_3=C_4=C_5=C_6=C_7=C_8=0.047µF)

Item	Code	Condition		Min.	Typ.	Max.	Unit
Liquid crystal drive voltage (Normal mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		1/2·V_{L2} -0.1		1/2·V_{L2} ×0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)	LC="0"	TYP×1.12	-1.80	TYP×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3/2·V_{L2}		3/2·V_{L2} ×0.95	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		2·V_{L2}		2·V_{L2} ×0.95	V
Liquid crystal drive voltage (Heavy load protection mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)	LC="0"	TYP×1.12	-0.92	TYP×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1}		2·V_{L1} ×0.90	V
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3·V_{L1}		3·V_{L1} ×0.90	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		4·V_{L1}		4·V_{L1} ×0.90	V

Item	Code	Condition		Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD0}	SVC = "0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC = "1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC = "2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC = "3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	µs
Consumed current	I_{Hlt}	During HALT	No panel load*1		2.5	5.0	µA
	I_{EX1}	During operation at 32kHz			6.5	9.0	µA
	I_{EX2}	During operation at 1MHz	No panel load*2		400	600	µA
	I_{EX3}	During operation at 2MHz	No panel load*3		1,000	1,500	µA
Consumed current*4 (OSC1•CR oscillation)	I_{Hlt}	During HALT	No panel load*5		20	70	µA
	I_{EX1}	During operation at f_{OSC1}			25	80	µA
	I_{EX2}	During operation at 1MHz			420	600	µA
	I_{EX3}	During operation at 2MHz	No panel load*6		1,000	1,500	µA

*1 The SVD circuit is in the OFF status. OSC1 is crystal oscillation circuit. VSC = "0", OSCC = "0"

*2 The SVD circuit is in the OFF status. OSC1 is crystal oscillation circuit. VSC = "1"

*3 The SVD circuit is in the OFF status. OSC1 is crystal oscillation circuit. VSC = "2", V_{SS} = -5.0 V

*4 Applies for S1C62440/4C0/480.

*5 The SVD circuit is in the OFF status. OSC1 is CR oscillation circuit. VSC = "0" or "1", OSCC = "0", R_{OSC} for OSC1 = 1.6 MΩ

*6 The SVD circuit is in the OFF status. OSC1 is CR oscillation circuit. VSC = "2", OSCC = "0", R_{OSC} for OSC1 = 1.6 MΩ

17.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

– OSC1 crystal oscillation characteristics

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Crystal: Q13MC146, Ta=25°C,
C_{GX}=25pF, C_{DX}=built-in, R_{fx}=10MΩ, VSC="0"

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	sec
Built-in drain capacitance	C_D	Package as assembled		22		pF
		Bare chip		21		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		+10	ppm
Frequency adjustment	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation	V_{hho}	C_G=5pF			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1and V_{DD}, V_{S1}	200			MΩ

– OSC1 CR oscillation characteristics ..... S1C62440/4C0/480 only

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="0" or "1"

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		+5	%
Oscillation frequency	f_{CR}	R_{OSC}=1.6MΩ	32×70%	32	32×130%	kHz

– OSC3 CR oscillation characteristics 1

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1"

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		+5	%
Oscillation frequency	f_{CR}	R_{OSC}=40kΩ	860×70%	860	860×130%	kHz

– OSC3 CR oscillation characteristics 2

If no special requirement

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2"

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-5		+5	%
Oscillation frequency	f_{CR}	R_{OSC}=20kΩ	1.7×70%	1.7	1.7×130%	MHz

– OSC3 ceramic oscillation characteristics 1

If no special requirement

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1"
Ceramic oscillator: CSB 1000J (Murata Mfg. Co.)
C_{GC}=C_{DC}=100pF, R_{fc}=1MΩ

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			3	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-3		+3	%

– OSC3 ceramic oscillation characteristics 2

If no special requirement

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2"
Ceramic oscillator: CSA 2.00MG (Murata Mfg. Co.)
C_{GC}=C_{DC}=100pF, R_{fc}=1MΩ

Item	Code	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			3	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-3		+3	%

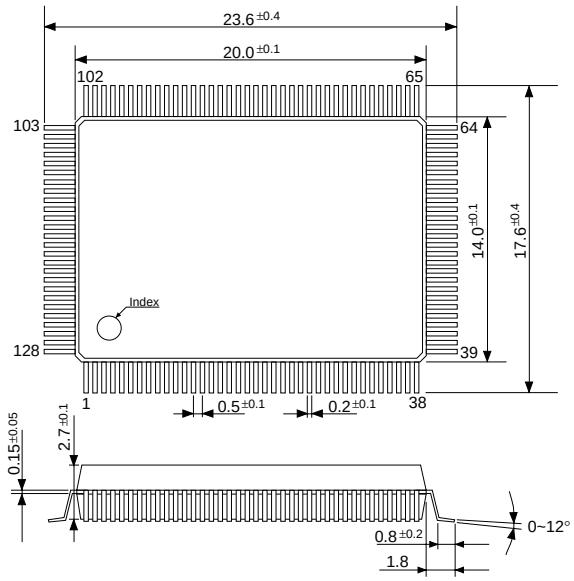
CHAPTER 18 PACKAGE

18.1 Plastic Package

(Unit: mm)

QFP5-128 pin

S1C62440/4A0



QFP8-144 pin

S1C624C0/480

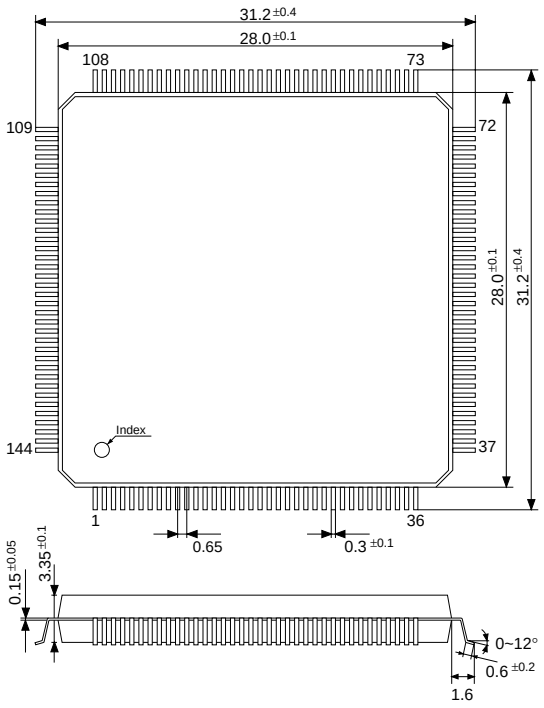


Fig. 18.1.1
Plastic packages

18.2 Ceramic Package for Test Samples

(Unit: mm)

Ceramic PGA-132 pin

S1C62440/4A0

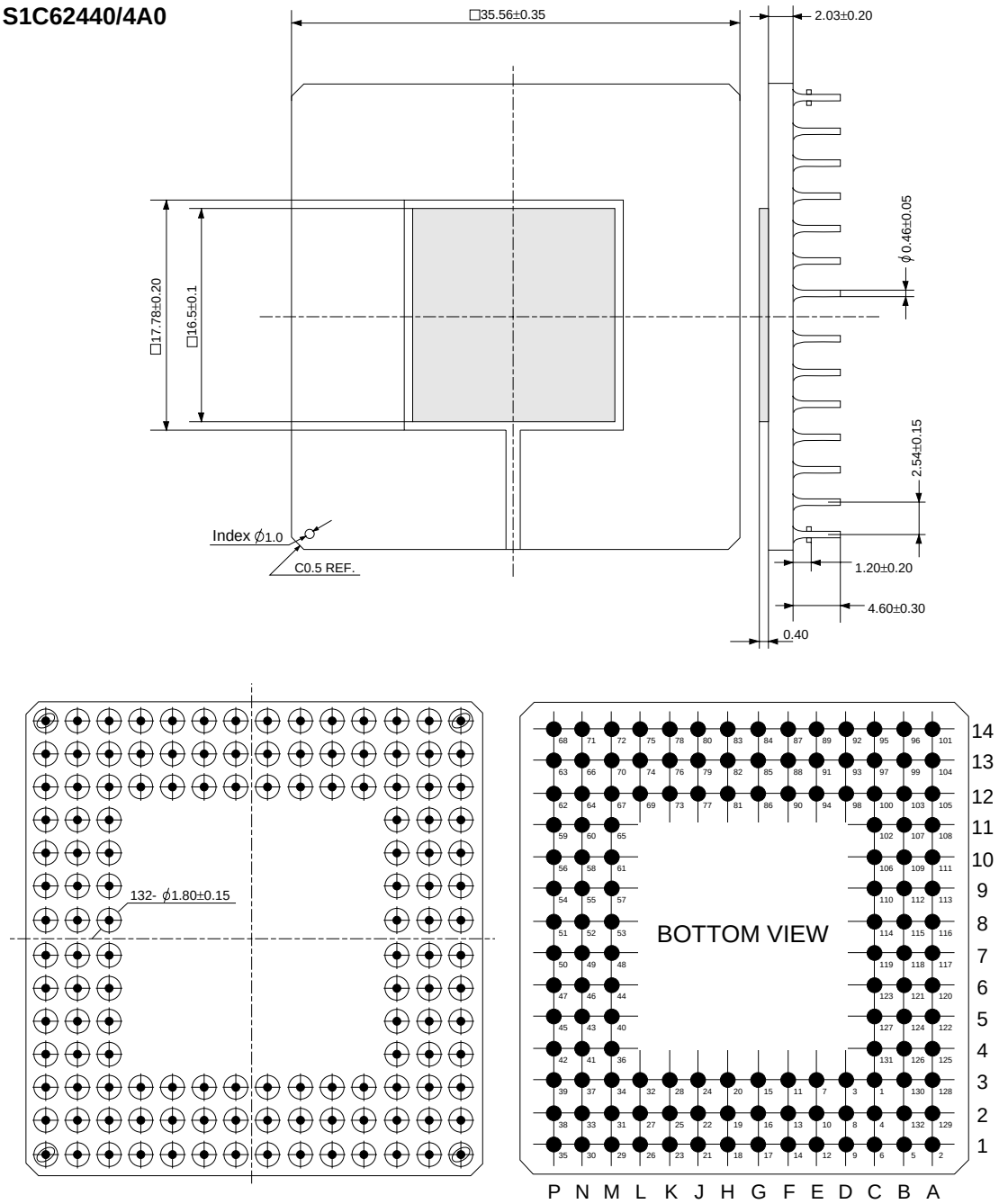


Fig. 18.2.1 Ceramic package for test samples (S1C62440/4A0)

Ceramic QFP8-144 pin

S1C624C0/480

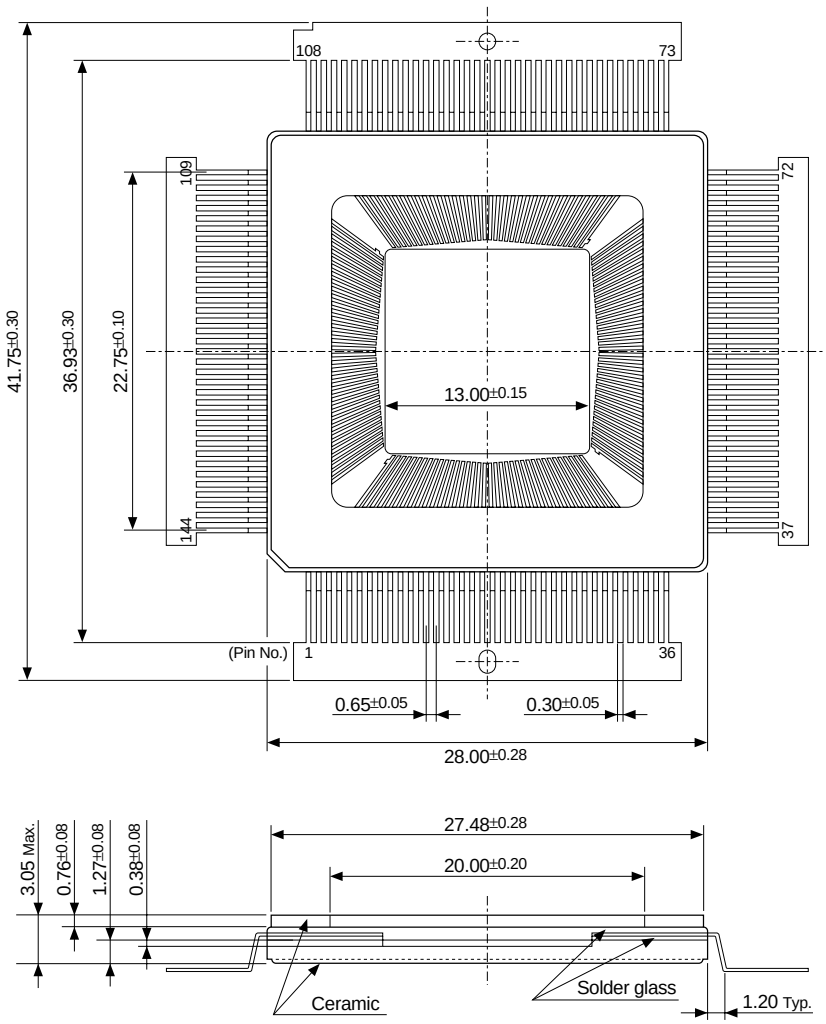


Fig. 18.2.2
Ceramic package for test sample (S1C624C0/480)

Table 18.2.1 Pin coordinates (S1C62440)

Pin No.	Coordinate	Name	Pin No.	Coordinate	Name	Pin No.	Coordinate	Name	Pin No.	Coordinate	Name
1	C3	V_{L5}	34	M3	SEG32	67	M12	N.C.	100	C12	N.C.
2	A1	CF	35	P1	SEG31	68	P14	N.C.	101	A14	R41
3	D3	CE	36	M4	SEG30	69	L12	$\overline{SCLK}$	102	C11	R40
4	C2	CD	37	N3	SEG29	70	M13	SOUT	103	B12	R33
5	B1	CC	38	P2	SEG28	71	N14	SIN	104	A13	R32
6	C1	CB	39	P3	SEG27	72	M14	K13	105	A12	R31
7	E3	CA	40	M5	SEG26	73	K12	K12	106	C10	R30
8	D2	COM0	41	N4	SEG25	74	L13	K11	107	B11	R23
9	D1	COM1	42	P4	SEG24	75	L14	K10	108	A11	R22
10	E2	COM2	43	N5	SEG23	76	K13	K03	109	B10	R21
11	F3	COM3	44	M6	SEG22	77	J12	K02	110	C9	R20
12	E1	COM4	45	P5	SEG21	78	K14	K01	111	A10	N.C.
13	F2	COM5	46	N6	SEG20	79	J13	K00	112	B9	N.C.
14	F1	COM6	47	P6	SEG19	80	J14	N.C.	113	A9	N.C.
15	G3	COM7	48	M7	SEG18	81	H12	N.C.	114	C8	N.C.
16	G2	COM8	49	N7	SEG17	82	H13	N.C.	115	B8	N.C.
17	G1	COM9	50	P7	SEG16	83	H14	N.C.	116	A8	N.C.
18	H1	COM10	51	P8	SEG15	84	G14	P23	117	A7	N.C.
19	H2	COM11	52	N8	SEG14	85	G13	P22	118	B7	N.C.
20	H3	COM12	53	M8	SEG13	86	G12	P21	119	C7	V_{SS}
21	J1	COM13	54	P9	SEG12	87	F14	P20	120	A6	$\overline{RESET}$
22	J2	COM14	55	N9	SEG11	88	F13	P13	121	B6	$\overline{TEST}$
23	K1	COM15	56	P10	SEG10	89	E14	P12	122	A5	OSC4
24	J3	SEG39	57	M9	SEG9	90	F12	P11	123	C6	OSC3
25	K2	SEG38	58	N10	SEG8	91	E13	P10	124	B5	V_{S1}
26	L1	SEG37	59	P11	SEG7	92	D14	P03	125	A4	OSC2
27	L2	SEG36	60	N11	SEG6	93	D13	P02	126	B4	OSC1
28	K3	SEG35	61	M10	SEG5	94	E12	P01	127	C5	V_{DD}
29	M1	SEG34	62	P12	SEG4	95	C14	P00	128	A3	V_{REF}
30	N1	SEG33	63	P13	SEG3	96	B14	R43	129	A2	V_{L1}
31	M2	N.C.	64	N12	SEG2	97	C13	R42	130	B3	V_{L2}
32	L3	N.C.	65	M11	SEG1	98	D12	N.C.	131	C4	V_{L3}
33	N2	N.C.	66	N13	SEG0	99	B13	N.C.	132	B2	V_{L4}

Table 18.2.2 Pin coordinates (S1C624A0)

Pin No.	Coordinate	Name	Pin No.	Coordinate	Name	Pin No.	Coordinate	Name	Pin No.	Coordinate	Name
1	C3	V_{L5}	34	M3	SEG32	67	M12	N.C.	100	C12	N.C.
2	A1	CF	35	P1	SEG31	68	P14	N.C.	101	A14	R41
3	D3	CE	36	M4	SEG30	69	L12	$\overline{SCLK}$	102	C11	R40
4	C2	CD	37	N3	SEG29	70	M13	SOUT	103	B12	R33
5	B1	CC	38	P2	SEG28	71	N14	SIN	104	A13	R32
6	C1	CB	39	P3	SEG27	72	M14	K13	105	A12	R31
7	E3	CA	40	M5	SEG26	73	K12	K12	106	C10	R30
8	D2	COM0	41	N4	SEG25	74	L13	K11	107	B11	R23
9	D1	COM1	42	P4	SEG24	75	L14	K10	108	A11	R22
10	E2	COM2	43	N5	SEG23	76	K13	K03	109	B10	R21
11	F3	COM3	44	M6	SEG22	77	J12	K02	110	C9	R20
12	E1	COM4	45	P5	SEG21	78	K14	K01	111	A10	R13
13	F2	COM5	46	N6	SEG20	79	J13	K00	112	B9	R12
14	F1	COM6	47	P6	SEG19	80	J14	P33	113	A9	R11
15	G3	COM7	48	M7	SEG18	81	H12	P32	114	C8	R10
16	G2	COM8	49	N7	SEG17	82	H13	P31	115	B8	R03
17	G1	COM9	50	P7	SEG16	83	H14	P30	116	A8	R02
18	H1	COM10	51	P8	SEG15	84	G14	P23	117	A7	R01
19	H2	COM11	52	N8	SEG14	85	G13	P22	118	B7	R00
20	H3	COM12	53	M8	SEG13	86	G12	P21	119	C7	V_{SS}
21	J1	COM13	54	P9	SEG12	87	F14	P20	120	A6	$\overline{RESET}$
22	J2	COM14	55	N9	SEG11	88	F13	P13	121	B6	$\overline{TEST}$
23	K1	COM15	56	P10	SEG10	89	E14	P12	122	A5	OSC4
24	J3	SEG39	57	M9	SEG9	90	F12	P11	123	C6	OSC3
25	K2	SEG38	58	N10	SEG8	91	E13	P10	124	B5	V_{S1}
26	L1	SEG37	59	P11	SEG7	92	D14	P03	125	A4	OSC2
27	L2	SEG36	60	N11	SEG6	93	D13	P02	126	B4	OSC1
28	K3	SEG35	61	M10	SEG5	94	E12	P01	127	C5	V_{DD}
29	M1	SEG34	62	P12	SEG4	95	C14	P00	128	A3	V_{REF}
30	N1	SEG33	63	P13	SEG3	96	B14	R43	129	A2	V_{L1}
31	M2	N.C.	64	N12	SEG2	97	C13	R42	130	B3	V_{L2}
32	L3	N.C.	65	M11	SEG1	98	D12	N.C.	131	C4	V_{L3}
33	N2	N.C.	66	N13	SEG0	99	B13	N.C.	132	B2	V_{L4}

Table 18.2.3 Pin coordinates (S1C624C0/480)

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	CB	37	SEG36	73	SEG1	109	R33
2	CA	38	SEG35	74	SEG0	110	R32
3	N.C.	39	SEG34	75	N.C.	111	R31
4	COM0	40	SEG33	76	$\overline{\text{SCLK}}$	112	R30
5	COM1	41	SEG32	77	SOUT	113	R23
6	COM2	42	SEG31	78	SIN	114	R22
7	COM3	43	SEG30	79	K13	115	R21
8	COM4	44	SEG29	80	K12	116	R20
9	COM5	45	SEG28	81	K11	117	R13
10	COM6	46	SEG27	82	K10	118	R12
11	COM7	47	SEG26	83	K03	119	R11
12	COM8	48	SEG25	84	N.C.	120	R10
13	COM9	49	SEG24	85	K02	121	R03
14	COM10	50	N.C.	86	K01	122	R02
15	COM11	51	SEG23	87	K00	123	R01
16	COM12	52	SEG22	88	P33	124	R00
17	COM13	53	SEG21	89	P32	125	V_{SS}
18	COM14	54	SEG20	90	P31	126	$\overline{\text{RESET}}$
19	N.C.	55	SEG19	91	P30	127	$\overline{\text{TEST}}$
20	COM15	56	SEG18	92	P23	128	OSC4
21	SEG50	57	SEG17	93	P22	129	OSC3
22	SEG49	58	SEG16	94	P21	130	V_{S1}
23	SEG48	59	SEG15	95	P20	131	OSC2
24	SEG47	60	SEG14	96	P13	132	OSC1
25	SEG46	61	SEG13	97	N.C.	133	N.C.
26	SEG45	62	SEG12	98	P12	134	V_{DD}
27	SEG44	63	SEG11	99	P11	135	V_{REF}
28	SEG43	64	SEG10	100	P10	136	V_{L1}
29	SEG42	65	SEG9	101	P03	137	V_{L2}
30	SEG41	66	SEG8	102	P02	138	V_{L3}
31	SEG40	67	SEG7	103	P01	139	V_{L4}
32	SEG39	68	SEG6	104	P00	140	V_{L5}
33	SEG38	69	SEG5	105	R43	141	CF
34	SEG37	70	SEG4	106	R42	142	CE
35	N.C.	71	SEG3	107	R41	143	CD
36	N.C.	72	SEG2	108	R40	144	CC

CHAPTER 19 PAD LAYOUT

19.1 Diagram of Pad Layout

S1C62440

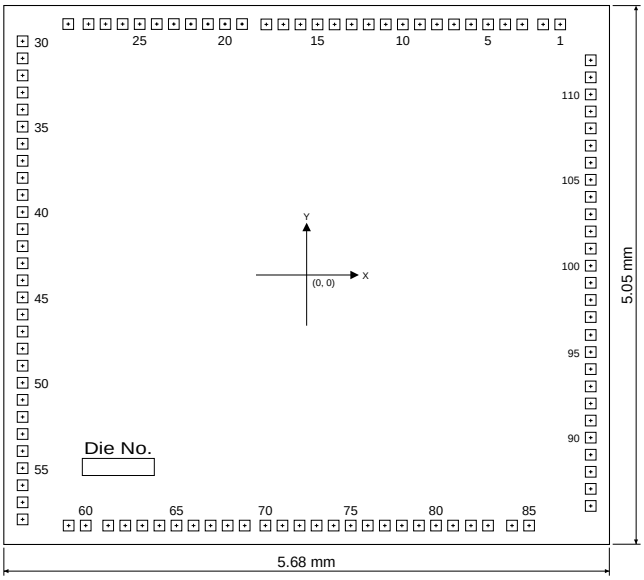


Fig. 19.1.1
Pad layout diagram
(S1C62440)

Chip size: 5.68 mm × 5.05 mm

S1C624A0

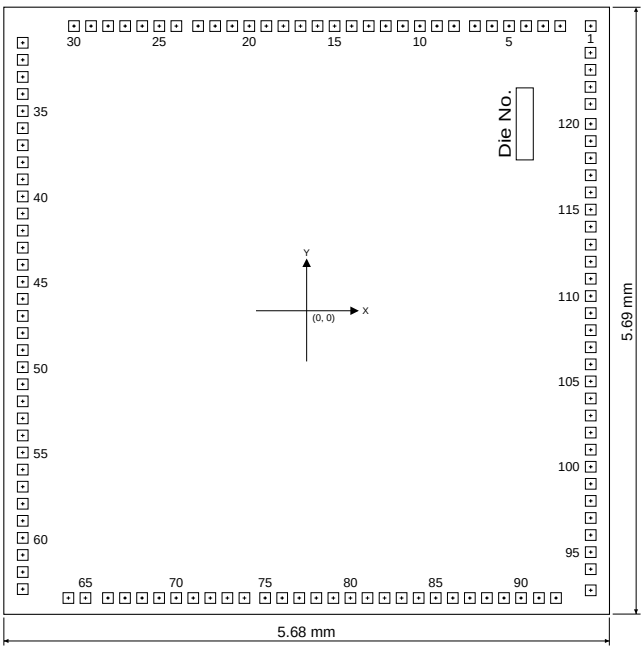


Fig. 19.1.2
Pad layout diagram
(S1C624A0)

Chip size: 5.68 mm × 5.69 mm

S1C624C0/480

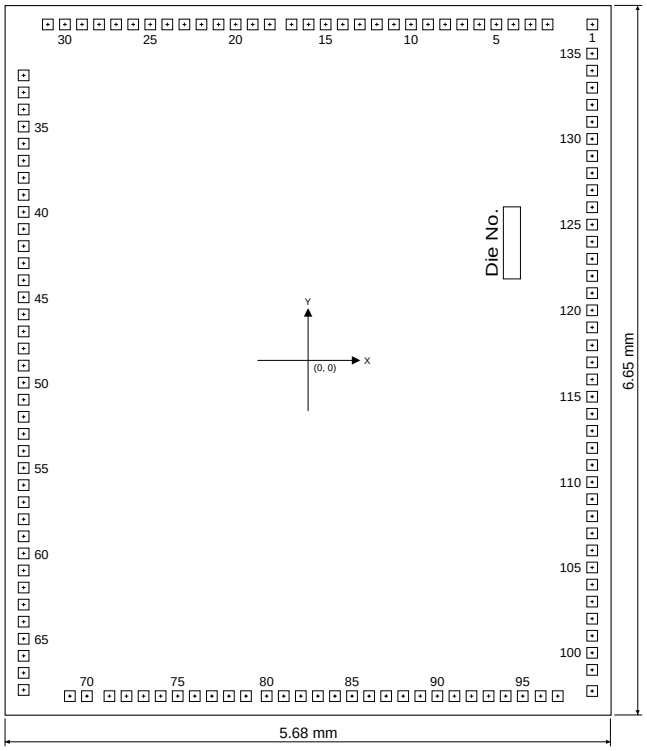


Fig. 19.1.3
Pad layout diagram
(S1C624C0/480)

Chip size: 5.68 mm × 6.65 mm

19.2 Pad Coordinates

Table 19.2.1 Pad coordinates (S1C62440)

Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]
1	CB	2.378	2.348	39	SEG19	-2.664	0.750	77	P10	0.733	-2.348
2	CA	2.218	2.348	40	SEG18	-2.664	0.590	78	P03	0.893	-2.348
3	COM0	2.022	2.348	41	SEG17	-2.664	0.430	79	P02	1.053	-2.348
4	COM1	1.862	2.348	42	SEG16	-2.664	0.270	80	P01	1.213	-2.348
5	COM2	1.702	2.348	43	SEG15	-2.664	0.110	81	P00	1.373	-2.348
6	COM3	1.542	2.348	44	SEG14	-2.664	-0.050	82	R43	1.541	-2.348
7	COM4	1.382	2.348	45	SEG13	-2.664	-0.210	83	R42	1.701	-2.348
8	COM5	1.222	2.348	46	SEG12	-2.664	-0.370	84	R41	1.926	-2.348
9	COM6	1.062	2.348	47	SEG11	-2.664	-0.530	85	R40	2.086	-2.348
10	COM7	0.902	2.348	48	SEG10	-2.664	-0.690	86	R33	2.664	-2.164
11	COM8	0.742	2.348	49	SEG9	-2.664	-0.850	87	R32	2.664	-2.004
12	COM9	0.582	2.348	50	SEG8	-2.664	-1.010	88	R31	2.664	-1.844
13	COM10	0.422	2.348	51	SEG7	-2.664	-1.170	89	R30	2.664	-1.684
14	COM11	0.262	2.348	52	SEG6	-2.664	-1.330	90	R23	2.664	-1.524
15	COM12	0.102	2.348	53	SEG5	-2.664	-1.490	91	R22	2.664	-1.364
16	COM13	-0.058	2.348	54	SEG4	-2.664	-1.650	92	R21	2.664	-1.204
17	COM14	-0.218	2.348	55	SEG3	-2.664	-1.810	93	R20	2.664	-1.044
18	COM15	-0.378	2.348	56	SEG2	-2.664	-1.970	94	V_{SS}	2.664	-0.882
19	SEG39	-0.582	2.348	57	SEG1	-2.664	-2.130	95	$\overline{RESET}$	2.664	-0.722
20	SEG38	-0.742	2.348	58	SEG0	-2.664	-2.290	96	$\overline{TEST}$	2.664	-0.562
21	SEG37	-0.902	2.348	59	$\overline{SCLK}$	-2.232	-2.348	97	OSC4	2.664	-0.394
22	SEG36	-1.062	2.348	60	SOUT	-2.072	-2.348	98	OSC3	2.664	-0.234
23	SEG35	-1.222	2.348	61	SIN	-1.861	-2.348	99	V_{S1}	2.664	-0.073
24	SEG34	-1.382	2.348	62	K13	-1.701	-2.348	100	OSC2	2.664	0.087
25	SEG33	-1.542	2.348	63	K12	-1.541	-2.348	101	OSC1	2.664	0.247
26	SEG32	-1.702	2.348	64	K11	-1.381	-2.348	102	V_{DD}	2.664	0.408
27	SEG31	-1.862	2.348	65	K10	-1.221	-2.348	103	V_{REF}	2.664	0.569
28	SEG30	-2.022	2.348	66	K03	-1.061	-2.348	104	V_{L1}	2.664	0.732
29	SEG29	-2.182	2.348	67	K02	-0.901	-2.348	105	V_{L2}	2.664	0.892
30	SEG28	-2.664	2.190	68	K01	-0.741	-2.348	106	V_{L3}	2.664	1.052
31	SEG27	-2.664	2.030	69	K00	-0.581	-2.348	107	V_{L4}	2.664	1.212
32	SEG26	-2.664	1.870	70	P23	-0.387	-2.348	108	V_{L5}	2.664	1.374
33	SEG25	-2.664	1.710	71	P22	-0.227	-2.348	109	CF	2.664	1.532
34	SEG24	-2.664	1.550	72	P21	-0.067	-2.348	110	CE	2.664	1.692
35	SEG23	-2.664	1.390	73	P20	0.093	-2.348	111	CD	2.664	1.852
36	SEG22	-2.664	1.230	74	P13	0.253	-2.348	112	CC	2.664	2.012
37	SEG21	-2.664	1.070	75	P12	0.413	-2.348				
38	SEG20	-2.664	0.910	76	P11	0.573	-2.348				

Table 19.2.2 Pad coordinates (S1C624A0)

Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]
1	V_{L5}	2.664	2.668	43	SEG20	-2.664	0.590	85	P11	1.213	-2.668
2	CF	2.378	2.668	44	SEG19	-2.664	0.430	86	P10	1.373	-2.668
3	CE	2.218	2.668	45	SEG18	-2.664	0.270	87	P03	1.533	-2.668
4	CD	2.058	2.668	46	SEG17	-2.664	0.110	88	P02	1.693	-2.668
5	CC	1.898	2.668	47	SEG16	-2.664	-0.050	89	P01	1.853	-2.668
6	CB	1.738	2.668	48	SEG15	-2.664	-0.210	90	P00	2.013	-2.668
7	CA	1.578	2.668	49	SEG14	-2.664	-0.370	91	R43	2.181	2.668
8	COM0	1.382	2.668	50	SEG13	-2.664	-0.530	92	R42	2.341	-2.668
9	COM1	1.222	2.668	51	SEG12	-2.664	-0.690	93	R41	2.664	-2.620
10	COM2	1.062	2.668	52	SEG11	-2.664	-0.850	94	R40	2.664	-2.422
11	COM3	0.902	2.668	53	SEG10	-2.664	-1.010	95	R33	2.664	-2.262
12	COM4	0.742	2.668	54	SEG9	-2.664	-1.170	96	R32	2.664	-2.102
13	COM5	0.582	2.668	55	SEG8	-2.664	-1.330	97	R31	2.664	-1.942
14	COM6	0.422	2.668	56	SEG7	-2.664	-1.490	98	R30	2.664	-1.782
15	COM7	0.262	2.668	57	SEG6	-2.664	-1.650	99	R23	2.664	-1.622
16	COM8	0.102	2.668	58	SEG5	-2.664	-1.810	100	R22	2.664	-1.462
17	COM9	-0.058	2.668	59	SEG4	-2.664	-1.970	101	R21	2.664	-1.302
18	COM10	-0.218	2.668	60	SEG3	-2.664	-2.130	102	R20	2.664	-1.142
19	COM11	-0.378	2.668	61	SEG2	-2.664	-2.290	103	R13	2.664	-0.982
20	COM12	-0.538	2.668	62	SEG1	-2.664	-2.450	104	R12	2.664	-0.822
21	COM13	-0.698	2.668	63	SEG0	-2.664	-2.610	105	R11	2.664	-0.662
22	COM14	-0.858	2.668	64	$\overline{SCLK}$	-2.232	-2.668	106	R10	2.664	-0.502
23	COM15	-1.018	2.668	65	SOUT	-2.072	-2.668	107	R03	2.664	-0.342
24	SEG39	-1.222	2.668	66	SIN	-1.861	-2.668	108	R02	2.664	-0.182
25	SEG38	-1.382	2.668	67	K13	-1.701	-2.668	109	R01	2.664	-0.022
26	SEG37	-1.542	2.668	68	K12	-1.541	-2.668	110	R00	2.664	0.138
27	SEG36	-1.702	2.668	69	K11	-1.381	-2.668	111	V_{SS}	2.664	0.300
28	SEG35	-1.862	2.668	70	K10	-1.221	-2.668	112	$\overline{RESET}$	2.664	0.460
29	SEG34	-2.022	2.668	71	K03	-1.061	-2.668	113	$\overline{TEST}$	2.664	0.620
30	SEG33	-2.182	2.668	72	K02	-0.901	-2.668	114	OSC4	2.664	0.788
31	SEG32	-2.664	2.510	73	K01	-0.741	-2.668	115	OSC3	2.664	0.948
32	SEG31	-2.664	2.350	74	K00	-0.581	-2.668	116	V_{S1}	2.664	1.109
33	SEG30	-2.664	2.190	75	P33	-0.387	-2.668	117	OSC2	2.664	1.270
34	SEG29	-2.664	2.030	76	P32	-0.227	-2.668	118	OSC1	2.664	1.430
35	SEG28	-2.664	1.870	77	P31	-0.067	-2.668	119	V_{DD}	2.664	1.590
36	SEG27	-2.664	1.710	78	P30	0.093	-2.668	120	V_{REF}	2.664	1.751
37	SEG26	-2.664	1.550	79	P23	0.253	-2.668	121	V_{L1}	2.664	1.914
38	SEG25	-2.664	1.390	80	P22	0.413	-2.668	122	V_{L2}	2.664	2.074
39	SEG24	-2.664	1.230	81	P21	0.573	-2.668	123	V_{L3}	2.664	2.234
40	SEG23	-2.664	1.070	82	P20	0.733	-2.668	124	V_{L4}	2.664	2.394
41	SEG22	-2.664	0.910	83	P13	0.893	-2.668				
42	SEG21	-2.664	0.750	84	P12	1.053	-2.668				

Table 19.2.3 Pad coordinates (S1C624C0/480)

Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]	Pad No	Name	X [mm]	Y [mm]
1	CA	2.664	3.148	46	SEG22	-2.664	0.430	91	P10	1.373	-3.148
2	COM0	2.244	3.148	47	SEG21	-2.664	0.270	92	P03	1.533	-3.148
3	COM1	2.084	3.148	48	SEG20	-2.664	0.110	93	P02	1.693	-3.148
4	COM2	1.924	3.148	49	SEG19	-2.664	-0.050	94	P01	1.853	-3.148
5	COM3	1.764	3.148	50	SEG18	-2.664	-0.210	95	P00	2.013	-3.148
6	COM4	1.604	3.148	51	SEG17	-2.664	-0.370	96	R43	2.181	-3.148
7	COM5	1.444	3.148	52	SEG16	-2.664	-0.530	97	R42	2.341	-3.148
8	COM6	1.284	3.148	53	SEG15	-2.664	-0.690	98	R41	2.664	-3.100
9	COM7	1.124	3.148	54	SEG14	-2.664	-0.850	99	R40	2.664	-2.902
10	COM8	0.964	3.148	55	SEG13	-2.664	-1.010	100	R33	2.664	-2.742
11	COM9	0.804	3.148	56	SEG12	-2.664	-1.170	101	R32	2.664	-2.582
12	COM10	0.644	3.148	57	SEG11	-2.664	-1.330	102	R31	2.664	-2.422
13	COM11	0.484	3.148	58	SEG10	-2.664	-1.490	103	R30	2.664	-2.262
14	COM12	0.324	3.148	59	SEG9	-2.664	-1.650	104	R23	2.664	-2.102
15	COM13	0.164	3.148	60	SEG8	-2.664	-1.810	105	R22	2.664	-1.942
16	COM14	0.004	3.148	61	SEG7	-2.664	-1.970	106	R21	2.664	-1.782
17	COM15	-0.156	3.148	62	SEG6	-2.664	-2.130	107	R20	2.664	-1.622
18	SEG50	-0.360	3.148	63	SEG5	-2.664	-2.290	108	R13	2.664	-1.462
19	SEG49	-0.520	3.148	64	SEG4	-2.664	-2.450	109	R12	2.664	-1.302
20	SEG48	-0.680	3.148	65	SEG3	-2.664	-2.610	110	R11	2.664	-1.142
21	SEG47	-0.840	3.148	66	SEG2	-2.664	-2.770	111	R10	2.664	-0.982
22	SEG46	-1.000	3.148	67	SEG1	-2.664	-2.930	112	R03	2.664	-0.822
23	SEG45	-1.160	3.148	68	SEG0	-2.664	-3.090	113	R02	2.664	-0.662
24	SEG44	-1.320	3.148	69	$\overline{\text{SCLK}}$	-2.232	-3.148	114	R01	2.664	-0.502
25	SEG43	-1.480	3.148	70	SOUT	-2.072	-3.148	115	R00	2.664	-0.342
26	SEG42	-1.640	3.148	71	SIN	-1.861	-3.148	116	V_{SS}	2.664	-0.180
27	SEG41	-1.800	3.148	72	K13	-1.701	-3.148	117	$\overline{\text{RESET}}$	2.664	-0.020
28	SEG40	-1.960	3.148	73	K12	-1.541	-3.148	118	$\overline{\text{TEST}}$	2.664	0.140
29	SEG39	-2.120	3.148	74	K11	-1.381	-3.148	119	OSC4	2.664	0.308
30	SEG38	-2.280	3.148	75	K10	-1.221	-3.148	120	OSC3	2.664	0.468
31	SEG37	-2.440	3.148	76	K03	-1.061	-3.148	121	V_{S1}	2.664	0.629
32	SEG36	-2.664	2.670	77	K02	-0.901	-3.148	122	OSC2	2.664	0.790
33	SEG35	-2.664	2.510	78	K01	-0.741	-3.148	123	OSC1	2.664	0.950
34	SEG34	-2.664	2.350	79	K00	-0.581	-3.148	124	V_{DD}	2.664	1.111
35	SEG33	-2.664	2.190	80	P33	-0.387	-3.148	125	V_{REF}	2.664	1.271
36	SEG32	-2.664	2.030	81	P32	-0.227	-3.148	126	V_{L1}	2.664	1.434
37	SEG31	-2.664	1.870	82	P31	-0.067	-3.148	127	V_{L2}	2.664	1.594
38	SEG30	-2.664	1.710	83	P30	0.093	-3.148	128	V_{L3}	2.664	1.754
39	SEG29	-2.664	1.550	84	P23	0.253	-3.148	129	V_{L4}	2.664	1.914
40	SEG28	-2.664	1.390	85	P22	0.413	-3.148	130	V_{L5}	2.664	2.074
41	SEG27	-2.664	1.230	86	P21	0.573	-3.148	131	CF	2.664	2.234
42	SEG26	-2.664	1.070	87	P20	0.733	-3.148	132	CE	2.664	2.394
43	SEG25	-2.664	0.910	88	P13	0.893	-3.148	133	CD	2.664	2.554
44	SEG24	-2.664	0.750	89	P12	1.053	-3.148	134	CC	2.664	2.714
45	SEG23	-2.664	0.590	90	P11	1.213	-3.148	135	CB	2.664	2.874

II. S1C62440/624A0/624C0/62480 Technical Software

CONTENTS

CHAPTER 1 INTRODUCTION

The S1C62440/4A0/4C0/480 are a microcomputer with a C-MOS 4-bit core CPU S1C6200 as main component, and ROM, RAM, dot matrix LCD driver, time base counter, clock synchronous serial interface, etc. built-in.
Moreover, the S1C624A0/4C0/480 external memory device control is possible, and are most suitable for applications with equipment requiring large memory and dot matrix display functions such as a highly functional electronic pocketbook.

Table 1.1 Configuration of the S1C62440/4A0/4C0/480

Model	ROM capacity	RAM capacity	Number of segment pins	External memory control
S1C62440	4,096 words	384 words	40	Not used
S1C624A0	6,144 words	640 words	40	Used
S1C624C0	5,120 words	1,152 words	51	Used
S1C62480	8,192 words	768 words	51	Used

CHAPTER 2 BLOCK DIAGRAM

S1C62440

The S1C62440/4A0/4C0/480 block diagrams are shown in Figures 2.1–2.4.

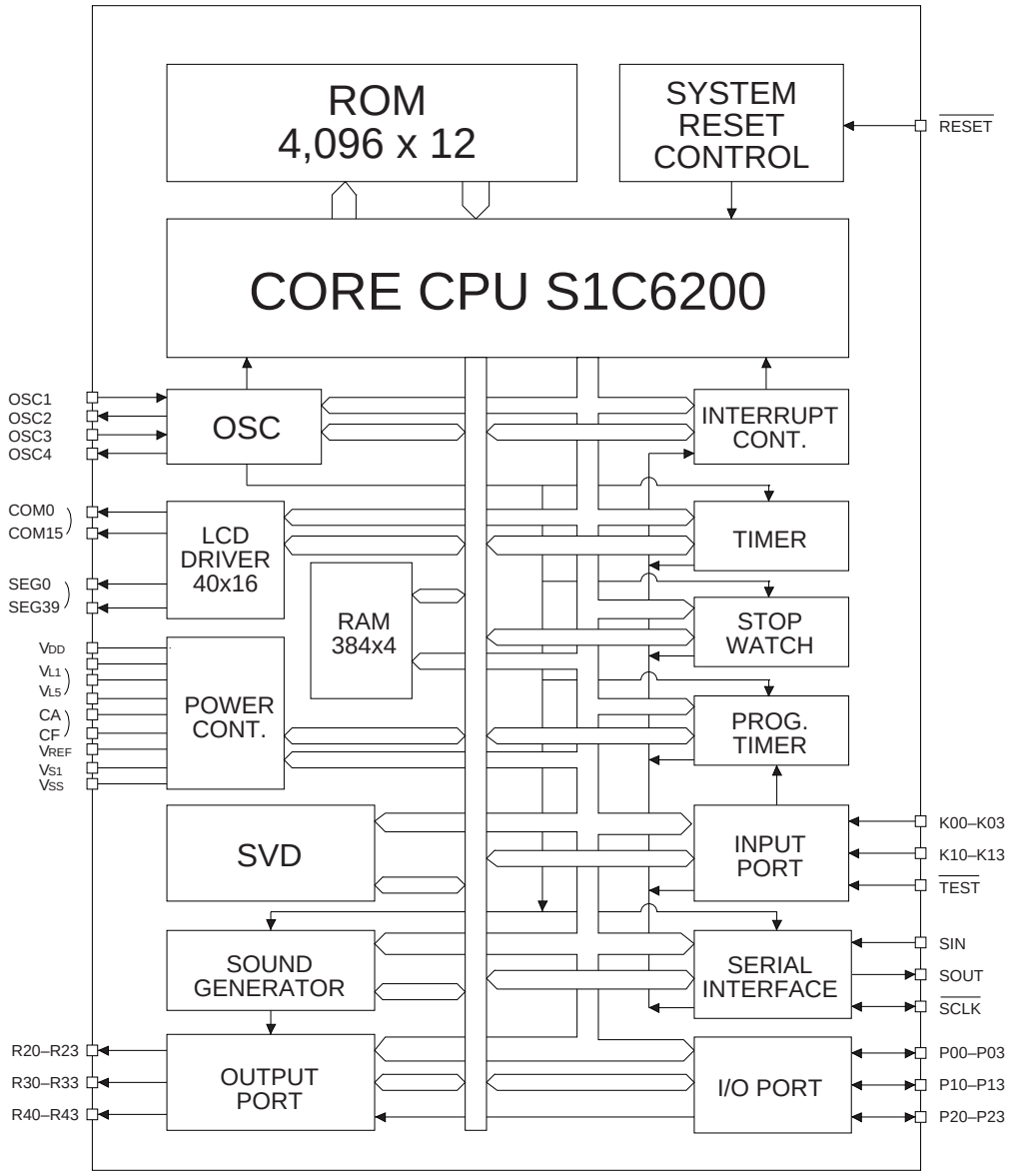


Fig. 2.1
S1C62440 block diagram

S1C624A0

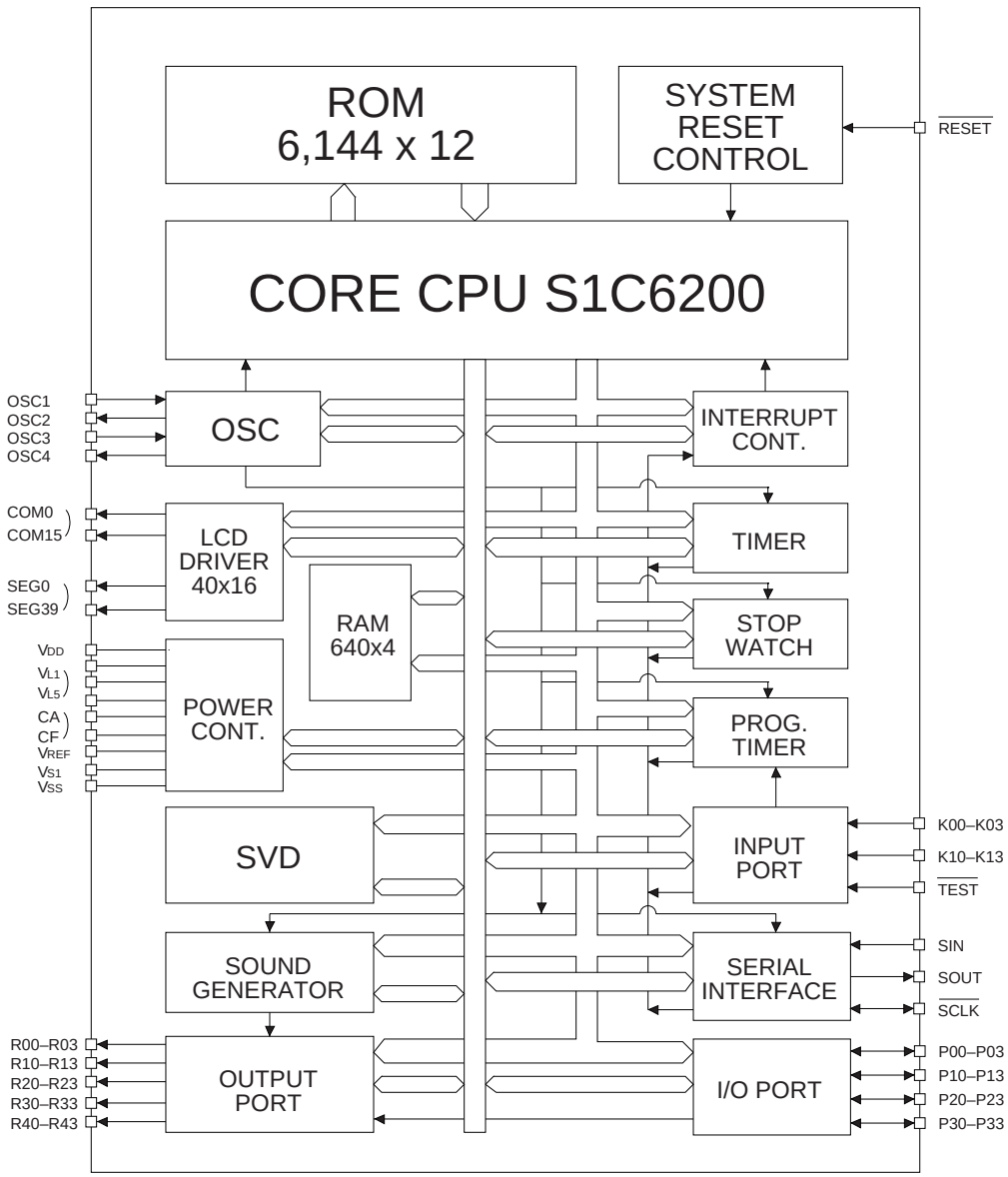


Fig. 2.2
S1C624A0 block diagram

S1C624C0

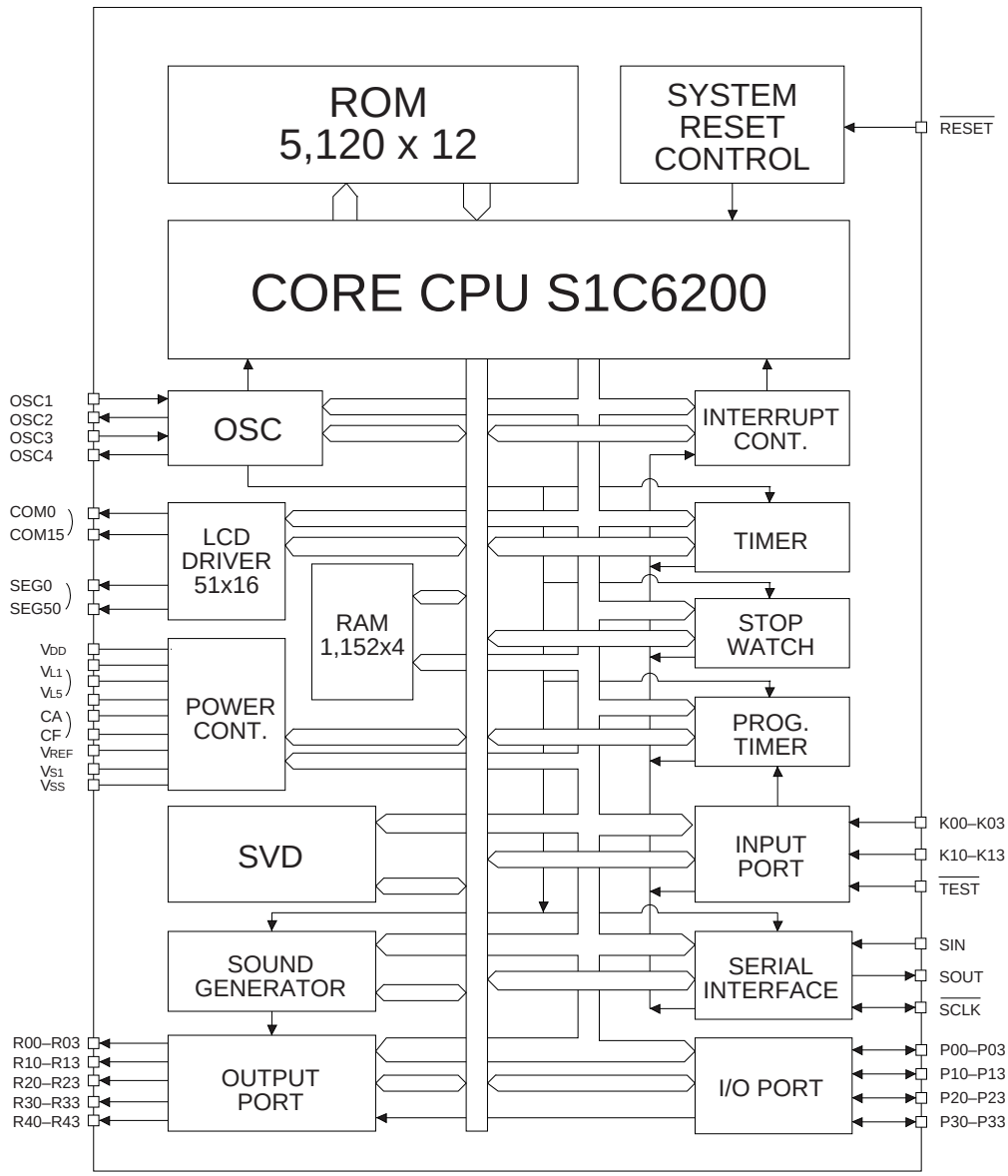


Fig. 2.3
S1C624C0 block diagram

S1C62480

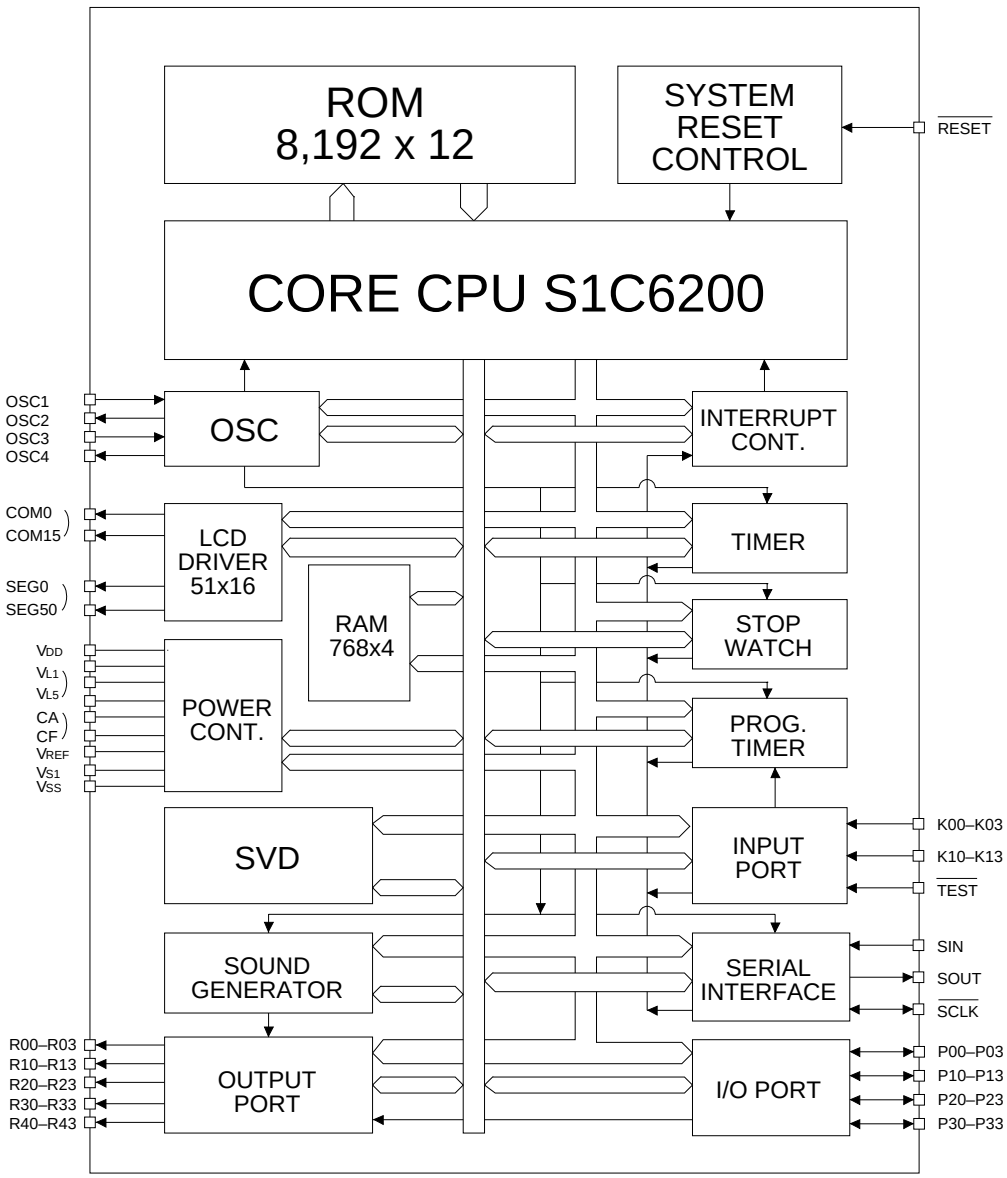


Fig. 2.4
S1C62480 block diagram

CHAPTER 3 PROGRAM MEMORY (ROM)

3.1 Configuration of the ROM

The S1C62440/4A0/4C0/480 have a built-in mask ROM with the following capacity for program storage.

Model	ROM capacity	Configuration
S1C62440	4,096 steps × 12 bits	0000H–0FFFH (bank 0: 16 page, bank 1: non)
S1C624A0	6,144 steps × 12 bits	0000H–17FFH (bank 0: 16 page, bank 1: 8 page)
S1C624C0	5,120 steps × 12 bits	0000H–13FFH (bank 0: 16 page, bank 1: 4 page)
S1C62480	8,192 steps × 12 bits	0000H–1FFFH (bank 0: 16 page, bank 1: 16 page)

* One page is composed of 256 steps.

After initial reset, the program beginning address is bank 0, page 1, step 00H. The interrupt vector is allocated to each page 1, steps 02H–0CH.
The configuration of the ROM is as shown in Figures 3.1.1(a)–(d).

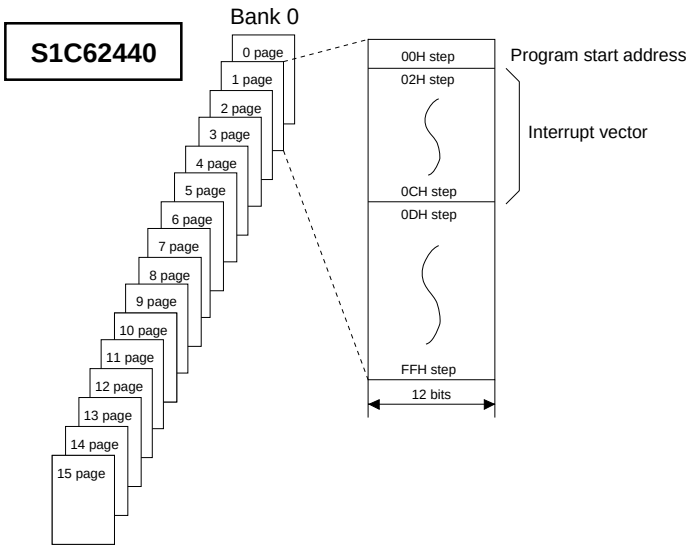


Fig. 3.1.1(a)
Configuration of
the built-in ROM (S1C62440)

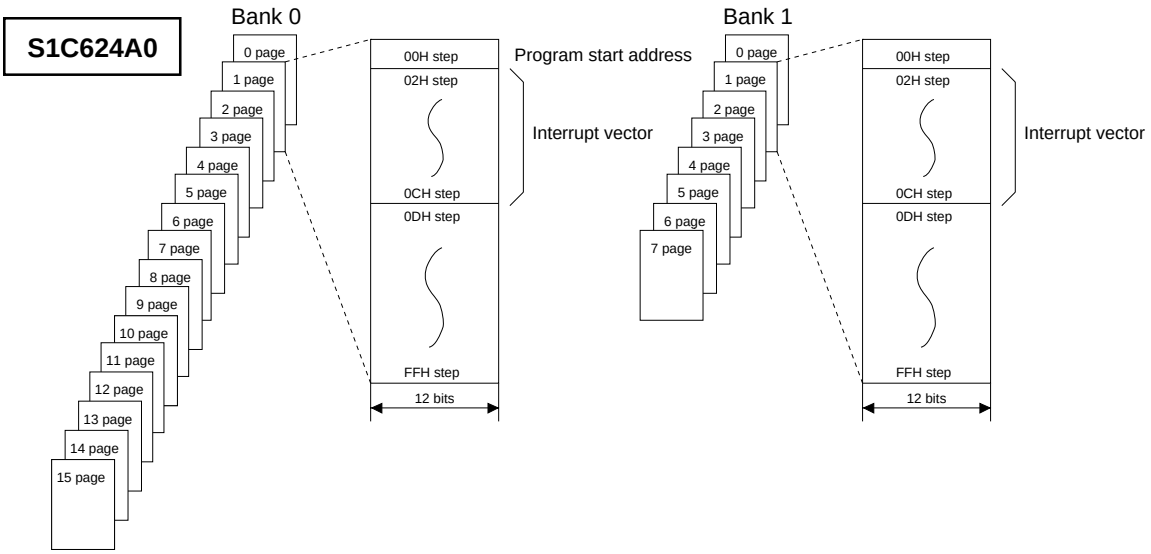


Fig. 3.1.1(b)
Configuration of
the built-in ROM (S1C624A0)

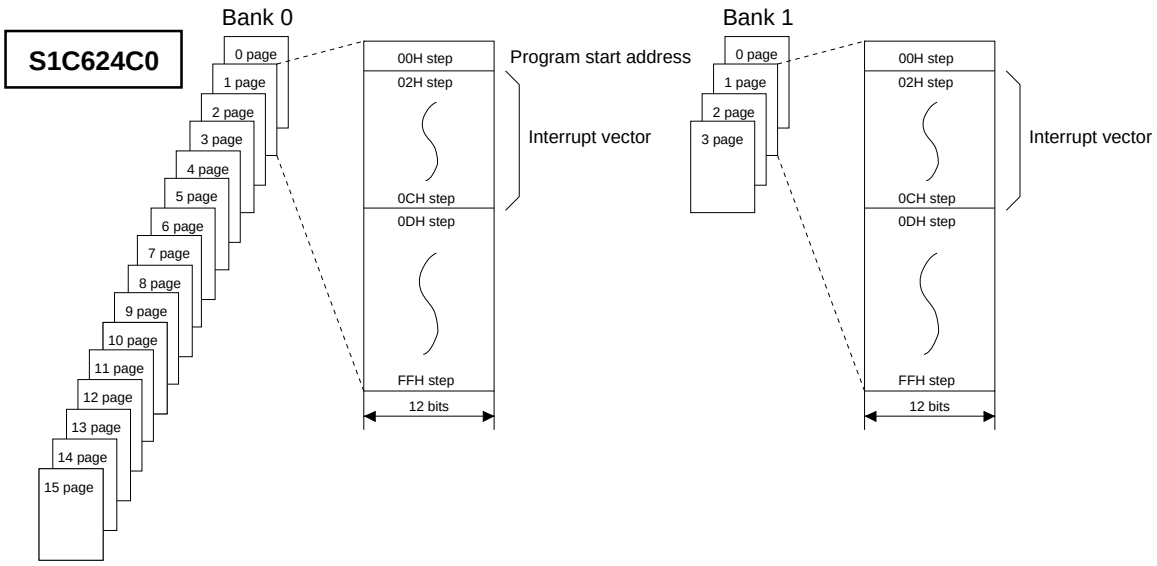


Fig. 3.1.1(c)
Configuration of
the built-in ROM (S1C624C0)

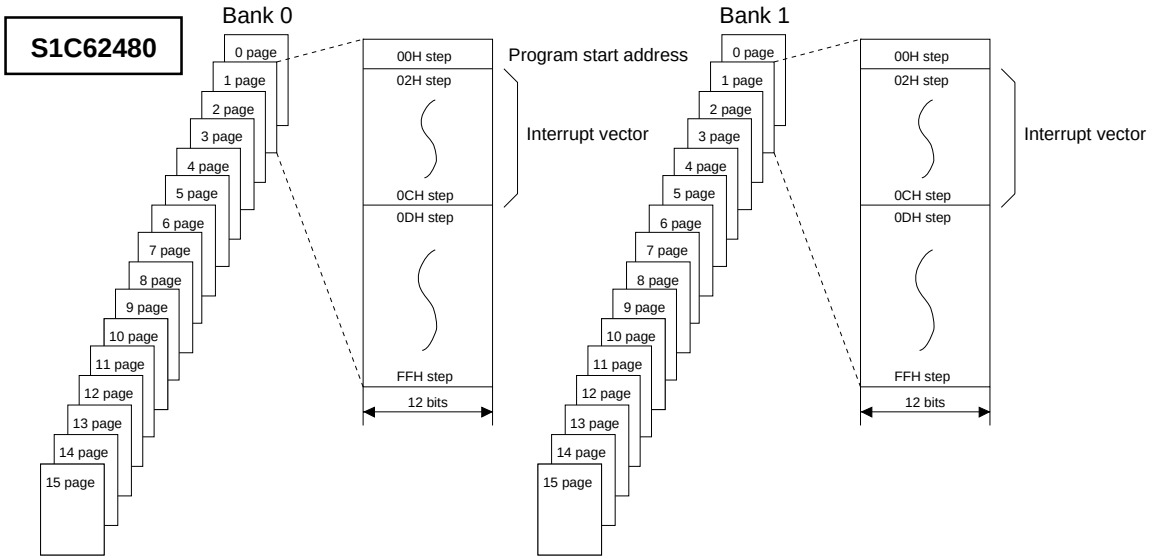


Fig. 3.1.1(d)
Configuration of
the built-in ROM (S1C62480)

3.2 Interrupt Vector

The interrupt vector and interrupt request correspondence is shown in Table 3.2.1.

Table 3.2.1
Interrupt request and interrupt vectors

Interrupt vector (PCS and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Serial interface interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

CHAPTER 4 DATA MEMORY

4.1 Configuration of the Data Memory

The S1C62440/4A0/4C0/480 built-in data memorys are configured a general-purpose RAM, display data memory of the LCD, and I/O data memory which controls the peripheral circuit.

Table 4.1.1 Data memory capacity

Model	RAM capacity	Display data memory
S1C62440	384 words × 4 bits (000H–17FH)	160 words × 4 bits (E00H–E4FH, E80H–ECFH)
S1C624A0	640 words × 4 bits (000H–27FH)	160 words × 4 bits (E00H–E4FH)
S1C624C0	1,152 words × 4 bits (000H–47FH)	204 words × 4 bits (E00H–E65H, E80H–EF5H)
S1C62480	768 words × 4 bits (000H–2FFH)	204 words × 4 bits (E00H–E65H, E80H–EF5H)

During programming, take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

The memory map of the built-in data memory (RAM) and details of the I/O data memory map are shown in Figures 4.1.1(a)–(d) and Tables 4.2.1(a)–(f), respectively.

Note *Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.*

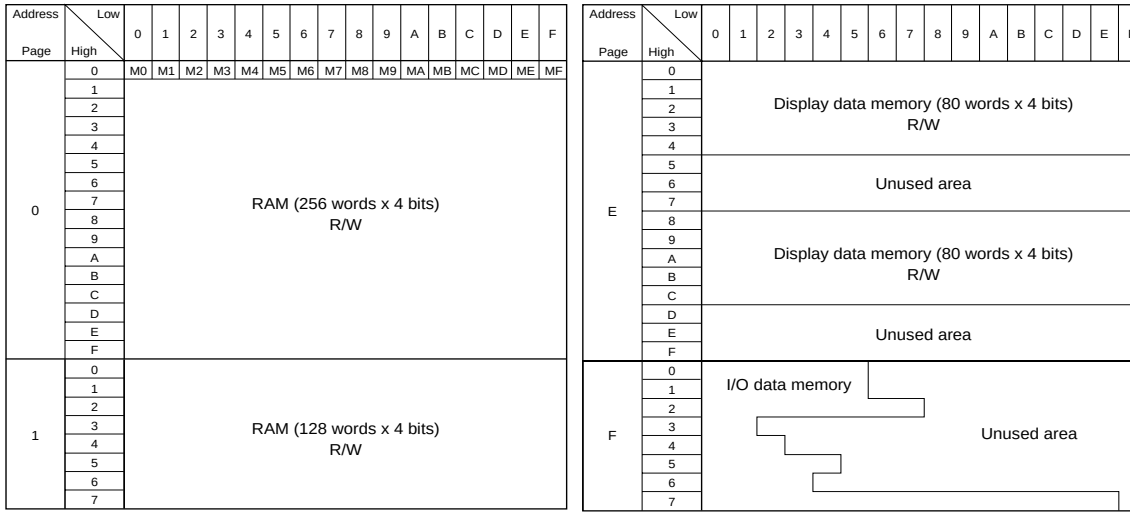


Fig. 4.1.1(a) Memory map (S1C62440)

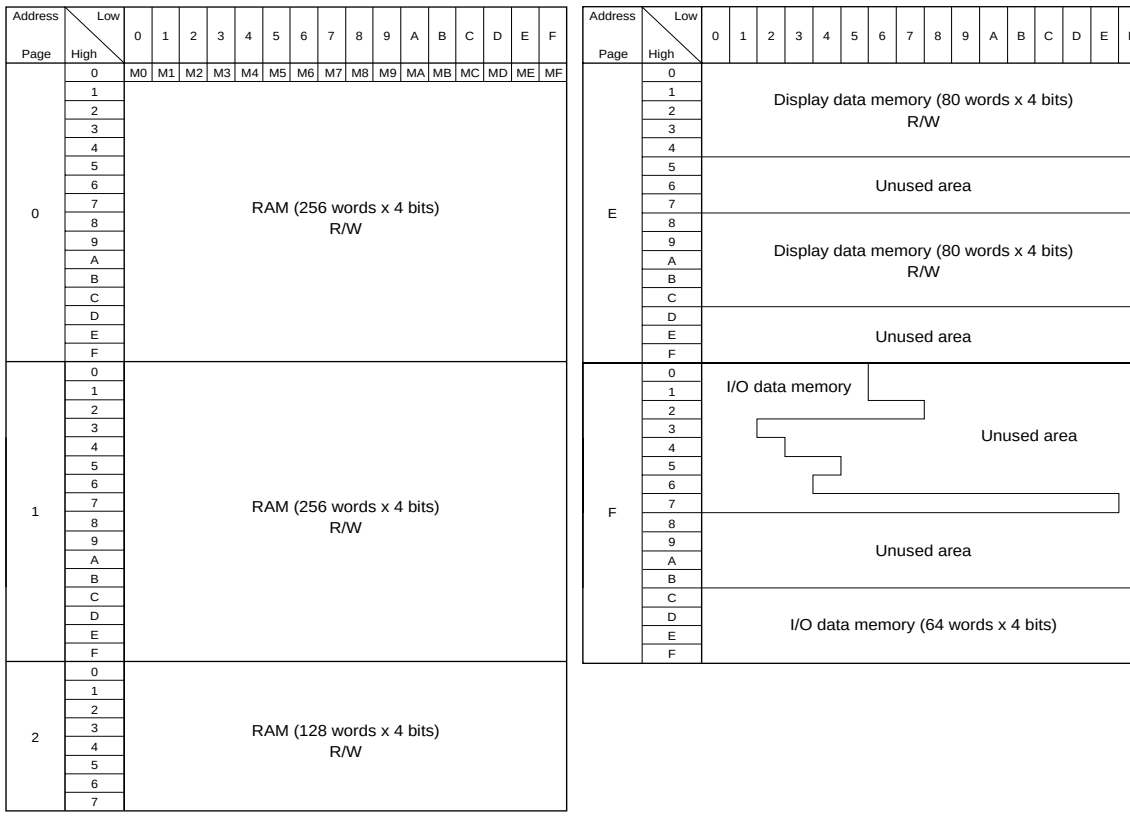


Fig. 4.1.1(b) Memory map (S1C624A0)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
0	1–F	RAM (256 words x 4 bits) R/W															
1	0–F	RAM (256 words x 4 bits) R/W															
2	0–F	RAM (256 words x 4 bits) R/W															
3	0–F	RAM (256 words x 4 bits) R/W															
4	0–7	RAM (128 words x 4 bits) R/W															

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0–6	Display data memory (102 words x 4 bits) R/W															
	7	Unused area															
	8–E	Display data memory (102 words x 4 bits) R/W															
	F	Unused area															
F	0	I/O data memory															
	1–3	Unused area															
	4–6	Unused area															
	7	Unused area															
	8–B	Unused area															
	C–F	I/O data memory (64 words x 4 bits)															

Fig. 4.1.1(c) Memory map (S1C624C0)

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM (256 words x 4 bits) R/W															
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
1	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
2	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0	Display data memory (102 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7	Unused area															
	8	Display data memory (102 words x 4 bits) R/W															
	9																
	A																
	B																
	C																
	D																
	E																
	F	Unused area															
F	0	I/O data memory															
	1																
	2																
	3	Unused area															
	4																
	5																
	6																
	7																
	8	Unused area															
	9																
	A																
	B																
	C	I/O data memory (64 words x 4 bits)															
	D																
	E																
	F																

Fig. 4.1.1(d) Memory map (S1C62480)

4.2 Detail Map of the I/O Data Memory

Tables 4.2.1(a)–(f) show the detail map of the I/O data memory.

Table 4.2.1(a) I/O data memory map (F00H–F05H, F10H–F15H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1 *3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F03H	0	0	0	ISIO	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					ISIO *3	0	Yes	No	Interrupt factor flag (serial interface)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0 *3	– *2			
					0 *3	– *2			
	R				0 *3	– *2			
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *3	– *2			
					0 *3	– *2			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F13H	0	0	0	EISIO	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Reset (0) immediately after being read
*4 Always "0" when being read

Table 4.2.1(b) I/O data memory map (F20H–F27H, F30H, F31H, F40H–F42H)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB Stopwatch timer
					SWL2	0			1/100 sec data (BCD)
	R				SWL1	0			
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB Stopwatch timer
					SWH2	0			1/10 sec data (BCD)
	R				SWH1	0			
					SWH0	0			LSB
F24H	PT3	PT2	PT1	PT0	PT3	X *3			MSB Programmable timer data (low-order)
					PT2	X *3			
	R				PT1	X *3			
					PT0	X *3			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X *3			MSB Programmable timer data (high-order)
					PT6	X *3			
	R				PT5	X *3			
					PT4	X *3			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X *3			MSB Programmable timer
					RD2	X *3			reload data (low-order)
	R/W				RD1	X *3			
					RD0	X *3			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X *3			MSB Programmable timer
					RD6	X *3			reload data (high-order)
	R/W				RD5	X *3			
					RD4	X *3			LSB
F30H	SD3	SD2	SD1	SD0	SD3	X *3			MSB Serial interface
					SD2	X *3			data register (low-order)
	R/W				SD1	X *3			
					SD0	X *3			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X *3			MSB Serial interface
					SD6	X *3			data register (high-order)
	R/W				SD5	X *3			
					SD4	X *3			LSB
F40H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
					DFK02	1	↓	↑	
	R/W				DFK01	1	↓	↑	
					DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	
					K10	– *2	High	Low	

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Undefined

Table 4.2.1(c) I/O data memory map (F50H–F54H, F60H–F63H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F50H *6	R03	R02	R01	R00	R03	X *2	High	Low	Output port (R03) / External memory address (A3)
					R02	X *2	High	Low	Output port (R02) / External memory address (A2)
	R/W				R01	X *2	High	Low	Output port (R01) / External memory address (A1)
					R00	X *2	High	Low	Output port (R00) / External memory address (A0)
F51H *6	R13	R12	R11	R10	R13	X *2	High	Low	Output port (R13) / External memory address (A7)
					R12	X *2	High	Low	Output port (R12) / External memory address (A6)
	R/W				R11	X *2	High	Low	Output port (R11) / External memory address (A5)
					R10	X *2	High	Low	Output port (R10) / External memory address (A4)
F52H	R23	R22	R21	R20	R23	X *2	High	Low	Output port (R23) / External memory address (A11) *4
					R22	X *2	High	Low	Output port (R22) / External memory address (A10) *4
	R/W				R21	X *2	High	Low	Output port (R21) / External memory address (A9) *4
					R20	X *2	High	Low	Output port (R20) / External memory address (A8) *4
F53H	R33	R32	R31	R30	R33	X *2	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						*3	*3	[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X *2	High	Low	Output port (R32)
							*3	*3	[External memory read ($\overline{\text{RD}}$)] *4
					R31	X *2	High	Low	Output port (R31) / External memory address (A13) *4
							*3	*3	[External memory write ($\overline{\text{WR}}$)] *4
					R30	X *2	High	Low	Output port (R30) / External memory address (A12) *4
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
							*3	*3	[Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
							Off	On	LCD synchronous signal (CL)
F60H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data (D3) *5
					P02	X *2	High	Low	I/O port (P02) / External memory data (D2) *5
	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data (D1) *5
					P00	X *2	High	Low	I/O port (P00) / External memory data (D0) *5
F61H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data (D7) *5
					P12	X *2	High	Low	I/O port (P12) / External memory data (D6) *5
	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data (D5) *5
					P10	X *2	High	Low	I/O port (P10) / External memory data (D4) *5
F62H	P23	P22	P21	P20	P23	X *2	High	Low	I/O port (P23) / External memory CS ($\overline{\text{CS3}}$) *5
					P22	X *2	High	Low	I/O port (P22) / External memory CS ($\overline{\text{CS2}}$) *5
	R/W				P21	X *2	High	Low	I/O port (P21) / External memory CS ($\overline{\text{CS1}}$) *5
	W				P20	X *2	High	Low	I/O port (P20) / External memory CS ($\overline{\text{CS0}}$) *5
F63H *6	P33	P32	P31	P30	P33	X *2	High	Low	I/O port / Dedicated output port (P33)
					P32	X *2	High	Low	I/O port / Dedicated output port (P32)
	R/W				P31	X *2	High	Low	I/O port / Dedicated output port (P31)
					P30	X *2	High	Low	I/O port / Dedicated output port (P30)

*1 Initial value following initial reset
*2 Undefined
*3 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs
*4 In the S1C62440, it can be used only as a port for output
*5 In the S1C62440, it can be used only as a port for I/O port
*6 In the S1C62440, the F50H, F51H and F63H cannot be used

Table 4.2.1(d) I/O data memory map (F70H–F79H)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X *4			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
					LC2	X *4			
	R/W				LC1	X *4			
					LC0	X *4			
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1 *5	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X *4			SVD criteria voltage setting
					SVC0	X *4			
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			Buzzer frequency selection
	R/W				BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
	W	W	R/W		ENVRST	RESET	Reset	–	Envelope reset
	R				ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *3	– *2			
					0 *3	– *2			
	R		W		TMRST *3	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	SWRST *3	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
F78H	0	0	PTRST	PTRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	PTRST *3	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			Programmable timer input clock selection
	R/W				PTC1	0			
					PTC0	0			

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 Undefined
*5 When SVD is off, "1" is read out

Table 4.2.1(e) I/O data memory map (F7AH–F7EH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG*3	–	Trigger	–	Serial interface clock trigger
					SEN	0	⌐↓	↓⌐	Serial interface clock edge selection
	W	R/W			SCS1	0			Serial interface clock mode selection
					SCS0	0			
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3*3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1*6	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0*6	0	Output	High-Z	R00–R03 output high-impedance control
F7CH	0	HZCS	ADINC	PICON	0 *3	– *2			
					HZCS *5, 7	0	Output	High-Z	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
	R	R/W	W	R/W	ADINC *3, 4, 6	– *2	Increment	–	External memory address increment (A0–A13)
					PICON *4, 7	0	Auto Inc.	Normal	External memory address auto increment mode
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3*6	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
	R/W				IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3*6	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
	R/W				PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 Initial value following initial reset
*2 Not set in the circuit
*3 Always "0" when being read
*4 These control bits are only valid during selection of external memory/address output as output port option
*5 These control bits are only valid during selection of external memory/chip select output as I/O port option
*6 In the S1C62440, it is a register that becomes invalid and during reading it is always "0"
*7 In the S1C62440, it is used as a general purpose register that does not have a function

Table 4.2.1(f) I/O data memory map (FC0H–FFFH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FC0H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P03) / External memory data bus (D3)
					P02	X *2	High	Low	I/O port (P02) / External memory data bus (D2)
FFEH (even)*3	R/W				P01	X *2	High	Low	I/O port (P01) / External memory data bus (D1)
					P00	X *2	High	Low	I/O port (P00) / External memory data bus (D0)
FC1H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P13) / External memory data bus (D7)
					P12	X *2	High	Low	I/O port (P12) / External memory data bus (D6)
FFFH (odd)*3	R/W				P11	X *2	High	Low	I/O port (P11) / External memory data bus (D5)
					P10	X *2	High	Low	I/O port (P10) / External memory data bus (D4)

*1 Initial value following initial reset
*2 Undefined
*3 Image area of I/O ports (P00–P03, P10–P13) .... S1C624A0/4C0/480 only
See 6.14, "External Memory Access (S1C624A0/4C0/480)"

CHAPTER 5 INITIAL RESET

5.1 Initialized Status

The CPU core and peripheral circuits are initialized by initial resetting as follows:

Table 5.1.1 Initialized status

CPU core			
Name	Symbol	Bit length	Setting value
Program counter, step	PCS	8	00H
Program counter, page	PCP	4	1H
Program counter, bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register • IX	IX	12	Undefined
Index register • IY	IY	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register	A	4	Undefined
General-purpose register	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral circuit		
Name	Bit length	Setting value
RAM	4	Undefined
Segment data	4	Undefined
Other peripheral circuits	4	*

* See Tables 4.2.1(a)–(f).

Note *Undefined values must be defined by the program.*

5.2 Example Program for the System Initialization

Following program shows the example of the procedure for system initialization.
The program example is of an S1C624C0 and for the S1C62440/4A0/480, it is necessary to change the RAM and the clear field of the display data memory.

```
;*
;* INITIAL RESET PROGRAM FOR E0C624C
;*
;
ZCLKCG EQU    70H
ZSVD   EQU    73H
;
       ORG    100H
;
       JP     INIT
;
;
       ORG    10EH
;
INIT:
;* INITIALIZE CPU CORE AT THE BEGINNING
;
       RST    F,0000B   ;CLEAR IDZC FLAGS
;
       LD     A,00H     ;SET STACKPOINTER TO 00H
       LD     SPH,A
       LD     A,00H
       LD     SPL,A
;
;* SETUP THE OSC CONDITION
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     XP,A
;
       LD     X,ZSVD
       LD     MX,0110B  ;TURN ON SVD CIRCUIT & SVD
                        ; VOLTAGE IS SET AS -3.3V
       CALL   DLY100    ;WAIT FOR 100µS
       LD     A,MX
       AND    A,1000B   ;MASK OF SVD & THE RESULT
                        ; IS STORED IN "A"
```

```
        LD      MX,A
        JP      NZ,DMC00  ;IF (VDD-VSS) IS LOWER THAN 3.3V
                          ; THEN VS1 SHOULD BE -1.2V
;
OP21:   LD      X,ZCLKCG
        LD      A,0001B   ;IF (VDD-VSS) IS 3.3V OR MORE
                          ; THEN VS1 SHOULD BE -2.1V
        LD      MX,A
;
;* CLEAR DATA MEMORY
;
DMC00:  LD      XP,A      ;CLEAR PAGE0
        LD      X,00H
;
        LD      Y,00H     ;SET UP THE COUNTER
        RCF
;
P0LP:   LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,P0LP
;
DMC10:  LD      A,1       ;CLEAR PAGE1
        LD      XP,A
;
        LD      Y,00H     ;SET UP THE COUNTER
        RCF               In the case of the S1C62440,
;                         set to "80H"
P1LP:   LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,P1LP
;
DMC20:  LD      A,2       ;CLEAR PAGE2
        LD      XP,A
;
        LD      Y,00H     ;SET UP THE COUNTER
        RCF               In the case of the S1C624A0,
;                         set to "80H"
P2LP:   LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,P2LP
;
```

In the S1C62440 these are not necessary

```
DMC30:  LD      A,3         ;CLEAR PAGE3
        LD      XP,A
;
        LD      Y,00H       ;SET UP THE COUNTER
        RCF
;
P3LP:   LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,P3LP
;
DMC40:  LD      A,4         ;CLEAR PAGE4
        LD      XP,A
;
        LD      Y,80H       ;SET UP THE COUNTER
        RCF
;
P4LP:   LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,P4LP
;
;* CLEAR SEGMENT DATA MEMORY
;
SEG1:   LD      A,0EH       ;CLEAR 1ST PART
        LD      XP,A
        LD      X,00H
;
        LD      Y,80H       ;SET UP THE COUNTER
        RCF
;
SP1LP:  LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,SP1LP
;
SEG2:   LD      X,80H       ;CLEAR 2ND PART
;
        LD      Y,080H      ;SET UP THE COUNTER
        RCF
;
SP2LP:  LBPX    MX,00H
        ADC     YL,2
        ADC     YH,0
        JP      NC,SP2LP
;
```

In the S1C62440/4A0/480 these are not necessary

In the case of the S1C62440/4A0, set to "B0H"

In the case of the S1C62440/4A0, set to "B0H"

```
;* INITIALIZE PERIPHERAL CIRCUITS
;
CNTLCD:LD     A,0FH     ;SET CONTRAST FOR LCD DISPLAY
       LD     XP,A      ;SET PAGE FOR PERIPHERAL
;
       LD     X,72H     ;SET ADDRESS FOR LCD CONTROL
       LD     MX,8      ;SET CONTRAST "8"
;
;
RSTCTM:LD     X,76H     ;RESET CLOCK TIMER
       OR     MX,0010B
;
RSTWD: OR     MX,0001B  ;RESET WATCHDOG TIMER
;
       LD     X,00H     ;RESET CLOCK TIMER INTERRUPT
                        ; FLAG
       LD     A,MX
;
       RST    F,0000B   ;CLEAR IDZC FLAGS
       LD     A,0
;
;
            :
            :
;
DLY100:                 ;THE SUBROUTINE TO WAIT 100µS
            :           ;SOFTWARE TIMER ROUTINE DEPENDS
            :           ; ON OSC FREQUENCY
       RET
```

5.3 Programming Note for the System Initialization

In some of initial registers and initial data memory area, the initial value is undefined after reset. Set them proper initial values by the program, as necessary.

CHAPTER 6 PERIPHERAL CIRCUITS

6.1 Watchdog Timer

I/O data memory of the watchdog timer

The control register of the watchdog timer is shown in Table 6.1.1.

Table 6.1.1 Control register of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F76H	0	0	TMRST	WDRST	0	–			
	R		W		0	–		–	
					TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

Example program for the watchdog timer

Following program shows the reset procedure for watchdog timer.

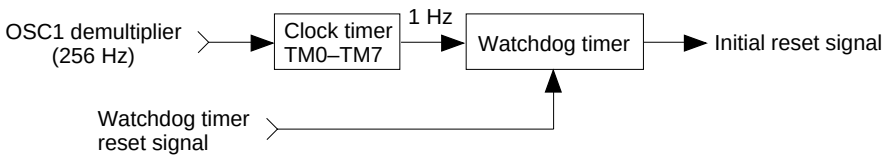


Fig. 6.1.1 Configuration of watchdog timer

```
;*
;*
;* RESET WATCHDOG TIMER
;*
ZWDRST  EQU     76H         ;WATCHDOG PORT ADDRESS
XWDR    EQU     0001B       ;WATCHDOG RESET BIT
;
        LD      A,0FH       ;SET TO I/O DATA MEMORY ADDRESS
        LD      XP,A
;
        LD      X,ZWDTM     ;SET WATCHDOG PORT ADDRESS
        OR      MX,XWDR     ;RESET WATCHDOG TIMER
;
;
```

Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST←"1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

6.2 Oscillation Circuit

I/O data memory of the oscillation circuit

The control registers of the oscillation circuit are shown in Table 6.2.1.

Table 6.2.1 Control registers of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock change
	R/W				OSCC	0	On	Off	OSC3 oscillation On/Off
					VSC1	0			CPU operating voltage switch
					VSC0	0			

Switches the operating voltage of the internal circuit in accordance to the oscillation frequency and power source voltage.
The corresponding setting description is shown in Table 6.2.2.

Table 6.2.2 Corresponding between oscillation frequency, power source voltage, and operating voltage (V_{S1})

VSC1	VSC0	V_{S1}	Oscillation circuit	Oscillation frequency	Power source voltage (V_{DD}–V_{SS})
0	0	-1.2 V	OSC1	32.768 kHz	Under 3.1 V
0	1	-2.1 V	OSC1	32.768 kHz	3.1 V or more (*)
0	1	-2.1 V	OSC3	1 MHz	2.2 V or more
1	×	-3.0 V	OSC3	2 MHz	3.1 V or more

The V_{DD} is reference voltage as 0 V. And the voltage value of V_{S1} is refered to V_{DD}.
In the case of using a lithium battery of which initial source voltage is around 3.6 V as power source, it will be permitted to use VSC1 = "0" and VSC0 = "0" condition instead of the (*) condition.
VSC1 and VSC0 are set to "0" at initial reset.

Note When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

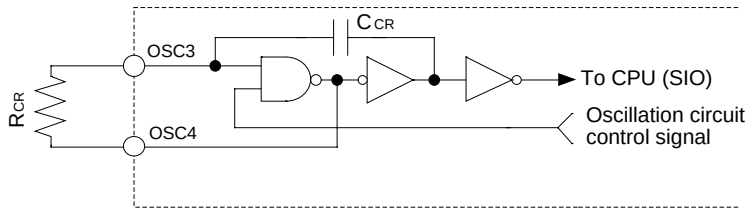
(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)
= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

– Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

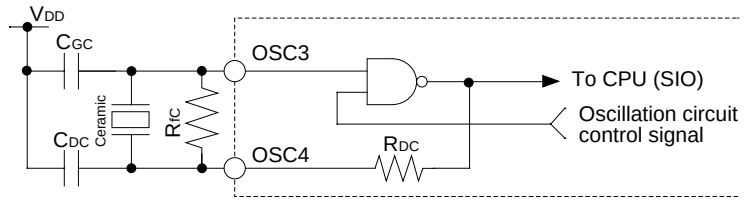
– In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option as OSC1, V_{S1} becomes -2.1 V even when VSC1 = VSC0 = 0 and will never become -1.2 V. In addition, since the current consumption is great for CR oscillation compared with the quartz crystal oscillation, when low power consumption is required, you should select quartz crystal oscillation as OSC1.

Example program for the oscillation circuit

Following program shows the oscillation clock controlling procedure.



(a) OSC3 CR oscillation circuit



(b) OSC3 ceramic oscillation circuit

Fig. 6.2.1 Configuration of OSC3 oscillation circuit

Table 6.2.3
Oscillation frequency and required operating voltage

Oscillation frequency	Oscillation circuit	Operating voltage V_{S1}
32.768 kHz	OSC1	-1.2 V or -2.1 V
1 MHz	OSC3	-2.1 V
2 MHz	OSC3	-3.0 V

Table 6.2.4
Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µs)		
	5-clock instruction	7-clock instruction	12-clock instruction
32.768 kHz	152.6	213.6	366.2
1 MHz	5.0	7.0	12.0
2 MHz	2.5	3.5	6.0

```
;*
;* OSCILLATION CLOCK CONTROL
;*
ZCLKCG    EQU    70H       ;OSC CONTROL REGISTER ADDRESS
XCLKH     EQU    1000B     ;CLOCK HIGH FREQ. SELECT
;
ZSVD      EQU    73H       ;SVD PORT ADDRESS
;
CLKLTH:
;* CHANGE CLOCK FREQ. FROM 32KHz TO 1MHz
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZSVD    ;CHECK VDD-VSS IS HIGHER THAN 3.3V
          LD     MX,0110B
          CALL   DLY100
          FAN    MX,1000B
          JP     NZ,RESIGN ;IF LOWER THAN 3.3V THEN RESIGN
;
          LD     X,ZCLKCG  ;SET VS1=-2.1V
          LD     MX,0001B
          CALL   DLY5MS    ;WAIT 5mS
;
          LD     MX,0111B  ;SET VS1=-3.0V & OSC3 ON
          CALL   DLY5MS    ;WAIT 5mS
;
```

```
          OR     MX,XCLKH  ;CHANGE CLOCK FROM 32KHz TO 1MHz
RESIGN:   RET
;
;
DLY100:    .               ;THE SUBROUTINE TO WAIT 100µS
           .
           .
          RET
;
;
DLY5MS:    .               ;THE SUBROUTINE TO WAIT 5mS
           .
           .
          RET
;
;
CLKHTL:
;* CHANGE CLOCK FREQ. FROM 1MHz TO 32KHz
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZCLKCG  ;CHANGE CLOCK FROM 1MHz TO 32KHz
          AND    MX,0111B
;
          LD     MX,0001B  ;SET VS1=-2.1V & OSC3 OFF
;
          LD     X,ZSVD    ;CHECK VSS & SETUP
          LD     MX,0110B  ;SUITABLE VS1 CONDITION
          CALL   DLY100
          LD     A,MX
          AND    A,1000B
          LD     MX,A
          JP     Z,ENDCLK
;
          CALL   DLY5MS    ;WAIT 5mS
;
          LD     MX,0000B  ;SET VS1=-1.2V
          RET
;
;
```

Programming notes

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) Before you use OSC1 as system clock, you should check the supply voltage (V_{SS}) using the SVD circuit.
If the SVD circuit detects supply voltage less than 3.1 V (V_{DD}–V_{SS} < 3.1 V) then set the operating voltage (V_{S1}) to -1.2 V. Or if the SVD circuit detects supply voltage 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V) then set V_{S1} to -2.1 V.
Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 6.2.2 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

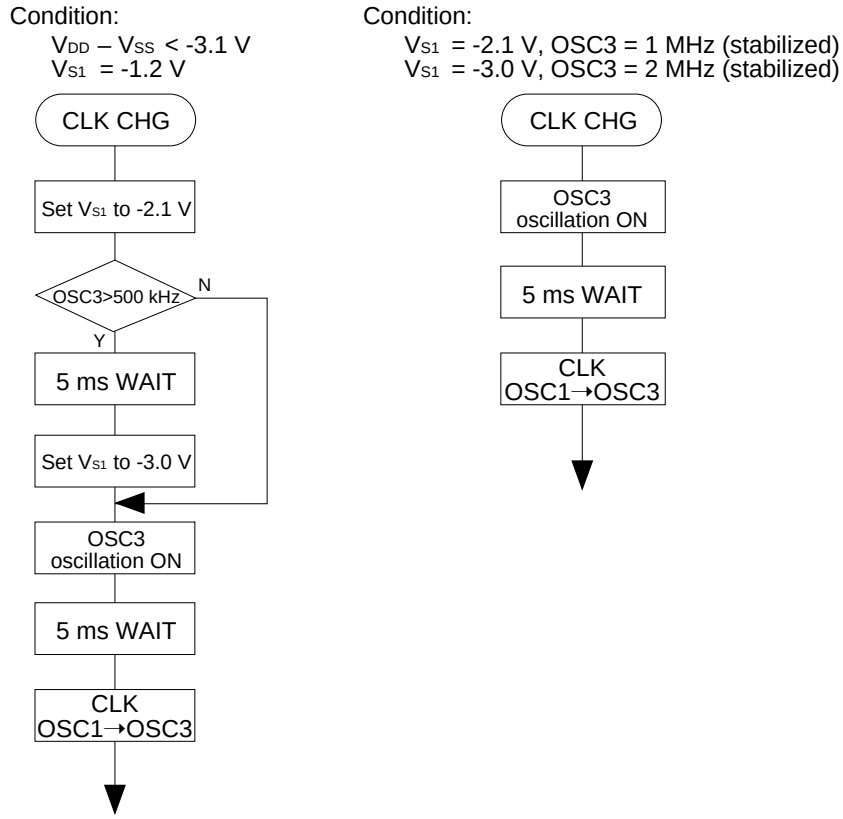


Fig. 6.2.2
CPU operating clock
control flow

6.3 Input Ports (Kxx)

I/O data memory of the input ports

The control registers of the input ports are shown in Tables 6.3.1(a) and (b).

Table 6.3.1(a) Control registers of input ports (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F04H	0	0	0	IK0	0	–			
	R				0	–			
					0	–			
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0	–			
	R				0	–			
					0	–			
					IK1	0	Yes	No	Interrupt factor flag (K10–K13)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
	R/W				EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
	R/W				EIK12	0	Enable	Mask	Interrupt mask register (K12)
					EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)

Table 6.3.1(b) Control registers of input ports (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F40H	K03	K02	K01	K00	K03	–	High	Low	Input port (K00–K03)
	R				K02	–	High	Low	
					K01	–	High	Low	
					K00	–	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
	R/W				DFK02	1	↓	↑	
					DFK01	1	↓	↑	
					DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	–	High	Low	Input port (K10–K13)
	R				K12	–	High	Low	
					K11	–	High	Low	
					K10	–	High	Low	

Example program for the input ports

Following program shows the input ports controlling procedure.

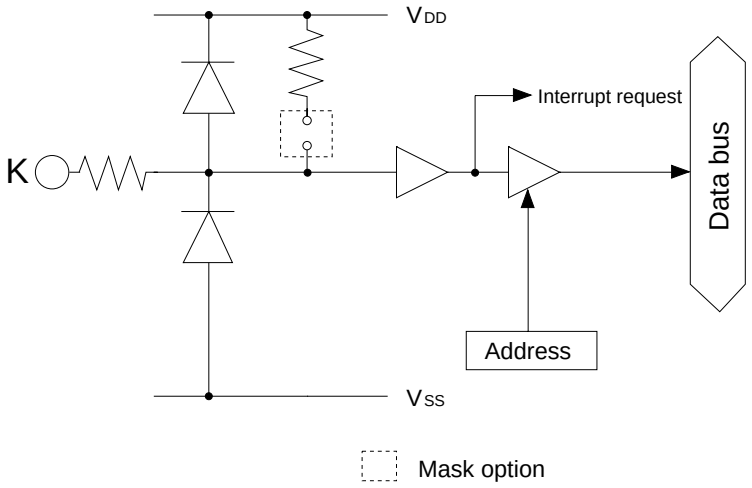


Fig. 6.3.1
Configuration of input port

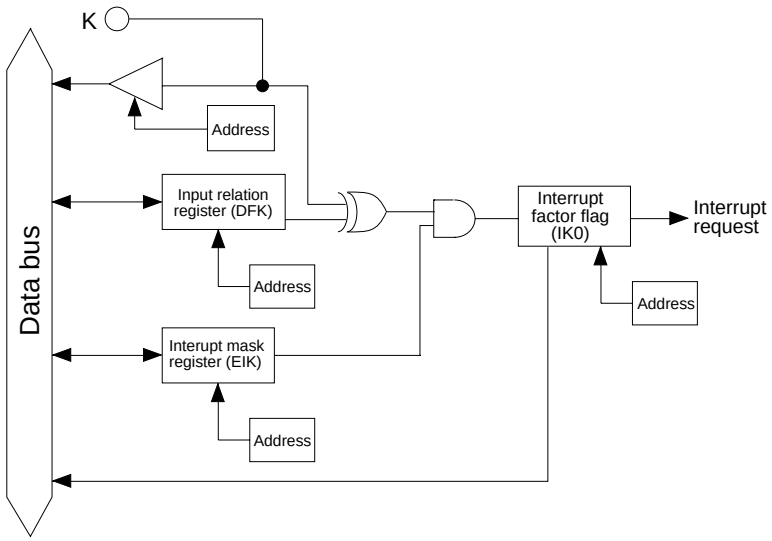


Fig. 6.3.2
Configuration of input (K00–K03) interrupt circuit

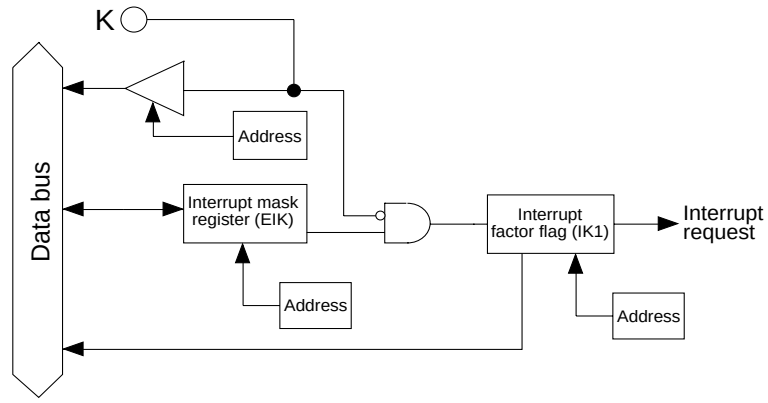


Fig. 6.3.3
Configuration of input (K10–K13) interrupt circuit

Interrupt mask register

EIK03	EIK02	EIK01	EIK00
1	1	1	0

Input relation register

DFK03	DFK02	DFK01	DFK00
1	0	1	0

With the above setting, the interrupt of K00–K03 is generated under the following condition:

Input ports

(1)

K03	K02	K01	K00
1	0	1	0

(Initial value)

↓

(2)

K03	K02	K01	K00
1	0	1	1

↓

(3)

K03	K02	K01	K00
0	0	1	1

→ Interrupt generation
Because K00 is masked, interrupt will be generated when no matching occurs between the contents of the 3 bits K01–K03 and the 3 bits input relation registers DFK01–DFK03.

↓

(4)

K03	K02	K01	K00
0	1	1	1

Fig. 6.3.4
Example of an interrupt for K00–K03

Interrupt mask register

EIK13	EIK12	EIK11	EIK10
0	1	1	1

With the above setting, the interrupt of K10–K13 is generated under the following condition:

Input ports

	K13	K12	K11	K10	
(1)	1	1	1	1	(Initial value)
	↓				
(2)	0	1	1	1	
	↓				
(3)	0	1	0	1	→ Interrupt generation
	↓				
(4)	0	1	0	0	

Because K13 is masked, interrupt will be generated when one or more terminals among the 3 bits K10–K12 become "0" from a state where all terminals were "1".

Fig. 6.3.5
Example of an interrupt for K10–K13

```
;*
;* INPUT PORT
;*
ZIK0   EQU    04H       ;INPUT PORT 0 INTERRUPT FLAG
ZIK1   EQU    05H       ;INPUT PORT 1 INTERRUPT FLAG
ZEIK0  EQU    14H       ;INPUT PORT 0 MASK REGISTER
ZEIK1  EQU    15H       ;INPUT PORT 1 MASK REGISTER
ZK0    EQU    40H       ;INPUT PORT 0 ADDRESS
ZDFK0  EQU    41H       ;INPUT PORT 0 INPUT RELATION
                         ;REGISTER ADDRESS
ZK1    EQU    42H       ;INPUT PORT 1 ADDRESS
;
K0INIT:
;* INPUT PORT 0 & 1 INITIAL ROUTINE
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     XP,A
;
       LD     X,ZK0     ;INITIALIZE FOR DFK0
```

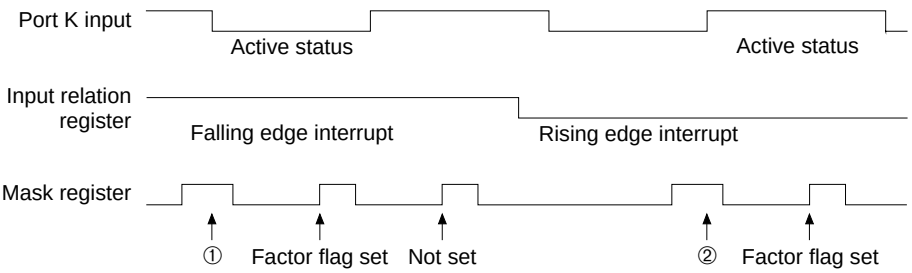
```
        LD      A,MX
        LD      Y,ZDFK0
        LD      MY,MX
;
        DI
        LD      X,ZEIK0
        LD      MX,0FH    ;ENABLE INPUT PORT 0 INTERRUPT
        LD      X,ZEIK1
        LD      MX,0FH    ;ENABLE INPUT PORT 1 INTERRUPT
        EI                ;ENABLE INTERRUPTS
        RET

K0INT:
;* K0 INTERRUPT SERVICE ROUTINE
;
        LD      X,ZIK0    ;CHECK INPUT PORT INTERRUPT FLAG
        DI
        LD      A,MX
        CP      A,00H     ;CHECK THE FLAG
        JP      Z,K0INT1  ;IF NO FLAG "ON" THEN JMP TO
                          ;K0INT1
        LD      X,ZK0
        LD      Y,ZDFK0   ;STORE TO INPUT RELATION REGISTER
        LD      MY,MX
        EI
;        .                ;DO THE SERVICE
;        .
;
;       DO THE PROCESS HERE
;
;        .
;        .

K0INT1:
        EI
        RET
;
;
K1INT:
;* K1 INTERRUPT SERVICE ROUTINE
;
```

```
        LD      X,ZIK1    ;CHECK INPUT PORT INTERRUPT FLAG
        DI
        LD      A,MX
        CP      A,00H
        JP      Z,K1INT1
        LD      X,ZK1     ;READ INPUT PORT 1 DATA
;        .
;        .
;
;       DO THE PROCESS HERE
;
;        .
;        .
K1INT1:
        EI
        RET
```

Programming notes

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

(2) Input interrupt programing related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 6.3.6
Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = Low status, when the falling edge interrupt is effected and

input terminal = High status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 6.3.6. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 6.3.6. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.

In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.4 Output Ports (Rxx)

I/O data memory of the output ports

The control registers of the output ports are shown in Tables 6.4.1(a) and (b).

Table 6.4.1(a) Control registers of output ports (1)

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F50H *2	R03	R02	R01	R00	R03	X	High	Low	Output port (R03)
							High	Low	External memory address (A3)
	R/W				R02	X	High	Low	Output port (R02)
							High	Low	External memory address (A2)
					R01	X	High	Low	Output port (R01)
							High	Low	External memory address (A1)
					R00	X	High	Low	Output port (R00)
							High	Low	External memory address (A0)
F51H *2	R13	R12	R11	R10	R13	X	High	Low	Output port (R13)
							High	Low	External memory address (A7)
	R/W				R12	X	High	Low	Output port (R12)
							High	Low	External memory address (A6)
					R11	X	High	Low	Output port (R11)
							High	Low	External memory address (A5)
					R10	X	High	Low	Output port (R10)
							High	Low	External memory address (A4)
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R23)
							High	Low	External memory address (A11) *1
	R/W				R22	X	High	Low	Output port (R22)
							High	Low	External memory address (A10) *1
					R21	X	High	Low	Output port (R21)
							High	Low	External memory address (A9) *1
					R20	X	High	Low	Output port (R20)
							High	Low	External memory address (A8) *1
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W								[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X	High	Low	Output port (R32)
									[External memory read ($\overline{\text{RD}}$)] *1
					R31	X	High	Low	Output port (R31)
							High	Low	External memory address (A13) *1
									[External memory write ($\overline{\text{WR}}$)] *1
					R30	X	High	Low	Output port (R30)
							High	Low	External memory address (A12) *1

Table 6.4.1(b) Control registers of output ports (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output ($\overline{BZ}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{FOUT}$)
							Off	On	LCD synchronous signal (CL)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
	R/W				HZR2	0	Output	High-Z	R20–R23 output high-impedance control
					HZR1	0	Output	High-Z	R10–R13 output high-impedance control *3
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control *3

*1 In the S1C62440, it can be used only as a port for output
*2 In the S1C62440, the F50H and F51H cannot be used
*3 In the S1C62440, it is a register that becomes invalid and during reading it is always "0"

Example program for the output ports

Following program shows the output ports controlling procedure in ordinary DC output case.

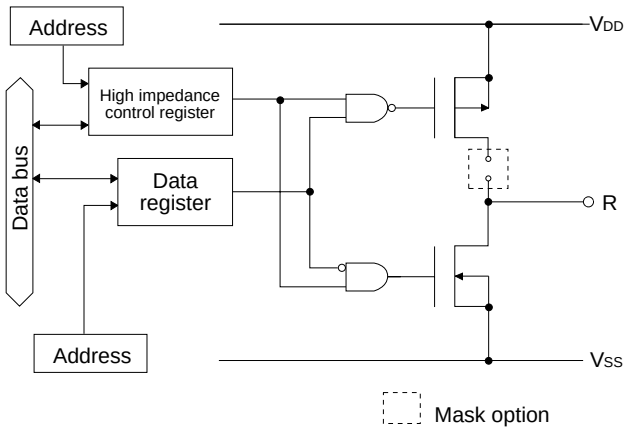


Fig. 6.4.1
Configuration of output port

```
;*
;* OUTPUT PORT
;*
;* LOADING DATA OF B REGISTER TO R20–R23
;
ZHZR   EQU    7BH       ;HIGH INPEDANCE CONTROL
                         ;REGISTER ADDRESS
ZR2    EQU    52H       ;OUTPUT PORT ADDRESS
XHZOFF EQU    0100B     ;HIGH IMPEDANCE OFF
                         ;(R2 PORT SET TO ACTIVE)
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     YP,A
;
       LD     Y,ZHZR    ;SET HIGH IMPEDANCE CONTROL
                         ;REGISTER ADDRESS
       LD     MY,XHZOFF ;ENABLE OUTPUT PORT
       LD     Y,ZR2     ;SET PORT ADDRESS
       LD     MY,B      ;OUTPUT B REG. TO R1 PORT
       RET
;
;
```

Programming notes

(1) When BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

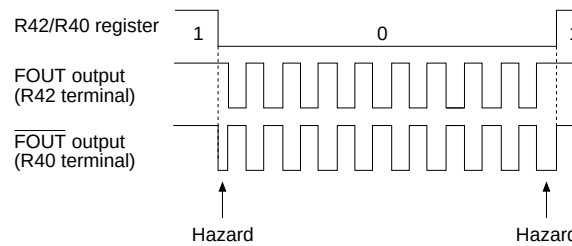


Fig. 6.4.2
Example of the hazard

6.5 I/O Ports (Pxx)

I/O data memory of the I/O ports

The control registers of the I/O ports are shown in Table 6.5.1.

Table 6.5.1 Control registers of I/O ports

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P03)
							High	Low	External memory data (D3) *1
	R/W				P02	X	High	Low	I/O port (P02)
							High	Low	External memory data (D2) *1
					P01	X	High	Low	I/O port (P01)
							High	Low	External memory data (D1) *1
					P00	X	High	Low	I/O port (P00)
							High	Low	External memory data (D0) *1
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P13)
							High	Low	External memory data (D7) *1
	R/W				P12	X	High	Low	I/O port (P12)
							High	Low	External memory data (D6) *1
					P11	X	High	Low	I/O port (P11)
							High	Low	External memory data (D5) *1
					P10	X	High	Low	I/O port (P10)
							High	Low	External memory data (D4) *1
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P23)
							High	Low	External memory chip select ($\overline{CS3}$) *1
	R/W W				P22	X	High	Low	I/O port (P22)
							High	Low	External memory chip select ($\overline{CS2}$) *1
					P21	X	High	Low	I/O port (P21)
							High	Low	External memory chip select ($\overline{CS1}$) *1
					P20	X	High	Low	I/O port (P20)
							High	Low	External memory chip select ($\overline{CS0}$) *1
F63H *2	P33	P32	P31	P30	P33	X	High	Low	I/O port (P33)
							High	Low	Dedicated output port (P33)
	R/W				P32	X	High	Low	I/O port (P32)
							High	Low	Dedicated output port (P32)
					P31	X	High	Low	I/O port (P31)
							High	Low	Dedicated output port (P31)
					P30	X	High	Low	I/O port (P30)
							High	Low	Dedicated output port (P30)
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33) *3
	R/W				IOC2	0	Output	Input	I/O control (P20–P23)
					IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33) *3
	R/W				PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
					PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 In the S1C62440, it can be used only as a port for I/O port
*2 In the S1C62440, the F63H cannot be used
*3 In the S1C62440, it is a register that becomes invalid and during reading it is always "0"

Example program for the I/O ports

Following program shows the I/O ports controlling procedure.
This program sets P00–P03, P20–P23, and P30–P33 as input port with pull up resistor and P10–P13 as output port.
Then it output the content of B register to P10–P13.
However, in the S1C62440 the P30–P33 settings are invalid.

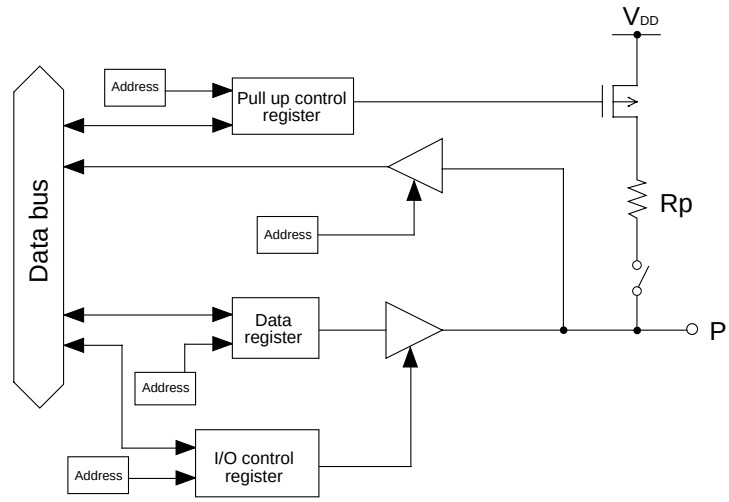


Fig. 6.5.1
Configuration of I/O port

```
;*
;* I/O PORT
;*
ZIOC    EQU     7DH       ;I/O CONTROL REGISTER
ZPUP    EQU     7EH       ;I/O PULL UP CONTROL REGISTER
ZP1     EQU     61H       ;P1 PORT ADDRESS
;
        LD      A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
        LD      XP,A
;
        LD      X,ZIOC    ;SET I/O PORT CONTROL ADDRESS
        LD      MX,0010B  ;SET I/O PORT 1 AS OUTPUT PORT
;
        LD      X,ZPUP    ;OFF THE PULL UP RESISTOR OF P1 PORT
        LD      MX,0010B
;       LD      X,ZP1     ;SET I/O PORT ADDRESS
        LD      MX,B      ;OUTPUT B REG. TO I/O PORT AS OUTPUT
        RET
;
;
```

Programming notes

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets any of the following 4 conditions, the reading data will be undefined:

- The input/output mode is set at output mode
- Output specification is set at Nch open drain
- The content of the data register is "1"
- The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

6.6 LCD Driver

I/O data memory of the LCD driver

The control registers of the LCD driver are shown in Table 6.6.1.

Table 6.6.1 Control registers of LCD driver

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
	R/W				ALON	0	All on	Normal	All LCD dots displayed control
					LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
	R/W				LC2	X			
					LC1	X			
					LC0	X			

Segment data memory

The segment data memory of S1C62440/4A0 is allocated to the built-in RAM addresses E00H–E4FH and E80H–ECFH, and S1C624C0/480 is allocated to the built-in RAM addresses E00H–E65H and E80H–EF5H.
Figures 6.6.1(a) and (b) show the correspondence between the segment data memory and the LCD dot matrix.

S1C62440/4A0

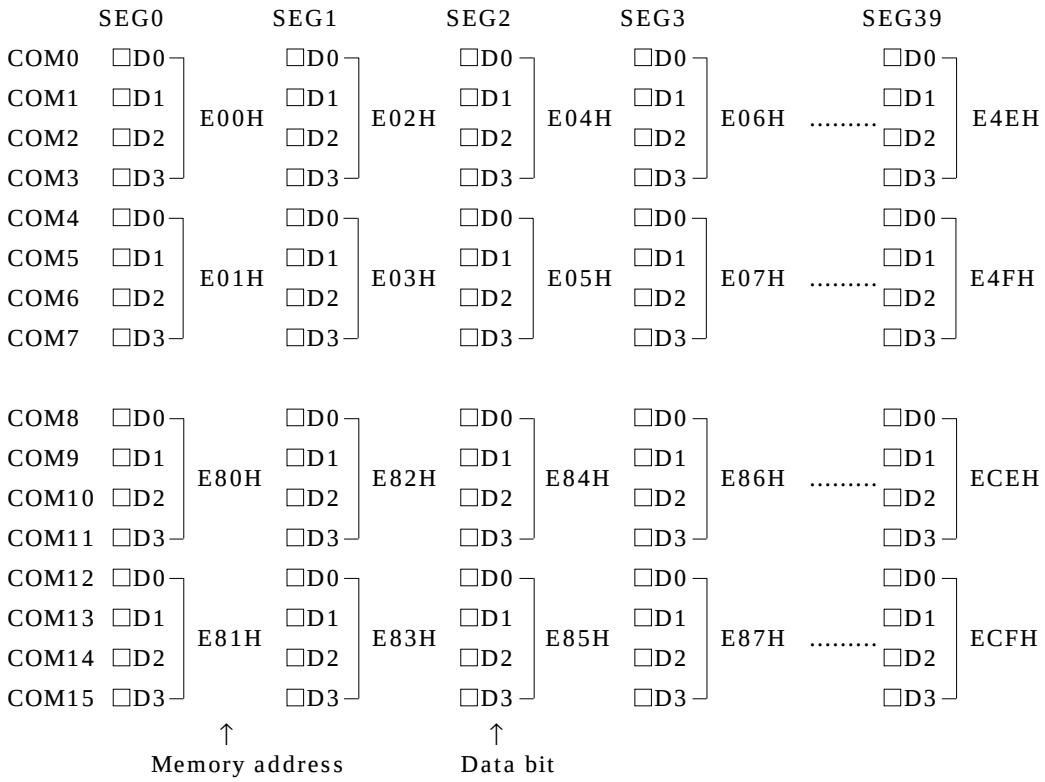


Fig. 6.6.1(a)
LCD dot matrix and segment data memory correspondence (S1C62440/4A0)

S1C624C0/480

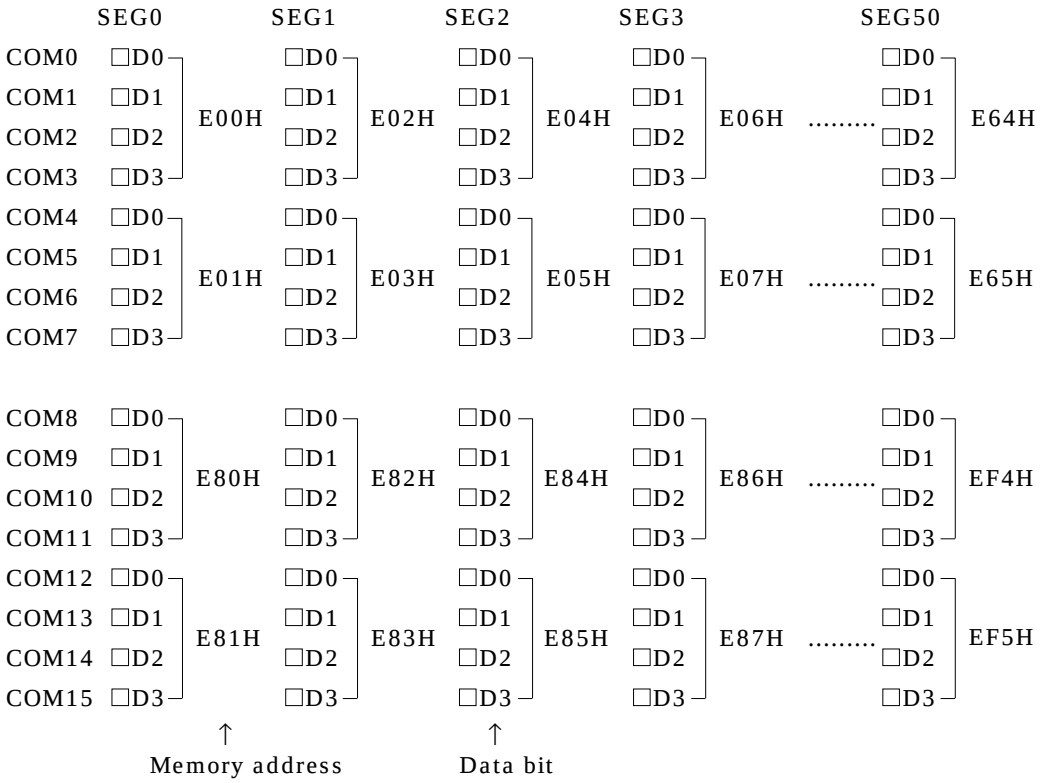


Fig. 6.6.1(b)
LCD dot matrix and segment data memory correspondence (S1C624C0/480)

Example program for the LCD driver

Following program shows the LCD driver controlling procedure.

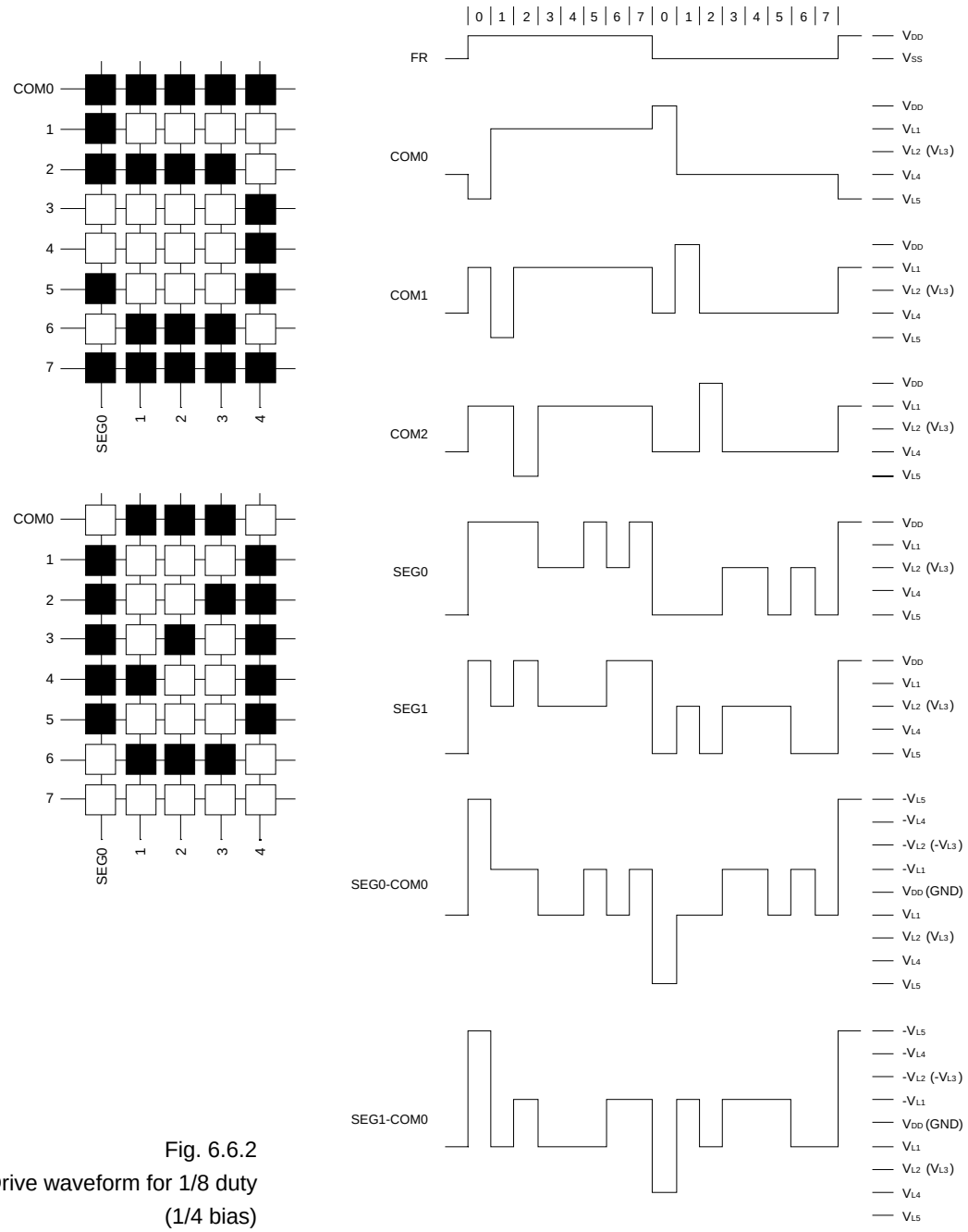


Fig. 6.6.2
Drive waveform for 1/8 duty
(1/4 bias)

```
;*
;* LCD DRIVER
;*
ZLDUTY    EQU    71H
ZLC       EQU    72H
XALON     EQU    0100B
XALOFF    EQU    1000B
;
YCOLUM    EQU    0250H
XCURSOR   EQU    01H
XNCURSR   EQU    00H
;
TSTLCD:
;* TESTING FOR LCD PANEL
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZLC     ;SET THE CONTRAST OF LCD
          LD     MX,8
;
          LD     A,00H
TSTLD1:
          LD     X,ZLDUTY
          AND    MX,0011B
          OR     MX,XALON  ;TURN ON
          CALL   WAITHS    ;WAIT 0.5 SEC
          AND    MX,0011B
          OR     MX,XALOFF ;TURN OFF
          CALL   WAITHS    ;WAIT 0.5 SEC
;
          ADD    A,1
          JP     NC,TSTLD1
;
;* TESTING THE TOLERANCE OF FRAME FREQUENCY
;
          AND    MX,0011B
          OR     MX,XALON  ;TURN ON & CONTINUE 5 SEC
          CALL   WAIT5S    ;WAIT 5 SEC
          AND    MX,0011B  ;TURN OFF AND SET LCD
                           ; TO NORMAL DRIVING CONDITION
;
```

```
NUMLCD:
;* DISPLAY NUMERAL ON THE LCD PANEL
;
          LD      X,ZLDUTY
          OR      MX,0010B  ;SELECT 1/8 DUTY
;
          LD      A,0EH     ;SET XP TO THE PAGE OF SEG. DATA
          LD      XP,A      ;MEMORY
;
          LD      A,02H     ;SET Y REG. TO COLUMN INDEX MEMORY
          LD      YP,A
          LD      Y,YCOLUM
          LD      MY,1      ;SELECT 1ST COLUMN
          LD      A,5       ;DISPLAY "5"
          LD      B,XCURSOR ;WITH CURSOR
          CALL    DSPLCD
;
          LD      MY,2      ;SELECT 2ND COLUMN
          LD      A,0       ;DISPLAY "0"
          LD      B,XNCURSR ;WITHOUT CURSOR
;
;          .
;          .
;         CONTINUE
;          .
;          .
;
WAITHS:    .                ;WAIT 0.5 SEC
           .
          RET
;
WAIT5S:    .                ;WAIT 5 SEC
           .
          RET
;
DSPLCD:
;* DISPLAY ONE NUMERAL
;
          LD      X,00H     ;SET UP THE COLUMN
DSPLCD1:
          ADD     MY,0FH
          CP      MY,0
```

```
          JP     Z,DSPLCD2
;
          RCF              ;SHIFT THE COLUMN
          ADC    XL,0AH
          ADC    XH,00H
          JP     DSPLCD1
;
DSPLCD2:
          PSET   0FH
          JPBA
;
;
          ORG    0F00H
;
NUM0:
          LBPX   MX,3EH    ;DISPLAY PATARN FOR "0" WITHOUT
          LBPX   MX,51H    ;CURSOR
          LBPX   MX,49H
          LBPX   MX,45H
          RETD   3EH
;
           .
           .
           .
;
          ORG    0F15H
;
NUM5C:
          LBPX   MX,0A7H   ;DISPLAY PATARN FOR "5" WITH
          LBPX   MX,0C5H   ;CURSOR
          LBPX   MX,0C5H
          LBPX   MX,0C5H
          RETD   0B9H
           .
           .
           .
```

Programming note

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

6.7 Clock Timer

I/O data memory of the clock timer

The control registers of the clock timer are shown in Table 6.7.1.

Table 6.7.1 Control registers of clock timer

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F00H	IT1	IT2	IT8	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
	R				IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
					IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
	R/W				EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
					EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
	R				TM2	0			Clock timer data (32 Hz)
					TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
	R				TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F76H	0	0	TMRST	WDRST	0	–			
	R		W		0	–			
					TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

Example program for the clock timer

Following program shows the clock timer controlling procedure.

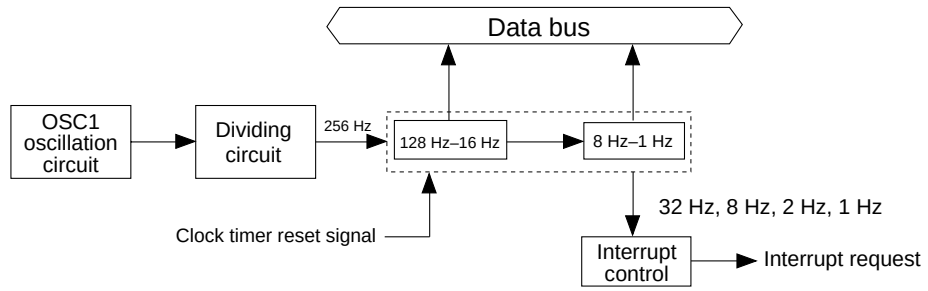


Fig. 6.7.1 Configuration of clock timer

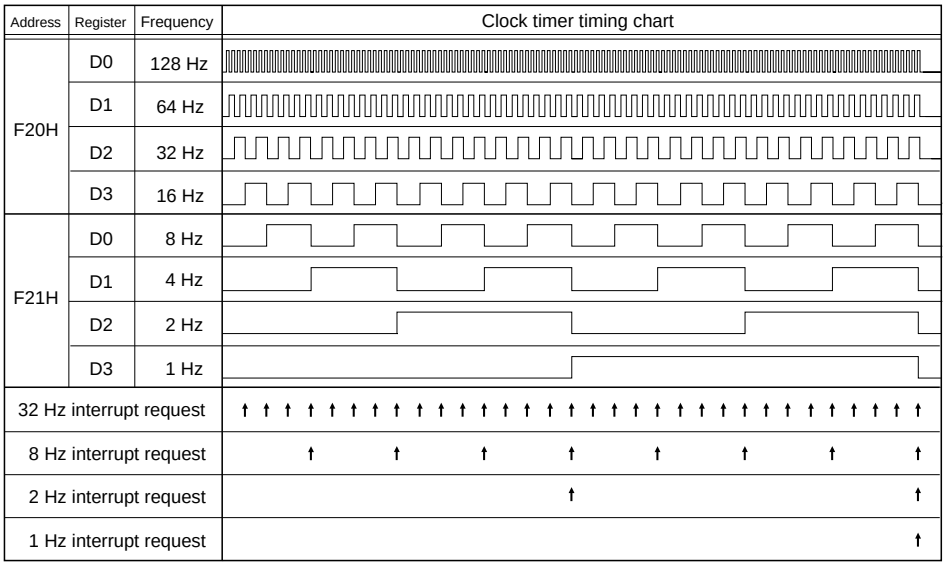


Fig. 6.7.2 Timing chart of clock timer

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT8, IT2, and IT1) is set to "1".

Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT8, EIT2, and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

```
;*
;* CLOCK TIMER
;*
ZTMRST    EQU    76H       ;RESET THE CLOCK TIMER
ZTML      EQU    20H       ;LOWER NIBBLE OF TIMER DATA
ZTMH      EQU    21H       ;HIGHER NIBBLE OF TIMER DATA
ZEIT      EQU    10H       ;TIMER INTERRUPT MASK REGISTER
ZIT       EQU    00H       ;TIMER INTERRUPT FLAG REGISTER
XTMRST    EQU    0010B
XWDRST    EQU    0001B
;
TMINIT:
;* ENABLE INTERRUPT FOR CLOCK TIMER AND RESET IT
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZTMRST  ;RESET TIMER
          OR     MX,XTMRST
          OR     MX,XWDRST ;RESET WATCHDOG TIMER
;
          DI
          LD     X,ZIT     ;RESET IT FLAGS
          LD     MX,MX
;
          LD     X,ZEIT    ;SET TO TIMER MASK REGISTER
          LD     MX,0001B  ;ENABLE TIMER 1Hz INTERRUPT
          EI
          RET

TMINT:
;* CLOCK TIMER INTERRUPT SERVICE ROUTINE
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
          LD     YP,A
;
          DI
          LD     X,ZIT     ;LOAD TIMER INTERRUPT FLAG REGISTER
          LD     A,MX
          FAN    A,1000B   ;CHECK TIMER 1Hz
          JP     Z,TMINT1  ;IF NO FLAG "ON" THEN JUMP TO TMINT1
          PUSH   A         ;SAVE THE INTERRUPT FLAG TO STACK
          LD     X,ZTMH    ;SET TO HIGHER NIBBLE OF THE TIMER
                           ;DATA REGISTER
```

```
TMINT2:   LD      A,MX      ;READ HIGHER NIBBLE OF THE TIMER DATA
          LD      Y,ZTML    ;READ LOWER NIBBLE OF THE TIMER DATA
          LD      B,MY
          CP      MX,A      ;READ HIGHER NIBBLE AGAIN
                            ;AND COMPARE WITH LAST CONTENT
          JP      NZ,TMINT2
;
          POP     A
;           .
;           .
;         DO THE PROCEDURE FOR 1Hz
;           .
;           .
TMINT1:   EI
          RET
```

Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.8 Stopwatch Timer

I/O data memory of the stopwatch timer

The control registers of the stopwatch timer are shown in Table 6.8.1.

Table 6.8.1 Control registers of stopwatch timer

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F01H	0	0	ISW1	ISW0	0	–			
	R				0	–			
					ISW1	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F11H	0	0	EISW1	EISW0	0	–			
	R		R/W		0	–			
					EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
	R				SWL2	0			Stopwatch timer 1/100 sec data (BCD)
					SWL1	0			
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
	R				SWH2	0			Stopwatch timer 1/10 sec data (BCD)
					SWH1	0			
					SWH0	0			LSB
F77H	0	0	SWRST	SWRUN	0	–			
	R		W	R/W	0	–			
					SWRST	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

Example program for the stopwatch timer

Following program shows the stopwatch timer controlling procedure.

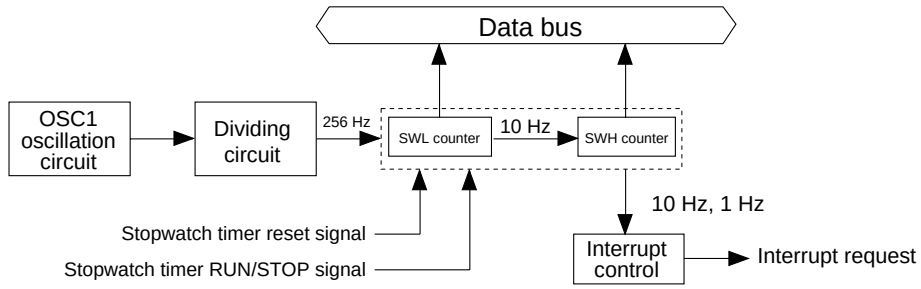


Fig. 6.8.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

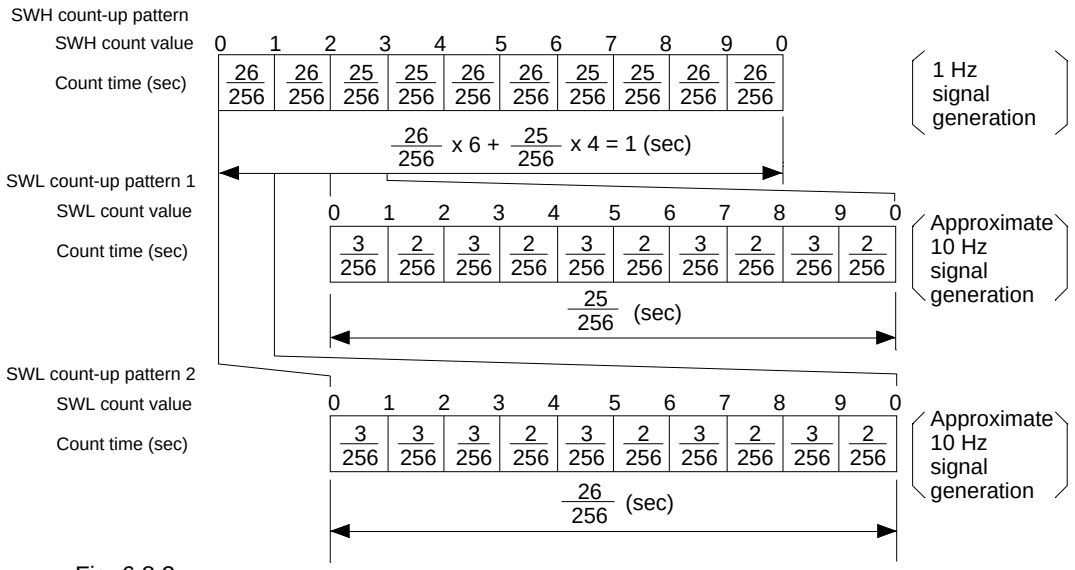


Fig. 6.8.2 Count-up pattern of stopwatch timer

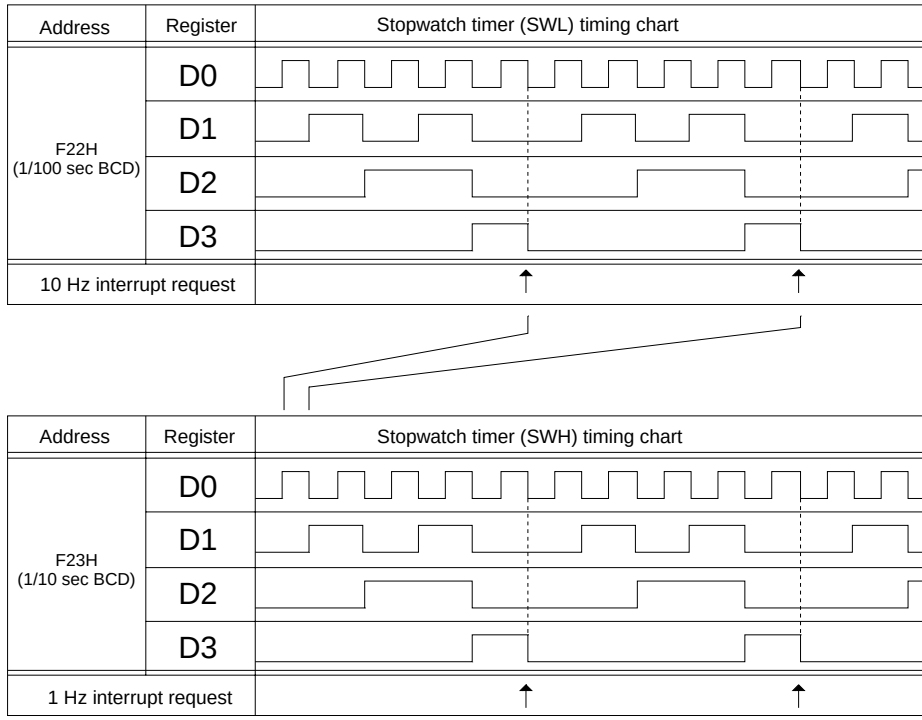


Fig. 6.8.3
Timing chart for
stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWL and SWH (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW0 and ISW1) are set to "1".
The respective interrupts can be masked separately through the interrupt mask registers (EISW0 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

```
;*
;* STOPWATCH TIMER
;*
ZSWRST    EQU    77H
ZSWRUN    EQU    77H
ZSWL      EQU    22H
ZSWH      EQU    23H
ZEISW     EQU    11H
ZISW      EQU    01H
;
;
SWINIT:
;* ENABLE INTERRUPT FOR STOPWATCH TIMER AND START IT.
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          DI
          LD     X,ZEISW
          LD     MX,0011B  ;ENABLE STOPWATCH INTERRUPT
;
          LD     X,ZSWRST
          LD     MX,0010B  ;RESET STOPWATCH TIMER
;
          OR     MX,0001B  ;START STOPWATCH TIMER
          EI
          RET
;
;
;
SWINT:
;* STOPWATCH INTERRUPT SERVICE ROUTINE
;
          LD     X,ZISW    ;CHECK STOPWATCH INTERRUPT
          DI
          LD     A,MX
          CP     A,00H     ;CHECK THE FLAG
          JP     Z,SWINT1  ;IF NO FLAG "ON" THEN JUMP TO SWINT1
;
          PUSH   A
          LD     B,0FH
          LD     YP,B
          LD     Y,ZSWL
          LD     X,ZSWRUN
```

```
            AND     MX,1110B  ;STOP STOPWATCH TIMER
            LDPY    A,MY      ;READ SWL DATA TO "A" REG.
            LD      B,MY      ;READ SWH DATA TO "B" REG.
            OR      MX,0001B  ;START STOPWATCH TIMER
             .
             .
            DO THE PROCEDURE FOR STOPWATCH
             .
             .
SWINT1:     EI
            RET
```

Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

(2) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.9 Programmable Timer

I/O data memory of the programmable timer

The control registers of the programmable timer are shown in Tables 6.9.1(a) and (b).

Table 6.9.1(a) Control registers of programmable timer (1)

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F02H	0	0	0	IPT	0	–			
	R				0	–			
					0	–			
					IPT	0	Yes	No	Interrupt factor flag (programmable timer)
F12H	0	0	0	EIPT	0	–			
	R			R/W	0	–			
					0	–			
					EIPT	0	Enable	Mask	Interrupt mask register (programmable timer)
F24H	PT3	PT2	PT1	PT0	PT3	X			MSB
	R				PT2	X			Programmable timer data (low-order)
					PT1	X			
					PT0	X			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X			MSB
	R				PT6	X			Programmable timer data (high-order)
					PT5	X			
					PT4	X			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X			MSB
	R/W				RD2	X			Programmable timer reload data (low-order)
					RD1	X			
					RD0	X			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X			MSB
	R/W				RD6	X			Programmable timer reload data (high-order)
					RD5	X			
					RD4	X			LSB

Table 6.9.1(b) Control registers of programmable timer (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F78H	0	0	PTRST	PTRUN	0	–			
	R		W	R/W	0	–			
					PTRST	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0			Programmable timer clock output
	R/W				PTC2	0			Programmable timer input clock selection
					PTC1	0			
					PTC0	0			

The PTC0–PTC2 setting and input clock correspondence is shown in Table 6.9.2.

Table 6.9.2 Input clock setting

PTC2	PTC1	PTC0	Input clock
0	0	0	K03 input (with noise rejector)
0	0	1	K03 input (direct)
0	1	0	256 Hz
0	1	1	512 Hz
1	0	0	1,024 Hz
1	0	1	2,048 Hz
1	1	0	4,096 Hz
1	1	1	8,192 Hz

Example program for the programmable timer

Following program shows the programmable timer controlling procedure.

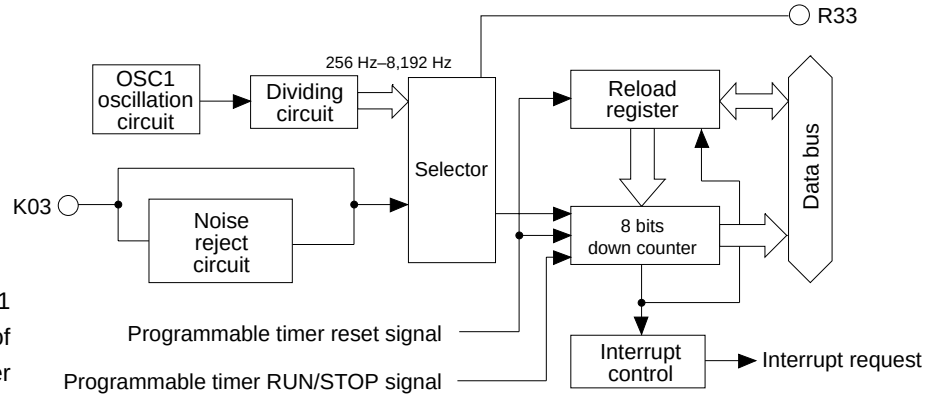


Fig. 6.9.1 Configuration of programmable timer

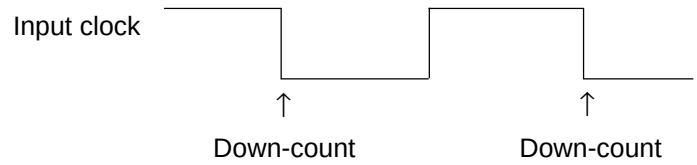


Fig. 6.9.2 Timing of down-counts

External clock of K03 input (with noise rejector) is for counting by key entry, the input signal from which passes the 256 Hz sampling noise reject circuit. With this, no more than 2 ms of chattering is purged, and at least 4 ms signal is received.

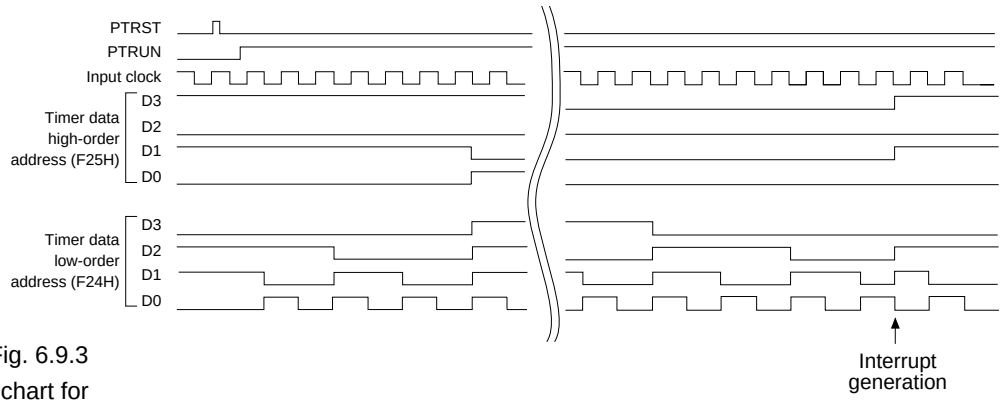


Fig. 6.9.3 Timing chart for programmable timer

Note: When "A6H" is set into reload register

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

```
;*
;* PROGRAMMABLE TIMER
;*
ZPTRST    EQU    78H
ZPTRUN    EQU    78H
ZPTCOU    EQU    79H
ZRDL      EQU    26H
ZRDH      EQU    27H
ZPTL      EQU    24H
ZPTH      EQU    25H
ZEIPT     EQU    12H
ZIPT      EQU    02H
;
;
PTINIT:
;* ENABLE INTERRUPT FOR PROGRAMMABLE TIMER,
;  PRESET AND START IT.
;
          LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          DI
          LD     X,ZEIPT   ;ENABLE PROGRAMMABLE TIMER INTERRUPT
          LD     MX,0001B
;
          LD     X,ZRDL    ;PRESET THE RELOAD REG TO 100.
          LDPX   MX,04H
          LD     MX,06H
;
          LD     X,ZPTCOU  ;SELECT K03 AS CLOCK
          LD     MX,0001B
;
          LD     X,ZPTRST
          OR     MX,0010B  ;RESET PROGRAMMABLE TIMER
```

```
          OR     MX,0001B  ;START PROGRAMMABLE TIMER
          EI
          RET
;
PTINT:
;* PROGRAMMABLE TIMER INTERRUPT SERVICE ROUTINE
;
          LD     A,0FH
          LD     XP,A
;
          LD     X,ZIPT    ;CHECK PROGRAMMABLE TIMER INTERRUPT
          DI
          LD     A,MX
          FAN    A,0001B   ;CHECK THE FLAG
          JP     Z,PTINT1  ;IF NO FLAG "ON" THEN JUMP TO PRINT1
           .
           .
;         DO THE PROCEDURE FOR PROGRAMMABLE TIMER
           .
           .
PTINT1:   EI
          RET
;
;
PTREAD:
;* READ PROGRAMMABLE TIMER ROUTINE
;
          LD     A,0FH
          LD     XP,A
;
          CALL   HSPCLK    ;CHANGE TO HIGH SPEED OSC CLOCK WHEN
                           ;INPUT CLOCK OF PROGRAMMABLE TIMER IS
                           ;HIGHER FREQUENCY THAN 280Hz
;
          LD     X,ZPTRUN  ;STOP PROGRAMMABLE TIMER
          AND    MX,1110B
;
          LD     X,ZRDL
          LDPX   A,MX
          LD     B,MX
;
          LD     X,ZPTRUN  ;START PROGRAMMABLE TIMER
          OR     MX,0001B
```

```
          RET
;
HSPCLK:                    ;THE SUBROUTINE TO CHANGE TO HIGH
                           ;SPEED OSC CLOCK
           .
           .
           .
          RET
;
;
```

Programming notes

(1) When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than a 256 Hz, high speed processing by OSC3 is required.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.10 SVD (Supply Voltage Detection) Circuit

I/O data memory of the SVD circuit

The control registers of the SVD circuit are shown in Table 6.10.1.

Table 6.10.1 Control registers of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1	Low	Normal	SVD evaluation data
	R	R/W			SVDON	0	On	Off	SVD circuit On/Off
					SVC1	X			SVD criteria voltage setting
					SVC0	X			

Criteria voltage for supply voltage detection is set as shown in Table 6.10.2.

Table 6.10.2
Criteria voltage for SVD circuit

SVC1	SVC0	Criteria voltage
0	0	-2.2 V
0	1	-2.5 V
1	0	-3.1 V
1	1	-4.2 V

The V_{DD} reference voltage is used as the criteria voltage.
At initial reset, this register becomes undefined.

Example program for the SVD circuit

Following program shows the SVD controlling procedure.

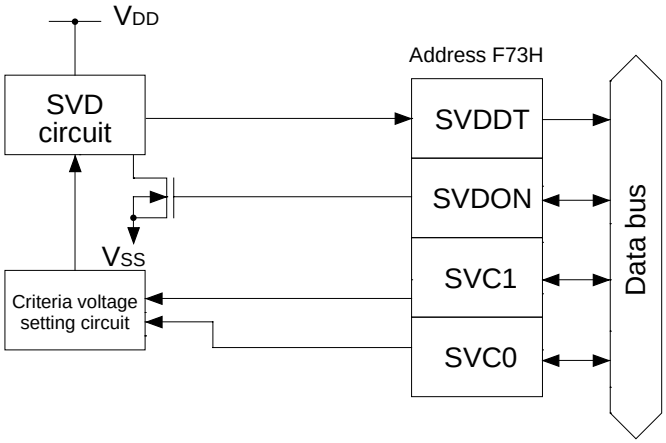


Fig. 6.10.1
Configuration of SVD circuit

```
;*
;* CHECK THE RESULT OF SUPPLY VOLTAGE DETECTION CIRCUIT
;*
ZSVD      EQU     73H         ;SVD PORT ADDRESS
XSVDON    EQU     01XXB       ;SVD ENABLE BIT & DETECT VOLTAGE
                              ;"XX" SHOULD BE DEFINED DUE TO
                              ;THE DETECT VOLTAGE
;
CHKSVD:   LD      A,0FH       ;SET TO I/O DATA MEMORY ADDRESS
          LD      XP,A
;
          LD      X,ZSVD
          LD      MX,XSVDON   ;TURN ON SVD CIRCUIT & SET DETECT
                              ;VOLTAGE
          CALL    DLY100      ;*1: WAIT FOR 100µS TO BE STABLE
                              ;SVD CIRCUIT
          LD      A,MX        ;READ SVD DATA
          AND     A,1000B     ;MASK OF SVD DATA & THE RESULT IS
                              ;STORED IN "A"
                              ;"1" MEANS BATTERY BECOME LOW
          LD      MX,A        ;*2: TURN OFF SVD CIRCUIT TO REDUCE
                              ;CURRENT CONSUMPTION
          RET
;
DLY100:                       ;THE SUBROUTINE TO WAIT 100µS
;           .
;           .
          RET
;
```

Programming notes

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

6.11 Heavy Load Protection Circuit

I/O data memory of the heavy load protection circuit

The control register of the heavy load protection circuit is shown in Table 6.11.1.

Table 6.11.1 Control register of heavy load protection circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
	R/W				ALON	0	All on	Normal	All LCD dots displayed control
					LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode

Example program for the heavy load protection circuit

Following program shows the heavy load protection circuit controlling procedure.

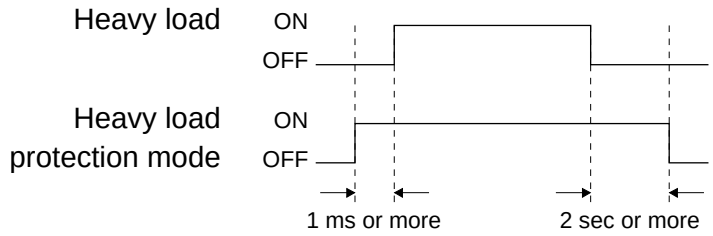


Fig. 6.11.1
Control timing for
heavy load protection mode

```
;*
;* ENABLE HEAVY LOAD PROTECTION MODE
;*
ZHLMOD    EQU    71H       ;HLMOD REGISTER ADDRESS
XHLON     EQU    0001B     ;HLMOD ENABLE BIT
;
ENHLP:    LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZHLMOD  ;SET HLMOD REGISTER ADDRESS
          OR     MX,XHLON  ;SET HLMOD TURN ON
          NOP5             ;*1: WAIT MORE THAN 4 STEPS TO BE
          NOP5             ;STABLE HLMOD CIRCUIT BEFORE TURN
          NOP5             ;ON THE HEAVY LOAD
          NOP5
          RET
;
;*
;* DISABLE HEAVY LOAD PROTECTION MODE DUE TO SVD
;*
ZHLMOD    EQU    71H       ;HLMOD REGISTER ADDRESS
XHLOFF    EQU    1110B     ;HLMOD DISABLE BIT
;
DISHLP:   CALL   SVD22     ;CHECK VDD-VSS IS LOWER THAN 2.2V
;
          AND    A,1000B   ;"1" MEANS BATTERY LOW
          JP     Z,TOFF
          RET              ;*2: RETURN WITHOUT HLMOD TURN OFF
                           ;WHEN BATTERY IS LOWER THAN 2.2V
;
;
TOFF:     LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
          LD     XP,A
;
          LD     X,ZHLMOD  ;SET HLMOD REGISTER ADDRESS
          AND    MX,XHLOFF ;*3: SET HLMOD TURN OFF TO REDUCE
                           ;THE CURRENT CONSUMPTION
          RET
;
SVD23:                     ;THE SUBROUTINE WHICH CHECKS
           .               ;WHETHER BLD SENCE LOWER THAN 2.2V
           .               ;OR NOT
          RET
;
```

Programming notes

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 6.11.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 6.11.1.)

6.12 Serial Interface Circuit

I/O data memory of the serial interface circuit

The control registers of the serial interface circuit are shown in Table 6.12.1.

Table 6.12.1 Control registers of serial interface circuit

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F03H	0	0	0	ISIO	0	–			
	R				0	–			
					0	–			
					ISIO	0	Yes	No	Interrupt factor flag (serial interface)
F13H	0	0	0	EISIO	0	–			
	R			R/W	0	–			
					0	–			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F30H	SD3	SD2	SD1	SD0	SD3	X			MSB
	R/W				SD2	X			Serial interface data register (low-order)
					SD1	X			
					SD0	X			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X			MSB
	R/W				SD6	X			Serial interface data register (high-order)
					SD5	X			
					SD4	X			LSB
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG	–	Trigger		Serial interface clock trigger
	W	R/W			SEN	0			Serial interface clock edge selection
					SCS1	0			Serial interface clock mode selection
					SCS0	0			

Table 6.12.2
Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

Synchronous clock ($\overline{SCLK}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

Example program for the serial interface circuit

Following program shows the serial interface controlling procedure.

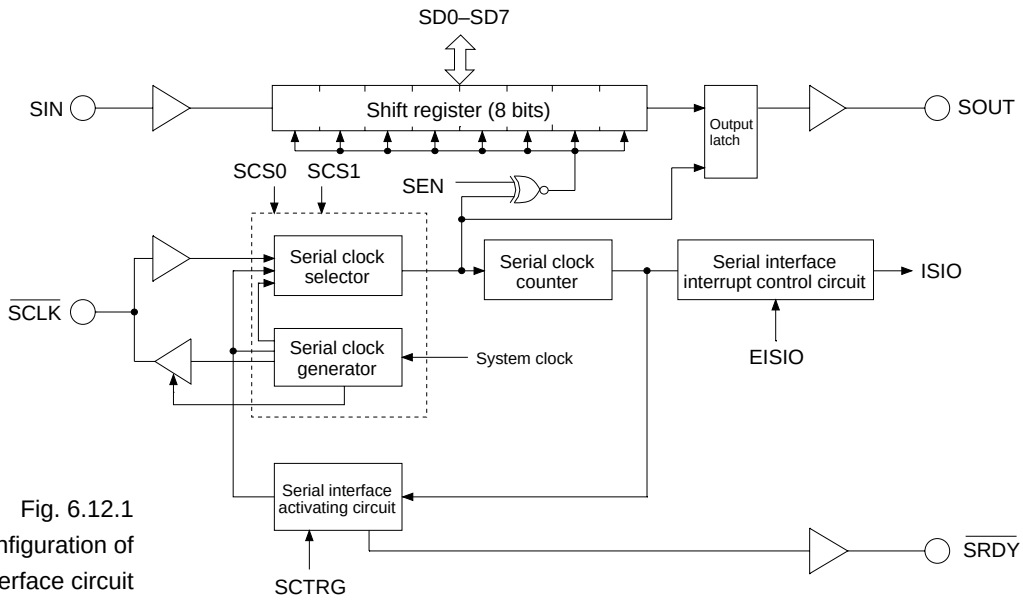


Fig. 6.12.1
Configuration of serial interface circuit

Table 6.12.3
Synchronous clock selection

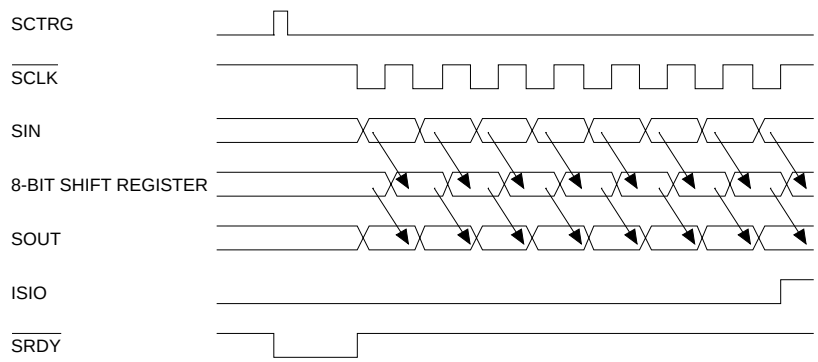
SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK / 2
0	1		CLK / 4
0	0	Slave mode	External clock

CLK : CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input /output of the 8 bits serial data, is controlled as follows:

– At master mode, after output of 8 clocks from the $\overline{SCLK}$ terminal, clock output is automatically suspended and $\overline{SCLK}$ terminal is fixed at high level.

– At slave mode, after input of 8 clocks to the $\overline{SCLK}$ terminal, subsequent clock inputs are masked.



Timing chart, SEN = "0"

Fig. 6.12.2
Serial interface timing chart

```
;*
;* SERIAL INTERFACE
;*
ZSCTRG EQU    7AH
ZISIO  EQU    03H
ZEISIO EQU    13H
ZSD03  EQU    30H
ZSD47  EQU    31H
ZSRDY  EQU    53H
;
YSIO03 EQU    00H       ;DATA BUFFER FOR SD03
YSIO04 EQU    01H       ;DATA BUFFER FOR SD47
;
ZPRDY  EQU    42H       ;K10 PORT EQU READY
ZPREQ  EQU    51H       ;R10 PORT EQU REQUEST
;
;OUTSIO:
;* OUTPUT DATA TO SERIAL INTERFACE
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     XP,A
;
       LD     X,ZSD03   ;RESET SERIAL INTERFACE CIRCUIT
       LDPX   A,MX
       LD     A,MX
;
       LD     X,ZSCTRG  ;SELECT CLK/4 RISE EDGE TIMING
       LD     MX,0001B  ;& MASTER MODE
;
       DI               ;PREPARE FOR INTERRUPT
       LD     X,ZISIO
       LD     A,MX
       LD     X,ZEISIO  ;ENABLE SERIAL INTERFACE INTERRUPT
       LD     MX,1
       EI
;
       LD     A,02H     ;SET UP DATA
       LD     YP,A
       LD     Y,YSIO03
       LD     X,ZSD03
       LDPY   A,MY
       LDPX   MX,A
       LD     A,MY
       LD     MX,A
;
       LD     X,ZSCTRG  ;START SERIAL INTERFACE
```

```
        OR      MX,1000B
;
         :
;
READSIO:
;* INPUT DATA FROM SERIAL INTERFACE
;
        LD      A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
        LD      XP,A
;
        LD      X,ZPREQ   ;SEND REQUEST SIGNAL
        OR      MX,0001B  ;TO SLAVE SYSTEM
;
        LD      X,ZSD03   ;RESET SERIAL INTERFACE CIRCUIT
        LDPX    A,MX
        LD      A,MX
;
        LD      X,ZCTRG   ;SELECT CLK/4 RISE EDGE
        LD      MX,0001B  ;TIMING & MASTER MODE
;
        DI                ;PREPARE FOR INTERRUPT
        LD      X,ZISIO
        LD      A,MX
        LD      X,ZEISIO  ;ENABLE SERIAL INTERFACE INTERRUPT
        LD      MX,1
        EI
;
        LD      A,02H     ;SET UP DATA TO SERIAL INTERFACE
        LD      YP,A      ;DATA REGISTER
        LD      Y,YSIO03
        LD      X,ZSD03
        LDPX    A,MX
        LDPY    MY,A
        LD      A,MX
        LD      MY,A
;
        LD      X,ZPRDY   ;CHECK READY
PRDYLP:
        FAN     MX,0001B
        JP      Z,PRDYLP  ;IF NOT READY THEN WAIT
;
        LD      X,ZSCTRG  ;IF READY THEN SEND DATA
        OR      MX,1000B
;
         :
```

Programming notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.13 Sound Generator

I/O data memory of the sound generator

The control registers of the sound generator are shown in Table 6.13.1.

Table 6.13.1 Control registers of sound generator

Address	Register D3	D2	D1	D0	Name	SR	1	0	Comment
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output ($\overline{BZ}$)]
					R41	1	High	Low	Output port (R41)
							Off	On	LCD frame signal (FR)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{FOUT}$)
							Off	On	LCD synchronous signal (CL)
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
	R/W				BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger
							BUSY	READY	Status
	W / R	W	R/W		ENVRST	Reset	Reset	–	Envelope reset
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off

Table 6.13.2 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

At initial reset, 4,096 Hz is selected.

Example program for the sound generator

Following program shows the sound generator controlling procedure.

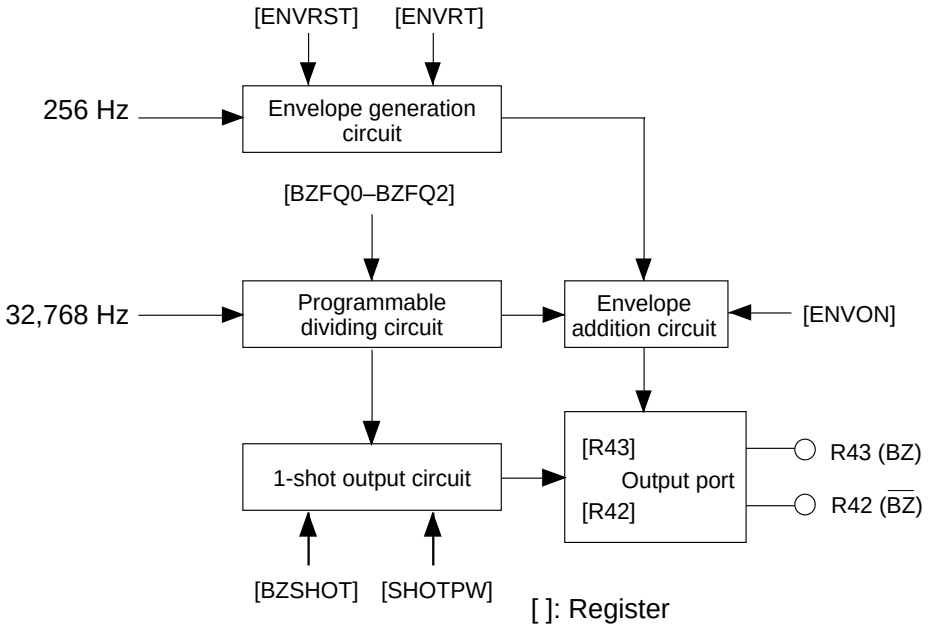


Fig. 6.13.1 Configuration of sound generator

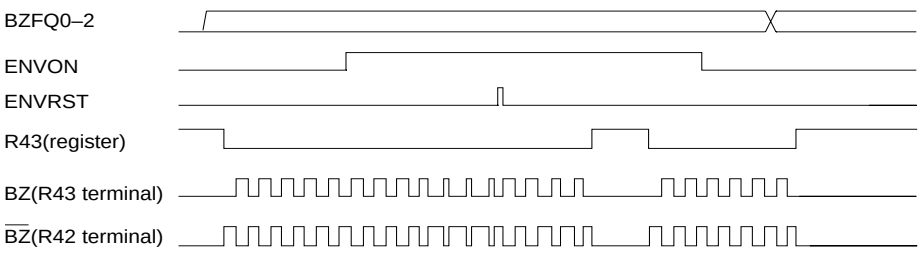


Fig. 6.13.2 Timing chart of sound generator

Table 6.13.3
Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

Note *A hazard may be observed in the output waveform of the BZ and $\overline{BZ}$ signals when switchs the buzzer frequency while the BZ and $\overline{BZ}$ signals being output.*

Table 6.13.4
Duty ratio and buzzer frequencies

Duty ratio	Buzzer frequencies			
	4,096.0	3,276.8	2,730.7	2,340.6
	2,048.0	1,638.4	1,365.3	1,170.3
Level 1 (maximum)	8/16	8/20	12/24	12/28
Level 2	7/16	7/20	11/24	11/28
Level 3	6/16	6/20	10/24	10/28
Level 4	5/16	5/20	9/24	9/28
Level 5	4/16	4/20	8/24	8/28
Level 6	3/16	3/20	7/24	7/28
Level 7	2/16	2/20	6/24	6/28
Level 8 (minimum)	1/16	1/20	5/24	5/28

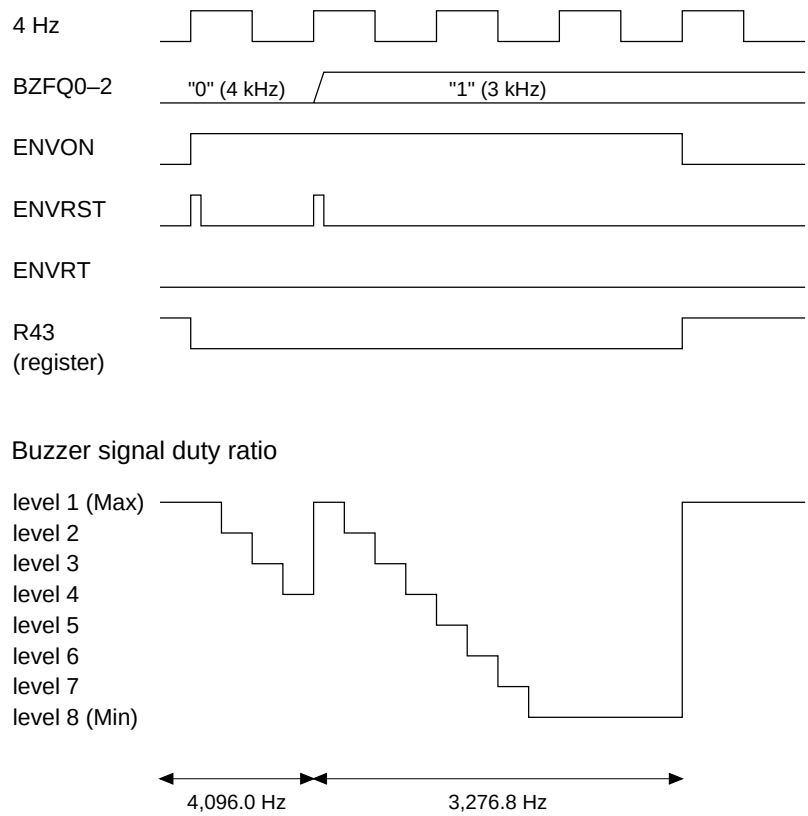


Fig. 6.13.3
Example waveform

```
;*
;* SOUND GENERATOR
;*
ZBFQ    EQU     74H
ZENV    EQU     75H
ZRBZ    EQU     54H
;
ZTMH    EQU     21H
X4HZ    EQU     0010B
;
;
ALARM:
;* ALARM SOUND GENERATOR SUB ROUTINE
;
        LD      A,0FH           ;SET TO I/O DATA MEMORY ADDRESS
        LD      XP,A
;
        LD      B,0             ;INIT. TIMING COUNTER
;
CKEDG:  LD      X,ZTMH          ;CHECK EDGE OF 4Hz SIGNAL
        LD      A,MX
CKEDGE:PUSH     A
        XOR     A,MX
        FAN     A,X4HZ
        POP     A
        JP      Z,CKEDGE
;
        CP      B,1             ;CHECK TIMING COUNTER
        JP      NC,NEXT1        ;IF T-CNT>1 THEN JUMP
        JP      Z,INCTC         ;IF T-CNT=1 THEN JUMP
;
        LD      X,ZBZFQ
        LBPX    MX,01010000B    ;BZ 4KHz, ENV.ON & RESET, RT 0.5SEC
;
        LD      X,ZRBZ          ;BZ, /BZ ON
        AND     MX,0011B
;
INCTC:  ADD     B,1
        JP      CKEDG
;
NEXT1:  CP      B,2
        JP      NZ,NEXT2        ;IF T-CNT/=2 THEN JUMP
;
        LD      X,ZBZFQ
        LBPX    MX,01010001B    ;BZ 3.3KHz, ENV.ON & RESET, RT 0.5SEC
        JP      INCTC
```

```
;
NEXT2:  CP      B,8
        JP      C,INCTC         ;IF T-CNT<8 THEN JUMP
;
        LD      X,ZENV          ;ENV.OFF
        LD      MX,0
;
        LD      X,ZRBZ
        OR      MX,1100B        ;BZ. /BZ OFF
;
        RET
;
;
```

Programming notes

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

6.14 External Memory Access (S1C624A0/4C0/480)

I/O data memory of the external memory access control

The control registers of the external memory access are shown in Tables 6.14.1(a) and (b).

Table 6.14.1(a) Control registers of external memory (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F50H	R03	R02	R01	R00	R03	X	High	Low	Output port (R03)
							High	Low	External memory address (A3)
	R/W				R02	X	High	Low	Output port (R02)
							High	Low	External memory address (A2)
					R01	X	High	Low	Output port (R01)
							High	Low	External memory address (A1)
					R00	X	High	Low	Output port (R00)
							High	Low	External memory address (A0)
F51H	R13	R12	R11	R10	R13	X	High	Low	Output port (R13)
							High	Low	External memory address (A7)
	R/W				R12	X	High	Low	Output port (R12)
							High	Low	External memory address (A6)
					R11	X	High	Low	Output port (R11)
							High	Low	External memory address (A5)
					R10	X	High	Low	Output port (R10)
							High	Low	External memory address (A4)
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R23)
							High	Low	External memory address (A11)
	R/W				R22	X	High	Low	Output port (R22)
							High	Low	External memory address (A10)
					R21	X	High	Low	Output port (R21)
							High	Low	External memory address (A9)
					R20	X	High	Low	Output port (R20)
							High	Low	External memory address (A8)
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						BUSY	READY	[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X	High	Low	Output port (R32)
									[External memory read ($\overline{\text{RD}}$)]
					R31	X	High	Low	Output port (R31)
							High	Low	External memory address (A13)
									[External memory write ($\overline{\text{WR}}$)]
					R30	X	High	Low	Output port (R30)
							High	Low	External memory address (A12)

Table 6.14.1(b) Control registers of external memory (2)

Address	Register								Comment
	D3	D2	D1	D0	Name	SR	1	0	
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P03)
							High	Low	External memory data (D3)
	R/W				P02	X	High	Low	I/O port (P02)
							High	Low	External memory data (D2)
					P01	X	High	Low	I/O port (P01)
							High	Low	External memory data (D1)
					P00	X	High	Low	I/O port (P00)
							High	Low	External memory data (D0)
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P13)
							High	Low	External memory data (D7)
	R/W				P12	X	High	Low	I/O port (P12)
							High	Low	External memory data (D6)
					P11	X	High	Low	I/O port (P11)
							High	Low	External memory data (D5)
					P10	X	High	Low	I/O port (P10)
							High	Low	External memory data (D4)
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P23)
							High	Low	External memory chip select ($\overline{CS3}$)
	R/W				P22	X	High	Low	I/O port (P22)
	W						High	Low	External memory chip select ($\overline{CS2}$)
					P21	X	High	Low	I/O port (P21)
							High	Low	External memory chip select ($\overline{CS1}$)
					P20	X	High	Low	I/O port (P20)
							High	Low	External memory chip select ($\overline{CS0}$)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
	R/W				HZR2	0	Output	High-Z	R20–R23 output high-impedance control
					HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control
F7CH	0	HZCS	ADINC	PICON	0	–			
	R	R/W	W	R/W	HZCS	0	Output	High-Z	$\overline{CS0}$–$\overline{CS3}$ output high-impedance control
					ADINC	–	Increment	–	External memory address increment (A0–A13)
					PICON	0	Auto Inc.	Normal	External memory address auto increment mode

Table 6.14.2
Relationships of Rxx registers and address

Address	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Register	R31	R30	R23	R22	R21	R20	R13	R12	R11	R10	R03	R02	R01	R00

Note *When a read-write device is connected to external memory, R31 become the $\overline{WR}$ output, and the A13 signal cannot be output.*

At initial reset, the above registers will be undefined.

Table 6.14.3
Relationships of registers Pxx and data bits

Data	D7	D6	D5	D4	D3	D2	D1	D0
Register	P13	P12	P11	P10	P03	P02	P01	P00

Note *The data is written and read in the order of low-order bits (D0–D3) then high-order bits (D4–D7).*

At initial reset, the above registers will be undefined.

Example program for the external memory control

Following program shows the external memory access controlling procedure.

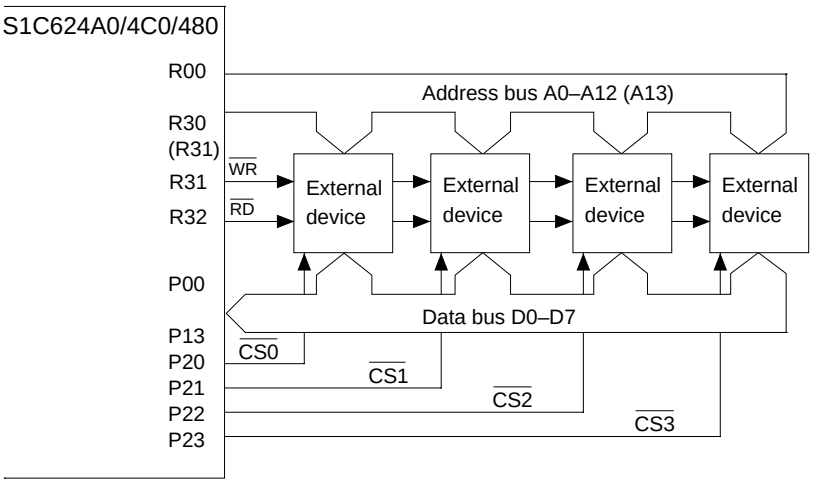


Fig. 6.14.1
External memory block diagram

Table 6.14.4
Output ports and address bus

Output port	Address bus
R00–R03	A0–A3 (select in units of 4 bits)
R10–R13	A4–A7 (select in units of 4 bits)
R20–R22	A8–A10 (select in units of 3 bits)
R23	A11 (select in units of 1bit)
R30	A12 (select in units of 1 bit)
R31	A13 (read-only device only)

The above address signals may be selected by mask option as shown in the table and therefore, unneeded address lines may used as regular output ports.

Moreover, address bus perform the following control functions by software:

– Can perform high impedance control.

– Address incrementing may be automatically accomplished through software and data read/write.

Table 6.14.5
I/O ports and data bus

I/O port	Data bus
P00–P03	D0–D3
P10–P13	D4–D7

Data is written and read in the order of low-order bits (D0–D3) then high-order bits (D4–D7). Through writing/read operation to this register, the write signal ($\overline{WR}$) and read signal ($\overline{RD}$) to the external memory are automatically output.

• Consecutive access of data and virtual data register

Output or input of external memory data to the external data bus is done by accessing registers P00–P03 and P10–P13. It requires access of low order data and high order data, and is related to the increase of program steps. Hence, the S1C624A0/4C0/480 allows even and odd number addresses in the RAM addresses (FC0H–FFFH) to be logically allocated to P00–P03 and P10–P13, respectively, as virtual data; S1C624A0/4C0/480 also makes consecutive access by LBPX and RETD instructions possible.
The memory map of this logical space is shown on Figure 6.14.2.

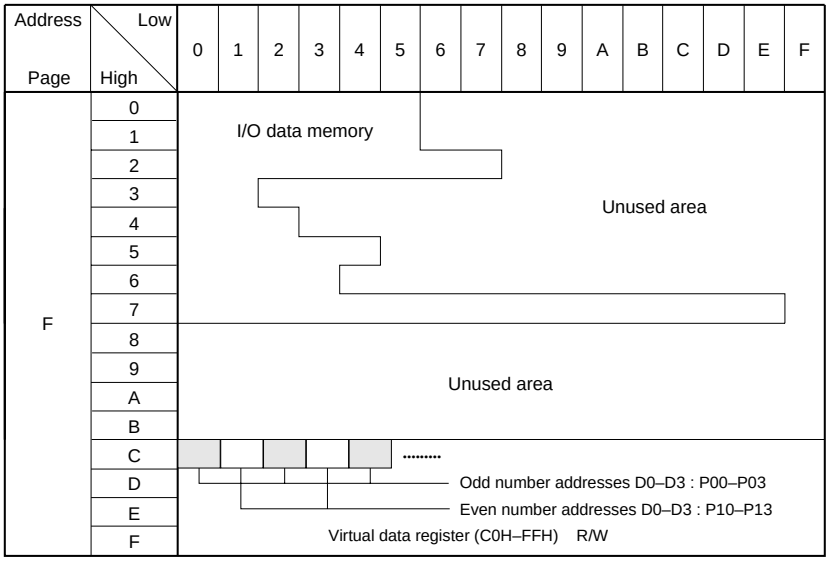


Fig. 6.14.2
Memory map
(virtual data registers)

Note *The virtual data register is a logical space and no memory is physically allocated. The actual writing/reading through access of this space is done for registers P00–P03, and P10–P13.*

Table 6.14.6
I/O ports and
chip selector signal

I/O port	Chip selector signal
P20	$\overline{CS0}$
P21	$\overline{CS1}$
P22	$\overline{CS2}$
P23	$\overline{CS3}$

By writing "0" on P2x, the $\overline{CSx}$ signal becomes active (low level setting); writing "1" will make it normal (high level setting).

By setting the chip select register (P20–P23) corresponding to the device desired to be accessed to "0" and then performing data reading/writing, the $\overline{CSx}$ terminal which selects the active signal will be automatically set to low level, in the same manner as $\overline{WR}$ and $\overline{RD}$ signals. Moreover, after the access, it is automatically set to high level.

Because of the write-only (W/O) function, the chip select register may not be re-written by logical arithmetic instructions.

$\overline{CS}$ signal can perform high impedance control by software. Note, however, that the pull up resistor is turned on to prevent misoperation of external devices.

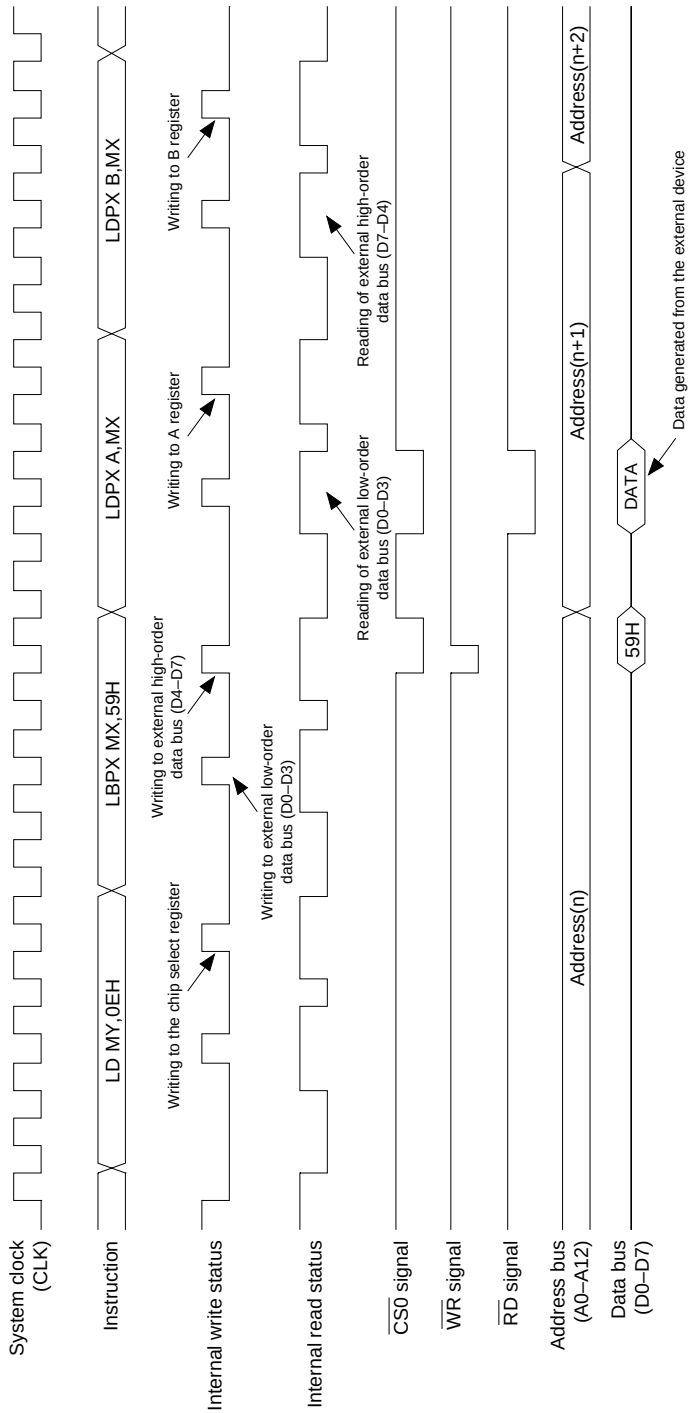


Fig. 6.14.3 Timing chart of external memory access

```
;*
;* EXTERNAL MEMORY ACCESS
;*
ZADDL  EQU    50H
ZADDM  EQU    51H
ZADDH  EQU    52H
ZADDHH EQU    53H
ZCS    EQU    62H
ZDL    EQU    C0H       ;PHYSICAL ADDRESS IS 60H
ZDH    EQU    C1H       ;PHYSICAL ADDRESS IS 61H
ZADINC EQU    7CH
ZADHZ  EQU    7BH
;
YBUF   EQU    0F0H      ;0F0H TO 0FFH ARE ASSIGNED
                        ;AS DATA BUFFER MEMORY
;
;
TRANS8:
;* 8 BYTE DATA TRANSFER FROM DATA BUFFER TO EXTERNAL MEMORY
;
       LD     A,00H     ;SET TOP ADDRESS OF DATA BUFFER MEMORY
       LD     YP,A
       LD     Y,YBUF
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     XP,A
;
       LD     X,ZADDL   ;SET TOP ADDRESS OF EXTERNAL MEMORY
       LDPX   MX,0
       LDPX   MX,0
       LDPX   MX,0
       LD     MX,0
;
       LD     X,ZADINC  ;ADDRESS OUTPUT & AUTO INC.
       OR     MX,0101B
;
       LD     X,ZCS     ;CHIP SELECT OUTPUT (1CS0)
       AND    MX,1110B
;
       LD     X,0C0H    ;SET DATA PORT ADDRESS
;
       LD     B,0H
```

```
;
TRLOP1:LDPX   MX,MY     ;1 BYTE TRANSFER
       INC    Y
       LDPX   MX,MY
       INC    Y
       ADD    B,2H
       JP     NZ,TRLOP1 ;IF <8 BYTE THEN JUMP
;
       LD     X,ZCS     ;CHIP SELECT DISABLE
       OR     MX,1111B
;
       LD     X,ZADHZ   ;MAKE 1CS & ADDRESS BUS TO HIZ
                        ;FOR THE OTHER CPU ACCESS
       LDPX   MX,0
       LD     MX,0
;
;
```

Programming notes

(1) Be sure to data writing/reading for external memory in the order of low-order bits (D0–D3) then high-order bits (D4–D7).

(2) Because of the write-only (W/O) function, the chip select register (P20–P23) may not be re-written by logical arithmetic instruction.

6.15 Interrupt

Interrupt vector, factor flag, and mask register

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

① The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

② The vector address (1 page 02H–0CH) for each interrupt request is set to the program counter.

③ Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Note *Time equivalent to 12 cycles of CPU system clock is required for steps ① and ②.*

The interrupt request and interrupt vector correspondence is shown in Table 6.15.1.

Table 6.15.1 Interrupt request and interrupt vectors

Interrupt vector (PCS and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Serial interface interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

The interrupt factor flags and interrupt mask registers correspondence are shown in Table 6.15.2.
The configuration of the interrupt circuit is shown in Figure 6.15.1.

Table 6.15.2 Interrupt factor flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1 (F00H [D3])	EIT1 (F10H [D3])
Falling edge of clock timer (2 Hz)	IT2 (F00H [D2])	EIT2 (F10H [D2])
Falling edge of clock timer (8 Hz)	IT8 (F00H [D1])	EIT8 (F10H [D1])
Falling edge of clock timer (32 Hz)	IT32 (F00H [D0])	EIT32 (F10H [D0])
Overflow of stopwatch timer (SWH) (1 Hz)	ISW1 (F01H [D1])	EISW1 (F11H [D1])
Overflow of stopwatch timer (SWL) (10 Hz)	ISW0 (F01H [D0])	EISW0 (F11H [D0])
No matching between input ports (K00–K03) and input relation registers (DFK00–DFK03)	IK0 (F04H [D0])	EIK03 (F14H [D3]) EIK02 (F14H [D2]) EIK01 (F14H [D1]) EIK00 (F14H [D0])
Falling edge of input ports (K10–K13)	IK1 (F05H [D0])	EIK13 (F15H [D3]) EIK12 (F15H [D2]) EIK11 (F15H [D1]) EIK10 (F15H [D0])
Data (8 bits) input/output of serial interface has completed	ISIO (F03H [D0])	EISIO (F13H [D0])
Counter value of programmable timer = 00H	IPT (F02H [D0])	EIPT (F12H [D0])

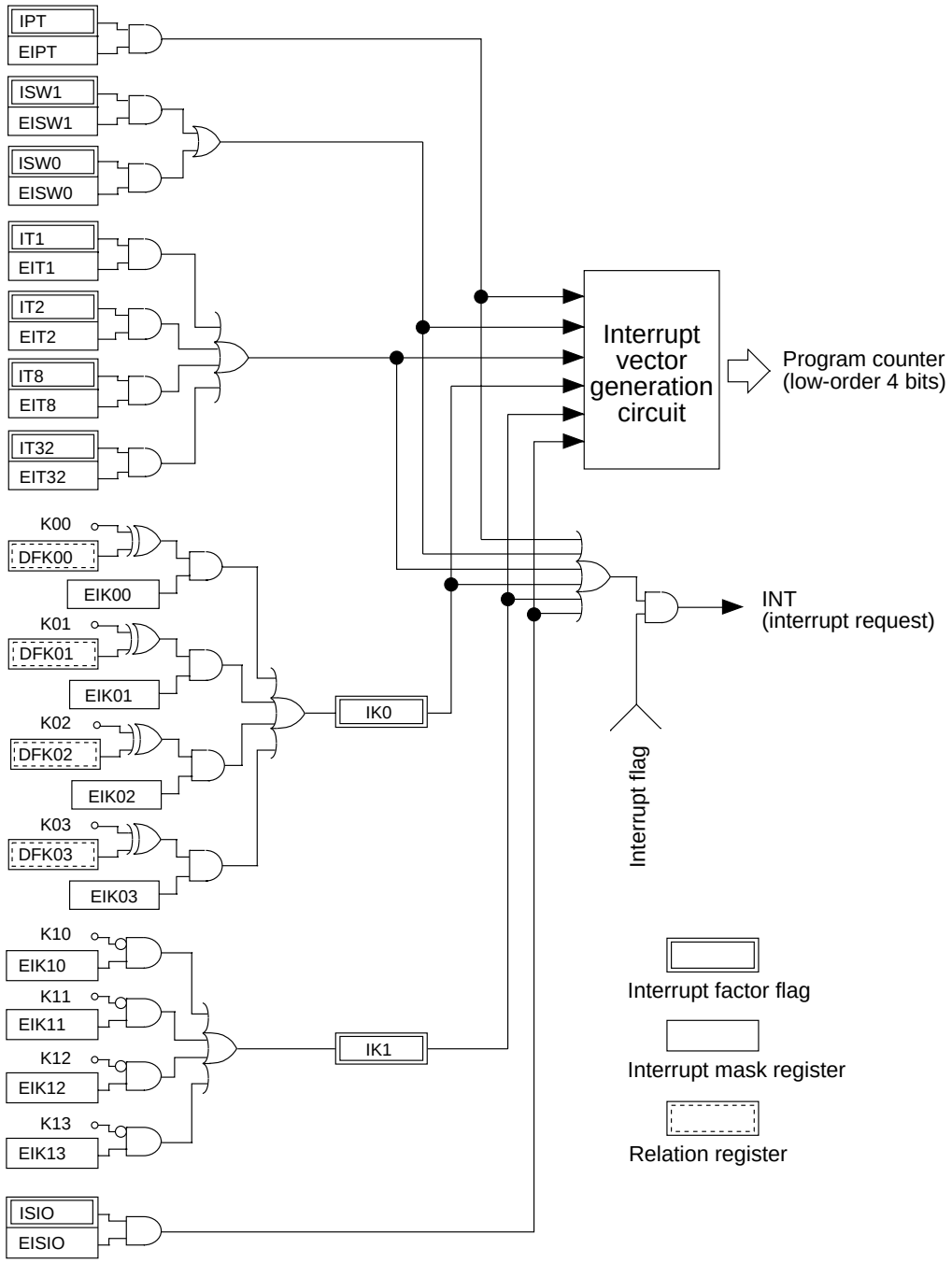


Fig. 6.15.1
Configuration of interrupt circuit

Example program for the interrupt

Following program shows the interrupt procedure.

```
;*
;* INTERRUPT
;*
ZIPT   EQU    02H
ZISIO  EQU    03H
ZIK1   EQU    05H
ZIK0   EQU    04H
ZISW   EQU    01H
ZIT    EQU    00H
;
;
       ORG    102H
;
       PSET   INTRPT
       JP     INTRPT    ;CLOCK TIMER (6th PRIORITY)
       PSET   INTRPT
       JP     INTRPT    ;STOPWATCH (5th PRIORITY)
       PSET   INTRPT
       JP     INTRPT    ;K00 TO K03 (4th PRIORITY)
       PSET   INTRPT
       JP     INTRPT    ;K10 TO K13 (3rd PRIORITY)
       PSET   INTRPT
       JP     INTRPT    ;SERIAL INTERFACE (2nd PRIORITY)
       PSET   INTRPT
       JP     INTRPT    ;PROG. TIMER (1st PRIORITY)
;
;
INTRPT:PUSH   XP        ;SAVE CURRENT CONDITION
       PUSH   XH
       PUSH   XL        ;STORED X REG. (12 BITS)
;
       PUSH   YP
       PUSH   YH
       PUSH   YL        ;STORED Y REG. (12 BITS)
;
       PUSH   B         ;STORE B,A,F REG.
       PUSH   A
       PUSH   F
;
       LD     A,0FH     ;SET TO I/O DATA MEMORY ADDRESS
       LD     XP,A
;
```

```
CHKPTM:LD     X,ZIPT    ;CHECK PROGRAMMABLE TIMER INT.
       FAN    MX,0001B
       JP     Z,CHKSIO  ;IF NO PROG. TIMER INT. THEN JUMP
;
       CALL   INTPTM    ;CALL PROG. TIMER INT. ROUTINE
;
CHKSIO:LD     X,ZISIO   ;CHECK SERIAL INTERFACE INT.
       FAN    MX,0001B
       JP     Z,CHKK1   ;IF NO SERIAL INTERFACE INT. THEN JUMP
;
       CALL   INTSIO    ;CALL SERIAL INTERFACE INT. ROUTINE
;
CHKK1: LD     X,ZIK1    ;CHECK K1 INT.
       FAN    MX,0001B
       JP     Z,CHKK0   ;IF NO K1 INT. THEN JUMP
;
       CALL   INTK1     ;CALL K1 INT. ROUTINE
;
CHKK0: LD     X,ZIK0    ;CHECK K0 INT.
       FAN    MX,0001B
       JP     Z,CHKSW0  ;IF NO K0 INT. THEN JUMP
;
       CALL   INTK0     ;CALL K0 INT. ROUTINE
;
CHKSW0:LD     X,ZISW    ;CHECK STOPWATCH INT.
       LD     B,MX      ;CHECK SW0
       FAN    B,0001B
       JP     Z,CHKSW1  ;IF NO SW0 INT. THEN JUMP
;
       CALL   INTSW0    ;CALL SW0 INT. ROUTINE
;
CHKSW1:FAN    B,0010B   ;CHECK SW1
       JP     Z,CHKT32  ;IF NO SW1 INT. THEN JUMP
;
       CALL   INTSW1    ;CALL SW1 INT. ROUTINE
;
CHKT32:LD     X,ZIT     ;CHECK CLOCK TIMER INT.
       LD     B,MX
       FAN    B,0001B   ;CHECK 32Hz INT.
       JP     Z,CHKT8   ;IF NO 32Hz INT. THEN JUMP
;
       CALL   INTT32    ;CALL T32 INT. ROUTINE
;
CHKT8: FAN    B,0010B   ;CHECK 8Hz INT.
       JP     Z,CHKT2   ;IF NO 8Hz INT. THEN JUMP
;
```

```
        CALL    INTT8     ;CALL T8 INT. ROUTINE
;
CHKT2:  FAN     B,0100B   ;CHECK 2Hz INT.
        JP      Z,CHKT1   ;IF NO 2Hz INT. THEN JUMP
;
        CALL    INTT2     ;CALL T2 INT. ROUTINE
;
CHKT1:  FAN     B,1000B   ;CHECK 1Hz INT.
        JP      Z,INTEND  ;IF NO 1Hz INT. THEN JUMP
;
        CALL    INTT1     ;CALL T1 INT. ROUTINE
;
;
INTEND:POP      F         ;RESTORE F,A,B FLAG
        POP     A
        POP     B
;
        POP     YL        ;RESTORE Y REG. (12 BITS)
        POP     YH
        POP     YP
;
        POP     XL        ;RESTORE X REG. (12 BITS)
        POP     XH
        POP     XP
        EI                ;ENABLE INTERRUPT
        RET
;
```

Programming notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(5) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.
Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.
Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.

Program example 1: To quit the interrupt processing if the interrupt factor flag has not been set

```
0100H    PSET   NIT
0101H    JP     INIT
0102H    PSET   TM_INT
0103H    JP     TM_INT
0104H    PSET   SW_INT
0105H    JP     SW_INT
0106H    PSET   K0X_INT
```

```
0107H     JP      K0X_INT
0108H     PSET    K1X_INT
0109H     JP      K1X_INT
010AH     PSET    SIO_INT
010BH     JP      SIO_INT
010CH     PSET    PT_INT
010DH     JP      PT_INT
010EH     PSET    PT_INT
010FH     JP      PT_INT
;
;INTERRUPT PROCESSING FOR PROGRAMMABLE TIMER
;
PT_INT:
          PUSH    F
          :       :
          LD      A,0FH
          LD      XP,A
          LD      X,02H
          FAN     MX,0001B    ;CHECK PROG. TIMER INT. FACTOR FLAG
          JP      Z,EXIT
          :       :
;
;INTERRUPT PROCESSING FOR SERIAL I/O
;
SIO_INT:
          PUSH    F
          :       :
          LD      A,0FH
          LD      XP,A
          LD      X,03H
          FAN     MX,0001B    ;CHECK SERIAL I/O INT. FACTOR FLAG
          JP      Z,EXIT
          :       :
;
;INTERRUPT PROCESSING FOR K10-K13
;
K1X_INT:
          PUSH    F
          :       :
          LD      A,0FH
          LD      XP,A
          LD      X,05H
          FAN     MX,00001B   ;CHECK K10–K13 PORT INT. FACTOR FLAG
          JP      Z,EXIT
          :        :
;
;INTERRUPT PROCESSING FOR K00-K03
;
K0X_INT:
          PUSH    F
          :       :
```

```
          LD      A,0FH
          LD      XP,A
          LD      X,04H
          FAN     MX,00001B   ;CHECK K00–K03 PORT INT. FACTOR FLAG
          JP      Z,EXIT
          :       :
;
;INTERRUPT PROCESSING FOR STOPWATCH TIMER
;
SW_INT:
          PUSH    F
          :       :
          LD      A,0FH
          LD      XP,A
          LD      X,01H
          FAN     MX,0011B    ;CHECK STOPWATCH INT. FACTOR FLAG
          JP      Z,EXIT
          :       :
;
;INTERRUPT PROCESSING FOR TIMER
;
TM_INT:
          PUSH    F
          :       :
          LD      A,0FH
          LD      XP,A
          LD      X,00H
          FAN     MX,1111B    ;CHECK TIMER INT. FACTOR FLAG
          JP      Z,EXIT
          :       :
EXIT:
          :       :
          POP     F
          EI
          RET                 ;RETURNES WITHOUT ANY PROCESS IF NO
                              ;INTERRUPT FACTOR FLAG IS SET
```

If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.

Program example 2: To branch the flow to the same processing routine from interrupt vectors and to check all the interrupt factor flags in the routine

```
0100H     PSET    INIT
0101H     JP      INIT
```

```
0102H     PSET   INTERRUPT
0103H     JP     INTERRUPT
0104H     PSET   INTERRUPT
0105H     JP     INTERRUPT
0106H     PSET   INTERRUPT
0107H     JP     INTERRUPT
0108H     PSET   INTERRUPT
0109H     JP     INTERRUPT
010AH     PSET   INTERRUPT
010BH     JP     INTERRUPT
010CH     PSET   INTERRUPT
010DH     JP     INTERRUPT
010EH     PSET   INTERRUPT
010FH     JP     INTERRUPT

INTERRUPT:
          PUSH   F
          :      :
          LD     A,0FH
          LD     XP,A
          LD     X,00H
          LDPX   A,MX
          OR     A,1111B
          JP     NZ,TM_INT   ;CHECK TIMER INT. FACTOR FLAG
          LDPX   A,MX
          OR     A,0011B
          JP     NZ,SW_INT   ;CHECK STOPWATCH INT. FACTOR FLAG
          LDPX   A,MX
          OR     A,0001B
          JP     NZ,PT_INT   ;CHECK PROG. TIMER INT. FACTOR FLAG
          LDPX   A,MX
          OR     A,0001B
          JP     NZ,SIO_INT  ;CHECK SERIAL I/O INT. FACTOR FLAG
          LDPX   A,MX
          OR     A,0001B
          JP     NZ,K0_INT   ;CHECK K00–K03 PORT INT. FACTOR FLAG
          LDPX   A,MX
          OR     A,0001B
          JP     NZ,K1_INT   ;CHECK K10–K13 PORT INT. FACTOR FLAG
          :      :
          POP    F
          EI
          RET                ;RETURNES WITHOUT ANY PROCESS IF NO
                             ;INTERRUPT FACTOR FLAG IS SET
```

Program example 3: To check all the interrupt factor flags in the main routine the RET instruction is placed in all interrupt vectors

```
0100H     PSET   INIT
0101H     JP     INIT
0102H     RET
```

```
0103H    NOP5
0104H    RET
0105H    NOP5
0106H    RET
0107H    NOP5
0108H    RET
0109H    NOP5
010AH    RET
010BH    NOP5
010CH    RET
010DH    NOP5
010EH    RET
010FH    NOP5

MAIN:
:        :      :
(Enable interrupt flags)
:        :      :
         HALT
         LD     A,0FH
         LD     XP,A
         LD     X,00H
         LDPX   A,MX
         OR     A,1111B
         JP     NZ,TM_INT   ;CHECK TIMER INT. FACTOR FLAG
         LDPX   A,MX
         OR     A,0011B
         JP     NZ,SW_INT   ;CHECK STOPWATCH INT. FACTOR FLAG
         LDPX   A,MX
         OR     A,0001B
         JP     NZ,PT_INT   ;CHECK PROG. TIMER INT. FACTOR FLAG
         LDPX   A,MX
         OR     A,0001B
         JP     NZ,SIO_INT  ;CHECK SERIAL I/O INT. FACTOR FLAG
         LDPX   A,MX
         OR     A,0001B
         JP     NZ,K0_INT   ;CHECK K00–K03 PORT INT. FACTOR FLAG
         LDPX   A,MX
         OR     A,0001B
         JP     NZ,K1_INT   ;CHECK K10–K13 PORT INT. FACTOR FLAG
         JP     MAIN        ;RETURNES WITHOUT ANY PROCESS IF NO
                            ;INTERRUPT FACTOR FLAG IS SET
```

When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER 7 SUMMARY OF NOTES

7.1 Notes for Low Current Consumption

The S1C62440/4A0/4C0/480 contain control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 7.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (*)
CPU operation frequency	CLKCHG, OSCC	See electrical characteristics (*)
Internal regulated voltage	VSC0, VSC1	See electrical characteristics (*)
Heavy load protection mode	HLMOD	See electrical characteristics (*)
SVD circuit	SVDON	Several tens µA

* "S1C62440/624A0/624C0/62480 Technical Hardware", Chapter 17

Below are the circuit statuses at initial reset.

CPU:	Operating
CPU operating frequency:	OSC1 side (CLKCHG = "0"), OSC3 oscillation circuit stoped (OSCC = "0")
Internal regulated voltage:	-1.2 V (VSC0, VSC1 = "0") In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V.
Heavy load protection mode:	Normal operating mode (HLMOD = "0")
SVD circuit:	OFF (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

7.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mined when programming.

System initialization

In some of initial registers and initial data memory area, the initial value is undefined after reset. Set them proper initial values by the program, as necessary.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

SVD (supply voltage detection) circuit

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

Heavy load protection mode

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 6.11.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 6.11.1.)

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST←"1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

Oscillation circuit

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) Before you use OSC1 as system clock, you should check the supply voltage (V_{SS}) using the SVD circuit.
If the SVD circuit detects supply voltage less than 3.1 V (V_{DD}–V_{SS} < 3.1 V) then set the operating voltage (V_{S1}) to -1.2 V. Or if the SVD circuit detects supply voltage 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V) then set V_{S1} to -2.1 V.
Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 6.2.2 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

(6) In the S1C62440/4C0/480, when CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V and will never become -1.2 V.

Input port (Kxx)

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

(2) Input interrupt programing related precautions

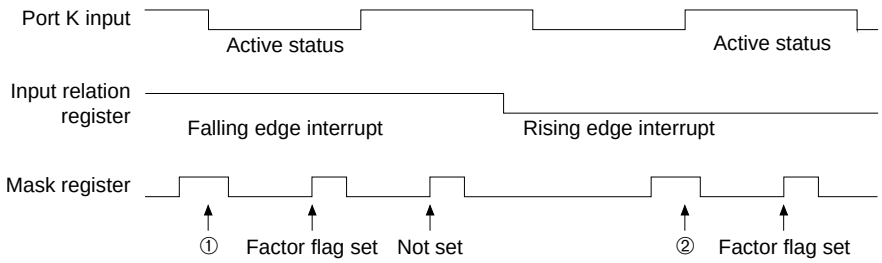


Fig. 7.2.1 Input interrupt timing

When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = Low status, when the falling edge interrupt is effected and

input terminal = High status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 7.2.1. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case.

When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 7.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.
In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

Output port (Rxx)

(1) When BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

I/O port (Pxx)

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
– The input/output mode is set at output mode
– Output specification is set at Nch open drain
– The content of the data register is "1"
– The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

LCD driver

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

Stopwatch timer

When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

Programmable timer

(1) When initiating programmable timer count, perform programming by the following steps:
1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than 256 Hz, high speed processing by OSC3 is required.

Serial interface (SIN, SOUT, and $\overline{SCLK}$)

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

Sound generator

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

External memory access

(1) Be sure to data writing/reading for external memory in the order of low-order bits (D0–D3) then high-order bits (D4–D7).

(2) Because of the write-only (W/O) function, the chip select register (P20–P23) may not be re-written by logical arithmetic instruction.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(5) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.
Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.
Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.
If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.
When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

APPENDIX A S1C62440/4A0/4C0/480 DATA MEMORY (RAM) MAP

S1C62440/4A0/4C0/480 data memory map (1) – RAM

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (2) – RAM

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (3) – RAM

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (4) – RAM < S1C624A0/4C0/480 only >

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (5) – RAM < S1C624A0/4C0/480 only >

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (6) – RAM < S1C624C0/480 only >

PROGRAM NAME : C24C/48

P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (7) – RAM < S1C624C0 only >

PROGRAM NAME : C24C																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (8) – RAM < S1C624C0 only >

PROGRAM NAME : C24C																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
3	8	NAME																
		MSB																
		LSB																
	9	NAME																
		MSB																
		LSB																
	A	NAME																
		MSB																
		LSB																
	B	NAME																
		MSB																
		LSB																
	C	NAME																
		MSB																
		LSB																
	D	NAME																
		MSB																
		LSB																
	E	NAME																
		MSB																
		LSB																
	F	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (9) – RAM < S1C624C0 only >

PROGRAM NAME : C24C																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4	0	NAME																
		MSB																
		LSB																
	1	NAME																
		MSB																
		LSB																
	2	NAME																
		MSB																
		LSB																
	3	NAME																
		MSB																
		LSB																
	4	NAME																
		MSB																
		LSB																
	5	NAME																
		MSB																
		LSB																
	6	NAME																
		MSB																
		LSB																
	7	NAME																
		MSB																
		LSB																

S1C62440/4A0/4C0/480 data memory map (10) – Segment data memory

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0	NAME																
		MSB	[3,0]	[7,0]	[3,1]	[7,1]	[3,2]	[7,2]	[3,3]	[7,3]	[3,4]	[7,4]	[3,5]	[7,5]	[3,6]	[7,6]	[3,7]	[7,7]
			[2,0]	[6,0]	[2,1]	[6,1]	[2,2]	[6,2]	[2,3]	[6,3]	[2,4]	[6,4]	[2,5]	[6,5]	[2,6]	[6,6]	[2,7]	[6,7]
			[1,0]	[5,0]	[1,1]	[5,1]	[1,2]	[5,2]	[1,3]	[5,3]	[1,4]	[5,4]	[1,5]	[5,5]	[1,6]	[5,6]	[1,7]	[5,7]
		LSB	[0,0]	[4,0]	[0,1]	[4,1]	[0,2]	[4,2]	[0,3]	[4,3]	[0,4]	[4,4]	[0,5]	[4,5]	[0,6]	[4,6]	[0,7]	[4,7]
	1	NAME																
		MSB	[3,8]	[7,8]	[3,9]	[7,9]	[3,10]	[7,10]	[3,11]	[7,11]	[3,12]	[7,12]	[3,13]	[7,13]	[3,14]	[7,14]	[3,15]	[7,15]
			[2,8]	[6,8]	[2,9]	[6,9]	[2,10]	[6,10]	[2,11]	[6,11]	[2,12]	[6,12]	[2,13]	[6,13]	[2,14]	[6,14]	[2,15]	[6,15]
			[1,8]	[5,8]	[1,9]	[5,9]	[1,10]	[5,10]	[1,11]	[5,11]	[1,12]	[5,12]	[1,13]	[5,13]	[1,14]	[5,14]	[1,15]	[5,15]
		LSB	[0,8]	[4,8]	[0,9]	[4,9]	[0,10]	[4,10]	[0,11]	[4,11]	[0,12]	[4,12]	[0,13]	[4,13]	[0,14]	[4,14]	[0,15]	[4,15]
	2	NAME																
		MSB	[3,16]	[7,16]	[3,17]	[7,17]	[3,18]	[7,18]	[3,19]	[7,19]	[3,20]	[7,20]	[3,21]	[7,21]	[3,22]	[7,22]	[3,23]	[7,23]
			[2,16]	[6,16]	[2,17]	[6,17]	[2,18]	[6,18]	[2,19]	[6,19]	[2,20]	[6,20]	[2,21]	[6,21]	[2,22]	[6,22]	[2,23]	[6,23]
			[1,16]	[5,16]	[1,17]	[5,17]	[1,18]	[5,18]	[1,19]	[5,19]	[1,20]	[5,20]	[1,21]	[5,21]	[1,22]	[5,22]	[1,23]	[5,23]
		LSB	[0,16]	[4,16]	[0,17]	[4,17]	[0,18]	[4,18]	[0,19]	[4,19]	[0,20]	[4,20]	[0,21]	[4,21]	[0,22]	[4,22]	[0,23]	[4,23]
	3	NAME																
		MSB	[3,24]	[7,24]	[3,25]	[7,25]	[3,26]	[7,26]	[3,27]	[7,27]	[3,28]	[7,28]	[3,29]	[7,29]	[3,30]	[7,30]	[3,31]	[7,31]
			[2,24]	[6,24]	[2,25]	[6,25]	[2,26]	[6,26]	[2,27]	[6,27]	[2,28]	[6,28]	[2,29]	[6,29]	[2,30]	[6,30]	[2,31]	[6,31]
			[1,24]	[5,24]	[1,25]	[5,25]	[1,26]	[5,26]	[1,27]	[5,27]	[1,28]	[5,28]	[1,29]	[5,29]	[1,30]	[5,30]	[1,31]	[5,31]
		LSB	[0,24]	[4,24]	[0,25]	[4,25]	[0,26]	[4,26]	[0,27]	[4,27]	[0,28]	[4,28]	[0,29]	[4,29]	[0,30]	[4,30]	[0,31]	[4,31]
	4	NAME																
		MSB	[3,32]	[7,32]	[3,33]	[7,33]	[3,34]	[7,34]	[3,35]	[7,35]	[3,36]	[7,36]	[3,37]	[7,37]	[3,38]	[7,38]	[3,39]	[7,39]
			[2,32]	[6,32]	[2,33]	[6,33]	[2,34]	[6,34]	[2,35]	[6,35]	[2,36]	[6,36]	[2,37]	[6,37]	[2,38]	[6,38]	[2,39]	[6,39]
			[1,32]	[5,32]	[1,33]	[5,33]	[1,34]	[5,34]	[1,35]	[5,35]	[1,36]	[5,36]	[1,37]	[5,37]	[1,38]	[5,38]	[1,39]	[5,39]
		LSB	[0,32]	[4,32]	[0,33]	[4,33]	[0,34]	[4,34]	[0,35]	[4,35]	[0,36]	[4,36]	[0,37]	[4,37]	[0,38]	[4,38]	[0,39]	[4,39]

[COM, SEG] . . . LCD dot

S1C62440/4A0/4C0/480 data memory map (11) – Segment data memory < S1C624C0/480 only >

PROGRAM NAME : C24C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	5	NAME																
		MSB	[3,40]	[7,40]	[3,41]	[7,41]	[3,42]	[7,42]	[3,43]	[7,43]	[3,44]	[7,44]	[3,45]	[7,45]	[3,46]	[7,46]	[3,47]	[7,47]
			[2,40]	[6,40]	[2,41]	[6,41]	[2,42]	[6,42]	[2,43]	[6,43]	[2,44]	[6,44]	[2,45]	[6,45]	[2,46]	[6,46]	[2,47]	[6,47]
			[1,40]	[5,40]	[1,41]	[5,41]	[1,42]	[5,42]	[1,43]	[5,43]	[1,44]	[5,44]	[1,45]	[5,45]	[1,46]	[5,46]	[1,47]	[5,47]
		LSB	[0,40]	[4,40]	[0,41]	[4,41]	[0,42]	[4,42]	[0,43]	[4,43]	[0,44]	[4,44]	[0,45]	[4,45]	[0,46]	[4,46]	[0,47]	[4,47]
	6	NAME																
		MSB	[3,48]	[7,48]	[3,49]	[7,49]	[3,50]	[7,50]										
			[2,48]	[6,48]	[2,49]	[6,49]	[2,50]	[6,50]										
			[1,48]	[5,48]	[1,49]	[5,49]	[1,50]	[5,50]										
		LSB	[0,48]	[4,48]	[0,49]	[4,49]	[0,50]	[4,50]										

[COM, SEG] . . . LCD dot

S1C62440/4A0/4C0/480 data memory map (12) – Segment data memory

PROGRAM NAME : C244/4A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	8	NAME																
		MSB	[11,0]	[15,0]	[11,1]	[15,1]	[11,2]	[15,2]	[11,3]	[15,3]	[11,4]	[15,4]	[11,5]	[15,5]	[11,6]	[15,6]	[11,7]	[15,7]
			[10,0]	[14,0]	[10,1]	[14,1]	[10,2]	[14,2]	[10,3]	[14,3]	[10,4]	[14,4]	[10,5]	[14,5]	[10,6]	[14,6]	[10,7]	[14,7]
			[9,0]	[13,0]	[9,1]	[13,1]	[9,2]	[13,2]	[9,3]	[13,3]	[9,4]	[13,4]	[9,5]	[13,5]	[9,6]	[13,6]	[9,7]	[13,7]
		LSB	[8,0]	[12,0]	[8,1]	[12,1]	[8,2]	[12,2]	[8,3]	[12,3]	[8,4]	[12,4]	[8,5]	[12,5]	[8,6]	[12,6]	[8,7]	[12,7]
	9	NAME																
		MSB	[11,8]	[15,8]	[11,9]	[15,9]	[11,10]	[15,10]	[11,11]	[15,11]	[11,12]	[15,12]	[11,13]	[15,13]	[11,14]	[15,14]	[11,15]	[15,15]
			[10,8]	[14,8]	[10,9]	[14,9]	[10,10]	[14,10]	[10,11]	[14,11]	[10,12]	[14,12]	[10,13]	[14,13]	[10,14]	[14,14]	[10,15]	[14,15]
			[9,8]	[13,8]	[9,9]	[13,9]	[9,10]	[13,10]	[9,11]	[13,11]	[9,12]	[13,12]	[9,13]	[13,13]	[9,14]	[13,14]	[9,15]	[13,15]
		LSB	[8,8]	[12,8]	[8,9]	[12,9]	[8,10]	[12,10]	[8,11]	[12,11]	[8,12]	[12,12]	[8,13]	[12,13]	[8,14]	[12,14]	[8,15]	[12,15]
	A	NAME																
		MSB	[11,16]	[15,16]	[11,17]	[15,17]	[11,18]	[15,18]	[11,19]	[15,19]	[11,20]	[15,20]	[11,21]	[15,21]	[11,22]	[15,22]	[11,23]	[15,23]
			[10,16]	[14,16]	[10,17]	[14,17]	[10,18]	[14,18]	[10,19]	[14,19]	[10,20]	[14,20]	[10,21]	[14,21]	[10,22]	[14,22]	[10,23]	[14,23]
			[9,16]	[13,16]	[9,17]	[13,17]	[9,18]	[13,18]	[9,19]	[13,19]	[9,20]	[13,20]	[9,21]	[13,21]	[9,22]	[13,22]	[9,23]	[13,23]
		LSB	[8,16]	[12,16]	[8,17]	[12,17]	[8,18]	[12,18]	[8,19]	[12,19]	[8,20]	[12,20]	[8,21]	[12,21]	[8,22]	[12,22]	[8,23]	[12,23]
	B	NAME																
		MSB	[11,24]	[15,24]	[11,25]	[15,25]	[11,26]	[15,26]	[11,27]	[15,27]	[11,28]	[15,28]	[11,29]	[15,29]	[11,30]	[15,30]	[11,31]	[15,31]
			[10,24]	[14,24]	[10,25]	[14,25]	[10,26]	[14,26]	[10,27]	[14,27]	[10,28]	[14,28]	[10,29]	[14,29]	[10,30]	[14,30]	[10,31]	[14,31]
			[9,24]	[13,24]	[9,25]	[13,25]	[9,26]	[13,26]	[9,27]	[13,27]	[9,28]	[13,28]	[9,29]	[13,29]	[9,30]	[13,30]	[9,31]	[13,31]
		LSB	[8,24]	[12,24]	[8,25]	[12,25]	[8,26]	[12,26]	[8,27]	[12,27]	[8,28]	[12,28]	[8,29]	[12,29]	[8,30]	[12,30]	[8,31]	[12,31]
	C	NAME																
		MSB	[11,32]	[15,32]	[11,33]	[15,33]	[11,34]	[15,34]	[11,35]	[15,35]	[11,36]	[15,36]	[11,37]	[15,37]	[11,38]	[15,38]	[11,39]	[15,39]
			[10,32]	[14,32]	[10,33]	[14,33]	[10,34]	[14,34]	[10,35]	[14,35]	[10,36]	[14,36]	[10,37]	[14,37]	[10,38]	[14,38]	[10,39]	[14,39]
			[9,32]	[13,32]	[9,33]	[13,33]	[9,34]	[13,34]	[9,35]	[13,35]	[9,36]	[13,36]	[9,37]	[13,37]	[9,38]	[13,38]	[9,39]	[13,39]
		LSB	[8,32]	[12,32]	[8,33]	[12,33]	[8,34]	[12,34]	[8,35]	[12,35]	[8,36]	[12,36]	[8,37]	[12,37]	[8,38]	[12,38]	[8,39]	[12,39]

[COM, SEG] . . . LCD dot

S1C62440/4A0/4C0/480 data memory map (13) – Segment data memory < S1C624C0/480 only >

PROGRAM NAME : C24C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	D	NAME																
		MSB	[11,40]	[15,40]	[11,41]	[15,41]	[11,42]	[15,42]	[11,43]	[15,43]	[11,44]	[15,44]	[11,45]	[15,45]	[11,46]	[15,46]	[11,47]	[15,47]
			[10,40]	[14,40]	[10,41]	[14,41]	[10,42]	[14,42]	[10,43]	[14,43]	[10,44]	[14,44]	[10,45]	[14,45]	[10,46]	[14,46]	[10,47]	[14,47]
			[9,40]	[13,40]	[9,41]	[13,41]	[9,42]	[13,42]	[9,43]	[13,43]	[9,44]	[13,44]	[9,45]	[13,45]	[9,46]	[13,46]	[9,47]	[13,47]
		LSB	[8,40]	[12,40]	[8,41]	[12,41]	[8,42]	[12,42]	[8,43]	[12,43]	[8,44]	[12,44]	[8,45]	[12,45]	[8,46]	[12,46]	[8,47]	[12,47]
	E	NAME																
		MSB	[11,48]	[15,48]	[11,49]	[15,49]	[11,50]	[15,50]										
			[10,48]	[14,48]	[10,49]	[14,49]	[10,50]	[14,50]										
			[9,48]	[13,48]	[9,49]	[13,49]	[9,50]	[13,50]										
		LSB	[8,48]	[12,48]	[8,49]	[12,49]	[8,50]	[12,50]										

[COM, SEG] . . . LCD dot

S1C62440/4A0/4C0/480 data memory map (14) – I/O data memory < S1C62440 >

PROGRAM NAME : C244

P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	0	NAME	ZTI	ZISW	ZIPT	ZISIO	ZIK0	ZIK1										
		MSB	IT1	0	0	0	0	0										
			IT2	0	0	0	0	0										
			IT8	ISW1	0	0	0	0										
		LSB	IT32	ISW0	IPT	ISIO	IK0	IK1										
	1	NAME	ZEIT	ZEISW	ZEIPT	ZEISIO	ZEIK0	ZEIK1										
		MSB	EIT1	0	0	0	EIK03	EIK13										
			EIT2	0	0	0	EIK02	EIK12										
			EIT8	EISW1	0	0	EIK01	EIK11										
		LSB	EIT32	EISW0	EIPT	EISIO	EIK00	EIK10										
	2	NAME	ZTML	ZTMH	ZSWL	ZSWH	ZPTL	ZPTH	ZRDL	ZRDH								
		MSB	TM3	TM7	SWL3	SWH3	PT3	PT7	RD3	RD7								
			TM2	TM6	SWL2	SWH2	PT2	PT6	RD2	RD6								
			TM1	TM5	SWL1	SWH1	PT1	PT5	RD1	RD5								
		LSB	TM0	TM4	SWL0	SWH0	PT0	PT4	RD0	RD4								
	3	NAME	ZSDL	ZSDH														
		MSB	SD3	SD7														
			SD2	SD6														
			SD1	SD5														
		LSB	SD0	SD4														
	4	NAME	ZK0	ZDFK0	ZK1													
		MSB	K03	DFK03	K13													
			K02	DFK02	K12													
			K01	DFK01	K11													
		LSB	K00	DFK00	K10													
	5	NAME			ZR2	ZR3	ZR4											
		MSB			R23	R33	R43											
					R22	R32	R42											
					R21	R31	R41											
		LSB			R20	R30	R40											
	6	NAME	ZP0	ZP1	ZP2													
		MSB	P03	P13	P23													
			P02	P12	P22													
			P01	P11	P21													
		LSB	P00	P10	P20													
	7	NAME	ZOSC	ZLCD	ZLC	ZSVD	ZBZ	ZENV	ZTRST	ZSWR	ZPTR	ZPTC	ZSC	ZHZR	ZEMA	ZIOC	ZPUP	
		MSB	CLKCHG	ALOFF	LC3	SVDDT	SHOTPW	BZSHOT	0	0	0	PTCOUT	SCTRG	HZR3	0			
			OSCC	ALON	LC2	SVDON	BZFQ2	ENVRST	0	0	0	PTC2	SEN	HZR2	HZCS	IOC2	PUP2	
			VSC1	LDUTY	LC1	SVC1	BZFQ1	ENVRT	TMRST	SWRST	PTRST	PTC1	SCS1		ADINC	IOC1	PUP1	
		LSB	VSC0	HLMOD	LC0	SVC0	BZFQ0	ENVON	WDRST	SWRUN	PTRUN	PTC0	SCS0		PICON	IOC0	PUP0	

S1C62440/4A0/4C0/480 data memory map (15) – I/O data memory < S1C624A0/4C0/480 >

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	0	NAME	ZTI	ZISW	ZIPT	ZISIO	ZIK0	ZIK1										
		MSB	IT1	0	0	0	0	0										
			IT2	0	0	0	0	0										
			IT8	ISW1	0	0	0	0										
		LSB	IT32	ISW0	IPT	ISIO	IK0	IK1										
	1	NAME	ZEIT	ZEISW	ZEIPT	ZEISIO	ZEIK0	ZEIK1										
		MSB	EIT1	0	0	0	EIK03	EIK13										
			EIT2	0	0	0	EIK02	EIK12										
			EIT8	EISW1	0	0	EIK01	EIK11										
		LSB	EIT32	EISW0	EIPT	EISIO	EIK00	EIK10										
	2	NAME	ZTML	ZTMH	ZSWL	ZSWH	ZPTL	ZPTH	ZRDL	ZRDH								
		MSB	TM3	TM7	SWL3	SWH3	PT3	PT7	RD3	RD7								
			TM2	TM6	SWL2	SWH2	PT2	PT6	RD2	RD6								
			TM1	TM5	SWL1	SWH1	PT1	PT5	RD1	RD5								
		LSB	TM0	TM4	SWL0	SWH0	PT0	PT4	RD0	RD4								
	3	NAME	ZSDL	ZSDH														
		MSB	SD3	SD7														
			SD2	SD6														
			SD1	SD5														
		LSB	SD0	SD4														
	4	NAME	ZK0	ZDFK0	ZK1													
		MSB	K03	DFK03	K13													
			K02	DFK02	K12													
			K01	DFK01	K11													
		LSB	K00	DFK00	K10													
	5	NAME	ZR0	ZR1	ZR2	ZR3	ZR4											
		MSB	R03	R13	R23	R33	R43											
			R02	R12	R22	R32	R42											
			R01	R11	R21	R31	R41											
		LSB	R00	R10	R20	R30	R40											
	6	NAME	ZP0	ZP1	ZP2	ZP3												
		MSB	P03	P13	P23	P33												
			P02	P12	P22	P32												
			P01	P11	P21	P31												
		LSB	P00	P10	P20	P30												
	7	NAME	ZOSC	ZLCD	ZLC	ZSVD	ZBZ	ZENV	ZTRST	ZSWR	ZPTR	ZPTC	ZSC	ZHZR	ZEMA	ZIOC	ZPUP	
		MSB	CLKCHG	ALOFF	LC3	SVDDT	SHOTPW	BZSHOT	0	0	0	PTCOUT	SCTRG	HZR3	0	IOC3	PUP3	
			OSCC	ALON	LC2	SVDON	BZFQ2	ENVRST	0	0	0	PTC2	SEN	HZR2	HZCS	IOC2	PUP2	
			VSC1	LDUTY	LC1	SVC1	BZFQ1	ENVRT	TMRST	SWRST	PTRST	PTC1	SCS1	HZR1	ADINC	IOC1	PUP1	
		LSB	VSC0	HLMOD	LC0	SVC0	BZFQ0	ENVON	WDRST	SWRUN	PTRUN	PTC0	SCS0	HZR0	PICON	IOC0	PUP0	

S1C62440/4A0/4C0/480 data memory map (16) – I/O data memory < S1C624A0/4C0/480 only >

PROGRAM NAME : C24A/4C/48																		
P	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	C	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	D	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	E	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'
	F	NAME																
		MSB	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'	P03'	P13'
			P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'	P02'	P12'
			P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'	P01'	P11'
		LSB	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'	P00'	P10'

APPENDIX B S1C62440/4A0/4C0/480 INSTRUCTION SET

S1C62440/4A0/4C0/480 Instruction set (1)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
	SLP *		1	1	1	1	1	1	1	1	1	0	0	1					5	SLEEP (stop oscillation)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

* Not in S1C62440/4A0/4C0/480

S1C62440/4A0/4C0/480 Instruction set (2)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~i0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~i0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X)←*l*3~*l*0, M(X+1)←*l*7~*l*4, X←X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ←1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ←0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP←SP-1, M(SP)←r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP←SP-1, M(SP)←XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP←SP-1, M(SP)←XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP←SP-1, M(SP)←XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP←SP-1, M(SP)←YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP←SP-1, M(SP)←YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP←SP-1, M(SP)←YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP←SP-1, M(SP)←F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP←M(SP), SP←SP+1

S1C62440/4A0/4C0/480 Instruction set (3)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL← M(SP), SP← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F← M(SP), SP← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★	↕	↕		7	r← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★	↕	↕		7	r← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★	↕	↕		7	r← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★	↕	↕		7	r← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★	↕	↕		7	r← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∧ i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0		↕			7	r← r∧ q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0		↕			7	r← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0		↕			7	r← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0		↕			7	r← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0		↕			7	r← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0		↕	↕		7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0		↕	↕		7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0		↕			7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0		↕			7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0		↕	↕		7	d3← d2, d2← d1, d1← d0, d0← C, C← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0		↕	↕		5	d3← C, d2← d3, d1← d2, d0← d1, C← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0		↕	↕		7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★	↕	↕		7	M(X) ← M(X)-r-C, X← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★	↕	↕		7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1		↕			7	r← $\overline{r}$

Abbreviations used in the explanations have the following meanings.

Symbols associated with registers and memory

A ..... A register
B ..... B register
X ..... XHL register (low order eight bits of index register IX)
Y ..... YHL register (low order eight bits of index register IY)
XH ..... XH register (high order four bits of XHL register)
XL ..... XL register (low order four bits of XHL register)
YH ..... YH register (high order four bits of YHL register)
YL ..... YL register (low order four bits of YHL register)
XP ..... XP register (high order four bits of index register IX)
YP ..... YP register (high order four bits of index register IY)
SP ..... Stack pointer SP
SPH ..... High-order four bits of stack pointer SP
SPL ..... Low-order four bits of stack pointer SP
MX, M(X) .. Data memory whose address is specified with index register IX
MY, M(Y)... Data memory whose address is specified with index register IY
Mn, M(n) .. Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP) ..... Data memory whose address is specified with stack pointer SP
r, q ..... Two-bit register code
r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Registers specified
r1	r0	q1	q0	
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP ..... New bank pointer
NPP ..... New page pointer
PCB ..... Program counter bank
PCP ..... Program counter page
PCS ..... Program counter step
PCSH .. Four high order bits of PCS
PCSL ... Four low order bits of PCS

Symbols associated with flags

F ..... Flag register (I, D, Z, C)
C ..... Carry flag
Z ..... Zero flag
D ..... Decimal flag
I ..... Interrupt flag
↓ ..... Flag reset
↑ ..... Flag set
↕ ..... Flag set or reset

Associated with immediate data

p ..... Five-bit immediate data or label 00H–1FH
s ..... Eight-bit immediate data or label 00H–0FFH
l ..... Eight-bit immediate data 00H–0FFH
i ..... Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+ ..... Add
- ..... Subtract
∧ ..... Logical AND
∨ ..... Logical OR
∀ ..... Exclusive-OR
★ ..... Add-subtract instruction for decimal operation when the D flag is set

APPENDIX C PSEUDO-INSTRUCTION TABLE OF THE CROSS ASSEMBLER

Item No.	Pseudo-instruction	Meaning	Example of Use
1	EQU (Equation)	To allocate data to label	ABC EQU 9 BCD EQU ABC+1
2	ORG (Origin)	To define location counter	ORG 100H ORG 256
3	SET (Set)	To allocate data to label (data can be changed)	ABC SET 0001H ABC SET 0002H
4	DW (Define Word)	To define ROM data	ABC DW 'AB' BCD DW 0FFBH
5	PAGE (Page)	To define boundary of page	PAGE 1H PAGE 15
6	SECTION (Section)	To define boundary of section	SECTION
7	BANK (Bank)	To define boundary of bank	BANK 0 BANK 1H
8	END (End)	To terminate assembly	END
9	MACRO (Macro)	To define macro	CHECK 1 CHECK MACRO DATA LOCAL LOOP LOOP CP MX,DATA JP NZ,LOOP ENDM
10	LOCAL (Local)	To make local specification of label during macro definition	
11	ENDM (End Macro)	To end macro definition	

APPENDIX D COMMAND TABLE OF ICE

Item No.	Function	Command Format	Outline of Operation
1	Assemble	#A,a ↵	Assemble command mnemonic code and store at address "a"
2	Disassemble	#L,a1,a2 ↵	Contents of addresses a1 to a2 are disassembled and displayed
3	Dump	#DP,a1,a2 ↵	Contents of program area a1 to a2 are displayed
		#DD,a1,a2 ↵	Content of data area a1 to a2 are displayed
4	Fill	#FP,a1,a2,d ↵	Data d is set in addresses a1 to a2 (program area)
		#FD,a1,a2,d ↵	Data d is set in addresses a1 to a2 (data area)
5	Set Run Mode	#G,a ↵	Program is executed from the "a" address
		#TIM ↵	Execution time and step counter selection
		#OTF ↵	On-the-fly display selection
6	Trace	#T,a,n ↵	Executes program while displaying results of step instruction from "a" address
		#U,a,n ↵	Displays only the final step of #T,a,n
7	Break	#BA,a ↵	Sets Break at program address "a"
		#BAR,a ↵	Breakpoint is canceled
		#BD ↵	Break condition is set for data RAM
		#BDR ↵	Breakpoint is canceled
		#BR ↵	Break condition is set for Evaluation Board CPU internal registers
		#BRR ↵	Breakpoint is canceled
		#BM ↵	Combined break conditions set for program data RAM address and registers
		#BMR ↵	Cancel combined break conditions for program data ROM address and registers
		#BRES ↵	All break conditions canceled
		#BC ↵	Break condition displayed
		#BE ↵	Enter break enable mode
		#BSYN ↵	Enter break disable mode
		#BT ↵	Set break stop/trace modes
		#BRKSEL,REM ↵	Set BA condition clear/remain modes
8	Move	#MP,a1,a2,a3 ↵	Contents of program area addresses a1 to a2 are moved to addresses a3 and after
		#MD,a1,a2,a3 ↵	Contents of data area addresses a1 to a2 are moved to addresses a3 and after
9	Data Set	#SP,a ↵	Data from program area address "a" are written to memory
		#SD,a ↵	Data from data area address "a" are written to memory
10	Change CPU Internal Registers	#DR ↵	Display Evaluation Board CPU internal registers
		#SR ↵	Set Evaluation Board CPU internal registers
		#I ↵	Reset Evaluation Board CPU
		#DXY ↵	Display X, Y, MX and MY
		#SXY ↵	Set data for X and Y display and MX, MY

Item No.	Function	Command Format	Outline of Operation
11	History	#H,p1,p2 ↵	Display history data for pointer 1 and pointer 2
		#HB ↵	Display upstream history data
		#HG ↵	Display 21 line history data
		#HP ↵	Display history pointer
		#HPS,a ↵	Set history pointer
		#HC,S/C/E ↵	Sets up the history information acquisition before (S), before/after (C) and after (E)
		#HA,a1,a2 ↵	Sets up the history information acquisition from program area a1 to a2
		#HAR,a1,a2 ↵	Sets up the prohibition of the history information acquisition from program area a1 to a2
		#HAD ↵	Indicates history acquisition program area
		#HS,a ↵	Retrieves and indicates the history information which executed a program address "a"
		#HSW,a ↵ #HSR,a ↵	Retrieves and indicates the history information which wrote or read the data area address "a"
12	File	#RF,file ↵	Move program file to memory
		#RFD,file ↵	Move data file to memory
		#VF,file ↵	Compare program file and contents of memory
		#VFD,file ↵	Compare data file and contents of memory
		#WF,file ↵	Save contents of memory to program file
		#WFD,file ↵	Save contents of memory to data file
		#CL,file ↵	Load ICE set condition from file
		#CS,file ↵	Save ICE set condition to file
13	Coverage	#CVD ↵	Indicates coverage information
		#CVR ↵	Clears coverage information
14	ROM Access	#RP ↵	Move contents of ROM to program memory
		#VP ↵	Compare contents of ROM with contents of program memory
		#ROM ↵	Set ROM type
15	Terminate ICE	#Q ↵	Terminate ICE and return to operating system control
16	Command Display	#HELP ↵	Display ICE instruction
17	Self Diagnosis	#CHK ↵	Report results of ICE self diagnostic test

↵ means press the RETURN key.

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