EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER
S1C6S480
Technical Manual
S1C6S480 Technical Hardware
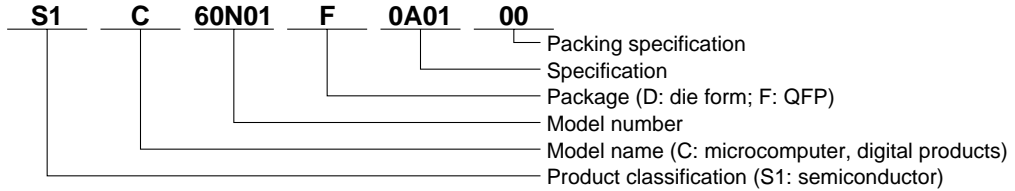
ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

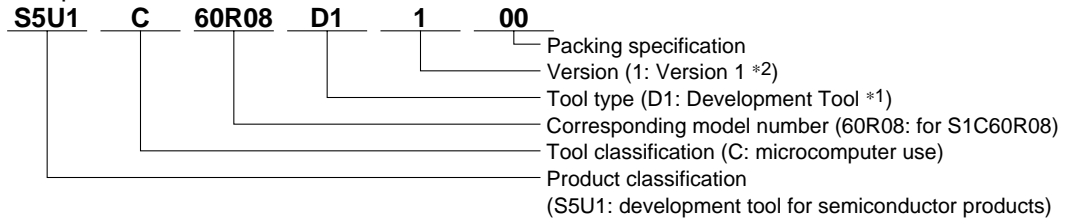## The information of the product number change

Starting April 1, 2001, the product number will be changed as listed below. To order from April 1, 2001 please use the new product number. For further information, please contact Epson sales representative.

Configuration of product number

Devices

```
S1    C    60N01    F    0A01    00
```
- Packing specification
- Specification
- Package (D: die form; F: QFP)
- Model number
- Model name (C: microcomputer, digital products)
- Product classification (S1: semiconductor)

Development tools

```
S5U1    C    60R08    D1    1    00
```
- Packing specification
- Version (1: Version 1 *2)
- Tool type (D1: Development Tool *1)
- Corresponding model number (60R08: for S1C60R08)
- Tool classification (C: microcomputer use)
- Product classification
  (S5U1: development tool for semiconductor products)

*1: For details about tool types, see the tables below. (In some manuals, tool types are represented by one digit.)
*2: Actual versions are not written in the manuals.

Comparison table between new and previous number

S1C60 Family processors

Previous No.	New No.
E0C6001	S1C60N01
E0C6002	S1C60N02
E0C6003	S1C60N03
E0C6004	S1C60N04
E0C6005	S1C60N05
E0C6006	S1C60N06
E0C6007	S1C60N07
E0C6008	S1C60N08
E0C6009	S1C60N09
E0C6011	S1C60N11
E0C6013	S1C60N13
E0C6014	S1C60140
E0C60R08	S1C60R08

S1C62 Family processors

Previous No.	New No.	Previous No.	New No.
E0C621A	S1C621A0	E0C6247	S1C62470
E0C6215	S1C62150	E0C6248	S1C62480
E0C621C	S1C621C0	E0C6S48	S1C6S480
E0C6S27	S1C6S2N7	E0C624C	S1C624C0
E0C6S37	S1C6S3N7	E0C6251	S1C62N51
E0C623A	S1C6N3A0	E0C6256	S1C62560
E0C623E	S1C6N3E0	E0C6292	S1C62920
E0C6S32	S1C6S3N2	E0C6262	S1C62N62
E0C6233	S1C62N33	E0C6266	S1C62660
E0C6235	S1C62N35	E0C6274	S1C62740
E0C623B	S1C6N3B0	E0C6281	S1C62N81
E0C6244	S1C62440	E0C6282	S1C62N82
E0C624A	S1C624A0	E0C62M2	S1C62M20
E0C6S46	S1C6S460	E0C62T3	S1C62T30

Comparison table between new and previous number of development tools

Development tools for the S1C60/62 Family

Previous No.	New No.	Previous No.	New No.	Previous No.	New No.
ASM62	S5U1C62000A	DEV6262	S5U1C62620D	EVA623B	S5U1C623B0E
DEV6001	S5U1C60N01D	DEV6266	S5U1C62660D	EVA623E	S5U1C623E0E
DEV6002	S5U1C60N02D	DEV6274	S5U1C62740D	EVA6247	S5U1C62470E
DEV6003	S5U1C60N03D	DEV6292	S5U1C62920D	EVA6248	S5U1C62480E
DEV6004	S5U1C60N04D	DEV62M2	S5U1C62M20D	EVA6251R	S5U1C62N51E1
DEV6005	S5U1C60N05D	DEV6233	S5U1C62N33D	EVA6256	S5U1C62N56E
DEV6006	S5U1C60N06D	DEV6235	S5U1C62N35D	EVA6262	S5U1C62620E
DEV6007	S5U1C60N07D	DEV6251	S5U1C62N51D	EVA6266	S5U1C62660E
DEV6008	S5U1C60N08D	DEV6256	S5U1C62560D	EVA6274	S5U1C62740E
DEV6009	S5U1C60N09D	DEV6281	S5U1C62N81D	EVA6281	S5U1C62N81E
DEV6011	S5U1C60N11D	DEV6282	S5U1C62N82D	EVA6282	S5U1C62N82E
DEV60R08	S5U1C60R08D	DEV6S27	S5U1C6S2N7D	EVA62M1	S5U1C62M10E
DEV621A	S5U1C621A0D	DEV6S32	S5U1C6S3N2D	EVA62T3	S5U1C62T30E
DEV621C	S5U1C621C0D	DEV6S37	S5U1C6S3N7D	EVA6S27	S5U1C6S2N7E
DEV623B	S5U1C623B0D	EVA6008	S5U1C60N08E	EVA6S32R	S5U1C6S3N2E2
DEV6244	S5U1C62440D	EVA6011	S5U1C60N11E	ICE62R	S5U1C62000H
DEV624A	S5U1C624A0D	EVA621AR	S5U1C621A0E2	KIT6003	S5U1C60N03K
DEV624C	S5U1C624C0D	EVA621C	S5U1C621C0E	KIT6004	S5U1C60N04K
DEV6248	S5U1C62480D	EVA6237	S5U1C62N37E	KIT6007	S5U1C60N07K
DEV6247	S5U1C62470D	EVA623A	S5U1C623A0E		

CONTENTS

CHAPTER 1   OUTLINE

The S1C6S480 is a microcomputer with a C-MOS 4-bit core CPU S1C6200 as main component, and ROM, RAM, dot matrix LCD driver, time base counter, clock synchronous serial interface, etc. built-in. Since the S1C6S480 can be driven with low voltage, it is suitable for portable equipment requiring dot matrix display functions.

The S1C6S480 is a smakker version of the S1C62480 and except for external memory access function, it has the same functions as the S1C62480. Thus it can be used for applications of the S1C62480 that do not need external memory. Note the following structure and characteristics differences between the S1C6S480 and the S1C62480.

Pad size and layout: Size 100 µm   Pitch 130 µm (Min.)
Electrical characteristics: External resistor value for CR oscillation (built-in capacitor is modified)
CR and ceramic oscillation start times
Low-level output current from output ports
Refer to Chapter 14, "Electrical Characteristics".

1.1   Features

Oscillation circuit .... OSC1: 32.768 kHz (Typ.) Crystal or CR oscillation circuit (∗1)
OSC3: 2 MHz (Max.)   CR or ceramic oscillation circuit (∗1)

Instruction set .... 108 types

Instruction execution time .... 32.768 kHz: 152.6 µsec   213.6 µsec   366.2 µsec
(differ depending on the instruction) 1 MHz: 5.0 µsec   7.0 µsec   12.0 µsec
2 MHz: 2.5 µsec   3.5 µsec   6.0 µsec

ROM capacity .... 8,192 words × 12 bits

RAM capacity .... Data memory: 768 words × 4 bits
Display memory: 204 words × 4 bits

Input port... 8 bits   (Pull-up resistors may be supplemented ∗1)

Output port .... 20 bits (Buzzer and clock outputs are possible ∗1)

I/O port .... 16 bits

Serial interface .... 8-bit clock synchronous system × 1 ch.

Dot matrix type LCD driver .... 51 segments × 16 or 8 commons (∗2)

Time base counter .... Clock timer, stopwatch timer

Programmable timer .... 8-bit timer × 1 ch., with event counter and clock output functions

Watchdog timer .... Built-in

Sound generator .... 8 programmable sounds (8 types of frequency)
with envelope and 1-shot output functions

Supply voltage detection (SVD) .... -2.2, -2.5, -3.1, -4.2 V programmable (V$_{DD}$ standard)

External interrupt .... Input port interrupt: 2 systems

Internal interrupt .... Clock timer interrupt: 1 system
Stopwatch timer interrupt: 1 system
Programmable timer interrupt: 1 system
Serial interface interrupt: 1 system

Power supply voltage .... 2.2 V to 5.5 V (Min. 1.8 V when the OSC3 oscillation circuit is not used)

Operating temperature range .... -20°C to 70°C

Current consumption (Typ.) .... During HALT: 32.768 kHz (crystal oscillation), 3.0 V   2.5 µA
During operation: 32.768 kHz (crystal oscillation), 3.0 V   6.5 µA
2 MHz (CR oscillation), 3.0 V   1 mA

Package .... QFP8-144pin (plastic) or chip

∗1: Can be selected with mask option   ∗2: Can be selected with software

1.2 Block Diagram
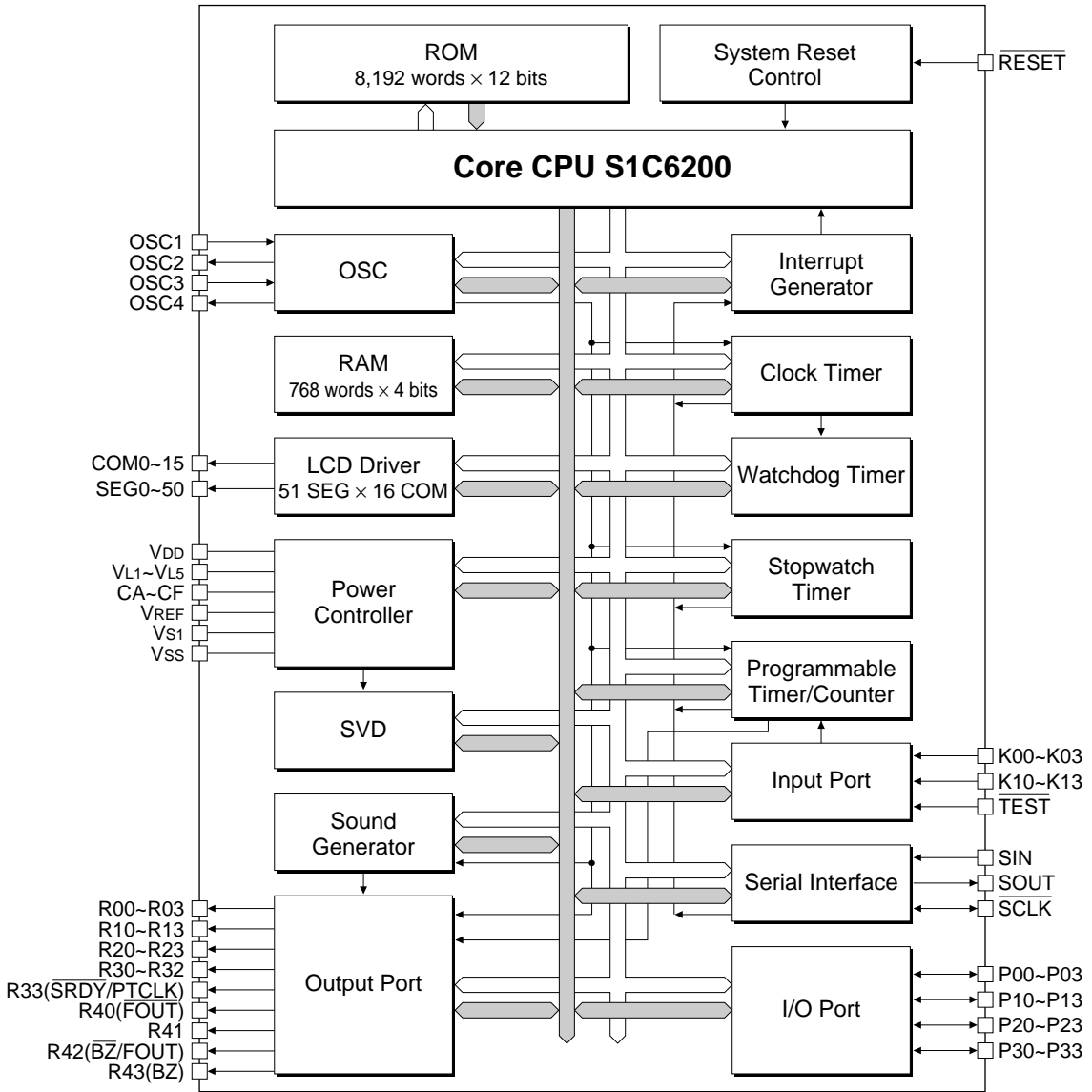
Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP8-144pin
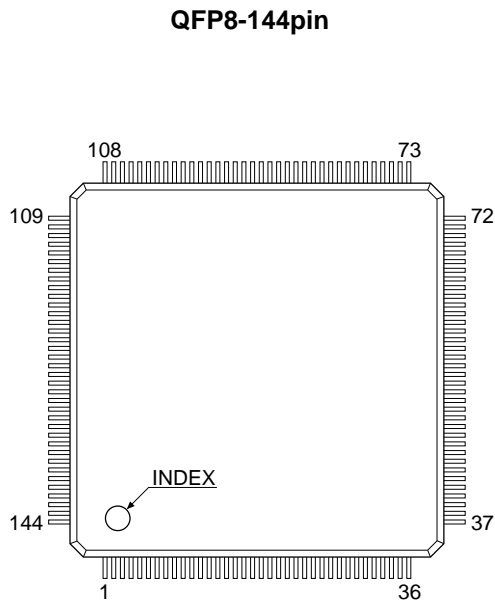
No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	CB	37	SEG36	73	SEG1	109	R33
2	CA	38	SEG35	74	SEG0	110	R32
3	N.C.	39	SEG34	75	N.C.	111	R31
4	COM0	40	SEG33	76	$\overline{\text{SCLK}}$	112	R30
5	COM1	41	SEG32	77	SOUT	113	R23
6	COM2	42	SEG31	78	SIN	114	R22
7	COM3	43	SEG30	79	K13	115	R21
8	COM4	44	SEG29	80	K12	116	R20
9	COM5	45	SEG28	81	K11	117	R13
10	COM6	46	SEG27	82	K10	118	R12
11	COM7	47	SEG26	83	K03	119	R11
12	COM8	48	SEG25	84	N.C.	120	R10
13	COM9	49	SEG24	85	K02	121	R03
14	COM10	50	N.C.	86	K01	122	R02
15	COM11	51	SEG23	87	K00	123	R01
16	COM12	52	SEG22	88	P33	124	R00
17	COM13	53	SEG21	89	P32	125	V_{SS}
18	COM14	54	SEG20	90	P31	126	$\overline{\text{RESET}}$
19	N.C.	55	SEG19	91	P30	127	$\overline{\text{TEST}}$
20	COM15	56	SEG18	92	P23	128	OSC4
21	SEG50	57	SEG17	93	P22	129	OSC3
22	SEG49	58	SEG16	94	P21	130	V_{S1}
23	SEG48	59	SEG15	95	P20	131	OSC2
24	SEG47	60	SEG14	96	P13	132	OSC1
25	SEG46	61	SEG13	97	N.C.	133	N.C.
26	SEG45	62	SEG12	98	P12	134	V_{DD}
27	SEG44	63	SEG11	99	P11	135	V_{REF}
28	SEG43	64	SEG10	100	P10	136	V_{L1}
29	SEG42	65	SEG9	101	P03	137	V_{L2}
30	SEG41	66	SEG8	102	P02	138	V_{L3}
31	SEG40	67	SEG7	103	P01	139	V_{L4}
32	SEG39	68	SEG6	104	P00	140	V_{L5}
33	SEG38	69	SEG5	105	R43	141	CF
34	SEG37	70	SEG4	106	R42	142	CE
35	N.C.	71	SEG3	107	R41	143	CD
36	N.C.	72	SEG2	108	R40	144	CC

N.C.: No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function	
V$_{DD}$	134	–	Power supply (+)	
V$_{SS}$	125	–	Power supply (-)	
V$_{S1}$	130	–	Internal logic system/oscillation system regulated voltage output	
V$_{L1}$–V$_{L5}$	136–140	–	LCD system power supply 1/4 bias generated internally, 1/5 bias generated externally *1	
V$_{REF}$	135	O	LCD system power test pin *2	
CA–CF	2, 1, 144–141	–	LCD system voltage booster condenser connecting pin	
OSC1	132	I	Crystal or CR oscillator input *1	
OSC2	131	O	Crystal or CR oscillator output *1, C$_D$ buiil-in	
OSC3	129	I	CR or ceramic oscillator input *1	
OSC4	128	O	CR or ceramic oscillator output *1	
COM0–COM15	4–18, 20	O	LCD common output (1/8 duty or 1/16 duty is selected on software)	
SEG0–SEG50	74–51, 49–37, 34–21	O	LCD segment output	
K00–K03	87–85, 83	I	Input port (pull up resistor is available by mask option) *1	
K10–K13	82–79	I	Input port (pull up resistor is available by mask option) *1	
P00–P03	104–101	I/O	I/O port	Complementary output or Nch open drain output *1
P10–P13	100–98, 96	I/O	I/O port	
P20–P23	95–92	I/O	I/O port	
P30–P33	91–88	I/O	I/O port or output port *1	
R00–R03	124–121	O	Output port	
R10–R13	120–117	O	Output port	
R20–R23	116–113	O	Output port	
R30–R32	112–110	O	Output port	
R33	109	O	Output port, $\overline{SRDY}$ output or PTCLK output *1	
R40	108	O	Output port or $\overline{FOUT}$ output *1	
R41	107	O	Output port	
R42	106	O	Output port, $\overline{BZ}$ output or FOUT output *1	
R43	105	O	Output port or BZ output *1	
SIN	78	I	Serial interface data input	
SOUT	77	O	Serial interface data output	
$\overline{SCLK}$	76	I/O	Serial interface clock input/output	
$\overline{RESET}$	126	I	Initial reset input terminal	
$\overline{TEST}$	127	I	Testing input terminal *3	

∗1 Selected by mask option

∗2 Leave the V$_{REF}$ pin unconnected (N.C.).

∗3 The $\overline{TEST}$ pin is used when the IC load is being detected. During ordinary operation be certain to connect this pin to V$_{DD}$.

CHAPTER 2   CPU AND BUILT-IN MEMORY

2.1   CPU and Instruction Set

The S1C6S480 uses the 4-bit core CPU S1C6200 for its CPU. It has almost the same register configurations, instructions, and other features as the other family devices which use the S1C6200/6200A/6200B, allowing full use of software assets. The instruction set of the S1C6S480 has 108 types of instructions, all consisting of one word (12 bits).

For detailed information on the CPU and the instruction set, refer to the "S1C6200/6200A Core CPU Manual".

Note, however, that because S1C6S480 does not assume SLEEP operation, the SLP instruction is not available in the S1C6200 instruction set.

The instruction list is shown in Tables 2.1.1(a)–(c).
The following lists the symbols used in the instruction list:

Symbols associated with registers and memory

A	A register
B	B register
X	XHL register
	(low order eight bits of index register IX)
Y	YHL register
	(low order eight bits of index register IY)
XH	XH register
	(high order four bits of XHL register)
XL	XL register
	(low order four bits of XHL register)
YH	YH register
	(high order four bits of YHL register)
YL	YL register
	(low order four bits of YHL register)
XP	XP register
	(high order four bits of index register IX)
YP	YP register
	(high order four bits of index register IY)
SP	Stack pointer SP
SPH	High-order four bits of stack pointer SP
SPL	Low-order four bits of stack pointer SP
MX, M(X)	Data memory whose address is specified with index register IX
MY, M(Y)	Data memory whose address is specified with index register IY
Mn, M(n)	Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP)	Data memory whose address is specified with stack pointer SP
r, q	Two-bit register code
	r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	Four high order bits of PCS
PCSL	Four low order bits of PCS

Symbols associated with flags

F	Flag register (I, D, Z, C)
C	Carry flag
Z	Zero flag
D	Decimal flag
I	Interrupt flag
↓	Flag reset
↑	Flag set
↕	Flag set or reset

Associated with immediate data

p	Five-bit immediate data or label 00H–1FH
s	Eight-bit immediate data or label 00H–0FFH
l	Eight-bit immediate data 00H–0FFH
i	Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+	Add
-	Subtract
∧	Logical AND
∨	Logical OR
∀	Exclusive-OR
★	Add-subtract instruction for decimal operation when the D flag is set

Table 2.1.1(a) Instruction sets (1)

Classification	Mnemonic	Operand	B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C	Clock	Operation
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ←p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ←NBP, PCP ←NPP, PCS ←s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ←NBP, PCP ←NPP, PCS ←s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ←NBP, PCP ←NPP, PCS ←s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ←NBP, PCP ←NPP, PCS ←s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ←NBP, PCP ←NPP, PCS ←s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ←NBP, PCP ←NPP, PCSH ←B, PCSL ←A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ←PCP, M(SP-2) ←PCSH, M(SP-3) ←PCSL+1 SP ←SP-3, PCP ←NPP, PCS ←s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ←PCP, M(SP-2) ←PCSH, M(SP-3) ←PCSL+1 SP ←SP-3, PCP ←0, PCS ←s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ←M(SP), PCSH ←M(SP+1), PCP ←M(SP+2) SP ←SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ←M(SP), PCSH ←M(SP+1), PCP ←M(SP+2) SP ←SP+3, PC ←PC+1
	RETD	l	0	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					12	PCSL ←M(SP), PCSH ←M(SP+1), PCP ←M(SP+2) SP ←SP+3, M(X) ←l3~l0, M(X+1) ←l7~l4, X ←X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ←X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ←Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ←x7~x4, XL ←x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ←y7~y4, YL ←y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ←r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ←r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ←r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ←r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ←r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ←r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ←XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ←XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ←XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ←YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ←YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ←YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ←XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ←XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ←YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ←YL+i3~i0+C

Table 2.1.1(b) Instruction sets (2)

Classification	Mne-monic	Operand	B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C	Clock	Operation
Index	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH–i3~i0
operation		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL–i3~i0
instructions		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH–i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL–i3~i0
Data	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r ← i3~i0
transfer		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r ← q
instructions		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A ← M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B ← M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0) ← A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0) ← B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X) ← i3~i0, X ← X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r ← q, X ← X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y) ← i3~i0, Y ← Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r ← q, Y ← Y+1
	LBPX	MX, *l*	1	0	0	1	*l7*	*l6*	*l5*	*l4*	*l3*	*l2*	*l1*	*l0*					5	M(X) ← *l3*~*l0*, M(X+1) ← *l7*~*l4*, X ← X+2
Flag	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F ← F∨i3~i0
operation	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F ← F∧i3~i0
instructions	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C ← 1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C ← 0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z ← 1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z ← 0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D ← 1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D ← 0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ← 1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ← 0 (Disables Interrupt)
Stack	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP ← SP+1
operation	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP ← SP-1
instructions	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP ← SP-1, M(SP) ← r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP ← SP-1, M(SP) ← XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP ← SP-1, M(SP) ← XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP ← SP-1, M(SP) ← XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP ← SP-1, M(SP) ← YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP ← SP-1, M(SP) ← YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP ← SP-1, M(SP) ← YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP ← SP-1, M(SP) ← F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r ← M(SP), SP ← SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP ← M(SP), SP ← SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH ← M(SP), SP ← SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL ← M(SP), SP ← SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP ← M(SP), SP ← SP+1

Table 2.1.1(c) Instruction sets (3)

Classification	Mne-monic	Operand	B A 9 8	7 6 5 4	3 2 1 0	I D Z C	Clock	Operation
Stack operation instructions	POP	YH	1 1 1 1	1 1 0 1	1 0 0 0		5	YH← M(SP), SP←SP+1
		YL	1 1 1 1	1 1 0 1	1 0 0 1		5	YL← M(SP), SP←SP+1
		F	1 1 1 1	1 1 0 1	1 0 1 0	↕ ↕ ↕ ↕	5	F←M(SP), SP←SP+1
	LD	SPH, r	1 1 1 1	1 1 1 0	0 0 r1 r0		5	SPH← r
		SPL, r	1 1 1 1	1 1 1 1	0 0 r1 r0		5	SPL ← r
		r, SPH	1 1 1 1	1 1 1 0	0 1 r1 r0		5	r← SPH
		r, SPL	1 1 1 1	1 1 1 1	0 1 r1 r0		5	r← SPL
Arithmetic instructions	ADD	r, i	1 1 0 0	0 0 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r←r+i3~i0
		r, q	1 0 1 0	1 0 0 0	r1 r0 q1 q0	★ ↕ ↕	7	r←r+q
	ADC	r, i	1 1 0 0	0 1 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r←r+i3~i0+C
		r, q	1 0 1 0	1 0 0 1	r1 r0 q1 q0	★ ↕ ↕	7	r←r+q+C
	SUB	r, q	1 0 1 0	1 0 1 0	r1 r0 q1 q0	★ ↕ ↕	7	r←r-q
	SBC	r, i	1 1 0 1	0 1 r1 r0	i3 i2 i1 i0	★ ↕ ↕	7	r←r-i3~i0-C
		r, q	1 0 1 0	1 0 1 1	r1 r0 q1 q0	★ ↕ ↕	7	r←r-q-C
	AND	r, i	1 1 0 0	1 0 r1 r0	i3 i2 i1 i0	↕	7	r←r∧i3~i0
		r, q	1 0 1 0	1 1 0 0	r1 r0 q1 q0	↕	7	r←r∧q
	OR	r, i	1 1 0 0	1 1 r1 r0	i3 i2 i1 i0	↕	7	r←r∨i3~i0
		r, q	1 0 1 0	1 1 0 1	r1 r0 q1 q0	↕	7	r←r∨q
	XOR	r, i	1 1 0 1	0 0 r1 r0	i3 i2 i1 i0	↕	7	r←r∀i3~i0
		r, q	1 0 1 0	1 1 1 0	r1 r0 q1 q0	↕	7	r←r∀q
	CP	r, i	1 1 0 1	1 1 r1 r0	i3 i2 i1 i0	↕ ↕	7	r-i3~i0
		r, q	1 1 1 1	0 0 0 0	r1 r0 q1 q0	↕ ↕	7	r-q
	FAN	r, i	1 1 0 1	1 0 r1 r0	i3 i2 i1 i0	↕	7	r∧i3~i0
		r, q	1 1 1 1	0 0 0 1	r1 r0 q1 q0	↕	7	r∧q
	RLC	r	1 0 1 0	1 1 1 1	r1 r0 r1 r0	↕ ↕	7	d3 ←d2, d2 ←d1, d1 ←d0, d0 ←C, C← d3
	RRC	r	1 1 1 0	1 0 0 0	1 1 r1 r0	↕ ↕	5	d3 ←C, d2 ←d3, d1 ←d2, d0 ←d1, C← d0
	INC	Mn	1 1 1 1	0 1 1 0	n3 n2 n1 n0	↕ ↕	7	M(n3~n0) ←M(n3~n0)+1
	DEC	Mn	1 1 1 1	0 1 1 1	n3 n2 n1 n0	↕ ↕	7	M(n3~n0) ←M(n3~n0)-1
	ACPX	MX, r	1 1 1 1	0 0 1 0	1 0 r1 r0	★ ↕ ↕	7	M(X) ←M(X)+r+C, X ←X+1
	ACPY	MY, r	1 1 1 1	0 0 1 0	1 1 r1 r0	★ ↕ ↕	7	M(Y) ←M(Y)+r+C, Y ←Y+1
	SCPX	MX, r	1 1 1 1	0 0 1 1	1 0 r1 r0	★ ↕ ↕	7	M(X) ←M(X)-r-C, X← X+1
	SCPY	MY, r	1 1 1 1	0 0 1 1	1 1 r1 r0	★ ↕ ↕	7	M(Y) ←M(Y)-r-C, Y ← Y+1
	NOT	r	1 1 0 1	0 0 r1 r0	1 1 1 1	↕	7	r←r̄

2.2 Program Memory (ROM)

The built-in ROM, a mask ROM for loading the program, has a capacity of 8,192 steps × 12 bits. The program area is two banks, each of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1 of each bank, steps 02H–0CH.
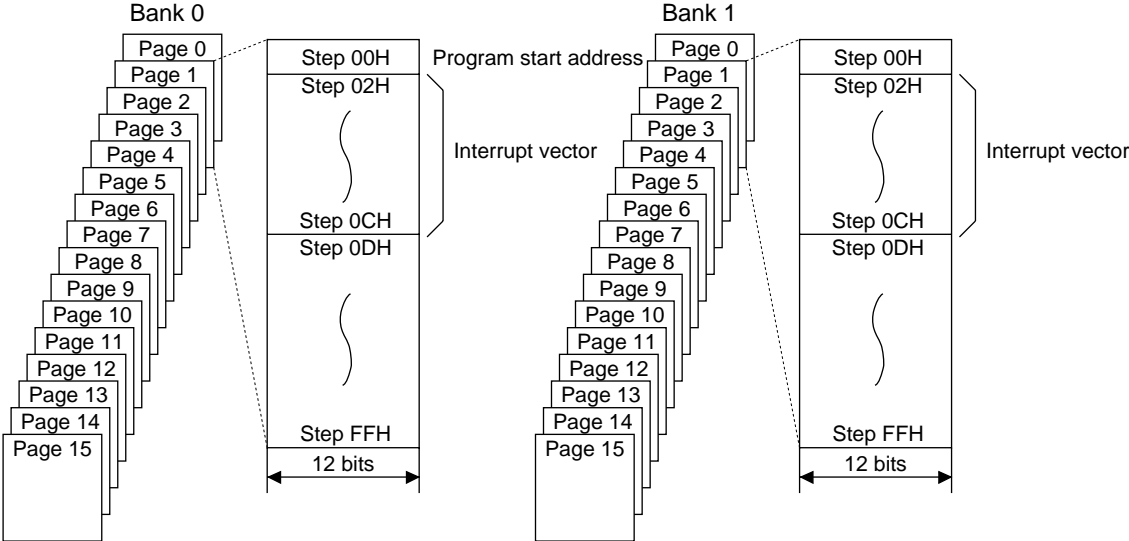
Fig. 2.2.1 Configuration of the built-in ROM

2.3 Data Memory (RAM)

The S1C6S480 built-in data memories are configured a general-purpose RAM, display data memory of the LCD, and I/O data memory which controls the peripheral circuit.

General-purpose RAM: 768 words × 4 bits (000H–2FFH)
Display data memory: 204 words × 4 bits (E00H–E65H, E80H–EF5H)
I/O memory: 48 words × 4 bits (F00H–F7EH)

During programming, take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

The memory map of the built-in data memory (RAM) and details of the I/O data memory map are shown in Figure 2.3.1 and Tables 2.3.1(a)–(d), respectively.

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Address Page	Low High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1–F	RAM (256 words x 4 bits) R/W															
1	0–F	RAM (256 words x 4 bits) R/W															
2	0–F	RAM (256 words x 4 bits) R/W															

Address Page	Low High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0–6	Display data memory (102 words x 4 bits) R/W															
	7	Unused area															
	8–E	Display data memory (102 words x 4 bits) R/W															
	F	Unused area															
F	0–7	I/O memory							Unused area								
	8–F	Unused area															
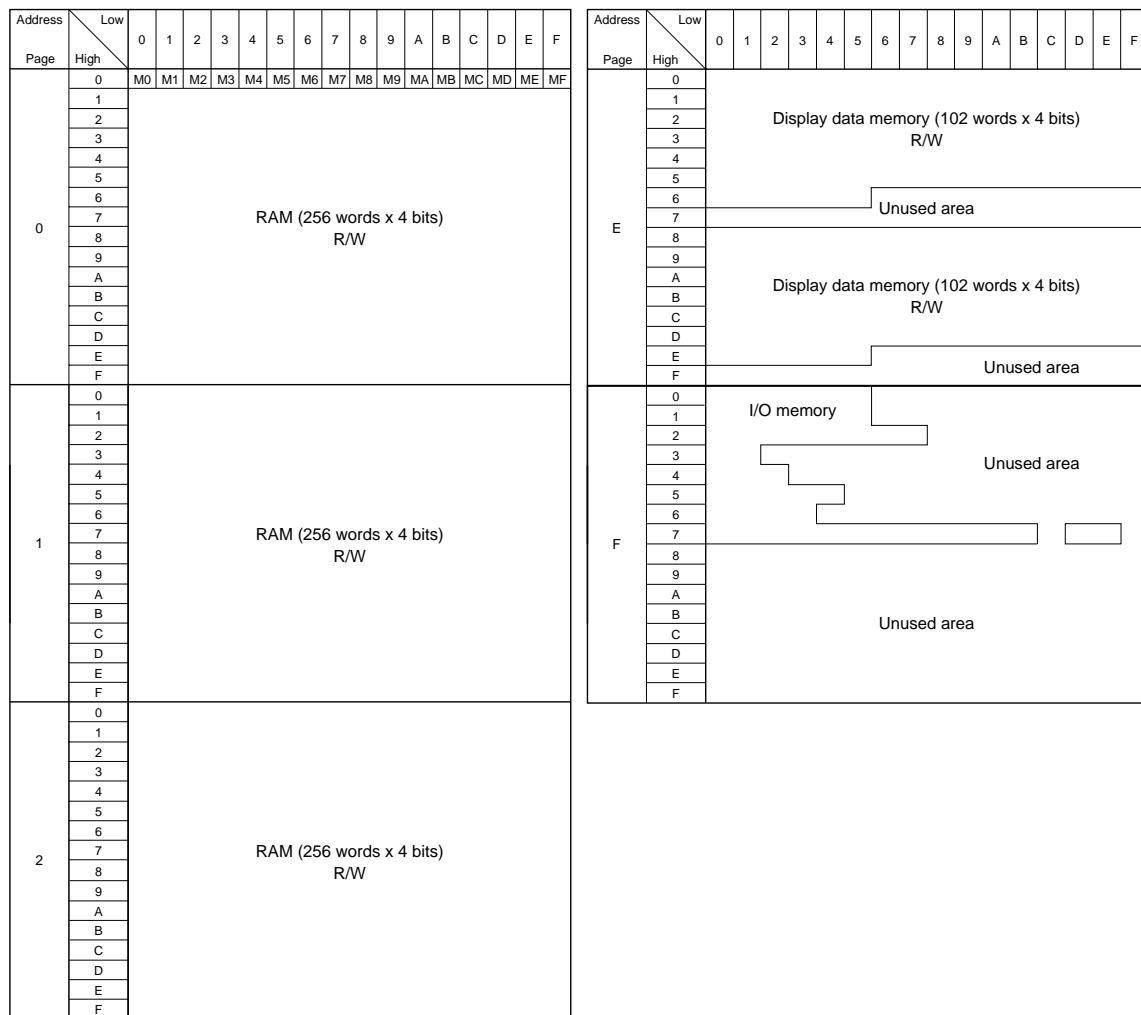
Fig. 2.3.1 Memory map

Table 2.3.1(a) I/O data memory map (1)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32 *3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1 *3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0 *3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F03H	0	0	0	ISIO	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					ISIO *3	0	Yes	No	Interrupt factor flag (serial interface)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0 *3	– *2			
					0 *3	– *2			
	R				0 *3	– *2			
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *3	– *2			
					0 *3	– *2			
	R	R/W			EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *3	– *2			
					0 *3	– *2			
	R	R/W			0 *3	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F13H	0	0	0	EISIO	0 *3	– *2			
					0 *3	– *2			
	R	R/W			0 *3	– *2			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Reset (0) immediately after being read

*4 Always "0" when being read

Table 2.3.1(b) I/O data memory map (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			⌐ MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			⌐ LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			⌐ MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			⌐ LSB
F24H	PT3	PT2	PT1	PT0	PT3	X *3			⌐ MSB
					PT2	X *3			
	R				PT1	X *3			Programmable timer data (low-order)
					PT0	X *3			⌐ LSB
F25H	PT7	PT6	PT5	PT4	PT7	X *3			⌐ MSB
					PT6	X *3			
	R				PT5	X *3			Programmable timer data (high-order)
					PT4	X *3			⌐ LSB
F26H	RD3	RD2	RD1	RD0	RD3	X *3			⌐ MSB
					RD2	X *3			Programmable timer
	R/W				RD1	X *3			reload data (low-order)
					RD0	X *3			⌐ LSB
F27H	RD7	RD6	RD5	RD4	RD7	X *3			⌐ MSB
					RD6	X *3			Programmable timer
	R/W				RD5	X *3			reload data (high-order)
					RD4	X *3			⌐ LSB
F30H	SD3	SD2	SD1	SD0	SD3	X *3			⌐ MSB
					SD2	X *3			Serial interface
	R/W				SD1	X *3			data register (low-order)
					SD0	X *3			⌐ LSB
F31H	SD7	SD6	SD5	SD4	SD7	X *3			⌐ MSB
					SD6	X *3			Serial interface
	R/W				SD5	X *3			data register (high-order)
					SD4	X *3			⌐ LSB
F40H	K03	K02	K01	K00	K03	– *2	High	Low	⌐
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	Input port (K00–K03)
					K00	– *2	High	Low	⌐
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	⌐⌐	⌐⌐	⌐
					DFK02	1	⌐⌐	⌐⌐	
	R/W				DFK01	1	⌐⌐	⌐⌐	Input relation register (DFK00–DFK03)
					DFK00	1	⌐⌐	⌐⌐	⌐
F42H	K13	K12	K11	K10	K13	– *2	High	Low	⌐
					K12	– *2	High	Low	
	R				K11	– *2	High	Low	Input port (K10–K13)
					K10	– *2	High	Low	⌐
F50H	R03	R02	R01	R00	R03	X *3	High	Low	⌐
					R02	X *3	High	Low	
	R/W				R01	X *3	High	Low	Output port (R00–R03)
					R00	X *3	High	Low	⌐
F51H	R13	R12	R11	R10	R13	X *3	High	Low	⌐
					R12	X *3	High	Low	
	R/W				R11	X *3	High	Low	Output port (R10–R13)
					R10	X *3	High	Low	⌐
F52H	R23	R22	R21	R20	R23	X *3	High	Low	⌐
					R22	X *3	High	Low	
	R/W				R21	X *3	High	Low	Output port (R20–R23)
					R20	X *3	High	Low	⌐

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Undefined

Table 2.3.1(c) I/O data memory map (3)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F53H	R33	R32	R31	R30	R33	X *2	High Off *3	Low On *3	Output port (R33) PTCLK output [SRDY (SIO READY)]
	R/W				R32 R31 R30	X *2 X *2 X *2	High High High	Low Low Low	Output port (R30–R32)
F54H	R43	R42	R41	R40	R43	1	High Off	Low On	Output port (R43) Buzzer output (BZ)
	R/W				R42	1	High Off *3	Low On *3	Output port (R42) Clock output (FOUT) [Buzzer inverted output (BZ)]
					R41	1	High	Low	Output port (R41)
					R40	1	High Off	Low On	Output port (R40) Clock inverted output (FOUT)
F60H	P03	P02	P01	P00	P03 P02 P01 P00	X *2 X *2 X *2 X *2	High High High High	Low Low Low Low	I/O port (P00–P03)
	R/W								
F61H	P13	P12	P11	P10	P13 P12 P11 P10	X *2 X *2 X *2 X *2	High High High High	Low Low Low Low	I/O port (P10–P13)
	R/W								
F62H	P23	P22	P21	P20	P23 P22 P21 P20	X *2 X *2 X *2 X *2	High High High High	Low Low Low Low	I/O port (P20–P23)
	R/W								
F63H	P33	P32	P31	P30	P33 P32 P31 P30	X *2 X *2 X *2 X *2	High High High High	Low Low Low Low	I/O port / Dedicated output port (P33) I/O port / Dedicated output port (P32) I/O port / Dedicated output port (P31) I/O port / Dedicated output port (P30)
	R/W								
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG OSCC VSC1 VSC0	0 0 0 0	OSC3 On	OSC1 Off	CPU system clock switch OSC3 oscillation On/Off CPU operating voltage switch
	R/W								
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF ALON LDUTY HLMOD	1 0 0 0	All off All on 1/8 HLMOD	Normal Normal 1/16 Normal	All LCD dots fade out control All LCD dots displayed control LCD drive duty switch Heavy load protection mode
	R/W								
F72H	LC3	LC2	LC1	LC0	LC3 LC2 LC1 LC0	X *2 X *2 X *2 X *2			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
	R/W								
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT SVDON	1 *4 0	Low On	Normal Off	SVD evaluation data SVD circuit On/Off
	R	R/W			SVC1 SVC0	X *2 X *2			SVD criteria voltage setting
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW BZFQ2	0 0	62.5 ms	31.25 ms	1-shot buzzer pulse width
	R/W				BZFQ1 BZFQ0	0 0			Buzzer frequency selection

∗1 Initial value following initial reset

∗2 Undefined

∗3 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs.

∗4 When SVD is off, "1" is read out.

Table 2.3.1(d) I/O data memory map (4)

Address	Register D3	D2	D1	D0	Name	Init*1	1	0	Comment
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger BUSY	– READY	1-shot buzzer trigger (W) / Status (R)
	W	W	R/W		ENVRST	Reset	Reset	–	Envelope reset
	R				ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *3	– *2			
					0 *3	– *2			
	R		W		TMRST*3	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	SWRST*3	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
F78H	0	0	PTRST	PTRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	PTRST*3	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			
	R/W				PTC1	0			Programmable timer input clock selection
					PTC0	0			
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG*3	–	Trigger ⎍	– ⎍	Serial interface clock trigger
					SEN	0	⎍	⎍	Serial interface clock edge selection
	W	R/W			SCS1	0			
					SCS0	0			Serial interface clock mode selection
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3*3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
	R/W				IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
	R/W				PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

∗1 Initial value following initial reset

∗2 Not set in the circuit

∗3 Always "0" when being read

CHAPTER *3*   P*OWER* S*OURCE*

3.1   Power Supply System

The S1C6S480 operating power voltage is as follows:

2.2–5.5 V (Min. 1.8 V, when OSC3 oscillation circuit is not used)

The S1C6S480 operates when a single power supply within the above range is applied between V_{DD} and V_{SS}. Even if the voltage is not within the above range necessary for the internal circuits, the IC itself can generate the following built-in power circuits.

Circuit	Power supply circuit	Output voltage
Oscillation circuit and internal circuits	Regulated voltage circuit	V_{S1}
LCD driver	LCD system voltage circuit	V_{L1}–V_{L5}

Notes: • *V_{L3} is used only when the driving voltage of the LCD system will be supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), it should be shorted with V_{L2}.*

• *See "14 Electrical Characteristics" for voltage values.*
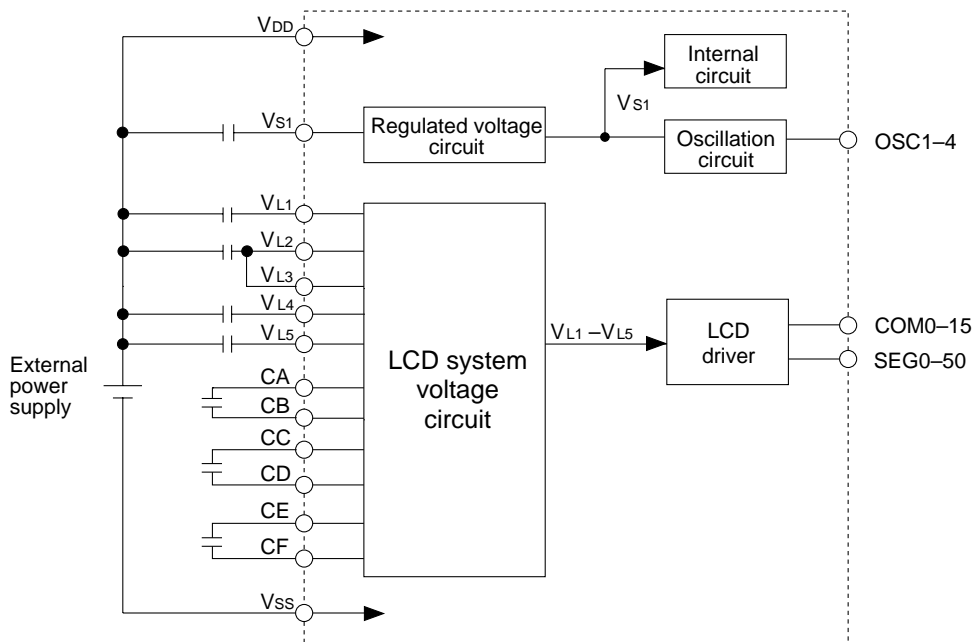
Fig. 3.1.1 Configuration of power supply

3.2 SVD (Supply Voltage Detection) Circuit

3.2.1 Configuration of SVD circuit

The S1C6S480 has a built-in SVD (supply voltage detection) circuit which allows detection of power voltage drop through software.

Turning the SVD operation on and off can be controlled through the software. Because the IC consumes a large amount of current during SVD operation, it is recommended that the SVD operation be kept OFF unless it is otherwise necessary.

Also, the SVD criteria voltage can be set by software. The criteria voltage can be set by matching to one of the 4 types of batteries below that can be used.

-2.2, -2.5, -3.1, -4.2 V (VDD reference voltage)

See "14 Electrical Characteristics" for the precision of the criteria voltage.

Figure 3.2.1.1 shows the configuration of the SVD circuit.

Fig. 3.2.1.1 Configuration of SVD circuit

3.2.2 Control of SVD circuit

The SVD operation control registers are explained below.

Table 3.2.2.1 Control registers of SVD circuit

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X			SVD criteria voltage setting
					SVC0	X			

SVC0 and SVC1 (F73H [D0 and D1], R/W)

Criteria voltage for supply voltage detection is set as shown in Table 3.2.2.2.

Table 3.2.2.2 Criteria voltage for SVD circuit

SVC1	SVC0	Criteria voltage
0	0	-2.2 V
0	1	-2.5 V
1	0	-3.1 V
1	1	-4.2 V

The VDD reference voltage is used as the criteria voltage.
At initial reset, this register becomes undefined.

SVDON (F73H [D2], R/W)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

By writing "1" to the SVDON, the SVD circuit is turned ON, and determination of supply voltage is initiated. Likewise, by writing "0", it is turned OFF.
At initial reset, it is set to "0" (OFF).

Note: The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

SVDDT (F73H [D3], R)

This is the result of supply voltage determination.

When "0" is read: Criteria voltage ≤ Source voltage (V_{DD}–V_{SS})
When "1" is read: Criteria voltage > Source voltage (V_{DD}–V_{SS})
Writing: Invalid

If the SVD circuit is ON, when the voltage of the battery is detected to be lower than the criteria voltage set at SVC0 and SVC1, SVDDT is "1". If it is more than the criteria voltage, it is "0".
The SVDDT reading is valid when SVDON is "1" and is always "1" when SVDON is "0".

Note: To obtain a stable detection result, after setting SVDON to "1", provide at least 100 μs waiting time before performing SVDDT reading.

3.2.3 Programming notes

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 μs waiting time before performing SVDDT reading.

3.3 Heavy Load Protection Mode

Because the load of the battery in the S1C6S480 becomes heavy due to the buzzer, lamp, and other features, it has been equipped with heavy load protection function in case of power voltage drop. This functions works in the heavy load protection mode.
Based on the workings of the heavy load protection function, the S1C6S480 realizes operation at 2.2 V (Min. 1.8 V, when OSC3 oscillation circuit is not used) source voltage.

During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. At the normal mode, the LCD system regulated voltage is created with V_{L2}; V_{L1} is $1/2$ reduced V_{L2} voltage while V_{L4} and V_{L5} are created by boosting to 1.5 and 2 times voltages, respectively. On the other hand, at the heavy load protection mode, the regulated voltage is V_{L1}; V_{L2}, V_{L4}, and V_{L5} are created by boosting to 2, 3 and 4 times voltages. Because of this, the consumed current becomes greater than that in the normal mode, be careful not to set the heavy load protection unless necessary.
The LCD system voltage modes are shown in Table 3.3.1.

Table 3.3.1 LCD system voltage mode

LCD voltage	Normal mode	Heavy load protection mode
V_{L1}	$1/2\ V_{L2}$	V_{L1} regulated voltage
V_{L2}	V_{L2} regulated voltage	$2\ V_{L1}$
V_{L4}	$3/2\ V_{L2}$	$3\ V_{L1}$
V_{L5}	$4/2\ V_{L2}$	$4\ V_{L1}$

3.3.1 Control of heavy load protection mode

The control register for the heavy load protection mode are explained below.

Table 3.3.1.1 Control register for heavy load protection mode

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode

HLMOD (F71H [D0], R/W)
Controls the heavy load protection mode.

When "1" is written: Heavy load protection mode is set
When "0" is written: Heavy load protection mode is released
Reading: Valid

Conversion to heavy load protection mode is done by writing "1" to HLMOD while cancellation of this mode is done by writing "0".
At initial reset, the mode is set to "0" (heavy load protection mode cancellation).

3.3.2 Programming notes

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.2.1.)
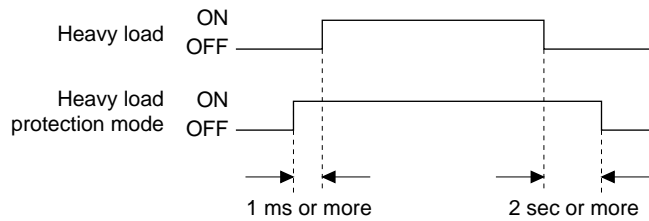
Fig. 3.3.2.1 Control timing for heavy load protection mode

3.4   CPU Operating Voltage Change

During operation, S1C6S480 can change OSC1 and OSC3 system clocks through the software, and operation at clock mode or high-speed mode is then possible. In this case, to obtain stable operating, operating voltage V_{S1} of the internal circuit is changed through the software. For details, see Chapter 5, "Oscillation Circuit".

CHAPTER *4* INITIAL RESET

4.1 Initial Reset Factors

The S1C6S480 requires initial reset function to initialize the circuits.

There are four types of initial reset factors:

(1) External reset through low level input to the $\overline{\text{RESET}}$ terminal

(2) External initial reset by simultaneous low level input of K00–K03 terminals (mask option)

(3) Initial reset by oscillation detector

(4) Initial reset by watchdog timer

Note: The S1C6S480 must be reset after turning power on using the initial reset factor (1) or (2).

Figure 4.1.1 shows the configuration of the initial reset circuit.
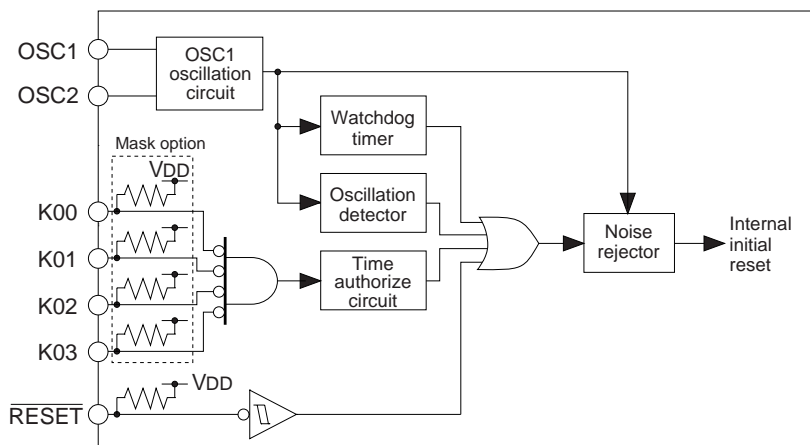
Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 External initial reset by the $\overline{\text{RESET}}$ terminal

Initial resetting can be done externally by placing the reset terminal at low level. When the reset terminal goes high, the CPU will start operating.

Power-on reset

When turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 4.1.1.1.
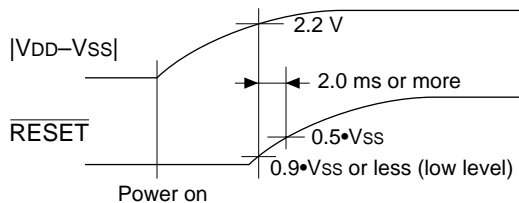
Fig. 4.1.1.1 Initial reset at power on

The reset terminal should be set to $0.9 \cdot \text{Vss}$ or less (low level) until the supply voltage becomes 2.2 V or more. After that, a level of $0.5 \cdot \text{Vss}$ or less should be maintained more than 2.0 ms.

Reset pulse

Because the initial reset circuit has noise rejector built-in, keep it at low level for at least 2 ms (in case oscillation frequency $f_{\text{OSC1}} = 32.768$ kHz).

4.1.2 External initial reset by simultaneous low level input of K00–K03 terminals

Initial reset may be done by simultaneously providing low level input externally to the input port (K00–K03) selected by mask option. Because the initial reset circuit has time authorize circuit built-in, keep the specified input port terminal at Low level for at least 2 seconds (in case oscillation frequency f_{OSC1} = 32.768 kHz). The input port combination which can be selected from the mask option are as follows:

- Not use
- K00∗K01
- K00∗K01∗K02
- K00∗K01∗K02∗K03

4.1.3 Initial reset by oscillation detector

The oscillation detector generates an initial reset signal until the crystal oscillation circuit (OSC1) starts oscillation during power charge.
However, depending on the power-on sequence (voltage rise timing), the circuit may not work properly. Therefore, use the reset terminal or reset by simultaneous low input to the input port (K00–K03) for initial reset after turning power on.

4.1.4 Initial reset by watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See "4.2 Watchdog Timer" for details.

4.1.5 Internal register at initial resetting

The CPU is initialized by initial resetting as follows:

Table 4.1.5.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register X	X	12	Undefined
Index register Y	Y	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	768×4	Undefined
Display memory	204×4	Undefined
Other peripheral circuits	–	∗

∗ See Tables 2.3.1(a)–(d).

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

S1C6S480 has a built-in watchdog timer with OSC1 (clock timer 1 Hz signal) basic oscillation. The watchdog timer needs to be reset periodically through the software, and if not reset within 3–4 seconds, it automatically generates an initial reset signal to the CPU.
Figure 4.2.1.1 shows the configuration of the watchdog timer.
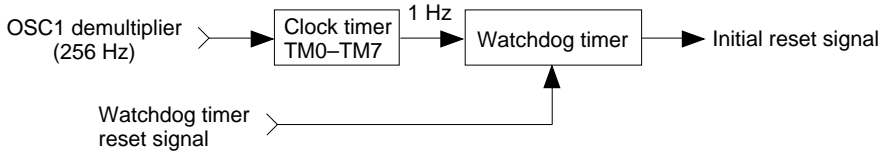
Fig. 4.2.1.1 Configuration of watchdog timer

By resetting the watchdog timer during the program's main routine, program runaways which do not pass the watchdog timer processing during main routine can be detected.
Note, however, that the watchdog timer operates even during HALT such that if the HALT condition continues for 3–4 seconds, it is re-initiated through initial resetting.

4.2.2 Control of watchdog timer

The control register of the watchdog timer is explained below.

Table 4.2.2.1 Control register of watchdog timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F76H	0	0	TMRST	WDRST	0 0	– –			
	R		W		TMRST WDRST	Reset Reset	Reset Reset	– –	Clock timer reset Watchdog timer reset

WDRST (F76H [D0], W)
This bit resets the watchdog timer.

    When "1" is written: Watchdog timer reset
    When "0" is written: No operation
             Reading: Always "0"

By writing "1" on WDRST, the watchdog timer is reset, after which it is immediately restarted. Writing "0" will mean no operation.
Because this bit is only for writing, it is always set to "0" during reading.

4.2.3 Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When the clock timer is reset (TMRST ← "1"), the watchdog timer is counted up; reset the watchdog immediately after if necessary.

CHAPTER 5   OSCILLATION CIRCUIT

5.1   Configuration of Oscillation Circuit

The S1C6S480 has two oscillation circuits (OSC1 and OSC3). OSC1 is either a crystal or a CR oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the S1C6S480 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage V_{S1} must be switched according to the oscillation circuit to be used. Figure 5.1.1 is the block diagram of this oscillation system.
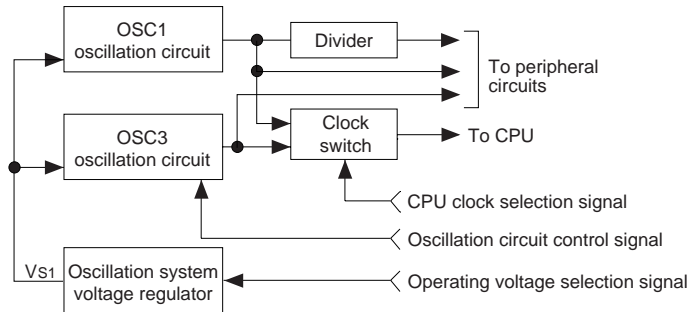
Fig. 5.1.1 Oscillation system block diagram

5.2   OSC1 Oscillation Circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Either the crystal oscillation circuit or the CR oscillation circuit can be selected as the circuit type by mask option. Figure 5.2.1 shows the configuration of the OSC1 oscillation circuit.

(1) Crystal oscillation circuit

(2) CR oscillation circuit
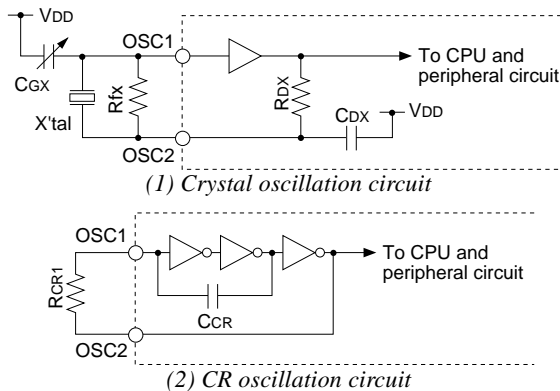
Fig. 5.2.1 OSC1 oscillation circuit

As shown in Figure 5.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) and the feedback resistor Rfx (10 MΩ) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{DD} terminals when crystal oscillation is selected.

When CR oscillation is selected by mask option, connect the resistor R_{CR1} between the OSC1 and OSC2 terminals. See "14 Electrical Characteristics" for resistance value of R_{CR1}.

Notes: • The current consumption of CR oscillation is larger than crystal oscillation.

• Be aware that the CR oscillation frequency changes slightly.
Pay special attention to the circuits that use f_{OSC1} as the source clock, such as the timer (time lag), the LCD frame frequency (display quality, flicker in low frequency) and the sound generator (sound quality).

5.3   OSC3 Oscillation Circuit

The S1C6S480 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 2 MHz) for high speed operation. The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. Figure 5.3.1 shows the configuration of the OSC3 oscillation circuit.

(1) CR oscillation circuit

(2) Ceramic oscillation circuit
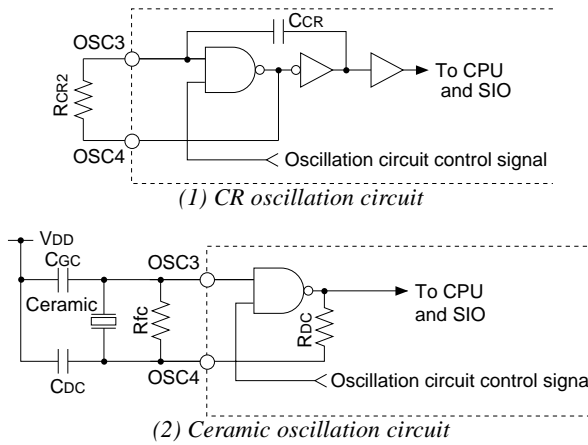
Fig. 5.3.1   OSC3 oscillation circuit

As shown in Figure 5.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See "14 Electrical Characteristics" for resistance value of R_{CR2}.

When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 2 MHz) and the feedback resistor R_{fc} (about 1 MΩ) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{DD} terminals. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

When the OSC3 oscillation circuit is not used, connect the OSC3 terminal to V_{S1}.
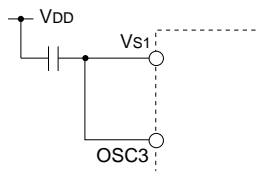
Fig. 5.3.2   Connection diagram when the OSC3 oscillation circuit is unused

5.4   Operating Voltage Change

S1C6S480 can change OSC1 and OSC3 system clocks through the software. In this case, to obtain stable operation, operating voltage V_{S1} of the internal circuit is changed through the software.

Likewise, when selecting OSC1 as the system clock, there is need to change operating voltage V_{S1} according to the value of the power voltage (V_{DD}–V_{SS}).

Oscillation frequency and the corresponding operating voltage V_{S1} are shown in Table 5.4.1.

Table 5.4.1   Oscillation frequency and operating voltage

Oscillation frequency	Oscillation circuit	Operating voltage V_{S1}
32.768 kHz	OSC1	-1.2 V or -2.1 V
1 MHz	OSC3	-2.1 V
2 MHz	OSC3	-3.0 V

The V_{DD} reference voltage is used as the operating voltage V_{S1}.

When OSC3 is to be used as the CPU system clock, change the operating voltage V_{S1} accordingly through the software and then turn the OSC3 oscillation ON and switch the clock frequency.

If the OSC3 oscillation frequency is to be fixed around 1 MHz, set the operating voltage to -2.1 V; at 2 MHz, set the operating voltage to -3.0 V.

Moreover, when the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). However, it can be used fixed at -1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

Note: Switching V_{S1} when the power source voltage is lower than the set voltage may cause misoperation. Perform the operating voltage only after making sure that power voltage by SVD is more than the V_{S1} setting voltage (absolute value).

5.5   Clock Frequency and Instruction Execution Time

Table 5.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 5.5.1   Clock frequency and instruction execution time

Clock frequency	Instruction execution time (µs)		
	5-clock instruction	7-clock instruction	12-clock instruction
32.768 kHz	152.6	213.6	366.2
1 MHz	5.0	7.0	12.0
2 MHz	2.5	3.5	6.0

5.6 Control of Oscillation Circuit

The control registers for the oscillation circuit are explained below.

Table 5.6.1 Control registers of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			

VSC0 and VSC1 (F70H [D0 and D1], R/W)

Switches the operating voltage of the internal circuit in accordance to the oscillation frequency and power source voltage.

The corresponding setting description is shown in Table 5.6.2.

Table 5.6.2 Corresponding between oscillation frequency, power source voltage, and operating voltage (V_{S1})

VSC1	VSC0	V_{S1}	Oscillation circuit	Oscillation frequency	Power source voltage (V_{DD}–V_{SS})
0	0	-1.2 V	OSC1	32.768 kHz	Under 3.1 V
0	1	-2.1 V	OSC1	32.768 kHz	3.1 V or more (∗)
0	1	-2.1 V	OSC3	1 MHz	2.2 V or more
1	×	-3.0 V	OSC3	2 MHz	3.1 V or more

The V_{DD} reference voltage is used as the operating voltage V_{S1}.

There is no need to set the (∗) state with regards to power whose initial value is 3.6 V or less as in lithium batteries.

VSC1 and VSC0 are set to "0" at initial reset.

Notes: • *When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.*

> *(VSC1, VSC0)   = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)*
> *= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)*
>
> *= (0, 0) → (1, ×) is prohibited*
> *= (1, ×) → (0, 0) is prohibited*

> *Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.*

• *When CR oscillation has been selected by the mask option as OSC1, V_{S1} becomes -2.1 V even when VSC1 = VSC0 = 0 and will never become -1.2 V. In addition, since the current consumption is great for CR oscillation compared with the quartz crystal oscillation, when low power consumption is required, you should select quartz crystal oscillation as OSC1.*

OSCC (F70H [D2], R/W)

Controls the oscillation of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When high-speed operation of the CPU is required, OSCC is set to "1"; otherwise, set it to "0" to minimize power current consumption.

At initial reset, OSCC is set to "0".

Note: It takes 5 ms for the OSC3 oscillation circuit to stabilize after oscillation turns ON. Since oscillation stabilization time differs according to external oscillation terminal and usage conditions, set the stand-by time with enough allowance when switching the clock frequency.

CLKCHG (F70H [D3], R/W)
Selects the CPU operating clock.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When assigning OSC3 as the CPU operating clock, set CLKCHG to "1"; when assigning OSC1, set it to "0". At initial reset, CLKCHG is set to "0".

Note: When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

Condition:
$V_{DD} - V_{SS} < -3.1$ V
$V_{S1} = -1.2$ V

Condition:
$V_{S1} = -2.1$ V, OSC3 = 1 MHz (stabilized)
$V_{S1} = -3.0$ V, OSC3 = 2 MHz (stabilized)

CLK CHG

Set V_{S1} to -2.1 V

OSC3 > 500 kHz — N

Y

5 ms WAIT

Set V_{S1} to -3.0 V

OSC3 oscillation ON

5 ms WAIT

CLK OSC1→OSC3

CLK CHG

OSC3 oscillation ON

5 ms WAIT

CLK OSC1→OSC3
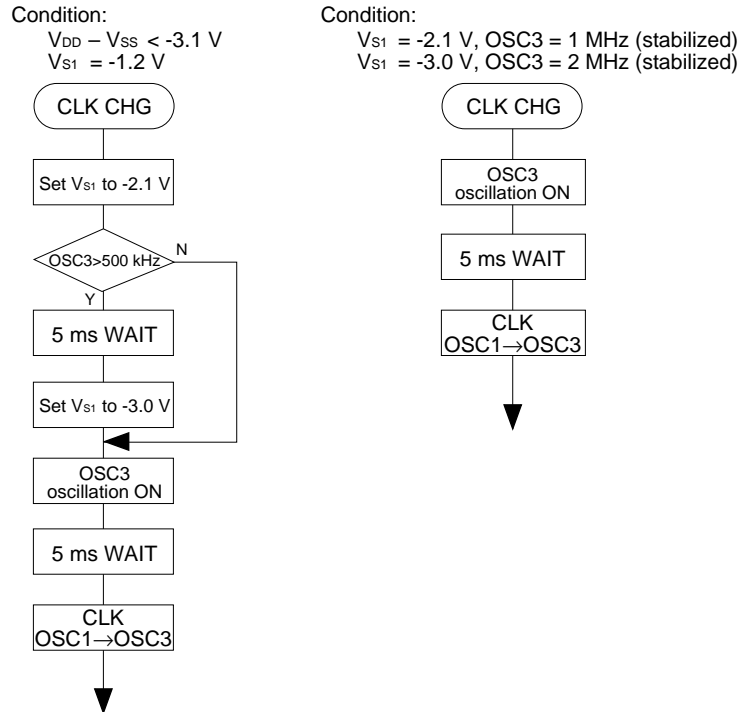
Fig. 5.6.1 CPU operating clock control flow

5.7 *Programming Notes*

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
                = (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

                = (0, 0) → (1, ×) is prohibited
                = (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

CHAPTER 6 INPUT/OUTPUT PORTS

6.1 Input Port (Kxx)

6.1.1 Configuration of input ports

The S1C6S480 has 8 bits (4 bits × 2, K00–K03, K10–K13) general input ports built-in.
Figure 6.1.1.1 shows the configuration of the input port.
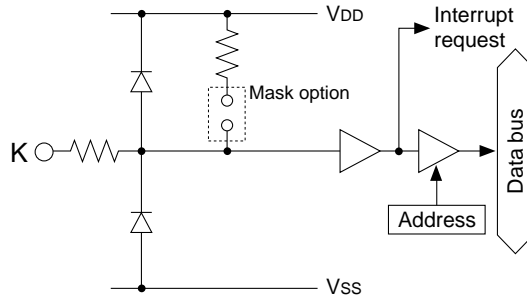
Fig. 6.1.1.1 Configuration of input port

The input port pin K03 is used as the clock input pins for the programmable timer. See "8.3 Programmable Timer" for details.

6.1.2 Mask option

The input ports (K00–K03 and K10–K13) are provided with built-in pull up resistor the use of which may be selected for every bit with the mask option.
Selection of "Pull up resistor enable" with the mask option suits input from the push switch, key matrix, and so forth. When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.
When "Pull up resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that floating state does not occur.

6.1.3 Interrupt function

All eight bits of the input ports K00–K03 and K10–K13 provide the interrupt function.
Whether to mask the interrupt function can be selected individually for all eight bits by the software.

Input interrupt (K00–K03) and input relation registers

The input ports K00–K03 are equipped with input relation registers. The condition for issuing an interrupt can be set by the software.
Figure 6.1.3.1 shows the configuration of the input (K00–K03) interrupt circuit.
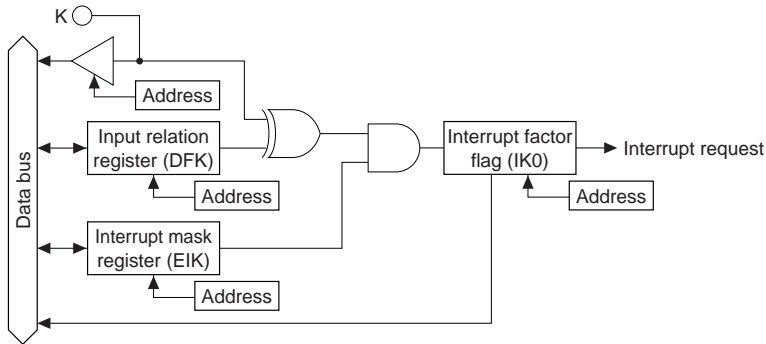
Fig. 6.1.3.1 Configuration of input (K00–K03) interrupt circuit

The input interrupt timing of K00–K03 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input relation registers DFK00–DFK03. Moreover, masking can be set individually to the interrupt of K00–K03. However, if the interrupt of any one of K00–K03 is enabled, interrupt will be generated when the content change from matched to no matched with the input relation register. When interrupt is generated, the interrupt factor flag IK0 is set to "1".
Figure 6.1.3.2 shows an example of an interrupt for K00–K03.
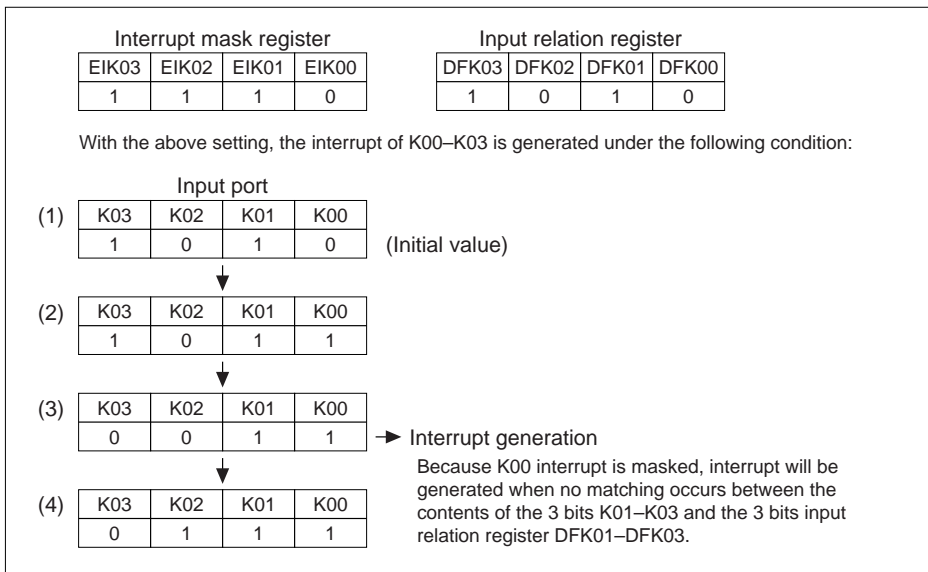
Fig. 6.1.3.2 Example of an interrupt for K00–K03

Because K00 is masked by an interrupt mask register (EIK00), interrupt will not be generated at the above step (2). Next, since K03 becomes "0" at step (3), interrupt is generated due to the no matching of the data of the terminal whose interrupt is enabled and the data of the input relation registers. No interrupt is generated from a no matched state to another no matched state as in step (4) because the condition for interrupt generation, as has been previously stated, is that the port data and the contents of the input relation registers must change from a matched state to a no matched one. Moreover, a terminal whose interrupt is masked will not affect the condition for interrupt generation.

Input interrupt (K10–K13)

Figure 6.1.3.3 shows the configuration of the input (K10–K13) interrupt circuit.
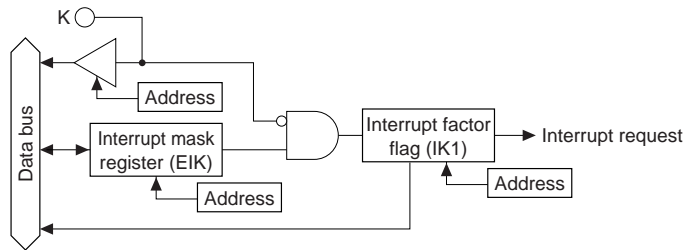
Fig. 6.1.3.3 Configuration of the input (K10–K13) interrupt circuit

There is no input relation registers for K10–K13, and interrupt is fixed to occur at the falling edge of input. The interrupt mask can be selected for each of the four pins with the interrupt mask register EIK10–EIK13. When all the enabled pins are "1", interrupt occurs when one or more of the pins changes to "0".

When interrupt is generated, the interrupt factor flag IK1 is set to "1".

Figure 6.1.3.4 shows an example of an interrupt for K10–K13.
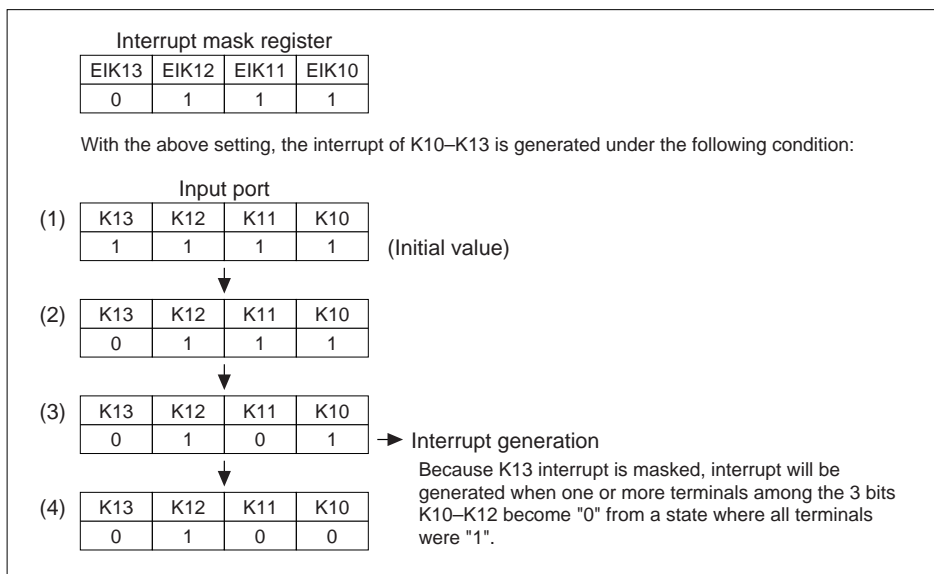
Fig. 6.1.3.4 Example of an interrupt for K10–K13

The mask register (EIK13) masks the interrupt of K13, so an interrupt does not occur at (2). At (3), K11 becomes "0", so that an interrupt occurs if the interrupt enabled pins were all "1" and at least one pin then changes to "0". At (4), the conditions for interrupt are not established, so an interrupt does not occur. Further, pins that have been masked for interrupt do not affect the conditions for interrupt generation.

6.1.4 Control of input ports

The control registers for the input ports are explained below.

Table 6.1.4.1 Control registers of input ports

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F04H	0	0	0	IK0	0	–			
					0	–			
	R				0	–			
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0	–			
					0	–			
	R				0	–			
					IK1	0		No	Interrupt factor flag (K10–K13)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
F40H	K03	K02	K01	K00	K03	–	High	Low	
					K02	–	High	Low	Input port (K00–K03)
	R				K01	–	High	Low	
					K00	–	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	⌐	⌐	
					DFK02	1	⌐	⌐	Input relation register (DFK00–DFK03)
	R/W				DFK01	1	⌐	⌐	
					DFK00	1	⌐	⌐	
F42H	K13	K12	K11	K10	K13	–	High	Low	
					K12	–	High	Low	Input port (K10–K13)
	R				K11	–	High	Low	
					K10	–	High	Low	

K00–K03, K10–K13 (F40H, F42H, R)

Input data of the input port terminal may be read out with these registers.

> When "1" is read: High level
> When "0" is read: Low level
>   Writing: Invalid

The terminal voltage of 8 bits input ports (K00–K03 and K10–K13) are each reading as "1" and "0" at high (VDD) level and low (VSS) level, respectively.
When these bits are used for reading only, writing operation becomes invalid.

DFK00–DFK03 (F41H, R/W)

These input relation registers which set the interrupt generating conditions of K00–K03.

> When "1" is written: Falling edge
> When "0" is written: Rising edge
>   Reading: Valid

When DFK0x is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". DFK0x respectively correspond to input ports K0x and may be set in units of 1 bit.
At initial reset, these registers are all set to "1".

EIK00–EIK03, EIK10–EIK13 (F14H, F15H, R/W)
These are interrupt mask registers of the input ports.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

EIK0x corresponds to input port K0x, and EIK1x corresponds to input port K1x. Whether to mask the interrupt function can be set in units of 1 bit.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IK0, IK1 (F04H [D0], F05H [D0], R)
These are interrupt factor flags of the input ports.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags will not be set even if the input conditions are established if, for every terminal series, the interrupt mask registers (EIKxx) are all set to "0" (i.e., EIK00–EIK03, or EIK10–EIK13 are all set to "0", or all are individually set to "0").
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

6.1.5 Programming notes

(1) When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.

(2) Input interrupt programming related precautions

When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 6.1.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

   input terminal = low status, when the falling edge interrupt is effected and
   input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 6.1.5.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 6.1.5.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.

In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.2 Output Port (Rxx)

6.2.1 Configuration of output ports

The S1C6S480 has 20 bits (4 bits × 5, R00–R03, R10–R13, R20–R23, R30–R33, and R40–R43) general output ports built-in.

Figure 6.2.1.1 shows the configuration of the output port.
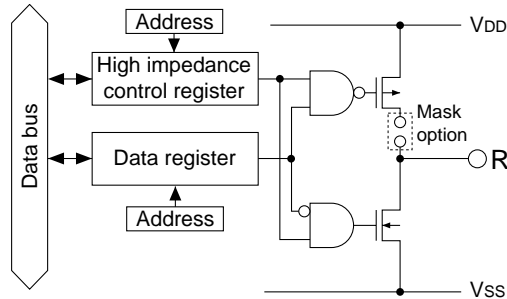
Fig. 6.2.1.1 Configuration of output port

6.2.2 Mask option

The output ports may be selected for the following by mask option.

(1) Output specification of output ports

The output specification of the output ports may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

R00–R03: Complementary or Nch open drain (selected with the 4 bits group)
R10–R13: Complementary or Nch open drain (selected with the 4 bits group)
R20–R22: Complementary or Nch open drain (selected with the 3 bits group)
R23:   Complementary or Nch open drain
R30–R33: Complementary or Nch open drain (select in units of 1 bit)
R40–R43: Complementary or Nch open drain (select in units of 1 bit)

(2) Special output

Output ports R33, R40, R42 and R43 may be selected, in addition to DC output, as special output port as follows:

R33: SIO Ready ($\overline{\text{SRDY}}$) or programmable timer operating clock output (PTCLK)
R40: Clock inverted output ($\overline{\text{FOUT}}$)
R42: Buzzer inverted output ($\overline{\text{BZ}}$) or clock output (FOUT)
R43: Buzzer output (BZ)

Buzzer outputs BZ (R43) and $\overline{BZ}$ (R42)

Through mask option selection, R43 and R42 may be assigned as buzzer outputs. BZ and $\overline{BZ}$ are buzzer signal outputs for driving piezo-electric buzzers, the buzzer signal being created by the division of fOSC1. Moreover, digital envelope may be added to the buzzer signal. See Chapter 10, "Sound Generator" for details.

Buzzer output BZ and $\overline{BZ}$ can be controlled simultaneously by register R43. Note, however, that register R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (output from the R42 terminal).

Notes: • *The BZ and $\overline{BZ}$ output signals could generate hazards during ON/OFF switching.*

• *When output port R43 is set to DC output, output port R42 may not be set to $\overline{BZ}$ output.*

Figure 6.2.2.1 shows the output waveform of BZ and $\overline{BZ}$.
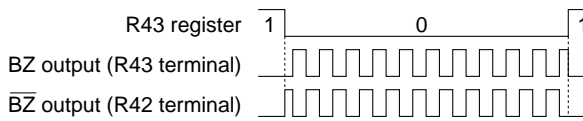
Fig. 6.2.2.1 Output waveform of BZ and $\overline{BZ}$

SIO Ready $\overline{SRDY}$ (R33)

When output port R33 is selected as $\overline{SRDY}$ output, it will generate a Ready signal which will indicate whether the serial interface is available to transmit or receive signals. See Chapter 9, "Serial Interface" for details.

PTCLK (R33)

The operating clock for the programmable timer is output externally from this port. In this case, the clock output ON or OFF may be controlled from the R33 register by setting PTCOUT (F79H [D3]) to "1". The clock frequency is selected by the 3 bits register of PTC0–PTC2.
Moreover, when PTCOUT is set to "0", output port R33 becomes DC output.
Because of the above functions, PTCLK output and DC output belong to a common option selection item. Refer to "8.3 Programmable Timer" regarding selection of clock frequency.

Control of R33 output

3 states output or 2 states output for output port R33 may be selected with the mask option.
When $\overline{SRDY}$ is selected for R33, 2 states output is ordinarily selected in compliance with it.
Moreover, although 2 states output may be selected even during the selection of DC output and PTCLK output, caution is required as output becomes undefined (i.e., it will not be initially reset) when power is supplied.

Clock outputs FOUT (R42), $\overline{FOUT}$ (R40)

When R40 and R42 are selected to clock output, it outputs the clock of fOSC3, fOSC1 or the demultiplied fOSC1. R40 ($\overline{FOUT}$) output generates an antiphase clock in relation to R42 (FOUT). Figure 6.2.2.2 shows the output waveform of FOUT and $\overline{FOUT}$. The clock frequency is selectable with the mask options, from the frequencies listed in Table 6.2.2.1.
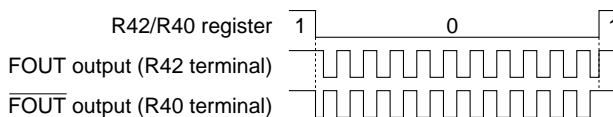
Fig. 6.2.2.2 Output waveform of FOUT and $\overline{FOUT}$

Note: *Clock output signal could generate hazards during ON/OFF switching.*

Table 6.2.2.1 FOUT clock frequency

Setting	Clock frequency (Hz)
f_{OSC3}	OSC3 oscillation frequency
$f_{OSC1}/$ 1	32,768
$f_{OSC1}/$ 2	16,384
$f_{OSC1}/$ 4	8,192
$f_{OSC1}/$ 8	4,096
$f_{OSC1}/$ 16	2,048
$f_{OSC1}/$ 32	1,024
$f_{OSC1}/$ 64	512
$f_{OSC1}/$128	256

6.2.3 High impedance control

The terminal output state of output ports R00–R03, R10–R13, R20–R23, and R30–R33, may be selected for high impedance state through the software in 4 bits groups. Control is done with the high impedance control registers (HZR0–HZR3).

6.2.4 Control of output ports

The control registers for the output ports are explained below.

Table 6.2.4.1 Control registers of output ports

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F50H	R03	R02	R01	R00	R03	X	High	Low	Output port (R00–R03)
					R02	X	High	Low	
	R/W				R01	X	High	Low	
					R00	X	High	Low	
F51H	R13	R12	R11	R10	R13	X	High	Low	Output port (R10–R13)
					R12	X	High	Low	
	R/W				R11	X	High	Low	
					R10	X	High	Low	
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R20–R23)
					R22	X	High	Low	
	R/W				R21	X	High	Low	
					R20	X	High	Low	
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output [$\overline{\text{SRDY}}$ (SIO READY)]
	R/W				R32	X	High	Low	Output port (R30–R32)
					R31	X	High	Low	
					R30	X	High	Low	
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT) [Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control

HZR0–HZR3 (F7BH, R/W)
Controls high impedance loading to output ports R00–R03, R10–13, R20–R23 and R30–R33 in units of 4 bits groups.

> When "1" is written: Data output
> When "0" is written: High impedance
>   Reading: Valid

By writing "1" in the control registers (HZR0–HZR3) corresponding to the groups, the output register data is generated in the terminal; writing "0" will generate high impedance state.
During initial reset, these registers are set to "0" and the ports acquire high impedance state.

When DC output is selected

R00–R03, R10–R13, R20–R23, R30–R33, R40–R43 (F50H, F51H, F52H, F53H, F54H, R/W)
Sets the output data for the output ports.

> When "1" is written: High level
> When "0" is written: Low level
>   Reading: Valid

Output port terminals will generate the data written into the corresponding registers (R00–R03, .. R40–R43) as it is. The output port terminal goes high (V$_{DD}$) when "1" is written to the register, and goes low (V$_{SS}$) when "0" is written.
At initial reset, only R40–R43 are set to "1" and the other output registers become undefined.

When special output is selected

R43 (F54H [D3], R/W) when BZ and $\overline{BZ}$ output is selected
Performs the output control of buzzer signal (BZ, $\overline{BZ}$).

> When "0" is written: Buzzer signal output
> When "1" is written: Low level (DC)
>   Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal; at the same time, $\overline{BZ}$ signal (BZ inverted signal) is generated from R42 terminal if R42 is set to $\overline{BZ}$ output.
When "1" is set on R43, R43 terminal (and R42 terminal too, when $\overline{BZ}$ output is selected) output goes low (V$_{SS}$).
Note, however, that R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (R42 terminal output).
At initial reset, R43 and R42 are set to "1".

R33 (F53H [D3], R/W) when PTCLK (DC) output is selected
Controls the output of the programmable timer operating clock (PTCLK).

> When "0" is written: Clock output
> When "1" is written: High level (DC)
>   Reading: Valid

With "1" written on PTCOUT (F79H [D3]), the operating clock of the programmable timer may be generated externally by writing "0" on R33 register. Moreover, the output will go high (V$_{DD}$) by writing "1". However, when PTCOUT is "0", the output becomes regular DC output.
Because this register is not initialized during initial reset, R33 terminal becomes undefined when 2 states output is selected with mask option.

R40, R42 (F54H [D0, D2], R/W) when FOUT and $\overline{\text{FOUT}}$ output is selected
Controls the FOUT and $\overline{\text{FOUT}}$ (clock) output.

When "0" is written: Clock output
When "1" is written: High level (DC)
　　　　　Reading: Valid

When R42 is set to FOUT output, clock with the specified frequency is generated from R42 terminal by writing "0" on R42 register.
By writing "1", the R42 terminal will go high (VDD).
The same applies to R40. The clock phase when $\overline{\text{FOUT}}$ signal is output from R40 is antiphase to that of R42.
At initial reset, R40 and R42 are set to "1".

6.2.5 Programming notes

(1) When BZ, $\overline{\text{BZ}}$, FOUT, $\overline{\text{FOUT}}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

6.3 I/O Port (Pxx)

6.3.1 Configuration of I/O ports

The S1C6S480 has 16 bits (4 bits × 4, P00–P03, P10–P13, P20–P23, and P30–P33) general I/O ports built-in. Figure 6.3.1.1 shows the configuration of the I/O port.
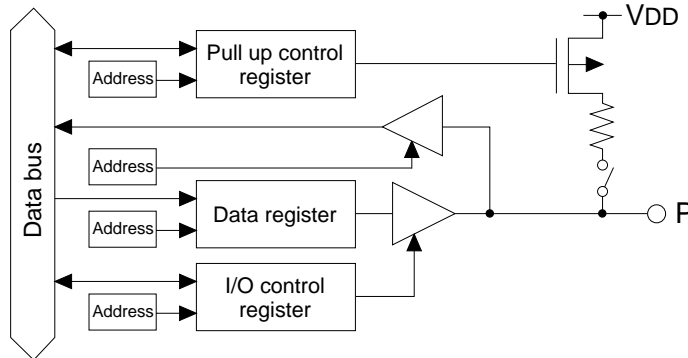
Fig. 6.3.1.1 Configuration of I/O port

6.3.2 Mask option

The following by mask option may be selected for the I/O ports P00–P03, P10–P13, P20–P23, P30–P33.

(1) Output specification during output mode

Output specification (during output) for each I/O port may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

P00–P03: Complementary or Nch open drain (selected with the 4 bits group)
P10–P13: Complementary or Nch open drain (selected with the 4 bits group)
P20–P22: Complementary or Nch open drain (select in units of 1 bit)
P30–P33: Complementary or Nch open drain (select in units of 1 bit)

(2) Dedicated output port

The I/O ports P30–P33 may be set with the mask option as dedicated output ports.
This selection may be conducted by 1 bit.

6.3.3 I/O control register and input/output mode

When using an I/O port as Pxx (x = 0 to 3), input/output direction may be set by group, with 4 bits each of Px0 to Px3 (x = 0 to 3) considered as one group. Modes can be set by writing input/output direction data to the I/O control register corresponding I/O port group.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance state and works as an input port.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (VDD) when the data of output register is "1", and a low level (VSS) when the data of output register is "0".

Setting of the I/O control register is not effective for the ports set as dedicated output through the mask option.

6.3.4 Pull up resistor

The common input/output ports can be selected through the software to apply pull up resistor in 4 bits groups.
Selection of pull up resistor application is done by writing data to the pull up resistor control registers (PUP0–PUP3).

6.3.5 Control of I/O ports

The control registers for the I/O ports are explained below.

Table 6.3.5.1 Control register of I/O ports

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P00–P03)
					P02	X	High	Low	
		R/W			P01	X	High	Low	
					P00	X	High	Low	
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P10–P13)
					P12	X	High	Low	
		R/W			P11	X	High	Low	
					P10	X	High	Low	
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P20–P23)
					P22	X	High	Low	
		R/W			P21	X	High	Low	
					P20	X	High	Low	
F63H	P33	P32	P31	P30	P33	X	High	Low	I/O port / Dedicated output port (P33)
					P32	X	High	Low	I/O port / Dedicated output port (P32)
		R/W			P31	X	High	Low	I/O port / Dedicated output port (P31)
					P30	X	High	Low	I/O port / Dedicated output port (P30)
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
		R/W			IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
		R/W			PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

IOC0, IOC1, IOC2, IOC3 (F7DH, R/W)
Input/output direction of I/O ports are set in units of 4 bits groups.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOCx (I/O control register) and port group correspondence are as follows:

IOC0: P00–P03
IOC1: P10–P13
IOC2: P20–P23
IOC3: P30–P33

By writing "1" to IOCx (x = 0 to 3), the I/O ports in the corresponding group are placed in the output mode, while writing "0" place them in the input mode.
At initial reset, IOCx are set to "0" and the I/O ports are all in the input mode.

PUP0, PUP1, PUP2, PUP3 (F7EH, R/W)

Whether the I/O ports will be pulled up or not is set in units of 4 bits groups.

When "0" is written: Pull up ON
When "1" is written: Pull up OFF
Reading: Valid

PUPx and port group correspondence are the same as that of the IOCx.
By writing "0" to PUPx (x = 0 to 3), the I/O ports in the corresponding group are pulled up, while writing "1" turns the pull up function OFF.
At initial reset, PUPx are set at "0", and all I/O ports are pulled up.

P00–P03, P10–P13, P20–P23, P30–P33 (F60H, F61H, F62H, F63H, R/W)

• **During writing operation**
When "1" is written: High level
When "0" is written: Low level

When the I/O port is set at output port, the data written is generated on the I/O port terminal as it is.
When "1" is written as port data, the port terminal goes high (V_{DD}) and goes low (V_{SS}) when "0" is written.
This is the same when P30–P33 are set as dedicated output ports through the mask option.
Note, however, that even at input mode, port data writing is also possible.

• **During reading operation**
When "1" is read: High level
When "0" is read: Low level

Reading the I/O port terminal voltage level. When the I/O port is at input mode, voltage level input of the port terminal is read; when set at output mode, output voltage level is read. When the terminal voltage is at high (V_{DD}) level, port data reading is "1"; at low (V_{SS}) level, it is "0".

6.3.6 Programming notes

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
   • The input/output mode is set at output mode
   • Output specification is set at Nch open drain
   • The content of the data register is "1"
   • The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

CHAPTER 7 LCD DRIVER

The S1C6S480 has 16 common terminals and 51 segment terminals and can drive a maximum of 816 (51 × 16) dots (10 characters × 2 lines) LCD.

This LCD driver performs the following control through the software.

- Drive duty can be set to 1/16 or 1/8 duty.
- LCD contrast can be adjusted through a 16 steps range.
- All dots of the LCD panel can be switched ON and OFF.

7.1 Drive Duty

Because the power for LCD driving is generated by the internal circuit of the CPU, there is no need to provide for it externally. Driving is done by 1/16 duty or 1/8 duty dynamic drive through 4 electric potentials (1/4 bias) : V_{L1}, V_{L2}, V_{L4}, and V_{L5}. The 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set.

Drive duty may be selected from the software. Dot number differences due to the selected duty are shown in Table 7.1.1.

Table 7.1.1 Differences due to selected duty

Duty	Common terminal in use	Maximum dot number	Frame frequency *
1/16	COM0–15	816 dots	32 Hz
1/8	COM0–7	408 dots	32 Hz

∗ Frame frequency = $f_{OSC1}/1{,}024$

Figure 7.1.1 shows the drive waveform for 1/16 duty (1/5 bias), and Figure 7.1.2 shows the drive waveform for 1/8 duty (1/4 bias).
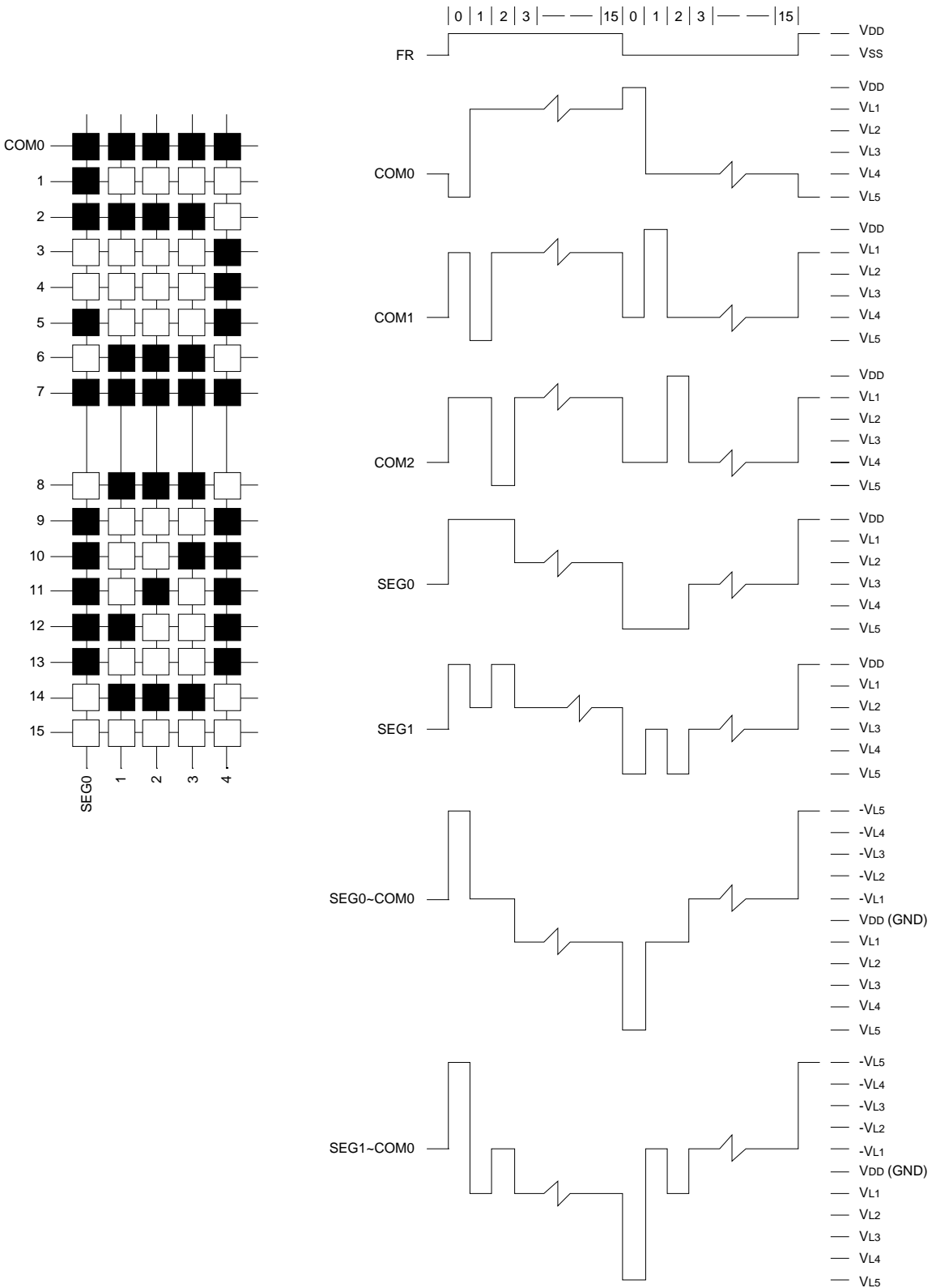
Fig. 7.1.1 Drive waveform for 1/16 duty (1/5 bias)

Note: 1/5 bias may only be utilized when power for LCD driving is supplied externally; when internal power circuit is used, 1/4 bias is utilized.
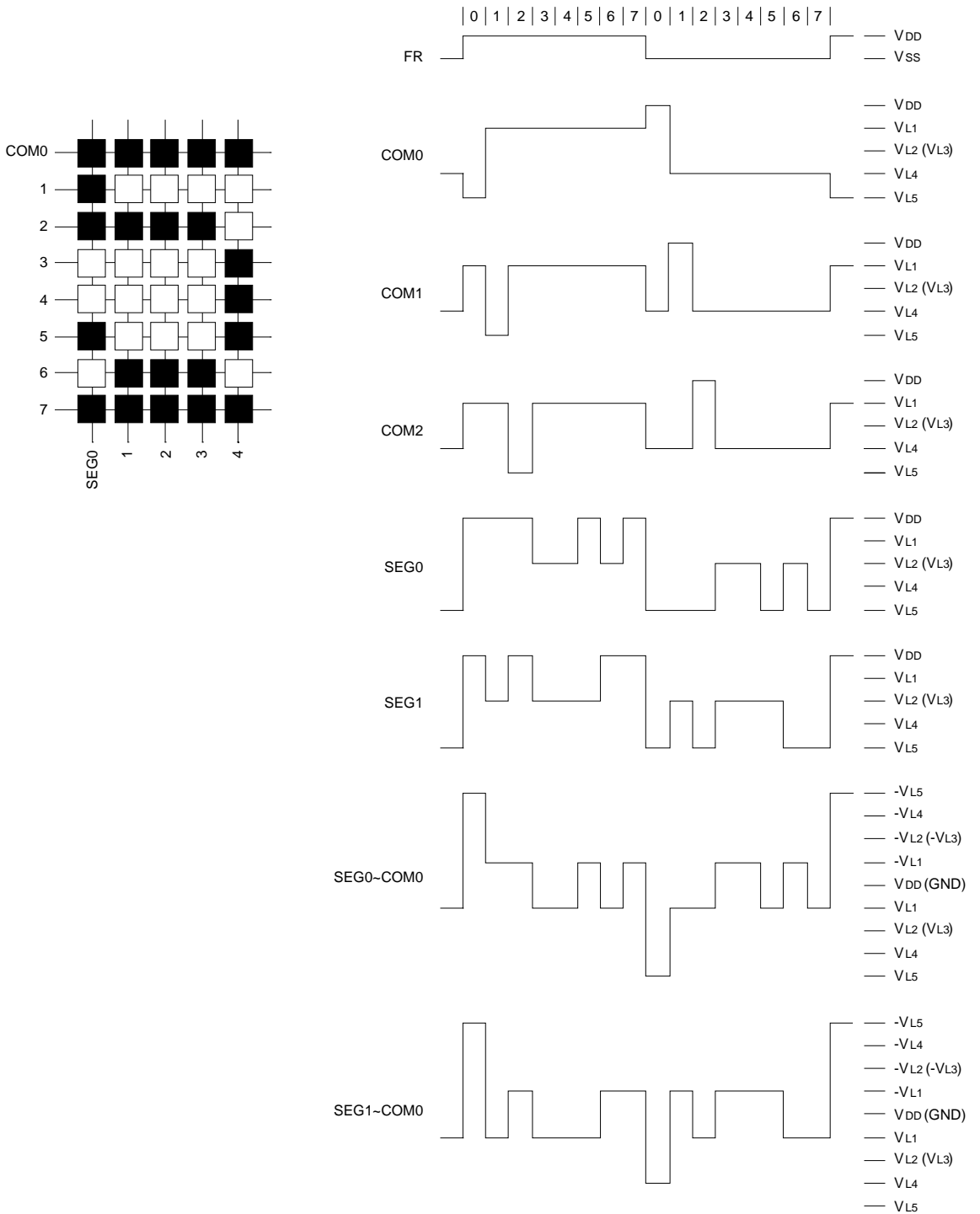
Fig. 7.1.2 Drive waveform for 1/8 duty (1/4 bias)

7.2 Mask Option

Disconnecting the internal power for LCD driving will enable electric potentials to be supplied externally. In such case, the 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.

Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 7.2.1.
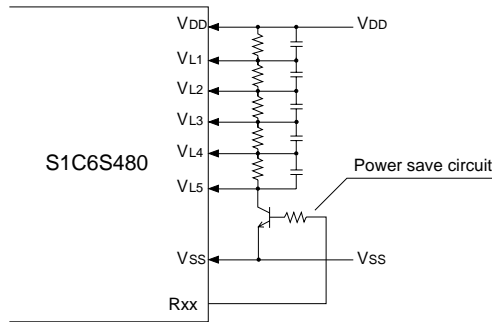
Fig. 7.2.1 Sample circuit of external power for LCD driving when power is supplied externally

7.3 Display Data Memory

The display data memory of the S1C6S480 is allocated to the built-in RAM addresses E00H–E65H and E80H–EF5H.

Figure 7.3.1 shows the correspondence between the display data memory and the LCD dot matrix.
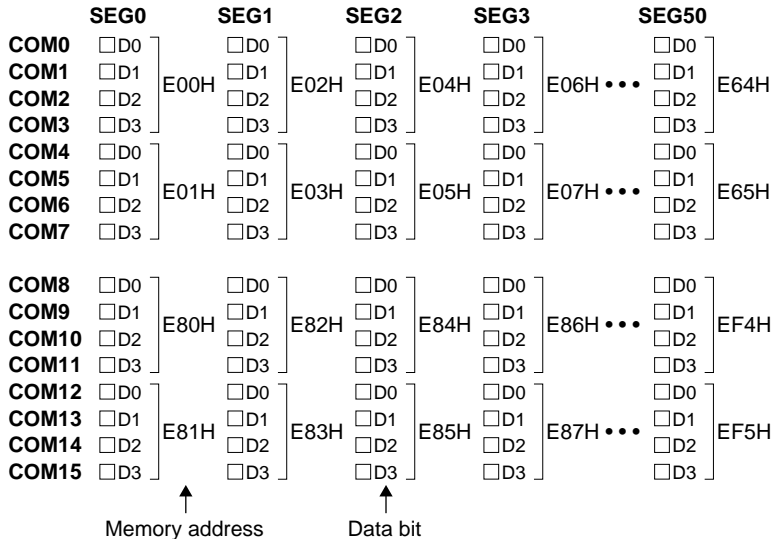
Fig. 7.3.1 LCD dot matrix and segment memory correspondence

When the segment memory bit is assigned as "1", the corresponding LCD dot lights up, and when assigned as "0", the dot dies out. At 1/16 duty drive and 1/8 duty drive, COM0 to COM15 lines and COM0 to COM7 lines light up, respectively.

At initial reset, the display data memory content becomes undefined and hence, there is need to initialize by software.

7.4 Control of LCD Driver

The control registers for the LCD driver are explained below.

Table 7.4.1 Control registers of LCD driver

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X			LCD contrast adjustment
					LC2	X			LC3–LC0 = 0 light
	R/W				LC1	X			:
					LC0	X			LC3–LC0 = 15 dark

LDUTY (F71H [D1], R/W)
Sets the LCD drive duty.

> When "1" is written: $1/8$ duty
> When "0" is written: $1/16$ duty
> Reading: Valid

Writing "1" or "0" on LDUTY will set is to $1/8$ duty or $1/16$ duty, respectively.
At initial reset, LDUTY is set at "0".

ALON (F71H [D2], R/W)
Displays the all LCD dots on.

> When "1" is written: All LCD dots displayed
> When "0" is written: Normal operation
> Reading: Valid

Writing "1" to ALON will display all the LCD dots on; writing "0" will set the LCD display back to normal. LCD panel testing may be conducted with this function.
Total LCD displaying at ALON = "1" is a static operation and does not affect the content of the display data memory.
ALON precedes ALOFF.
At initial reset, ALON is set at "0".

ALOFF (F71H [D3], R/W)
Fade outs the all LCD dots.

> When "1" is written: All LCD dots fade out
> When "0" is written: Normal operation
> Reading: Valid

When "1" is written on ALOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at ALOFF = "1" is due to light out signals and does not affect the content of the display data memory.
Flashing of the entire LCD panel is performed by this function.
At initial reset, ALOFF is set to "1".

LC0, LC1, LC2, LC3 (F72H, R/W)
Will adjust the LCD contrast.
Contrast may be adjusted to 16 levels as shown in Table 7.4.2.

Table 7.4.2 LCD contrast

	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
A	1	0	1	0	
B	1	0	1	1	
C	1	1	0	0	
D	1	1	0	1	
E	1	1	1	0	↓
F	1	1	1	1	dark

At room temperature, use setting number **7** or **8** as standard.
The voltage of the LCD system power terminals V_{L1}, V_{L2}, V_{L4} and V_{L5} changes through this function
(only when the voltage is generated by the internal power supply circuit).
Because at initial reset, the contents of LC0–LC3 are undefined, initialize it by the software.

7.5 *Programming Note*

Because at initial reset, the contents of display data memory and LC0–LC3 are undefined, there is need to
initialize by software.

CHAPTER 8   TIMERS

8.1   Clock Timer

8.1.1 Configuration of clock timer

The S1C6S480 has a clock timer with OSC1 (crystal oscillation) as basic oscillation built-in. The clock timer is configured with an 8 bits binary counter with 256 Hz signal divided from OSC1 as input clock, allowing 128 Hz–1 Hz of data to be read by the software. Figure 8.1.1.1 shows the configuration of the clock timer.
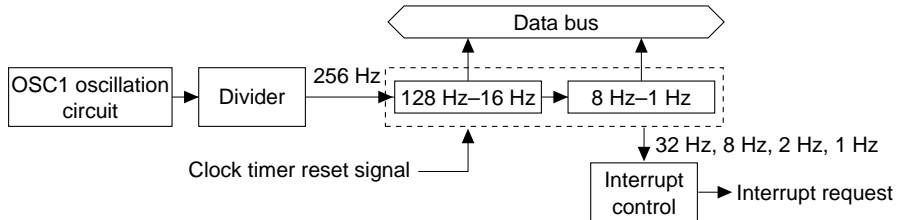
Fig. 8.1.1.1 Configuration of clock timer

8.1.2 Interrupt function

The clock timer has interrupt capability, and interrupt is generated by the falling edge of 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals.
Figure 8.1.2.1 shows the timing chart of the clock timer.

Fig. 8.1.2.1 Timing chart of clock timer

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT8, IT2, and IT1) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT8, EIT2, and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

8.1.3 Control of clock timer

The control registers for the clock timer are explained below.

Table 8.1.3.1 Control registers of clock timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F00H	IT1	IT2	IT8	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	\	R			IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	\	R/W			EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	\	R			TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	\	R			TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F76H	0	0	TMRST	WDRST	0	–			
					0	–			
	R		W		TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

TMRST (F76H [D1], W)
This bit resets the clock timer.

> When "1" is written: Clock timer reset
> When "0" is written: No operation
> Reading: Always "0"

By writing "1" on TMRST, the clock timer is reset and all timer data are set to "0".
Because this bit is only for writing, it is always "0" during reading.

TM0–TM7 (F20H, F21H, R)
Will read the data of the clock timer.
TMx (x = 0–7) and frequency correspondence are as follows:

F20H	F21H
TM0 (D0): 128 Hz	TM4 (D0): 8 Hz
TM1 (D1): 64 Hz	TM5 (D1): 4 Hz
TM2 (D2): 32 Hz	TM6 (D2): 2 Hz
TM3 (D3): 16 Hz	TM7 (D3): 1 Hz

The above 8 bits are only for reading and render writing operation invalid.
At initial reset, timer data is initialized to "0".

EIT32, EIT8, EIT2, EIT1 (F10H, R/W)
There are the interrupt mask registers of the clock timer.

> When "1" is written: Enabled
> When "0" is written: Masked
> Reading: Valid

EIT32, EIT8, EIT2, and EIT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IT32, IT8, IT2, IT1 (F00H, R)

There are the interrupt factor flags of the clock timer.

> When "1" is read: Interrupt has occurred
> When "0" is read: Interrupt has not occurred
> Writing: Invalid

IT32, IT8, IT2, and IT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.

The occurrence of clock timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" due to the falling edge of the corresponding signal.

Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

At initial reset, these flags are set to "0".

8.1.4 Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.2 Stopwatch Timer

8.2.1 Configuration of stopwatch timer

The S1C6S480 has 1/100 sec unit (SWL) and 1/10 sec unit (SWH) stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4 bits BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software.

Figure 8.2.1.1 shows the configuration of the stopwatch timer.
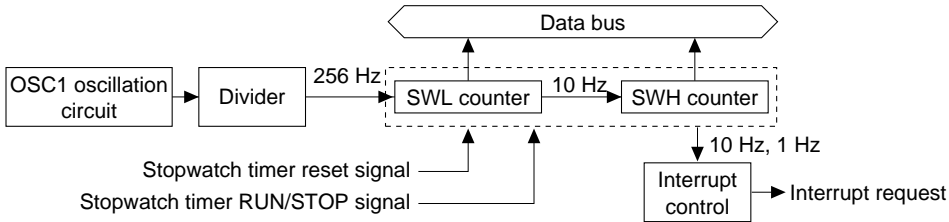
Fig. 8.2.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

8.2.2 Count-up pattern

The stopwatch timer is configured of 4 bits BCD counters SWL and SWH.

The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.

Figure 8.2.2.1 shows the count-up pattern of the stopwatch timer.
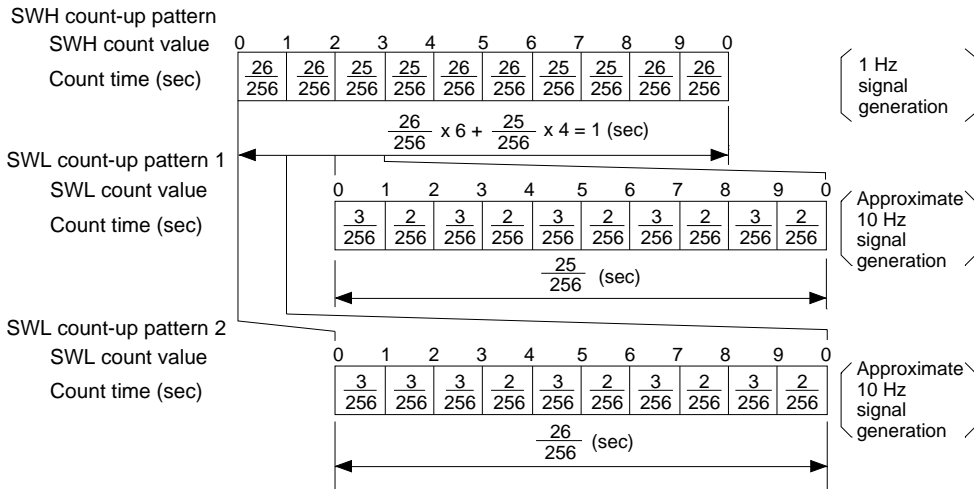
Fig. 8.2.2.1 Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.

SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

8.2.3 Interrupt function

Stopwatch timers SWL and SWH, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.

Figure 8.2.3.1 shows the timing chart for the stopwatch timer.
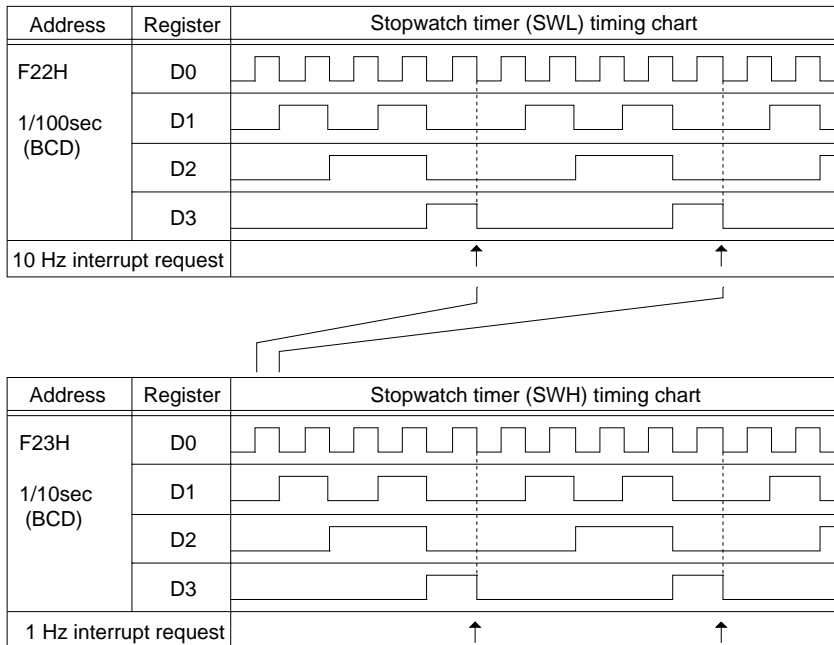
Fig. 8.2.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWL and SWH (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW0 and ISW1) are set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW0 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

8.2.4 Control of stopwatch timer

The control registers for the stopwatch timer are explained below.

Table 8.2.4.1 Control registers of stopwatch timer

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F01H	0	0	ISW1	ISW0	0	–			
					0	–			
	R				ISW1	0		No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0		No	Interrupt factor flag (stopwatch 10 Hz)
F11H	0	0	EISW1	EISW0	0	–			
					0	–			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			┬ MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			┴ LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			┬ MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			┴ LSB
F77H	0	0	SWRST	SWRUN	0	–			
					0	–			
	R		W	R/W	SWRST	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

SWRST (F77H [D1], W)
This bit resets the stopwatch timer.

> When "1" is written: Stopwatch timer reset
> When "0" is written: No operation
> Reading: Always "0"

By writing "1" on SWRST, the stopwatch timer is reset. All timer data is set to "0".
When the stopwatch timer is reset in the RUN mode, it will re-start counting immediately after the reset and at STOP mode, the reset data is maintained.
Because this bit is for writing only, it is always "0" during reading.

SWRUN (F77H [D0], R/W)
This register controls RUN/STOP of the stopwatch timer.

> When "1" is written: RUN
> When "0" is written: STOP
> Reading: Valid

By writing "1" on SWRUN, the stopwatch timer performs counting operation. Writing "0" will make the stopwatch stop counting.
Even if the stopwatch is stopped, the timer data at that point is kept.
When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWL) into high-order digits (SWH) (i.e., in case SWL and SWH reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).
At initial reset, SWRUN is set to "0".

SWL0–SWL3 (F22H, R)

Will read the stopwatch timer data to the 1/100 sec digits (BCD).

Since these bits are for reading only, writing operation is invalidated.

At initial reset, timer data is set to "0".

SWH0–SWH3 (F23H, R)

Will read the stopwatch timer data to the 1/10 sec digits (BCD).

Since these bits are for reading only, writing operation is invalidated.

At initial reset, timer data is set to "0".

EISW0, EISW1 (F11H [D0, D1], R/W)

There are the interrupt mask registers of the stopwatch timer.

> When "1" is written: Enabled
> When "0" is written: Masked
> Reading: Valid

EISW0 and EISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).

Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

At initial reset, these registers are all set to "0" (mask).

ISW0, ISW1 (F01H [D0, D1], R)

There are the interrupt factor flags of the stopwatch timer.

> When "1" is read: Interrupt has occurred
> When "0" is read: Interrupt has not occurred
> Writing: Invalid

ISW0 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.

The occurrence of stopwatch timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" by the overflow of the corresponding counters.

Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

At initial reset, these flags are set to "0".

8.2.5 Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

(2) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.3 Programmable Timer

8.3.1 Configuration of programmable timer

The S1C6S480 has a programmable timer with OSC1 (crystal oscillation) as basic oscillation built-in. The programmable timer is configured with an 8 bits pre-settable down counter and it has been down-count at initial value by 256 Hz–8,192 Hz signal or by the input signal of input port K03.

The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.

The down-counter data may be read through the software. Moreover, the input clock being selected may be generated to output port R33.

Figure 8.3.1.1 shows the configuration of the programmable timer.
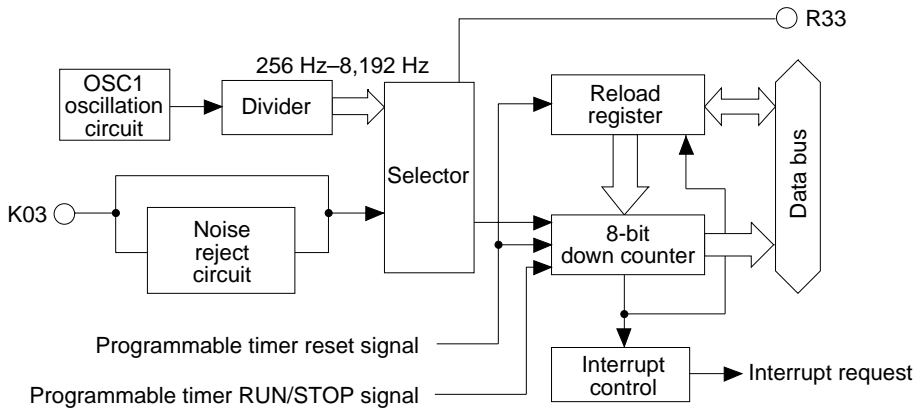
Fig. 8.3.1.1 Configuration of programmable timer

One input clock may be selected by software from any of the following 8 types:

(1) K03 input (with noise rejector)
(2) K03 input (direct)
(3) 256 Hz
(4) 512 Hz
(5) 1,024 Hz
(6) 2,048 Hz
(7) 4,096 Hz
(8) 8,192 Hz

Note, however, that down-count is done at falling edges of the input signal as shown in Figure 8.3.1.2.
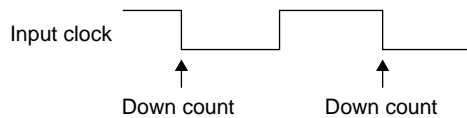
Fig. 8.3.1.2 Timing of down-counts

Type (1) K03 input (with noise rejector) is for counting by key entry, the input signal from which passes the 256 Hz sampling noise reject circuit. With this, no more than 2 ms of chattering is purged, and at least 4 ms signal is received.

8.3.2 Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.

After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.

Figure 8.3.2.1 shows the timing chart of the programmable timer.

Note: When "A6H" is set into reload register
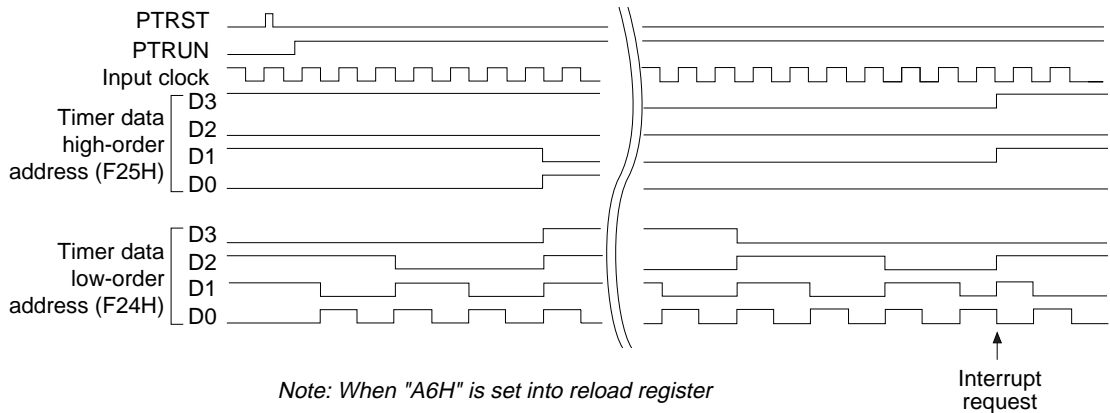
Fig. 8.3.2.1 Timing chart of programmable timer

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

8.3.3 Control of programmable timer

The control registers for the programmable timer are explained below.

Table 8.3.3.1 Control registers of programmable timer

Address	Register D3	Register D2	Register D1	Register D0	Name	Init	1	0	Comment
F02H	0	0	0	IPT	0	–			
					0	–			
		R			0	–			
					IPT	0	Yes	No	Interrupt factor flag (programmable timer)
F12H	0	0	0	EIPT	0	–			
					0	–			
		R		R/W	0	–			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F24H	PT3	PT2	PT1	PT0	PT3	X			⌐ MSB
					PT2	X			
		R			PT1	X			Programmable timer data (low-order)
					PT0	X			⌐ LSB
F25H	PT7	PT6	PT5	PT4	PT7	X			⌐ MSB
					PT6	X			
		R			PT5	X			Programmable timer data (high-order)
					PT4	X			⌐ LSB
F26H	RD3	RD2	RD1	RD0	RD3	X			⌐ MSB
					RD2	X			Programmable timer
		R/W			RD1	X			reload data (low-order)
					RD0	X			⌐ LSB
F27H	RD7	RD6	RD5	RD4	RD7	X			⌐ MSB
					RD6	X			Programmable timer
		R/W			RD5	X			reload data (high-order)
					RD4	X			⌐ LSB
F78H	0	0	PTRST	PTRUN	0	–			
					0	–			
		R	W	R/W	PTRST	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			
		R/W			PTC1	0			Programmable timer input clock selection
					PTC0	0			

PTC0, PTC1, PTC2 (F79H [D0–D2], R/W)
Selects the input clock.
The PTC0–PTC2 setting and input clock correspondence is shown in Table 8.3.3.2.

Table 8.3.3.2 Input clock setting

PTC2	PTC1	PTC0	Input clock
0	0	0	K03 input (with noise rejector)
0	0	1	K03 input (direct)
0	1	0	256 Hz
0	1	1	512 Hz
1	0	0	1,024 Hz
1	0	1	2,048 Hz
1	1	0	4,096 Hz
1	1	1	8,192 Hz

PTCOUT (F79H [D3], R/W)
Generates the input clock being selected to output port R33.
Refer to Section 6.2, "Output Port" regarding control methods.

RD0–RD3, RD4–RD7 (F26H, F27H, R/W)
These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is 00H.
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, this register will be undefined.

PTRST (F78H [D1], W)
This bit resets the programmable timer.

When "1" is written: Programmable timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on PTRST, the programmable timer is reset.
The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN (F78H [D0], R/W)
This register controls RUN/STOP of the programmable timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
When data of the counter is read at the RUN mode, proper reading may not be obtained due to the carry from the low-order digits (PT0–PT3) into the high-order digits (PT4–PT7) (when the reading of the low-order digits and high-order digits span the timing of the carry). To avoid this occurrence, perform the reading after suspending the programmable timer once, and set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty).
At initial reset, PTRUN is set to "0".

PT0–PT3, PT4–PT7 (F24H, F25H, R)
Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
At initial reset, timer data will be undefined.

EIPT (F12H [D0], R/W)
This is the interrupt mask register of the programmable timer.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

IPT (F02H [D0], R)
This is the interrupt factor flag of the programmable timer.

> When "1" is read: Interrupt has occurred
> When "0" is read: Interrupt has not occurred
> Writing: Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

8.3.4 Programming notes

(1) When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within $1/4$ cycle of the input clock (in case of $1/2$ duty). Accordingly, when the input clock is a fast clock faster than a 256 Hz, high speed processing by OSC3 is required.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER *9* SERIAL INTERFACE

9.1 Configuration of Serial Interface

The S1C6S480 has a synchronous clock type 8 bits serial interface built-in.

The configuration of the serial interface is shown in Figure 9.1.1.

The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal. The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the S1C6S480 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the S1C6S480 is to be the slave for serial input/output).

Also, when the serial interface is used at slave mode, $\overline{\text{SRDY}}$ (SIO READY) signal which indicates whether or not the serial interface is available to transmit or receive can be output to output port R33 by mask option.
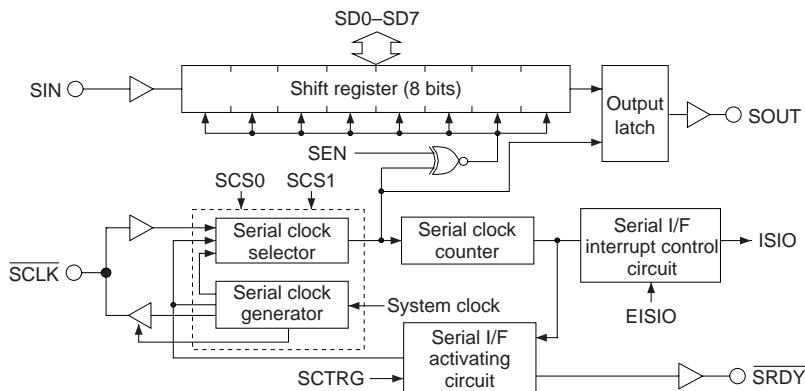
Fig. 9.1.1 Configuration of serial interface

9.2 Mask Option

The serial interface may be selected for the following by mask option.

(1) Whether or not the SIN terminal will use built-in pull up resistor may be selected.
If the use of no pull up resistor is selected, take care that floating state does not occur at the SIN terminal.

(2) Either complementary output or N channel (Nch) open drain as output specification for the SOUT terminal may be selected.
However, even if Nch open drain has been selected, application of voltage exceeding power source voltage to the SOUT terminal will be prohibited.

(3) Whether or not the $\overline{\text{SCLK}}$ terminal will use pull up resistor which is turned ON during input mode (external clock) may be selected. If the use of no pull up resistor is selected, take care that floating state does not occur at the $\overline{\text{SCLK}}$ terminal during input mode.
Normally, the use of pull up resistor should be selected.

(4) As output specification during output mode, either complementary output or N channel (Nch) open drain output may be selected for the $\overline{\text{SCLK}}$ terminal. However, even if the same Nch open drain as that of the SOUT terminal is selected, application of voltage exceeding the power current voltage is not permitted.

(5) LSB first or MSB first as input/output permutation of serial data may be selected.

(6) Output port R33 may be assigned as $\overline{\text{SRDY}}$ output terminal which will indicate whether the serial interface is available to transmit or receive signals.

9.3   Master Mode and Slave Mode of Serial Interface

The serial interface of the S1C6S480 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the $\overline{\text{SCLK}}$ terminal and controls the external (slave side) serial interface.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{\text{SCLK}}$ terminal and uses it as the synchronous clock to the built- in shift register.
The master mode and slave mode are selected through registers SCS0 and SCS1; when the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 9.3.1.

Table 9.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the $\overline{\text{SCLK}}$ terminal, clock output is automatically suspended and $\overline{\text{SCLK}}$ terminal is fixed at high level.

- At slave mode, after input of 8 clocks to the $\overline{\text{SCLK}}$ terminal, subsequent clock inputs are masked.

Note: When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.

A sample basic serial input/output portion connection is shown in Figure 9.3.1.
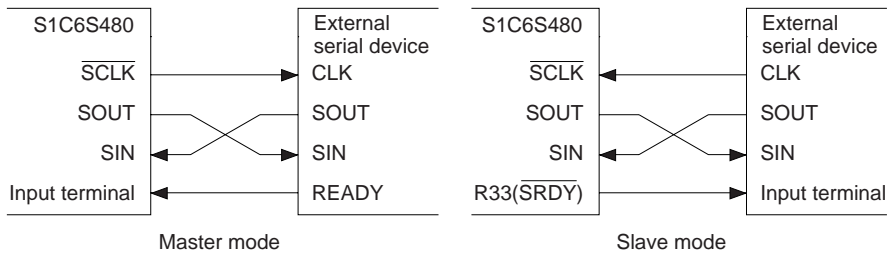
Fig. 9.3.1 Sample basic connection of serial input/output section

9.4   Data Input/Output and Interrupt Function

The serial interface of S1C6S480 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from $\overline{\text{SCLK}}$ terminal (master mode), or the synchronous clock input to $\overline{\text{SCLK}}$ (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock ($\overline{\text{SCLK}}$); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure

The S1C6S480 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to data registers SD0–SD3 and SD4–SD7 individually and writing "1" to SCTRG (F7AH [D3]), it synchronizes with the synchronous clock and serial data is output at the SOUT terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ terminal. The serial output of the SOUT terminal changes with the falling edge of the clock that is input or output from the $\overline{SCLK}$ terminal.

When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8 bits data.

(2) Serial data input procedure

The S1C6S480 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. By writing "1" to SCTRG, the serial data is input from the SIN terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{SCLK}$ terminal while in the slave mode, external clock which is input from the $\overline{SCLK}$ terminal. The serial data to the built-in shift register is read with the falling edge of the $\overline{SCLK}$ signal when SEN bit is "1" and is read with the rising edge of the $\overline{SCLK}$ signal when SEN bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

Also, the data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The S1C6S480 allow the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 9.4.1.
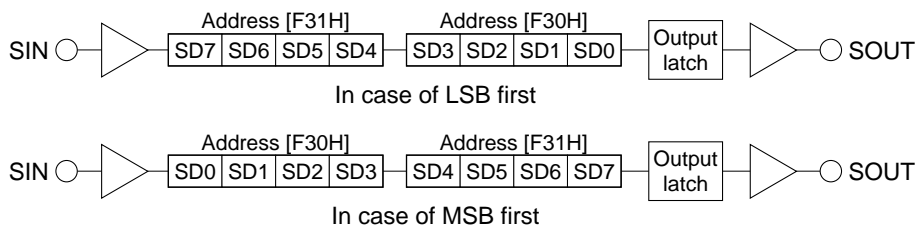
Fig. 9.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the S1C6S480 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is generated from output port R33 by mask option.

$\overline{\text{SRDY}}$ signal becomes "0" (low) when the S1C6S480 serial interface becomes available to transmit or receive data; normally, it is at "1" (high).

$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to $\overline{\text{SCLK}}$ terminal (i.e., when the serial input/output begins transmitting or receiving data).

Moreover, when data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".

The operating state (wait state or transmitting/receiving state) of the serial interface may be checked by connecting output port R33 ($\overline{\text{SRDY}}$) to input port (Kxx) or I/O port (Pxx) and performing reading.

(5) Timing chart

The S1C6S480 serial interface timing chart is shown in Figure 9.4.2.

(1) SEN = "1"

(2) SEN = "0"
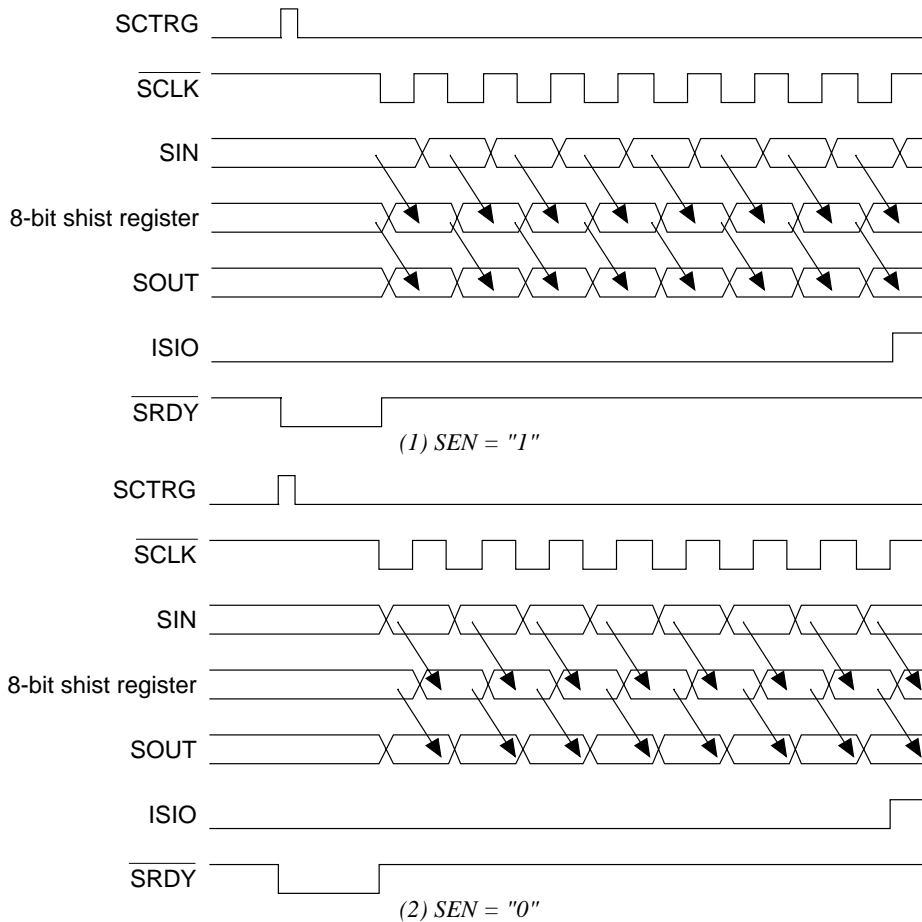
Fig. 9.4.2 Serial interface timing chart

9.5   Control of Serial Interface

The control registers for the serial interface are explained below.

Table 9.5.1 Control registers of serial interface

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F03H	0	0	0	ISIO	0	–			
					0	–			
	R				0	–			
					ISIO	0	Yes	No	Interrupt factor flag (serial interface)
F13H	0	0	0	EISIO	0	–			
					0	–			
	R			R/W	0	–			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F30H	SD3	SD2	SD1	SD0	SD3	X			⌐ MSB
					SD2	X			Serial interface
	R/W				SD1	X			data register (low-order)
					SD0	X			⌐ LSB
F31H	SD7	SD6	SD5	SD4	SD7	X			⌐ MSB
					SD6	X			Serial interface
	R/W				SD5	X			data register (high-order)
					SD4	X			⌐ LSB
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG	–	Trigger	–	Serial interface clock trigger
					SEN	0	⌐	⌐	Serial interface clock edge selection
	W		R/W		SCS1	0			⌐
					SCS0	0			Serial interface clock mode selection

SD0–SD3, SD4–SD7 (F30H, F31H, R/W)

This is the data register of the serial interface.

• **During writing operation**
    When "1" is written: High level
    When "0" is written: Low level

Writes serial data will be output to SOUT terminal. From the SOUT terminal, the data converted to serial data as high (VDD) level bit for bits set at "1" and as low (VSS) level bit for bits set at "0". Perform data writing only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

• **During reading operation**
    When "1" is read: High level
    When "0" is read: Low level

The serial data input from the SIN terminal can be read by this register.
The data converted to parallel data, as high (VDD) level bit "1" and as low (VSS) level bit "0" input from SIN terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
At initial reset, these registers will be undefined.

SCS1, SCS0 (F7AH [D1, D0], R/W)

Selects the synchronous clock for the serial interface ($\overline{\text{SCLK}}$).

Table 9.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1		CLK
1	0	Master mode	CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

Synchronous clock ($\overline{\text{SCLK}}$) is selected from among the above 4 types: 3 types of internal clock and external clock.

At initial reset, external clock is selected.

SEN (F7AH [D2], R/W)

Selects the timing for reading in the serial data input.

When "1" is written: Falling edge of $\overline{\text{SCLK}}$
When "0" is written: Rising edge of $\overline{\text{SCLK}}$
          Reading: Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the falling edge (at "1" writing) or rising edge (at "0" writing) of the $\overline{\text{SCLK}}$ signal.

The input data fetching timing may be selected but output timing for output data is fixed at $\overline{\text{SCLK}}$ falling edge.

At initial reset, rising edge of $\overline{\text{SCLK}}$ (SEN = "0") is selected.

SCTRG (F7AH [D3], W)

This is a trigger to start input/output of synchronous clock.

When "1" is written: Trigger
When "0" is written: No operation
          Reading: Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{\text{SCLK}}$) input/output is started.

As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)

Supply trigger only once every time the serial interface is placed in the RUN state.

Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

EISIO (F13H [D0], R/W)

This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
          Reading: Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

At initial reset, this register is set to "0" (mask).

ISIO (F03H [D0], R)
This is the interrupt factor flag of the serial interface.

> When "1" is read: Interrupt has occurred
> When "0" is read: Interrupt has not occurred
> Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

9.6   Programming Notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER *10* SOUND GENERATOR

10.1 Configuration of Sound Generator

The S1C6S480 is capable of generating buzzer signals (BZ and $\overline{BZ}$) to drive a piezo-electric buzzer.
The buzzer signal frequency may be selected by software from 8 types of signal divided from f_{OSC1} (32.768 kHz).
Also, digital envelope which is duty ratio controlled may be added to the buzzer signal.
In addition, 1-shot output circuit is built-in to output key operation check sound, and the like.
Figure 10.1.1 shows the sound generator configuration. Figure 10.1.2 shows the sound generator timing chart.
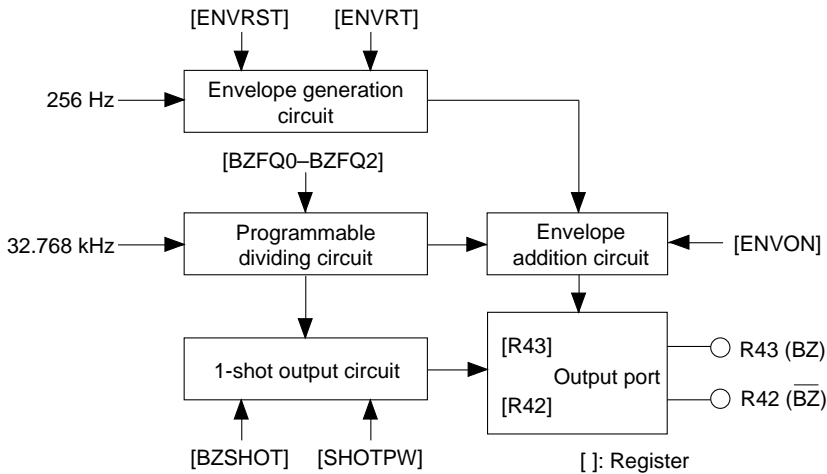
Fig. 10.1.1 Configuration of sound generator

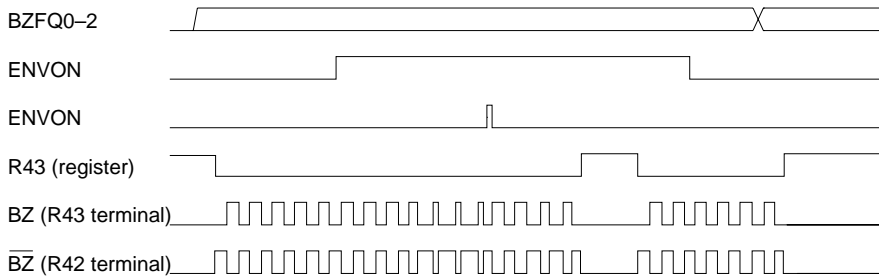*Fig. 10.1.2 Timing chart of sound generator*

10.2 Mask Option

(1) Selection can be made whether to output the BZ signal from the R43 terminal.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R42 terminal.
    However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

See Section 6.2, "Output Port" for details of the above mask option.

10.3 Frequency Setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2.
Table 10.3.1 lists the register setting values and the frequencies that can be set.

Table 10.3.1 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

Note: A hazard may be observed in the output waveform of the buzzer signals when switches the buzzer frequency while the buzzer signals being output.

10.4 Digital Envelope

A duty ratio control data envelope (with duty ratio change in 8 steps) can be added to the buzzer signal (BZ, $\overline{BZ}$).
Duty ratio refers to the ratio of pulse width to the pulse cycle; given that high level output time is TH, and low level output time is TL, BZ output becomes TH/(TH+TL).
$\overline{BZ}$ output becomes TL/(TH+TL) owing to the inverted output of the BZ output. Moreover, care is necessary as the duty ratio differs according to the buzzer frequency.
Envelope addition is performed by writing "1" to ENVON; when "0" is written, the duty ratio is fixed at the maximum (1/2 duty). Moreover, when envelope is added, writing "1" to ENVRST will cause the BZ signal duty ratio to be returned to maximum.
The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 ms (16 Hz) when "0" is written, and 125 ms (8 Hz) when "1" is written. However, a maximum difference of 4 ms is taken from envelope-ON until the first change.
Table 10.4.1 lists the duty ratio and buzzer frequencies.
Figure 10.4.1 shows the digital envelope timing chart.

Table 10.4.1 Duty ratio and buzzer frequencies

Duty ratio	Buzzer frequencies			
	4,096.6	3,276.8	2,730.7	2,340.6
	2,048.0	1,638.4	1,365.3	1,170.3
Level 1 (max.)	8/16	8/20	12/24	12/28
Level 2	7/16	7/20	11/24	11/28
Level 3	6/16	6/20	10/24	10/28
Level 4	5/16	5/20	9/24	9/28
Level 5	4/16	4/20	8/24	8/28
Level 6	3/16	3/20	7/24	7/28
Level 7	2/16	2/20	6/24	6/28
Level 8 (min.)	1/16	1/20	5/24	5/28

No change of duty level

BZFQ0–2

ENON

ENVRST

ENVRT

R43 (register)

BZ signal
duty ratio   Level   1 (MAX)
2
3
4
5
6
7
8 (MIN)

t_{01}
t_{02}
t_{03}
t_{04}
t_{05}
t_{06}
t_{07}

t_{01}

t_{11}
t_{12}
t_{13}
t_{14}
t_{15}
t_{16}
t_{17}

$t_{01} = 62.5\,^{+0}_{-4}$ msec

$t_{02-07} = 62.5$ msec

$t_{11} = 125\,^{+0}_{-4}$ msec

$t_{12-17} = 125$ msec
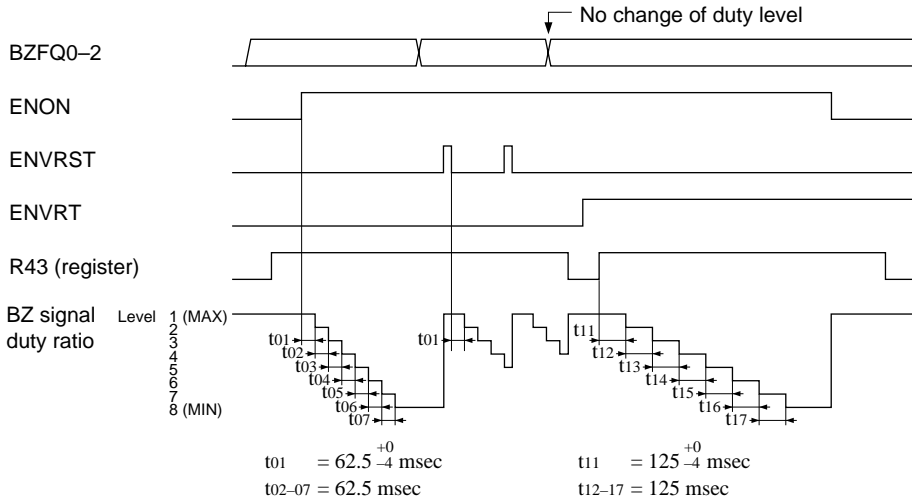
Fig. 10.4.1 Digital envelope timing chart

10.5 1-shot Output

In order to cause the buzzer to ring in a short period of time as in the case of key operation check sound, 1-shot output function is built-in. The time duration for buzzer signal to be output (BZ and $\overline{BZ}$) may be selected by SHOTPW; when "0" is written on SHOTPW, it is set to 31.25 ms and to 62.5 ms when "1" written.

Actual output operation is performed by writing "1" on BZSHOT; after performing the previously described writing operation, it synchronizes with the internal 256 Hz signal and buzzer signal is output in output port R43 (R42).

Moreover, after the set time has lapsed, it synchronizes with the same 256 Hz previously described and the buzzer signal is automatically turned off. Also, by reading BZSHOT, whether the 1-shot circuit is in operation or not may be determined with the software.

Figure 10.5.1 shows the timing chart of the 1-shot output.

256 Hz

SHOTPW

BZSHOT•W
(trigger)

BZSHOT•R
(status)

BZ (R43 terminal)
$\overline{BZ}$ (R42 terminal)
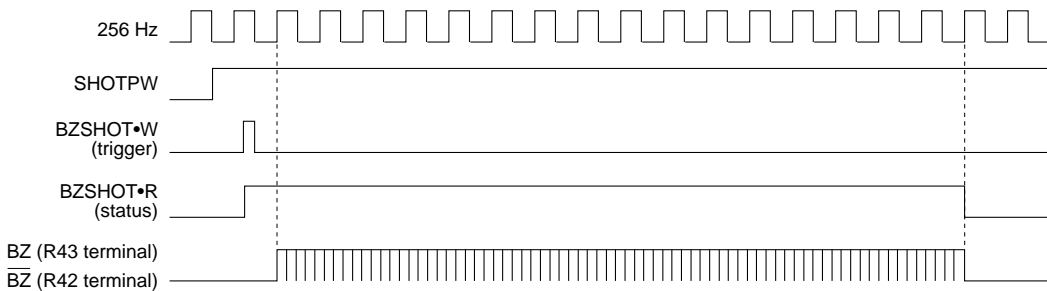
Fig. 10.5.1 Timing chart of 1-shot output

10.6 Control of Sound Generator

The control registers for the sound generator are explained below.

Table 10.6.1 Control registers of sound generator

Address	Register				Name	Init	1	0	Comment
	D3	D2	D1	D0					
F54H	R43	R42	R41	R40	R43	1	High Off	Low On	Output port (R43) Buzzer output (BZ)
			R/W		R42	1	High Off	Low On	Output port (R42) Clock output (FOUT) [Buzzer inverted output ($\overline{BZ}$)]
					R41	1	High	Low	Output port (R41)
					R40	1	High Off	Low On	Output port (R40) Clock inverted output ($\overline{FOUT}$)
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			
			R/W		BZFQ1	0			Buzzer frequency selection
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger BUSY	– READY	1-shot buzzer trigger (W) Status (R)
	W / R	W	R/W		ENVRST	Reset	Reset	–	Envelope reset
					ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off

BZFQ0–BZFQ2 (F74H [D0, D1, D2], R/W)

Will select the buzzer signal frequency.

Table 10.6.2 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

At initial reset, 4,096 Hz is selected.

ENVRST (F75H [D2], W)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written: Reset input
When "0" is written: No operation
          Reading: Always "0"

When envelope is added to the buzzer signal, by writing "1" on ENVRST, the envelope is reset and duty ratio becomes maximum. When envelope is not added, or when buzzer signal is not being output, reset operation is ineffective.

ENVON (F75H [D0], R/W)
This controls adding the envelope to the buzzer signal.

When "1" is written: Envelope added (ON)
When "0" is written: No envelope (OFF)
            Reading: Valid

By writing "1" on ENVON, envelope is added to the buzzer signal. Writing "0" means envelope will not be added.
At initial reset, ENVON is set to "0" and envelope OFF will be selected.

ENVRT (F75H [D1], R/W)
Selects the attenuation time of the envelope added to the buzzer signal.

When "1" is written: 1.0 sec (125 ms $\times$ 7 = 875 ms)
When "0" is written: 0.5 sec (62.5 ms $\times$ 7 = 437.5 ms)
            Reading: Valid

The attenuation time of digital envelopes is determined by the time change for duty ratio. When "1" is written on ENVRT, attenuation time is set in 125 ms (8 Hz) units (125 ms $\times$ 7 = 875 ms), and in 62.5 ms (16 Hz) unit (62.5 ms $\times$ 7 = 437.5 ms) when "0" is written.
However, there is a maximum error of 4 ms from envelope ON to the first change in both cases.
At initial reset, ENVRT is set to "0".

R43, R42 (F54H [D3, D2], R/W)
Controls the output of the buzzer signals (BZ, $\overline{\text{BZ}}$).

When "0" is written: Buzzer signal output
When "1" is written: Low level (DC)
            Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal, and if R42 is set to $\overline{\text{BZ}}$ output, $\overline{\text{BZ}}$ signal (inverted signal of BZ) is generated at the same time.
When "1" is set on R43, R43 terminal (R42 too, if $\overline{\text{BZ}}$ output is selected) becomes of low (V$_{SS}$) level output.
However, R42 with $\overline{\text{BZ}}$ output selected, may be used as a 1-bit general register capable of read/write function, the data of which register does not affect $\overline{\text{BZ}}$ (R42 terminal output).
At initial reset, both R43 and R42 are set to "1".

Note: BZ and $\overline{\text{BZ}}$ output signals may produce hazards during ON/OFF switching.

SHOTPW (F74H [D3], R/W)
Sets the output time duration of the 1-shot buzzer.

When "1" is written: 62.5 ms
When "0" is written: 31.25 ms
            Reading: Valid

Output time duration is set to 62.5 ms or 31.25 ms by writing "1" or "0", respectively, on SHOTPW.
At initial reset, SHOTPW is set to "0".

BZSHOT (F75H [D3], W, R)

Controls the output of the 1-shot buzzer.

• During writing operation

When "1" is written: Trigger
When "0" is written: No operation

When "1" is written on BZSHOT, the 1-shot circuit operates and the buzzer signal (BZ and $\overline{BZ}$) is output.
The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

• During reading operation

When "1" is read: Busy
When "0" is read: Ready

The BZSHOT reads "1" when the 1-shot buzzer is ringing and "0" when it is not ringing. The period of "1" is from the time of the trigger until the buzzer output is turned OFF.
At initial reset, "0" is read.

10.7 Programming Notes

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

• When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.

• When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

CHAPTER 11 INTERRUPT AND HALT

The S1C6S480 has the following interrupt functions built-in, and masking is possible for each one.

External interrupt   • Input interrupt (2 systems)
Internal interrupt   • Clock timer interrupt (3 systems)
                            • Stopwatch timer interrupt (2 systems)
                            • Programmable timer interrupt (1 system)
                            • Serial interface interrupt (1 system)

To allow the interrupt to function, it is necessary that the interrupt mask register of the required system be set to "1" (enable) and, at the same time, the interrupt flag be set to "1" (EI).
When interrupt occurs, the interrupt flag is automatically reset to "0" (DI), prohibiting the any consequent interrupts.

The CPU stops the operating clock when a HALT instruction is executed and then enters the HALT state.
Re-running the CPU from the HALT state requires issuance of interrupt request.
If return through interrupt request is not effective, return is effected from initial reset by the watchdog timer.

Figure 11.1 shows the configuration of the interrupt circuit.

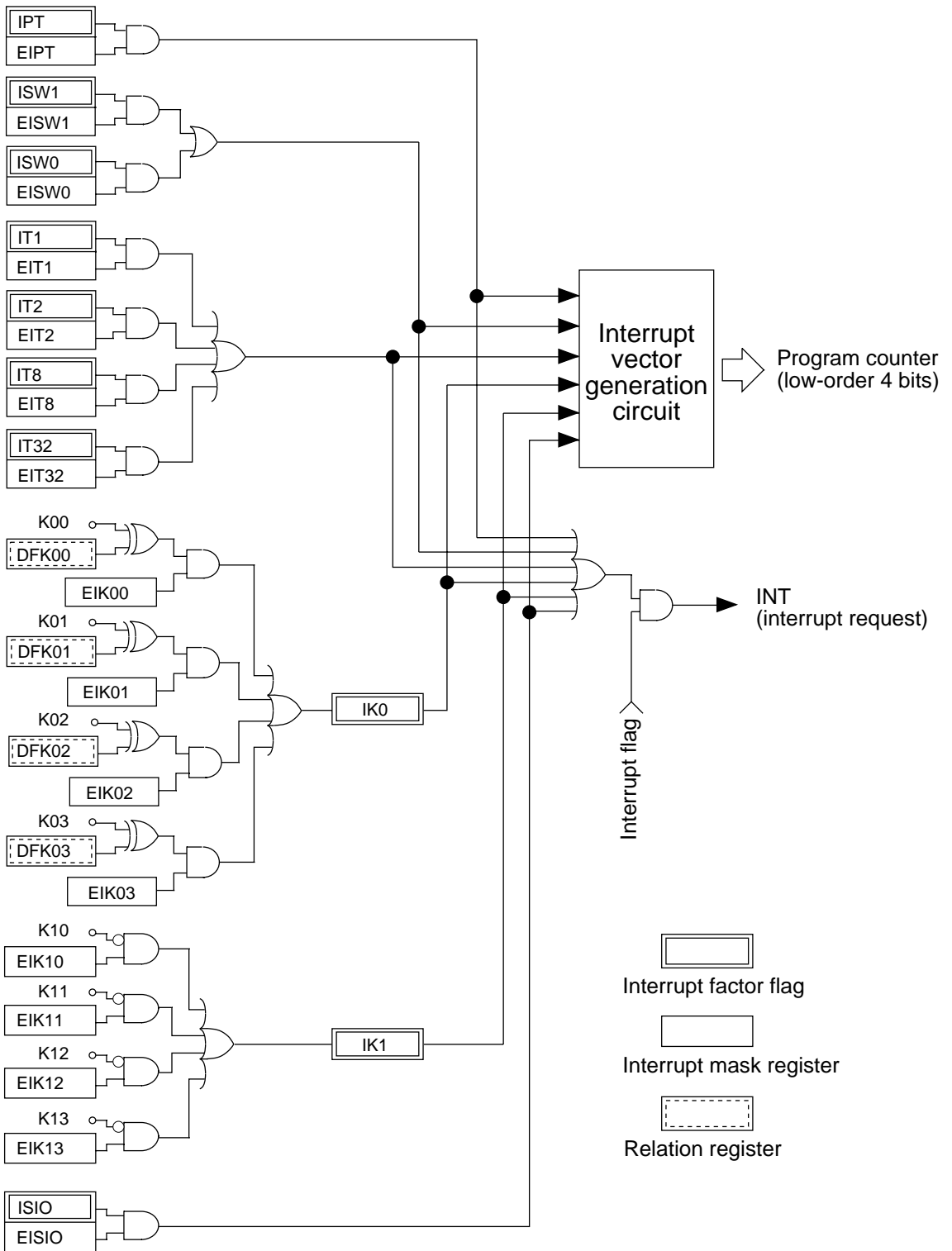See the explanations of the relevant circuits for interrupt details.

Fig. 11.1 Configuration of interrupt circuit

11.1 Interrupt Factor Flag and Interrupt Mask

The corresponding interrupt factor flag is set to "1" with the individual interrupt element.
If the following conditions exist, interrupt for the CPU occurs when the interrupt factor flag is set to "1".

- The corresponding interrupt mask register is set at "1" (enable).
- The interrupt flag is set at "1" (EI).

The interrupt factor flag is reset to "0" at the read-only register by reading the data.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt factor flag is reset to "0".

The interrupt can be masked by the corresponding interrupt mask register.
The interrupt mask register is a register capable of read/write operation; by writing "1", it is enabled (interrupt is allowed) and by writing "0", it is masked (interrupt is prohibited).
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt mask register is set to "0".

The interrupt factor flag is set to "1" by interrupt factor even if the interrupt is masked. (The input interrupt factor flags IK0 and IK1 will be eliminated.)

Table 11.1.1 shows the correspondence between interrupt factor flags and interrupt mask registers.

Table 11.1.1 Interrupt factor flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1 (F00H [D3])	EIT1 (F10H [D3])
Falling edge of clock timer (2 Hz)	IT2 (F00H [D2])	EIT2 (F10H [D2])
Falling edge of clock timer (8 Hz)	IT8 (F00H [D1])	EIT8 (F10H [D1])
Falling edge of clock timer (32 Hz)	IT32 (F00H [D0])	EIT32 (F10H [D0])
Overflow of stopwatch timer (SWH) (1 Hz)	ISW1 (F01H [D1])	EISW1 (F11H [D1])
Overflow of stopwatch timer (SWL) (10 Hz)	ISW0 (F01H [D0])	EISW0 (F11H [D0])
No matching between input ports (K00–K03) and input relation registers (DFK00–DFK03)	IK0 (F04H [D0])	EIK03 (F14H [D3]) EIK02 (F14H [D2]) EIK01 (F14H [D1]) EIK00 (F14H [D0])
Falling edge of input ports (K10–K13)	IK1 (F05H [D0])	EIK13 (F15H [D3]) EIK12 (F15H [D2]) EIK11 (F15H [D1]) EIK10 (F15H [D0])
Data (8 bits) input/output of serial interface has completed	ISIO (F03H [D0])	EISIO (F13H [D0])
Counter value of programmable timer = 00H	IPT (F02H [D0])	EIPT (F12H [D0])

11.2 Interrupt Vector

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

① The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

② The vector address (1 page 02H–0CH) for each interrupt request is set to the program counter.

③ Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Time equivalent to 12 cycles of CPU system clock is required for steps ① and ②.

The interrupt request and interrupt vector correspondence is shown in Table 11.2.1.

Table 11.2.1 Interrupt request and interrupt vectors

Interrupt vector (PCP and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Serial interface interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

11.3 Programming Notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.

Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.

Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.

If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.

When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER *12* SUMMARY OF NOTES

12.1 Notes for Low Current Consumption

The S1C6S480 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.

The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 12.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (Chapter 14)
CPU operation frequency	CLKCHG, OSCC	See electrical characteristics (Chapter 14)
Internal regulated voltage	VSC0, VSC1	See electrical characteristics (Chapter 14)
Heavy load protection mode	HLMOD	See electrical characteristics (Chapter 14)
SVD circuit	SVDON	Several tens μA

Below are the circuit status at initial reset.

CPU: Operating
CPU operating frequency: OSC1 side (CLKCHG = "0"), OSC3 oscillation circuit is stooped (OSCC = "0")
Internal regulated voltage: -1.2 V (VSC0, VSC1 = "0")
Heavy load protection mode: Normal operating mode (HLMOD = "0")
SVD circuit: OFF (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several μA on account of the LCD panel characteristics.

12.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mined when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

SVD (Supply voltage detection) circuit

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 μs waiting time before performing SVDDT reading.

Heavy load protection mode

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.2.1.)

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST ← "1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

Oscillation circuit

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

$$(VSC1, VSC0) = (0, 0) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (1, \times)$$
$$= (1, \times) \rightarrow (0, 1) \rightarrow 5 \text{ ms WAIT} \rightarrow (0, 0)$$

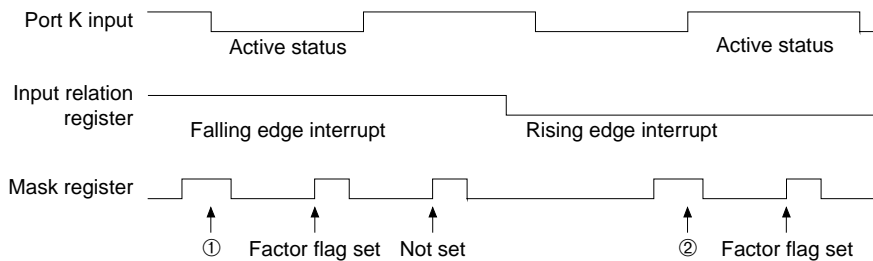$$= (0, 0) \rightarrow (1, \times) \text{ is prohibited}$$
$$= (1, \times) \rightarrow (0, 0) \text{ is prohibited}$$

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.5.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

(6) When CR oscillation has been selected by the mask option, internal regulated voltage becomes -2.1 V and will never become -1.2 V.

Input port (Kxx)

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 µs waiting time is required.

(2) Input interrupt programming related precautions

When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 12.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies
    input terminal = Low status, when the falling edge interrupt is effected and
    input terminal = High status, when the rising edge interrupt is effected.
When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 12.2.1. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.
Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case.
When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).
When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 12.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.
In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

Output port (Rxx)

(1) When BZ, $\overline{\text{BZ}}$, FOUT, $\overline{\text{FOUT}}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

I/O port (Pxx)

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
   • The input/output mode is set at output mode
   • Output specification is set at Nch open drain
   • The content of the data register is "1"
   • The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

LCD driver

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

Stopwatch timer

When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µs (1/4 cycle of 256 Hz).

Programmable timer

(1) When initiating programmable timer count, perform programming by the following steps:
   1. Set the initial data to RD0–RD7.
   2. Reset the programmable timer by writing "1" to PTRST.
   3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than 256 Hz, high speed processing by OSC3 is required.

Serial interface (SIN, SOUT, and $\overline{SCLK}$)

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock (fOSC1 ↔ fOSC3) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

Sound generator

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:
  • When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
  • When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "1") state and writing to BZSHOT becomes invalid in the ON (R43 = "0") state.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.

Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set. Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.

If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.

When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

12.3 Precautions on Mounting

Oscillation Circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.

- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1 (OSC3) and OSC2 (OSC4) terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the figure, make a V_{DD} pattern as large as possible at circumscription of the OSC1 (OSC3) and OSC2 (OSC4) terminals and the components connected to these terminals.
  Furthermore, do not use this V_{DD} pattern for any purpose other than the oscillation system.


Sample V_{DD} pattern (OSC3)
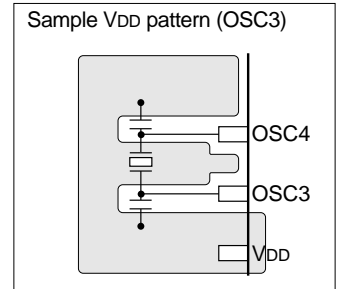
- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 (OSC3) and V_{SS}, please keep enough distance between OSC3 and V_{SS} or other signals on the board pattern.

Reset Circuit

- The power-on reset signal which is input to the $\overline{RESET}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
When using the built-in pull-up resistor of the $\overline{RESET}$ terminal, take into consideration dispersion of the resistance for setting the constant.

- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{RESET}$ terminal in the shortest line.

Power Supply Circuit

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD} and V_{SS} terminal with patterns as short and large as possible.
  Furthermore, similar consideration is necessary when V_{L1}–V_{L5} are supplied from outside the IC.

  (2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.


Bypass capacitor connection example
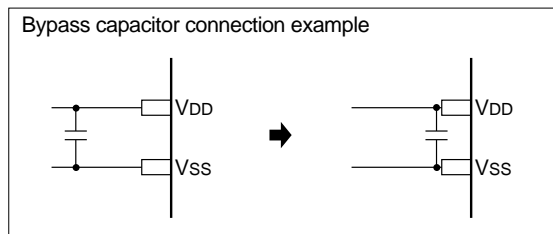
  (3) Components which are connected to the V_{S1}, V_{L1}–V_{L5} terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the V_{L1}–V_{L5} voltages affect the display quality.

- Do not connect anything to the V_{L1}–V_{L5} terminals when the LCD driver is not used.

Arrangement of Signal Lines

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.

- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.

Prohibited pattern
OSC4
OSC3
V_{DD}
Large current signal line
High-speed signal line
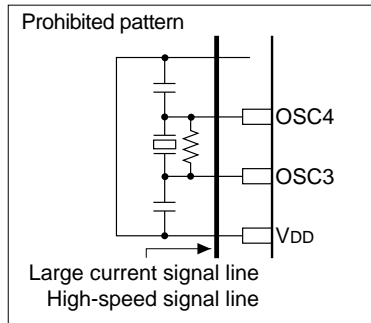
Precautions for Visible Radiation (when bare chip is mounted)

- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiation.

    (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

    (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

    (3) As well as the face of the IC, shield the back and side too.

CHAPTER 13   BASIC EXTERNAL CONNECTION DIAGRAM
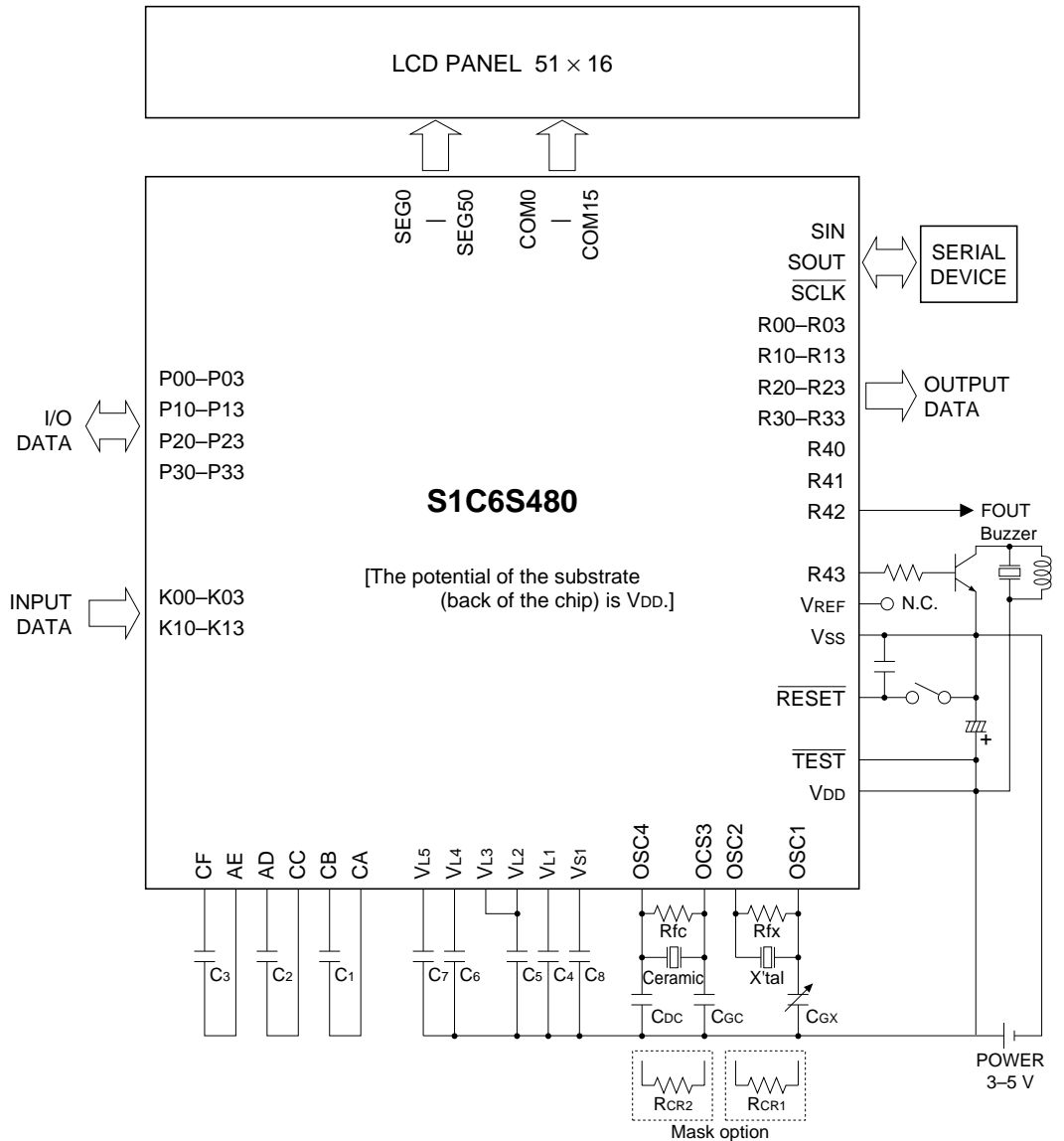
X'tal	Crystal oscillator	32.768 kHz, C_I(Max)=35 kΩ
Rfx	Feedback resistor	10 MΩ
C_{GX}	Trimmer capacitor	5–25 pF
(R_{CR1})	Resistor for OSC1 CR oscillation	1.6 MΩ (32 kHz Typ.)
Ceramic	Ceramic oscillator	500 kHz–2 MHz
Rfc	Feedback resistor	1 MΩ
C_{GC}	Gate capacitor	100 pF
C_{DC}	Drain capacitor	100 pF
(R_{CR2})	Resistor for OSC3 CR oscillation	20 kΩ–100 kΩ (VSC=2) 40 kΩ–100 kΩ (VSC=1)

C_1	Booster capacitor (1)	0.1μF *1
C_2	Booster capacitor (2)	0.1μF *1
C_3	Booster capacitor (3)	0.1μF *1
C_4	Capacitor between V_{DD} and V_{L1}	0.1μF *1
C_5	Capacitor between V_{DD} and V_{L2}	0.1μF *1
C_6	Capacitor between V_{DD} and V_{L4}	0.1μF *1
C_7	Capacitor between V_{DD} and V_{L5}	0.1μF *1
C_8	Capacitor between V_{DD} and V_{S1}	0.1μF

*1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C_1–C_3) and the capacitors between V_{DD} and liquid crystal system power (C_4–C_7).

Note: The above table is simply an example. Refer to Chapter 14, "Electrical Characteristics", for detailed characteristics.

CHAPTER *14* ELECTRICAL CHARACTERISTICS

14.1 Absolute Maximum Rating

(VDD=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW
Electrostatic proof pressure	V_E	EIAJ test method (C=200pF) 150V or more	V
		MIL test method (C=100pF, R=1.5kΩ) 900V or more	

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

14.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-5.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C_1				0.1		μF
Voltage booster capacitor (2)	C_2				0.1		μF
Voltage booster capacitor (3)	C_3				0.1		μF
Capacitor between V_{DD} and V_{L1}	C_4				0.1		μF
Capacitor between V_{DD} and V_{L2}	C_5				0.1		μF
Capacitor between V_{DD} and V_{L4}	C_6				0.1		μF
Capacitor between V_{DD} and V_{L5}	C_7				0.1		μF
Capacitor between V_{DD} and V_{S1}	C_8				0.1		μF

14.3 DC Characteristics

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047μF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level input voltage (1)	V_{IH1}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03, K10–13, P00–03, P10–13, P20–23, P30–33, SIN, $\overline{SCLK}$	0.2·V_{SS}		0	V
Low-level input voltage (1)	V_{IL1}			V_{SS}		0.8·V_{SS}	V
High-level input voltage (2)	V_{IH2}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage (2)	V_{IL2}			V_{SS}		V_{SS}+0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V, V_{IH}=0V	K00–03, K10–13, P00–03, P10–13, P20–23, P30–33, SIN, $\overline{SCLK}$, $\overline{RESET}$	0		0.5	μA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V, V_{IL1}=V_{SS} With Pull-up resistor		-45		-15	μA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V, V_{IL2}=V_{SS} No Pull-up resistor		-0.5		0	μA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03, P10–13, P20–23, P30–33, R00–03, R10–13, R20–23, R30–33, R40, R41, SOUT, $\overline{SCLK}$			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V, V_{OL1}=V_{SS}+0.5V		2.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42, R43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V, V_{OL2}=V_{SS}+0.5V		4.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	μA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			μA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–50			-10	μA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			μA

14.4 Analog Circuit Characteristics and Consumed Current

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047μF

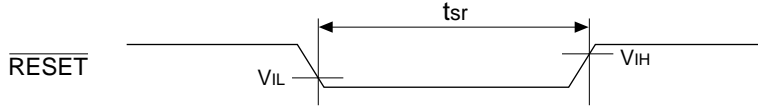| Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (Normal mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		1/2·V_{L2} -0.1		1/2·V_{L2} ×0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)	LC="0"		-1.80		
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"	Typ. ×1.12	-2.17	Typ. ×0.88	V
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3/2·V_{L2}		3/2·V_{L2} ×0.95	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		2·V_{L2}		2·V_{L2} ×0.95	V
LCD drive voltage (Heavy load protection mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)	LC="0"		-0.92		
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"	Typ. ×1.12	-1.11	Typ. ×0.88	V
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1}		2·V_{L1} ×0.90	V
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3·V_{L1}		3·V_{L1} ×0.90	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		4·V_{L1}		4·V_{L1} ×0.90	V
SVD voltage	V_{SVD0}	SVC="0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC="1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC="2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC="3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	μs
Current consumption [1] (OSC1/crystal oscillation)	I_{hlt}	During HALT (VSC="0", OSCC="0")			2.5	5.0	μA
	I_{EX1}	During operation at 32kHz (VSC="0", OSCC="0")			6.5	9.0	μA
	I_{EX2}	During operation at 1MHz (VSC="1")			400	600	μA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	μA
Current consumption [1] (OSC1/CR oscillation)	I_{hlt}	During HALT (VSC="0" or "1", OSCC="0")			20	70	μA
	I_{EX1}	During operation at f_{OSC1} (VSC="0" or "1", OSCC="0")			25	80	μA
	I_{EX2}	During operation at 1MHz (VSC="1")			420	600	μA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	μA

[1] No panel loard. The SVD circuit is in OFF status.

14.5 AC Characteristics

14.5.1 $\overline{\text{RESET}}$ input

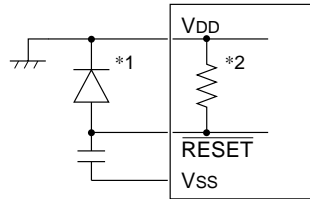Condition: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC1}=32.768kHz$, $Ta=25°C$, $V_{IH}=0.5V_{SS}$, $V_{IL}=0.9V_{SS}$

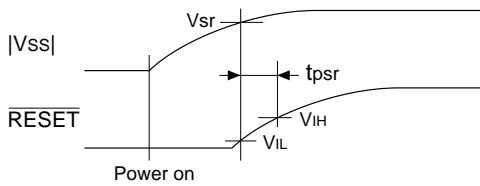| Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ input time	tsr	2.0			ms

14.5.2 Power-on reset

Condition: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC1}=32.768kHz$, $Ta=25°C$

Item	Symbol	Min.	Typ.	Max.	Unit
Operating power voltage	Vsr	-2.2			V
$\overline{\text{RESET}}$ input time	tpsr	2.0			ms

*1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

*2 Built-in pull-up resistor

14.6 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation characteristics

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Crystal: Q13MC146, C_{GX}=25pF, C_{DX}=built-in, Rfx=10MΩ, Ta=25°C, VSC="0"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V			5	s
Built-in drain capacitance	C_D	Package as assembled		20		pF
		Bare chip		19		pF
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustable range	$\partial f/\partial C_G$	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{SS})			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC1 CR oscillation characteristics

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="0" or "1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC1}	R_{CR1}=1.6MΩ	Typ. ×70%	32	Typ. ×130%	kHz
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR oscillation characteristics 1

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=60kΩ	Typ. ×70%	1,000	Typ. ×130%	kHz
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR oscillation characteristics 2

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=30kΩ	Typ. ×70%	2.0	Typ. ×130%	MHz
Oscillation start time	t_{sta}	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-3.5 to -5.5V	-5		+5	%

OSC3 ceramic oscillation characteristics 1

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1", Ceramic oscillator: CSB 1000J [1] (1MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-2.2 to -5.5V	-3		+3	%

∗1 Made by Murata Mfg. Co.
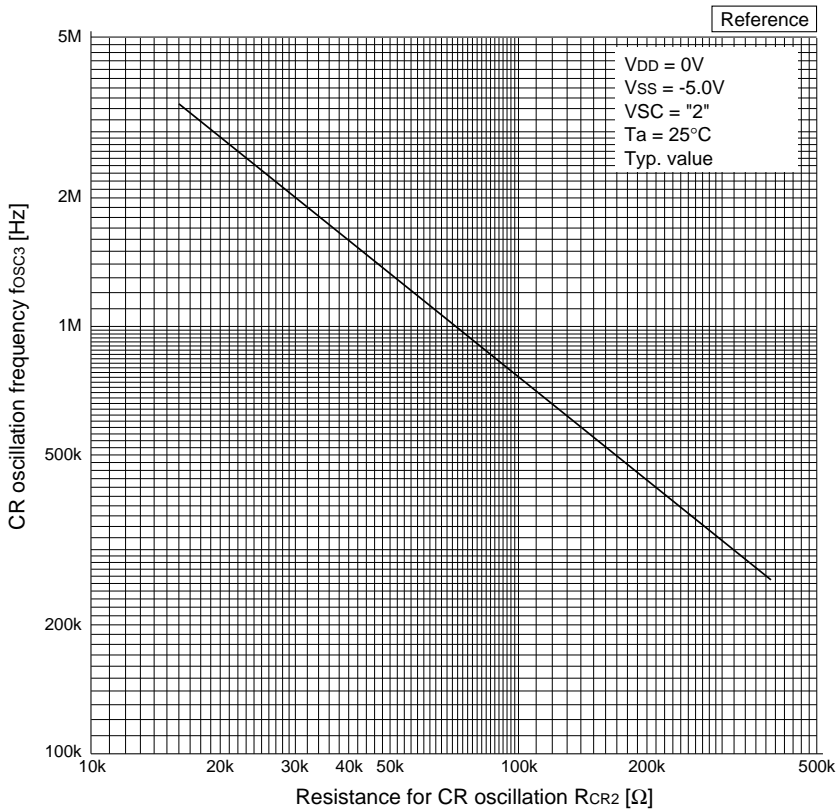
OSC3 ceramic oscillation characteristics 2

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2", Ceramic oscillator: CSA 2.00MG [1] (2MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

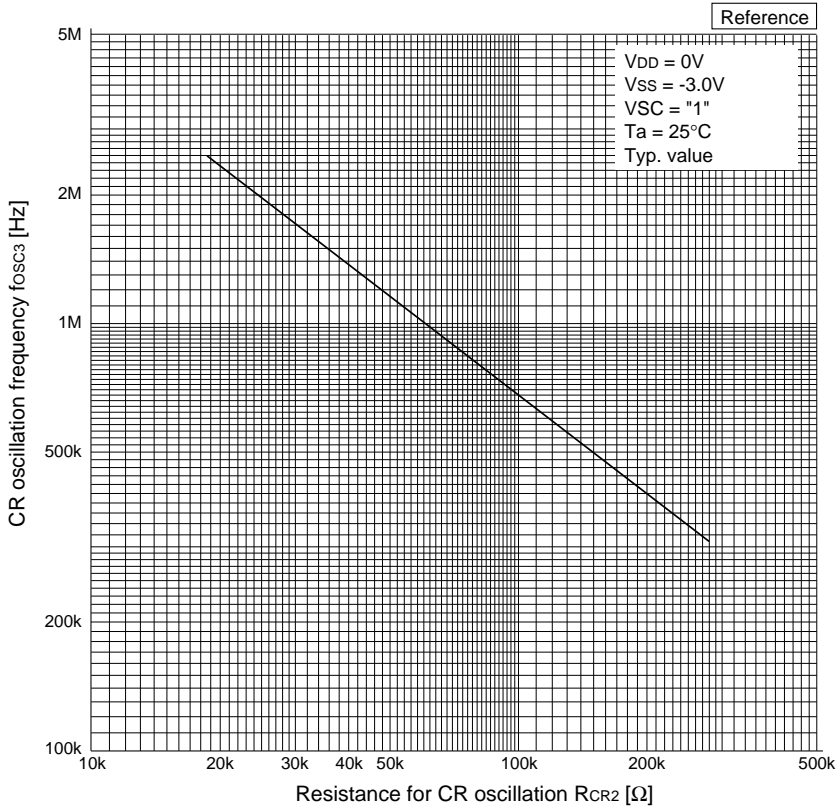| Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	$\partial f/\partial V$	V_{SS}=-3.5 to -5.5V	-3		+3	%

∗1 Made by Murata Mfg. Co.

OSC3 CR oscillation frequency - resistance characteristic

Reference

VDD = 0V
VSS = -3.0V
VSC = "1"
Ta = 25°C
Typ. value

CR oscillation frequency f_{OSC3} [Hz]

Resistance for CR oscillation R_{CR2} [Ω]

Reference

VDD = 0V
VSS = -5.0V
VSC = "2"
Ta = 25°C
Typ. value

CR oscillation frequency f_{OSC3} [Hz]

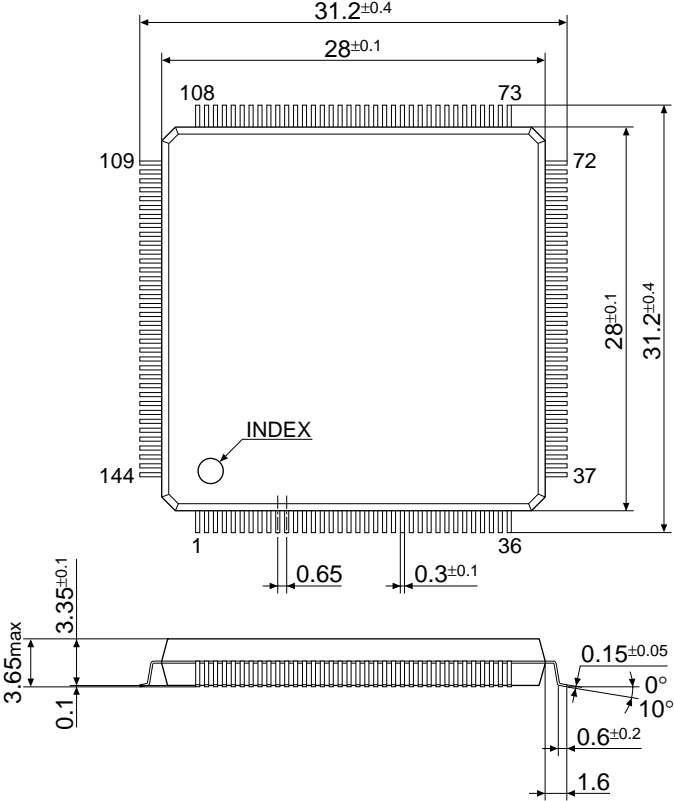Resistance for CR oscillation R_{CR2} [Ω]

CHAPTER 15 PACKAGE

15.1 Plastic Package

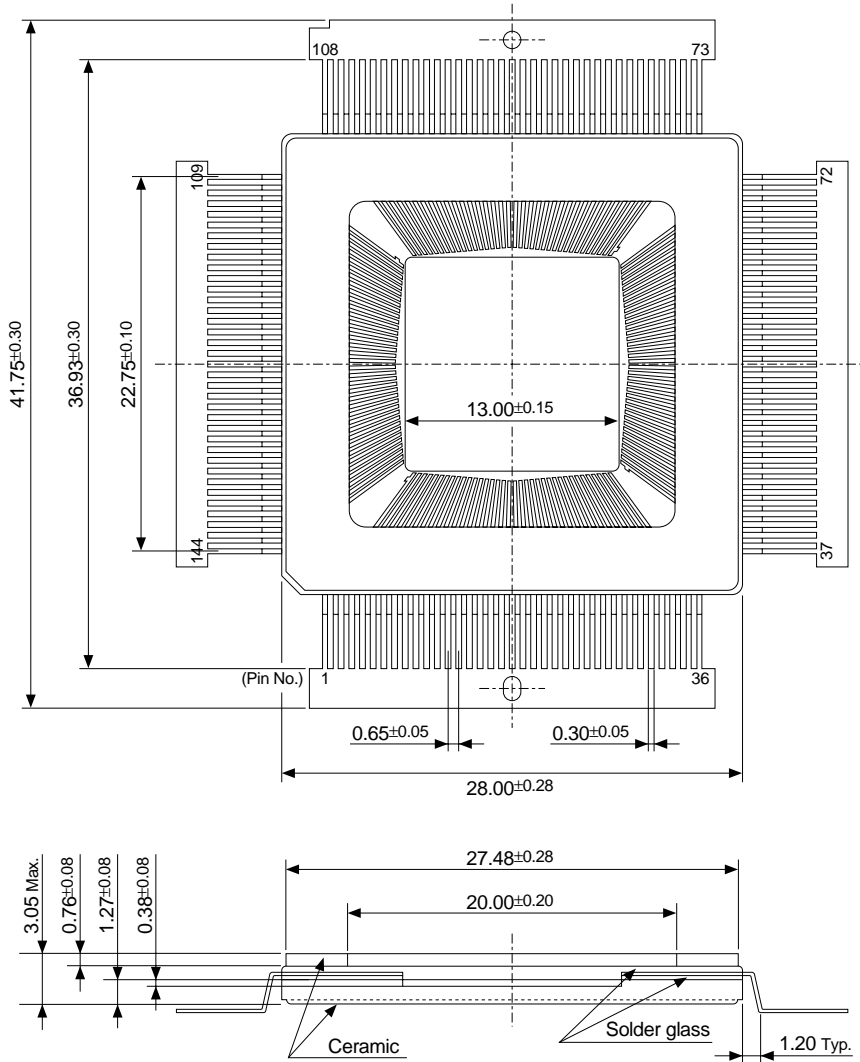**QFP8-144pin**

(Unit: mm)

15.2 Ceramic Package for Test Samples
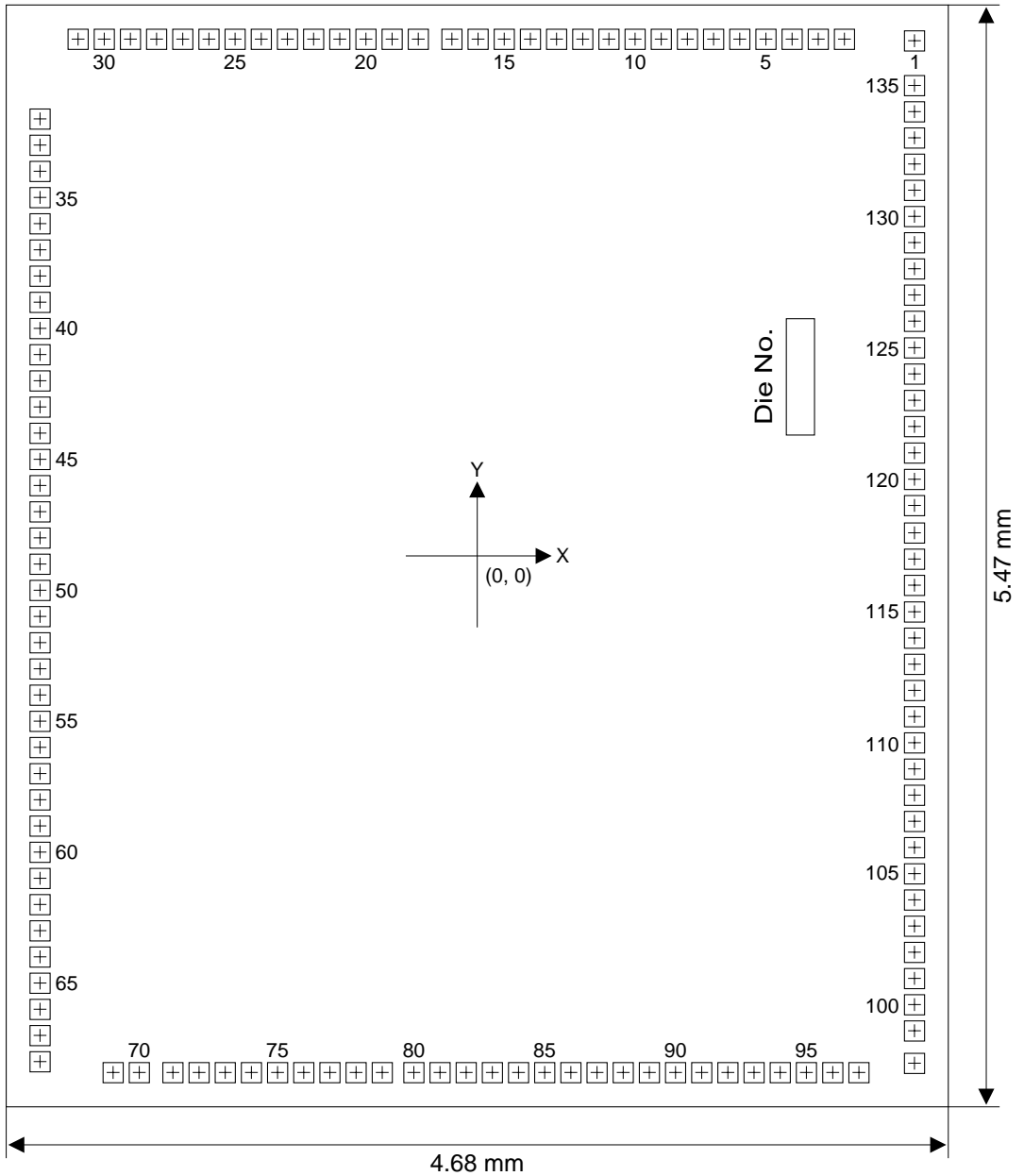
QFP8-144pin

(Unit: mm)

CHAPTER *16* P*AD* L*AYOUT*

16.1 Diagram of Pad Layout

Chip size: 4.68 mm × 5.47 mm
Pad size: 0.1 mm × 0.1 mm

16.2 Pad Coordinates

(unit: μm)

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
	Pad	Coordinate			Pad	Coordinate			Pad	Coordinate	
1	CA	2,172	2,557	46	SEG22	-2,172	349	91	P10	1,115	-2,565
2	COM0	1,824	2,565	47	SEG21	-2,172	219	92	P03	1,245	-2,565
3	COM1	1,694	2,565	48	SEG20	-2,172	89	93	P02	1,375	-2,565
4	COM2	1,564	2,565	49	SEG19	-2,172	-41	94	P01	1,505	-2,565
5	COM3	1,434	2,565	50	SEG18	-2,172	-171	95	P00	1,635	-2,565
6	COM4	1,304	2,565	51	SEG17	-2,172	-301	96	R43	1,766	-2,565
7	COM5	1,174	2,565	52	SEG16	-2,172	-431	97	R42	1,896	-2,565
8	COM6	1,044	2,565	53	SEG15	-2,172	-561	98	R41	2,172	-2,519
9	COM7	914	2,565	54	SEG14	-2,172	-691	99	R40	2,172	-2,358
10	COM8	784	2,565	55	SEG13	-2,172	-821	100	R33	2,172	-2,228
11	COM9	654	2,565	56	SEG12	-2,172	-951	101	R32	2,172	-2,098
12	COM10	524	2,565	57	SEG11	-2,172	-1,081	102	R31	2,172	-1,968
13	COM11	394	2,565	58	SEG10	-2,172	-1,211	103	R30	2,172	-1,838
14	COM12	264	2,565	59	SEG9	-2,172	-1,341	104	R23	2,172	-1,708
15	COM13	134	2,565	60	SEG8	-2,172	-1,471	105	R22	2,172	-1,578
16	COM14	4	2,565	61	SEG7	-2,172	-1,601	106	R21	2,172	-1,448
17	COM15	-126	2,565	62	SEG6	-2,172	-1,731	107	R20	2,172	-1,318
18	SEG50	-293	2,565	63	SEG5	-2,172	-1,861	108	R13	2,172	-1,188
19	SEG49	-423	2,565	64	SEG4	-2,172	-1,991	109	R12	2,172	-1,058
20	SEG48	-553	2,565	65	SEG3	-2,172	-2,121	110	R11	2,172	-928
21	SEG47	-683	2,565	66	SEG2	-2,172	-2,251	111	R10	2,172	-798
22	SEG46	-813	2,565	67	SEG1	-2,172	-2,381	112	R03	2,172	-668
23	SEG45	-943	2,565	68	SEG0	-2,172	-2,511	113	R02	2,172	-538
24	SEG44	-1,073	2,565	69	$\overline{SCLK}$	-1,809	-2,565	114	R01	2,172	-408
25	SEG43	-1,203	2,565	70	SOUT	-1,679	-2,565	115	R00	2,172	-278
26	SEG42	-1,333	2,565	71	SIN	-1,512	-2,565	116	V$_{SS}$	2,172	-146
27	SEG41	-1,463	2,565	72	K13	-1,382	-2,565	117	$\overline{RESET}$	2,172	-16
28	SEG40	-1,593	2,565	73	K12	-1,252	-2,565	118	$\overline{TEST}$	2,172	114
29	SEG39	-1,723	2,565	74	K11	-1,122	-2,565	119	OSC4	2,172	250
30	SEG38	-1,853	2,565	75	K10	-992	-2,565	120	OSC3	2,172	380
31	SEG37	-1,983	2,565	76	K03	-862	-2,565	121	V$_{S1}$	2,172	511
32	SEG36	-2,172	2,169	77	K02	-732	-2,565	122	OSC2	2,172	642
33	SEG35	-2,172	2,039	78	K01	-602	-2,565	123	OSC1	2,172	772
34	SEG34	-2,172	1,909	79	K00	-472	-2,565	124	V$_{DD}$	2,172	903
35	SEG33	-2,172	1,779	80	P33	-315	-2,565	125	V$_{REF}$	2,172	1,033
36	SEG32	-2,172	1,649	81	P32	-185	-2,565	126	V$_{L1}$	2,172	1,165
37	SEG31	-2,172	1,519	82	P31	-55	-2,565	127	V$_{L2}$	2,172	1,295
38	SEG30	-2,172	1,389	83	P30	75	-2,565	128	V$_{L3}$	2,172	1,425
39	SEG29	-2,172	1,259	84	P23	205	-2,565	129	V$_{L4}$	2,172	1,555
40	SEG28	-2,172	1,129	85	P22	335	-2,565	130	V$_{L5}$	2,172	1,685
41	SEG27	-2,172	999	86	P21	465	-2,565	131	CF	2,172	1,815
42	SEG26	-2,172	869	87	P20	595	-2,565	132	CE	2,172	1,945
43	SEG25	-2,172	739	88	P13	725	-2,565	133	CD	2,172	2,075
44	SEG24	-2,172	609	89	P12	855	-2,565	134	CC	2,172	2,205
45	SEG23	-2,172	479	90	P11	985	-2,565	135	CB	2,172	2,335

EPSON   International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.

- HEADQUARTERS -
1960 E. Grand Avenue
El Segundo, CA 90245, U.S.A.
Phone: +1-310-955-5300   Fax: +1-310-955-5400

- SALES OFFICES -

West
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-408-922-0200   Fax: +1-408-922-0238

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
Phone: +1-815-455-7630   Fax: +1-815-455-7633

Northeast
301 Edgewater Place, Suite 120
Wakefield, MA 01880, U.S.A.
Phone: +1-781-246-3600   Fax: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-EEA-0020   Fax: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH

- HEADQUARTERS -
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-(0)89-14005-0   Fax: +49-(0)89-14005-110

SALES OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-(0)2171-5045-0   Fax: +49-(0)2171-5045-10

UK BRANCH OFFICE
Unit 2.4, Doncastle House, Doncastle Road
Bracknell, Berkshire RG12 8PE, ENGLAND
Phone: +44-(0)1344-381700   Fax: +44-(0)1344-381701

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-(0)1-64862350   Fax: +33-(0)1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Prima Sant Cugat
Avda. Alcalde Barrils num. 64-68
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490   Fax: +34-93-544-2491

ASIA

EPSON (CHINA) CO., LTD.
28F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: 64106655   Fax: 64107319

SHANGHAI BRANCH
4F, Bldg., 27, No. 69, Gui Jing Road
Caohejing, Shanghai, CHINA
Phone: 21-6485-5552   Fax: 21-6485-0775

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 Fax: +852-2827-4346
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EPSON TAIWAN TECHNOLOGY & TRADING LTD.
10F, No. 287, Nanking East Road, Sec. 3
Taipei
Phone: 02-2717-7360   Fax: 02-2712-9164
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HSINCHU OFFICE
13F-3, No. 295, Kuang-Fu Road, Sec. 2
HsinChu 300
Phone: 03-573-9900   Fax: 03-573-9169

EPSON SINGAPORE PTE., LTD.
No. 1 Temasek Avenue, #36-00
Millenia Tower, SINGAPORE 039192
Phone: +65-337-7911   Fax: +65-334-2716

SEIKO EPSON CORPORATION KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: 02-784-6027   Fax: 02-767-3677

SEIKO EPSON CORPORATION
ELECTRONIC DEVICES MARKETING DIVISION

Electronic Device Marketing Department
IC Marketing & Engineering Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5816   Fax: +81-(0)42-587-5624

ED International Marketing Department Europe & U.S.A.
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5812   Fax: +81-(0)42-587-5564

ED International Marketing Department Asia
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-(0)42-587-5814   Fax: +81-(0)42-587-5110

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