3-Pin Microprocessor Reset with Time-out and Voltage Window

Features

- Voltage Window monitoring
- Clear microprocessor restart after power up
- Processor reset at power down
- Reset output guaranteed down to V_{DD} = 1 V
- Low power consumption: typ. 3 µA at V_{DD} = 5 V
- - 40 to +85 °C temperature range
- On request extended temperature range, -40 to +125 °C
- On-chip oscillator
- No external components required
- Push-pull or Open drain output
- TO-92 package
- Pin compatible with MC 33164

Description

The V6330 is a CMOS device which monitors the supply voltage of any electronic system, and generates the appropriate Reset signal. The gap between the two thresholds defines the allowed voltage range. As long as V_{DD} stays inside this voltage window, the output stays inactive. If V_{DD} drops below V_{THlow}, or rises above V_{THhigh}, the output gets active. When V_{DD} enters into the allowed range, the output remains active for an additional 50 ms (typ.). This allows the system to stabilize before getting fully active. The lower threshold voltage may be obtained in different versions:

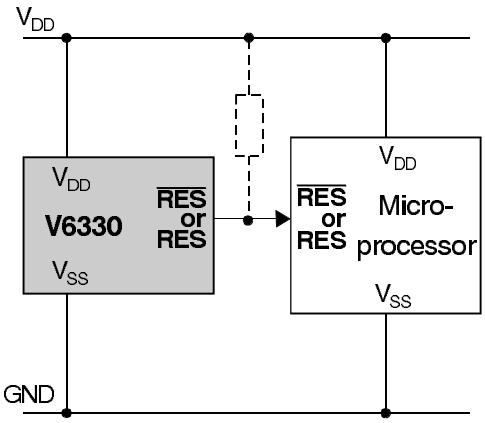
2.0 V to 6 V
2.4 V to 6 V
2.8 V to 6 V
3.5 V to 6 V
4.0 V to 6 V
4.5 V to 6 V

Applications

All microprocessor applications where an automatic restart is required:

- Computer electronics
- White / Brown goods
- Automotive electronics
- Industrial electronics
- Telecom systems
- Hand-held systems

Typical Operating Configuration



For Open drain version: - - - - - -

Fig. 1

Pin Assignment

TO-92

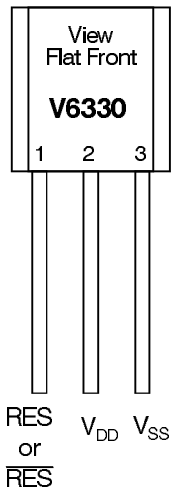


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage at V_{DD} to V_{SS}	V_{DD}	-0.3V to+10 V
Min. voltage at RES or $\overline{RES}$	V_{min}	V_{SS} - 0.3 V
Max. voltage at RES or $\overline{RES}$	V_{max}	V_{DD} + 0.3 V
Storage temperature range	T_{STO}	-65° to +150 °C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature[1)]	T_A	-40		+125	°C
Positive supply voltage	V_{DD}	1		8	V

Table 2

[1)] The maximum operating temperature is confirmed by sampling at initial device qualification.

Electrical Characteristics

T_A = -40 to +85 °C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Min. at 25 °C	Typ.	Max. at 25 °C	Max.	Units
Supply current [1)]	I_{DD}	V_{DD} = 2 V			1.5	2.1	3.1	µA
	I_{DD}	V_{DD} = 5 V			3.0	3.9	5.7	µA
	I_{DD}	V_{DD} = 8 V			5.2	6.8	10.0	µA
Threshold Low Voltage	$V_{TH\ low}$	Version: A,G,M	1.77	1.84	1.95	2.04	2.17	V
	$V_{TH\ low}$	Version: B,H,N	2.09	2.18	2.32	2.41	2.55	V
	$V_{TH\ low}$	Version: C,I,O	2.48	2.59	2.73	2.86	3.03	V
	$V_{TH\ low}$	Version: D,J,P	3.11	3.23	3.42	3.59	3.80	V
	$V_{TH\ low}$	Version: E,K,Q	3.55	3.70	3.88	4.08	4.32	V
	$V_{TH\ low}$	Version: F,L,R	4.05	4.22	4.42	4.67	4.95	V
Threshold High Voltage	$V_{TH\ high}$		5.58	5.79	6.10	6.42	6.82	V
Threshold hysteresis	V_{HYS}				25			mV
RES Output Low Level	V_{OL}	V_{DD} = 5 V, I_{OL} = 8 mA			175		400	mV
	V_{OL}	V_{DD} = 3 V, I_{OL} = 4 mA			140		300	mV
	V_{OL}	V_{DD} = 1 V, I_{OL} = 50 µA			20		90	mV
RES Output High Level	V_{OH}	V_{DD} = 5 V, I_{OH} = -8 mA	4.3		4.5			V
	V_{OH}	V_{DD} = 3 V, I_{OH} = -4 mA	2.3		2.6			V
	V_{OH}	V_{DD} = 1 V, I_{OH} = -100 µA	850		950			mV
Output leakage current [2)]	I_{LEAK}	V_{DD} = 5.5 V			0.05		1	µA

[1)] RES or $\overline{RES}$ open

[2)] Only for Open drain versions

Table 3

Timing Characteristics

V_{DD} = 5.0 V, T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Power on reset time	t_{POR}		25	50	75	ms
Sensitivity around V_{THhigh} [3)]	$t_{SEN\ high}$	for V_{DD} = 5 V to 7 V in 5 µs	18	0.8 t_{Rhigh}		µs
Sensitivity around V_{THlow} [3)]	$t_{SEN\ low}$	for V_{DD} = 5 V to 3 V in 5 µs	20	0.8 t_{Rlow}		µs
Reaction time around V_{THhigh} [3)]	$t_{R\ high}$	for V_{DD} = 5 V to 7 V in 5 µs	20	55	90	µs
Reaction time around V_{THlow} [3)]	$t_{R\ low}$	for V_{DD} = 5 V to 3 V in 5 µs	22	75	150	µs

[3)] Tested on versions with V_{THlow} higher than 3 V

Table 4

Timing Waveforms

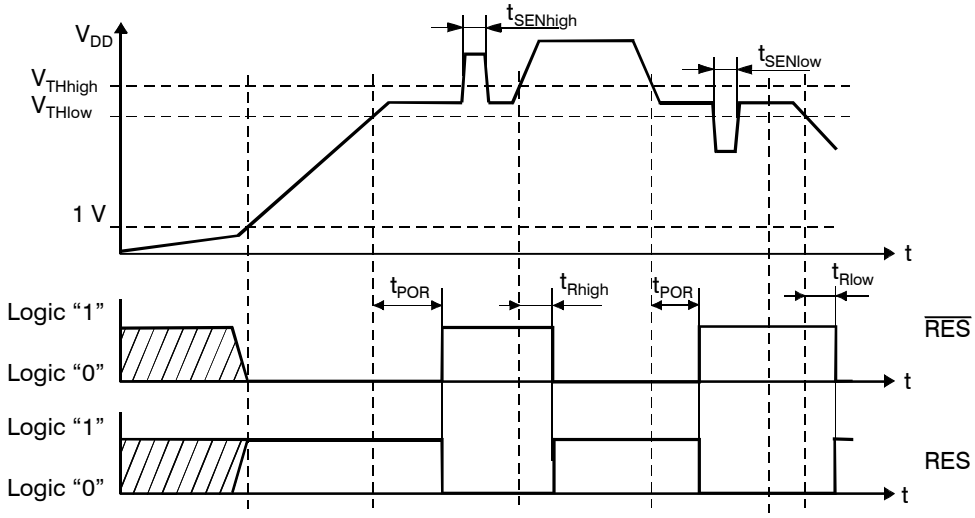


Fig.3

Block Diagram

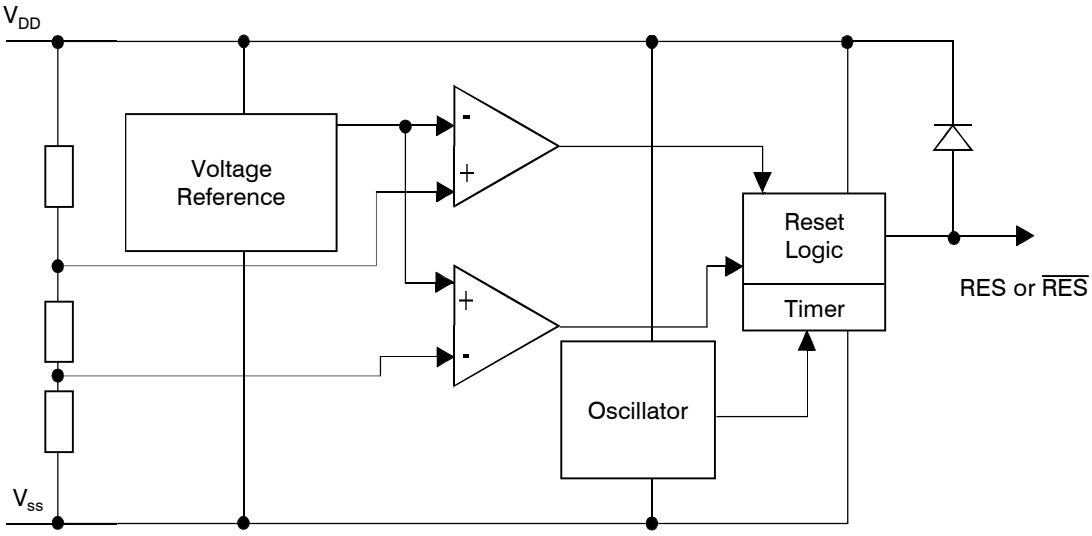


Fig.4

Pin Description

TO-92

Pin	Name	Function
1	RES or $\overline{RES}$	Reset output
2	V_{DD}	Positive Supply
3	V_{SS}	Supply ground

Table 5

Ordering Information

The V6330 is available with Push-pull or Open output stage and Reset active low or high.

Ordering form: V6330 <version letter> < packaging>

Example: Smart reset with: - Reset active low

- Open drain output

- 3.5 V threshold

- TO-92 package

V6330 P TO-92

When ordering, please specify the complete part number.

Version letter definition

Output stage	Threshold Low Voltage [V]					
	2.0	2.4	2.8	3.5	4.0	4.5
Push-pull, Reset active low	A[1)]	B[1)]	C[1)]	D[1)]	E	F
Push-pull, Reset active high	G[1)]	H[1)]	I[1)]	J[1)]	K[1)]	L[1)]
Open drain, Reset active low	M[1)]	N[1)]	O[1)]	P	Q[1)]	R[1)]

Table 6

Chip form on request

[1)] Non-stock items, minimum order 30 K pieces.