Parallel EEPROMs Compiler

Preliminary

Features

- **Flexible Architecture**
  - 16-16K words
  - Max 64K bits
  - Support Data Bus width 4-128 bits in 4 bit increments
- **Fast Read Access Time**
  - 100ns
- **Fast Self-Timed Byte Write Cycle**
  - 1ms
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- **Fast Self-Timed Write All**
  - 8ms
  - Automatic Clear Before Write
- **Direct Microprocessor Control**
  - READY/BUSY
- **3.3V ± 10% Supply**
- **Low Power**
  - 5 mA Active Current
  - 10 µA CMOS Standby Current
- **High Reliability**
  - Endurance: 10^5 Cycles
  - Data Retention: 10 Years
- **Direct Microprocessor Control**
  - Asynchronous clear
  - Independent output enables
- **Commercial and Industrial Temperature Ranges**
- **Advanced Double Poly Triple Metal Embedded EEPROM Process**

General Description

The EEPROM Compiler will generate low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The device is manufactured with ICT's reliable nonvolatile CMOS technology.

The EEPROM Compiler is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes a method for detecting the end of a write cycle, level detection of RDY/BUSY. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 100 ns at low power dissipation. When the chip is deselected the standby current is less than 10 µA.

Figure 1 Pin Configurations

Pin Name	Function
A0 - A13*	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O31*	Data Inputs/Outputs
RDY/$\overline{BUSY}$	Ready/$\overline{Busy}$ Output
$\overline{ALLEN}$	Write All Enable
RESET	$\overline{RESET}$ Input

* number of addresses and I/O's are determined by user specified architecture

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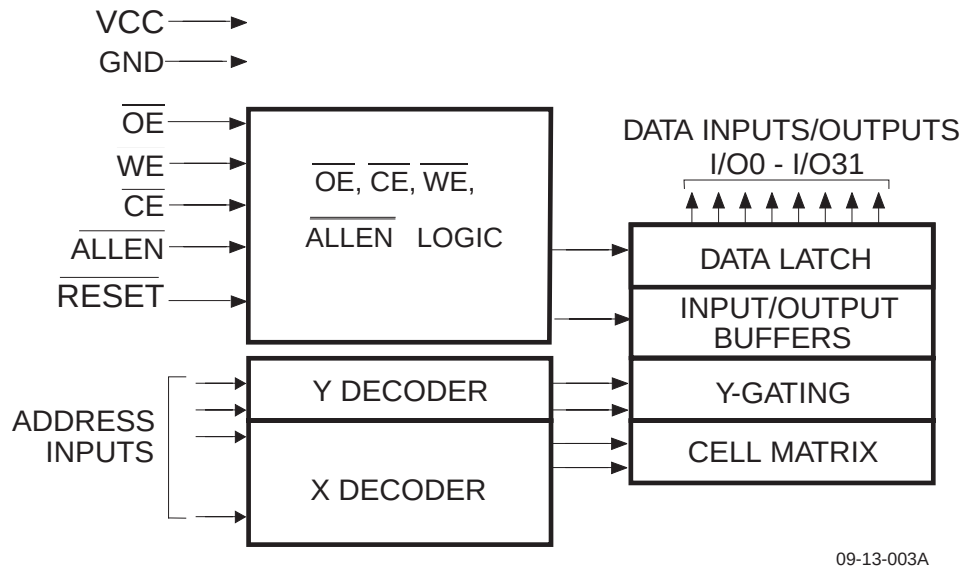
BLOCK DIAGRAM



Device Operation

READ: The EEPROM is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the EEPROM is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{ALLEN}$ and $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion.

READY/$\overline{BUSY}$: READY/$\overline{BUSY}$ output can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write.

WRITE PROTECTION: Inadvertent writes to the device are protected against by holding any one of $\overline{CE}$ high, $\overline{RESET}$ low or $\overline{WE}$ high inhibits byte write cycles.

See the operating modes table for NORMAL, ERASE ALL, WRITE ALL operation.

Write ALL: Writing data into the EEPROM is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{ALLEN}$ low and $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a WRITE ALL. Internally, the device performs a selfclear before write. Once a WRITE ALL has been started, it will automatically time itself to completion.

DC and AC Operating Range

EEPROM		
Operating Temperature (Case)	Commercial	0°C - 70°C
	Industrial	-40°C - 85°C
Supply Voltage		3.3V ± 10%

Operating Modes

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	$\overline{ALLEN}$	$\overline{RESET}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	X	V_{IH}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{IH}	V_{IH}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z	X	V_{IH}
Write Inhibit	X	X	V_{IH}		X	X
Write Inhibit	X	X	X		X	V_{IL}
Output Disable	X	V_{IH}	X	High Z	X	V_{IH}
WRAL	V_{IL}	V_{IH}	V_{IL}	High Z	V_{IL}	V_{IH}

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

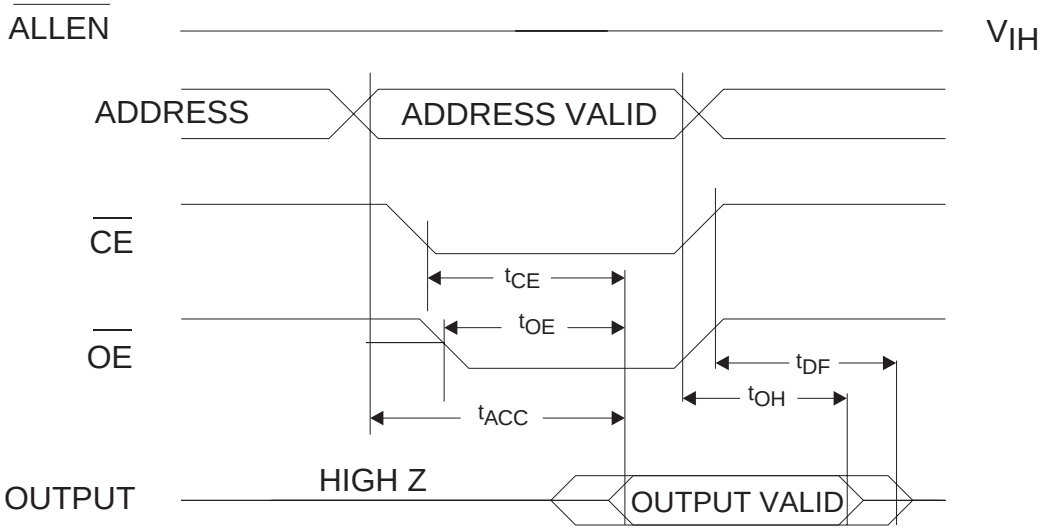
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MH_Z; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		5	mA
			Ind.		5	mA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} =600µA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -600µA		2.0		V

AC Read Characteristics

Symbol	Parameter	EEPROM		Units
		Min	Max	
T_{ACC}	Address to Output Delay		100	ns
T_{CE}(1)	$\overline{CE}$ to Output Delay		100	ns
T_{OE}(2)	$\overline{OE}$ to Output Delay	10	70	ns
T_{DF}(3)(4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	ns
T_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms (1)(2)(3)(4)



Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

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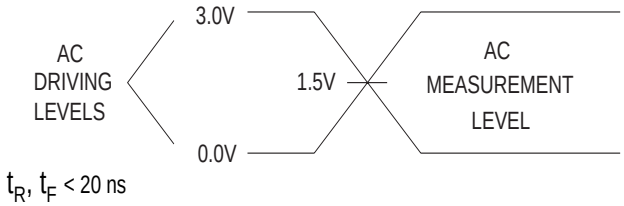
Input Test Waveforms and Measurement Level



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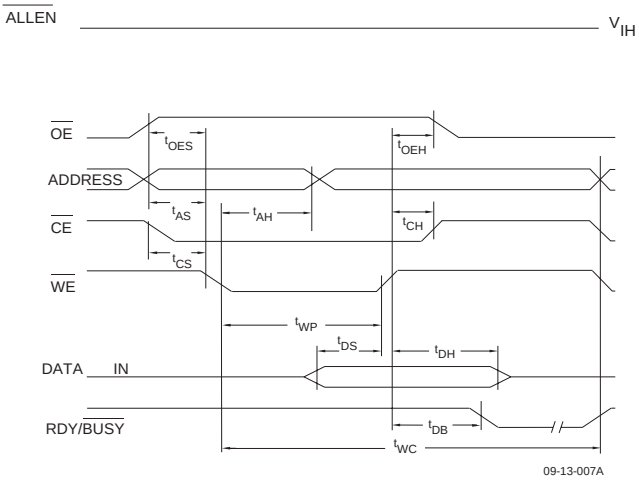
AC Write Characteristics

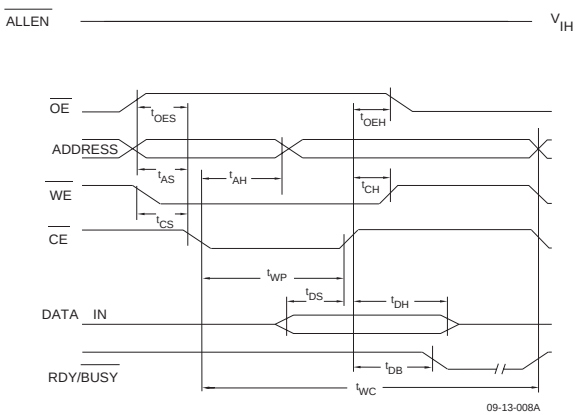
Symbol	Parameter	Min	Type	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10			ns
t_{AH}	Address Hold Time	50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		1000	ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}, T_{OEH}	Data, $\overline{OE}$ Hold Time	10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time	0			ns
t_{DB}	Time to Device Busy			50	ns
t_{WC}	Write Cycle Time		0.5	1.0	ms
T_{WCALL}	Write All Cycle Time		5	10	ms

AC Write Waveforms

$\overline{WE}$ Controlled

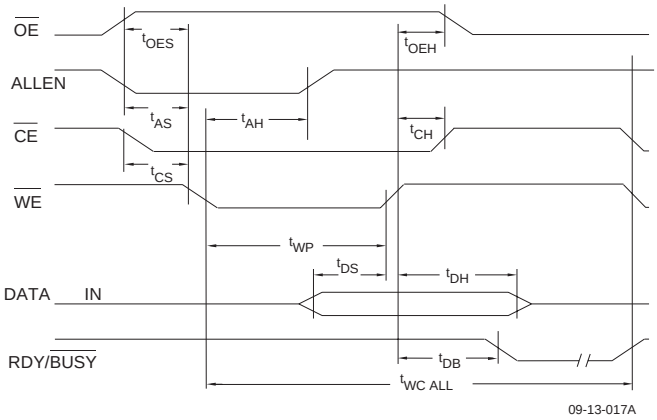


$\overline{CE}$ Controlled

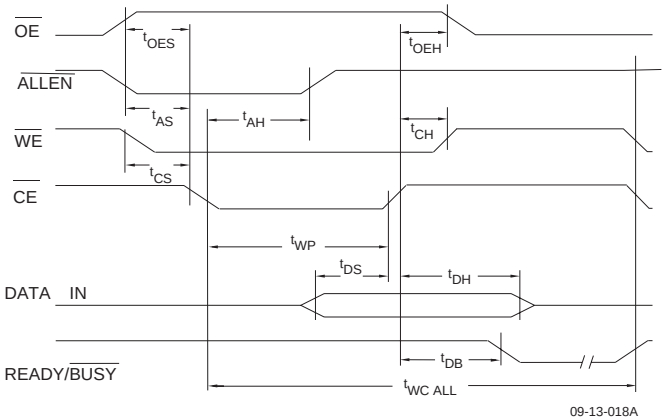


Write All Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



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