

1.5V 1:10 HSTL Fanout Buffer

Features

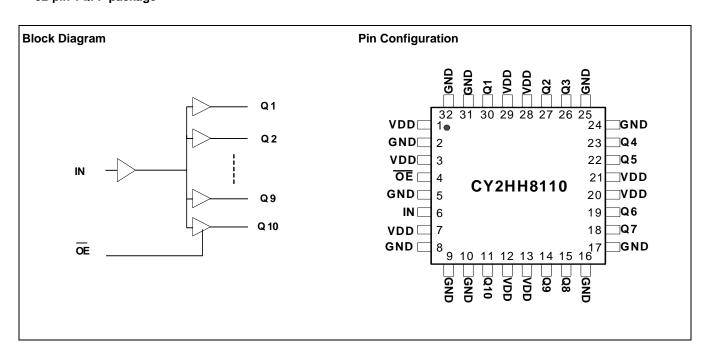
- DC to 150-MHz operation
- 1.5V power supply
- One single-ended HSTL input
- Ten single-ended Class II HSTL outputs
- Less than 1.9% Duty Cycle distortion
- Balanced 16-mA output drive
- Output Enable/Disable
- · Low output-output skew
- Operating temperature range: 0°C to +85°C
- 32-pin TQFP package

Description

The CY2HH8110 is a low-voltage HSTL fanout buffer designed for data communications, clock management, and specialty memory applications.

The class II HSTL outputs are balanced Push-Pull in design capable of delivering 16 mA into 10 pF load. This class allows both source series termination and symmetrically double parallel termination.

The CY2HH8110 low-output duty cycle distortion makes it suitable for Double Data Rate (DDR) applications.





Pin Description^[1]

Pin	Name	I/O	Туре	Description
6	IN	I	HSTL	HSTL reference clock input
30, 27, 26, 23, 22, 19, 18, 15, 14, 11	Q(1:10)	0	HSTL	HSTL clock outputs
4	OE	I, PD	LVCMOS	Output enable/disable input. When held LOW, outputs are enabled. When set HIGH, all outputs are disabled LOW.
1, 3, 7, 12, 13, 20, 21, 28, 29	VDD	Supply	VDD	1.5V power supply ^[2]
2, 5, 8, 9, 10, 16, 17, 24, 25, 31, 32	GND	Supply	Ground	Common ground

Notes:

PD = Internal pull down.
 A 0.1-uF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the trace.



Absolute Maximum Conditions

C Supply Voltage C Operating Voltage C Input Voltage C Output Voltage Itput termination Voltage Itch Up Immunity	Functional Relative to V _{SS} , with or V _{DD} applied Relative to V _{SS}	-0.5 1.35 -0.5 -0.5	2.5 1.65 V _{DD} + 0.5 V _{DD} + 0.5 V _{DD} ÷ 2	V V V V
C Input Voltage C Output Voltage Itput termination Voltage	Relative to V _{SS} , with or V _{DD} applied Relative to V _{SS}	-0.5 -0.5	V _{DD} + 0.5	V
C Output Voltage Itput termination Voltage	applied Relative to V _{SS}	-0.5	V _{DD} + 0.5	V
tput termination Voltage	30			•
	Functional	222	V _{DD} ÷ 2	V
tch Up Immunity	Functional	000		
		200		mA
wer Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
mperature, Storage	Non-functional	-65	+150	°C
mperature, Operating Ambient	Functional	0	+85	°C
mperature, Junction	Functional		+150	°C
ssipation, Junction to Case	Functional		42	°C/W
ssipation, Junction to Ambient	Functional		105	°C/W
D Protection (Human Body odel)		1600		V
ilure in Time	Manufacturing test	10 ppm		
n n Si Si	nperature, Storage nperature, Operating Ambient nperature, Junction sipation, Junction to Case sipation, Junction to Ambient D Protection (Human Body del) lure in Time	nperature, Storage nperature, Operating Ambient nperature, Junction sipation, Junction to Case sipation, Junction to Ambient D Protection (Human Body del) lure in Time Non-functional Functional Functional Functional Functional Functional	nperature, Storage Non-functional —65 nperature, Operating Ambient Functional 0 nperature, Junction Functional sipation, Junction to Case Functional sipation, Junction to Ambient Functional D Protection (Human Body del) Iure in Time Manufacturing test	nperature, Storage Non-functional —65 +150 nperature, Operating Ambient Functional 0 +85 nperature, Junction Functional +150 sipation, Junction to Case Functional 42 sipation, Junction to Ambient Functional 105 D Protection (Human Body del)

DC Electrical Specifications (V_{DD} = 1.5V \pm 8%, T_A = 0°C to +85°C)

Parameter	Description	Condition	Min.	Тур.	Max.	Unit
V _{IL}	Input Voltage, Low	HSTL input, V _{REF} = 0.75V	-0.30	_	0.65	V
V _{IH}	Input Voltage, High		0.85	_	1.80	V
V _{IL}	Input Voltage, Low	OE# input	-0.30	_	0.3 * V _{DD}	V
V _{IH}	Input Voltage, High		0.7 * V _{DD}	_	V _{DD} + 0.3	V
V _{OL}	Output Voltage, Low ^[3]	I _{OL} = 16 mA	-0.3	_	0.4	V
V _{OH}	Output Voltage, High ^[3]	I _{OH} = -16 mA	1.0	_	V _{DD} + 0.3	V
I _{IL}	Input Current, Low ^[4]	$V_{IL} = V_{SS}$	-	_	-10	μΑ
I _{IH}	Input Current, High ^[4]	$V_{IH} = V_{DD}$	-	_	100	μΑ
I _{DDQ}	Quiescent Supply Current	V _{IN} = 0V, outputs disabled	-	_	1	mΑ
I _{DD}	Dynamic Supply Current	Outputs loaded @ 62.5 MHz	_	215	250	mΑ
C _{IN}	Input Pin Capacitance		_	_	6	pF
C _{OUT}	Output Pin Capacitance		_	4.5	6	pF
Z _{OUT}	Output Impedance		_	25	_	Ω

AC Electrical Specifications (V_{DD} = 1.5V ± 8%, T_A = 0°C to +85°C) [5]

Parameter	Description	Description Condition		Тур.	Max.	Unit	
f _{in}	Input Frequency		_	_	150	MHz	
V _{IL} (AC)	AC Input HIGH Voltage	V _{REF} =V _{DD} /2, Internal Voltage	0.95	_		V	
V _{IH} (AC)	AC Input LOW Voltage	Reference	_	_	0.55	V	
t _r , t _f	Output rise/fall time ^[6]	20% to 80%	0.3	_	1.5	ns	
DC	Output duty cycle	Fout < 100 MHz	48	_	52	%	
1		Fout > 100 MHz	45	_	55	1	

Notes:

- 3. Driving 50Ω series terminated or symmetrically double parallel terminated transmission line to a termination voltage of V_{TT} .
- Inputs have pull-down resistors that affect the input current.

 AC characteristics apply for series or parallel output termination to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.
- tr/tf times are faster with parallel terminated loads.



AC Electrical Specifications ($V_{DD} = 1.5V \pm 8\%$, $T_A = 0$ °C to +85°C) (continued)^[5]

Parameter	Description	Condition	Min.	Тур.	Max.	Unit
tjit_DCD	Output Duty Cycle Distortion	Measure Jitter delay between input and output at V _{DD} /2 @ f _{REF} = 62.5 MHz	-	-	300	ps
l		DCD @ f _{REF} = 62.5 MHz	_	_	1.9	%
t _{sk(O)}	Output-to-Output Skew		_	_	200	ps
tsk(pp)	Part-to-Part Skew		_	_	2	ns
t _{PLH}	Propagation Delay, Low to High		_	_	7	ns
t _{PHL}	Propagation Delay, High to Low		_	-	7	ns
t _{Qoff}	Output Disable Time		_	_	7	ns
t _{Qon}	Output Enable Time		_	_	7	ns
t _{JIT(CC)}	Cycle-to-Cycle Jitter, Deterministic jitter		_	10	50	ps

Parameter Measurement Information

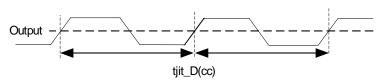


Figure 1. Cycle-to-Cycle Jitter

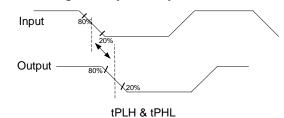


Figure 2. Propagation Delay from Input Reference to Output n

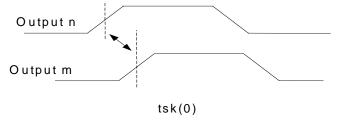


Figure 3. Output to Output Skew

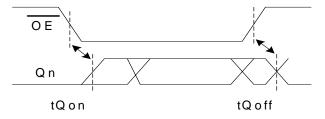


Figure 4. Output Enable/Disable Time



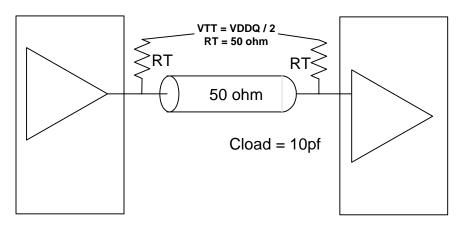


Figure 5. An Example HSTL Symmetrically Double Parallel Terminated Output Load | and CLASS II HSTL AC Test Load $^{[7,8]}$

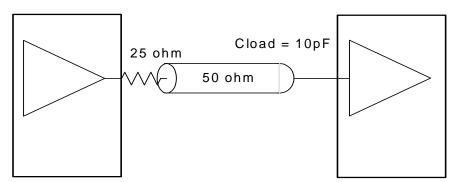


Figure 6. An Example HSTL Source Series Terminated Output Load $^{[7,8]}$

Ordering Information

Part Number	Package Type	Product Flow	
CY2HH8110AC	32-pin TQFP	Commercial, 0°C to +85°C	
CY2HH8110ACT	32-pin TQFP – Tape and Reel	Commercial, o C to +05 C	

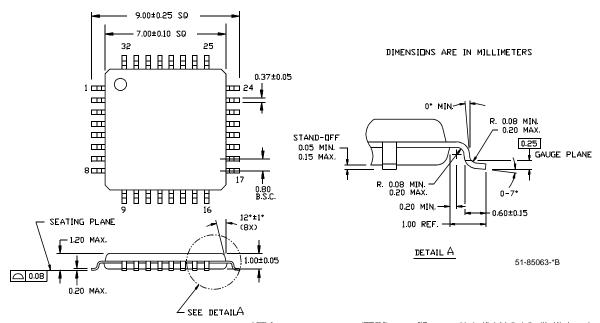
Notes:

- HSTL to HSTL input. Cload includes probe and test board capacitance.



Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



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Document History Page

Document Title:CY2HH8110 1.5V 1:10 HSTL Fanout Buffer Document Number: 38-07556				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	128398	08/04/03	RGL	New Data Sheet