BlueCore™3-Multimedia

Single Chip Bluetooth® System

Advance Information Datasheet For

BC358239A

June 2003

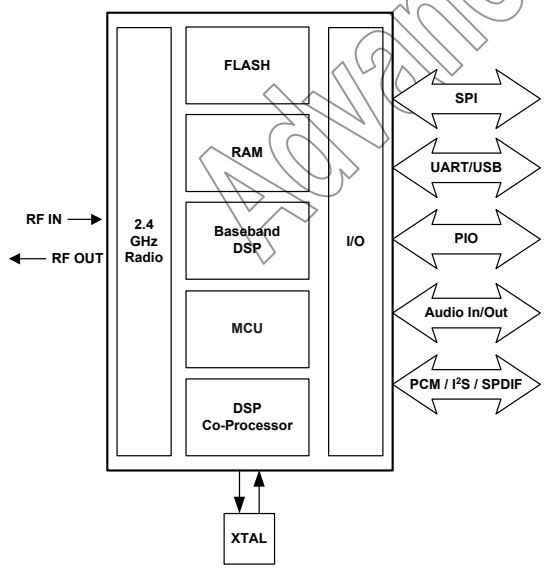
Device Features

- Fully Qualified Bluetooth system
- Bluetooth v1.2 Specification Compliant
- DSP Open Platform Co-Processor
- Full Speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Low Power 1.8V Operation
- 10 x 10mm 96-ball LFBGA Package
- Minimum External Components
- Integrated 1.8V regulator
- Dual UART Ports
- 16-bit Stereo Audio CODEC
- I^2S and SPDIF Interfaces
- RF 'Plug 'n' Go' package

General Description

BlueCore3-Multimedia is a single chip radio and baseband IC for Bluetooth 2.4GHz systems.

BC358239A contains 8Mbit of internal Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v1.2 of the specification for data and voice communications.



BlueCore3-Multimedia System Architecture

Applications

- Stereo Headphones
- Automotive Hands-Free Kits
- Echo Cancellation
- High Performance Telephony Headsets
- Enhanced Audio Applications
- A/V Profile Support

BlueCore3-Multimedia contains an open platform digital signal processor (DSP) co-processor allowing for support of enhanced audio applications.

BlueCore3-Multimedia has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v1.2 Specification.

Contents

List of Figures

List of Tables

1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time and no external trimming required in production
- Full RF reference designs available
- Bluetooth v1.2 Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier, a power control terminal controlled by an internal 8-bit DAC and external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down, wake up commands and an integrated low power oscillator for ultra-low power Park/Sniff/Hold mode
- Can use external master oscillator and provides 'clock request signal' to control external clock
- On-chip linear regulator; 1.8V output from a 2.2-4.2V input
- Power-on-reset cell detects low supply voltage
- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications

Package Options

- 96-ball LFBGA, 10 x 10 x 1.4mm, 0.8mm pitch

DSP Co-Processor

- 32MIPs, 24-bit fixed point DSP core
- Single cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 4Kword program memory, 2 x 8Kword data memory
- Flexible interfaces to BlueCore3 subsystem

Baseband and Software

- Internal 8Mbit Flash for complete system solution
- Internal 32Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 1.5Mbaud with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces
- Stereo serial audio interface supporting PCM, I^2S and SPDIF formats
- Optional I^2C™ compatible interface

Stereo Audio CODEC

- 16-bit resolution, standard sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz and 48kHz
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving microphone and speakers with minimum external components
- Compatible with DSP co-processor

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

2 Device Pinout Diagram with 10 x 10 LFBGA Package

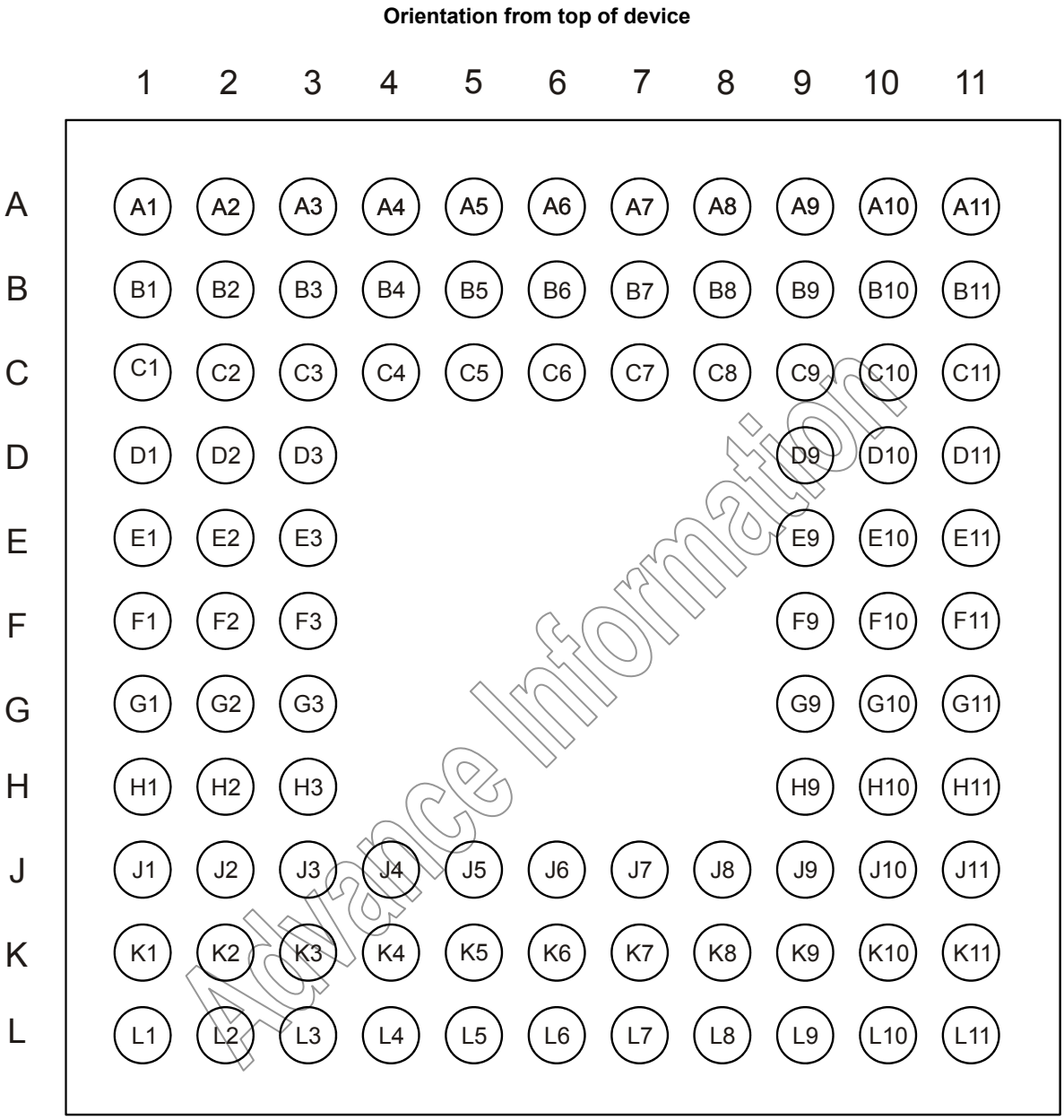


Figure 2.1: BC358239A BlueCore3-Multimedia Device Pinout

3 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D2	Analogue	Single ended receiver input
PIO[0]/RXEN	D3	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C4	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted for Class 1)
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50Ω RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tri-state, with weak internal pull-up	UART data output active high
UART_RX	J11	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	L11	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L9	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C10	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D11	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C11	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description
PIO[2]/CLK_REQ	C3	Bi-directional with programmable strength internal pull-up/down	PIO or external clock request
PIO[3]/USB_WAKE_UP/ HOST_CLK_REQ	B2	Bi-directional with programmable strength internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or clock request input from host controller
PIO[4]/USB_ON/ UART_TX(1)	H9	Bi-directional with programmable strength internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore3-Multimedia)
PIO[5]/USB_DETACH/ UART_RTS(1)	J9	Bi-directional with programmable strength internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[6]/CLK_REQ/ UART_CTS(1)	K8	Bi-directional with programmable strength internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[7]/UART_RX(1)/ CLK_OUT	K9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or programmable frequency clock output
PIO[8]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	K5	Bi-directional	Programmable input/output line
AIO[1]	J7	Bi-directional	Programmable input/output line
AIO[2]	K7	Bi-directional	Programmable input/output line
AIO[3]	J8	Bi-directional	Programmable input/output line

CODEC	Ball	Pad Type	Description
AUDIO_IN_P_LEFT	L1	Analogue	Microphone input positive (left side)
AUDIO_IN_N_LEFT	L2	Analogue	Microphone input negative (left side)
AUDIO_IN_P_RIGHT	K2	Analogue	Microphone input positive (right side)
AUDIO_IN_N_RIGHT	K3	Analogue	Microphone input negative (right side)
AUDIO_OUT_P_LEFT	J6	Analogue	Speaker output positive (left side)
AUDIO_OUT_N_LEFT	J5	Analogue	Speaker output negative (left side)
AUDIO_OUT_P_RIGHT	J4	Analogue	Speaker output positive (right side)
AUDIO_OUT_N_RIGHT	J3	Analogue	Speaker output negative (right side)

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	VDD / Regulator input	Linear regulator input
VDD_USB	L10	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC(2)
VDD_PADS	E11	VDD	Positive supply for all other digital Input/Output ports (3)
VDD_CORE	F11, C7, L6	VDD	Positive supply for internal digital circuitry
VDD_RADIO	E3	VDD / Regulator sense	Positive supply for RF circuitry
VDD_LO	J2	VDD	Positive supply for local oscillator circuitry
VDD_ANA	L5	VDD / Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VDD_BAL	F1	VDD	Positive supply for balun
VDD_MEM	C8, B11, K6	VDD	Positive supply for internal memory, AIO and extended PIO ports
VSS_PADS	D9, E10, K10	VSS	Ground connections for input/output
VSS_CORE	F10, C6	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_LO	G3, H3	VSS	Ground connections for local oscillator
VSS_ANA	K4	VSS	Ground connections for analogue circuitry
VSS	C9	VSS	Ground connection for internal package shield
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_BAL	G1	VSS	Ground connection for balun
VSS_MEM	C5	VSS	Ground connection for internal memory, AIO and extended PIO ports
VSS_RF	J1, K1	VSS	Ground connection for RF circuitry

Notes:

(1) Transparent UART port maps directly to main UART port

(2) Positive supply for PIO[3:0] and PIO[11:8]

(3) Positive supply for SPI/PCM ports and PIO[7:4]

Unconnected Terminals	Ball	Description
	A6, A7, A8, A9, A10, A11, B5, B6, B7, B8, B9, B10, C1, D1, E1, F2, H1, H2	Leave unconnected

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE, VDD_BAL	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.4V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range	-40°C	+105°C
Guaranteed RF performance range (1)	-25°C	+85°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE, VDD_BAL	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V

Note:

(1) Typical figures are given for RF performance between -40°C and +105°C

Input/Output Terminal Characteristics[1]				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/C
Output Noise[2][3]	-	-	1	mV rms
Load Regulation (Iload < 100 mA)	-	-	50	mV/A
Settling Time[2][4]	-	-	50	µs
Line Regulation[2][5]	-20	-	-	dB
Maximum Output Current	140	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	4.2	V
Dropout Voltage (Iload = 70 mA)	-	-	350	mV
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	µA
Low Power Mode[6]	**Min**	**Typ**	**Max**	**Unit**
Quiescent Current (excluding load, Iload < 100mA)	4	7	10	µA
Disabled Mode[7]	**Min**	**Typ**	**Max**	**Unit**
Quiescent Current	1.5	2.5	3.5	µA

Notes:

(1) These parameters guaranteed for 2.2 to 3.6V. Between 3.6V and 4.2V the output voltage is not guaranteed to remain below 1.85V but full functionality of the IC will be preserved and no change will ensue.

(2) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(3) Frequency range 100Hz to 100kHz.

(4) 1mA to 70mA pulsed load.

(5) Frequency range 100Hz to 10MHz.

(6) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(7) Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels					
VIL input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
VIH input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
VOL output logic level low, (I_O = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
VOL output logic level low, (I_O = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
VOH output logic level high, (I_O = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
VOH output logic level high, (I_O = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5	-1	0	µA
Weak pull-down		0	+1	+5	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
VIL input logic level low	-	-	0.3VDD_USB	V
VIH input logic level high	0.7VDD_USB	-	-	V
Input leakage current				
VSS_PADS< V_{IN}< VDD_USB[1]	-1	1	5	µA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage levels To correctly terminated USB Cable				
VOL output logic level low	0.0	-	0.2	V
VOH output logic level high	2.8	-	VDD_USB	V

Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Min**	**Typ**	**Max**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size(2)	12.5	14.5	17.0	mV
Output Voltage		monotonic(2)		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100mA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity(2)	-2	-	+2	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency(3)(6)	8.0	-	32.0	MHz
Digital trim range(4)	5.0	6.2	8.0	pF
Trim step size(4)	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(5)	870	1500	2400	Ω
External Clock	**Min**	**Typ**	**Max**	**Unit**
Input frequency(6)	7.5	-	40.0	MHz
Clock input level(7)	0.2	-	VDD_ANA	V pk-pk
Phase noise (at zero crossing)	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

Input/Output Terminal Characteristics (Continued)				
Stereo Audio CODEC, 16-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Input Stage/Microphone Amplifier				
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain	-	400	-	mV rms
Gain resolution	-	3	-	dB
Distortion at 1kHz	-		-74	dB
Input referenced rms noise	-	5	-	μV rms
Bandwidth	-	17	-	kHz
Input impedance	-	20	-	kΩ
SNR (microphone input) at maximum gain	-	>60	-	dBc
Analogue to Digital Converter				
Number of channels	-	-	2	
Resolution	-	-	16	bits
Input sample rate	8	-	32[8]	kHz
Signal to (Noise + Distortion) with 1kHz tone, Full scale and 0 - F_{sample} /2				
F_{sample} = 8 kHz	-	84	-	dB
F_{sample} = 11.025 kHz	-	83	-	dB
F_{sample} = 16 kHz	-	84	-	dB
F_{sample} = 22.050 kHz	-	83	-	dB
F_{sample} = 32 kHz	-	80	-	dB
F_{sample} = 44.1 kHz	-	74	-	dB
Digital Gain	-24		21.5	dB
Digital to Analogue Converter				
Number of channels	-	-	2	
Resolution	-	-	16	bits
Output sample rate	8	-	48	kHz
Gain Resolution	-	3	-	dB
Signal to (Noise + Distortion) with 1kHz tone, Full scale and 0 – 20 kHz				
F_{sample} = 8 kHz	-	79	-	dB
F_{sample} = 11.025 kHz	-	78	-	dB
F_{sample} = 16 kHz	-	79	-	dB
F_{sample} = 22.050 kHz	-	88	-	dB
F_{sample} = 32 kHz	-	90	-	dB
F_{sample} = 44.1 kHz	-	90	-	dB
F_{sample} = 48 kHz	-	89	-	dB
Digital Gain	-24	-	21.5	dB

Input/Output Terminal Characteristics (Continued)				
Output Stage/Loudspeaker Driver	**Min**	**Typ**	**Max**	**Unit**
Output power into 100Ω	-	10	-	mW
Output voltage full scale swing	-	2.0	-	V pk-pk
Output current drive (at full scale swing)(9)	10	20	40	mA
Output full scale current (at reduced swing)(9)	-	75	-	mA
Gain bandwidth	-	1	-	MHz
Distortion and noise (relative to full scale), THD	-	-75	-	dBc
Allowed Load: resistive	8	-	O.C.	Ω
Allowed Load: capacitive	-	500	-	pF

Notes:

VDD_CORE, VDD_RADIO, VDD_LO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

(2) Specified for an output voltage between 0.2V and VDD_PIO -0.2V

(3) Integer multiple of 250kHz

(4) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(5) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(6) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz + CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(7) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

(8) Interpolated to 44.1kHz within DSP

(9) For specified THD, much greater current can be supplied by the loudspeaker driver with compromised THD

5 Radio Characteristics

5.1 Transmitter – Temperature +20°C

Radio Characteristics VDD = 1.8V Temperature = +20°C						
		Min	Typ	Max	Bluetooth Specification	Unit
Maximum RF transmit power[1][2][3]		3	6.5	-	-6 to +4[4]	dBm
RF power control range[1][2]		25	35	-	≥16	dB
RF power range control resolution		-	0.5	-	-	dB
20dB bandwidth for modulated carrier		-	820	1000	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$[5]		-	-35	-20	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$[5]		-	-45	-40	≤-40	dBm
Δf1avg "Maximum Modulation"		140	165	175	140<f1avg<175	kHz
Δf2max "Minimum Modulation"		115	140	-	115	kHz
Δf1avg/Δf2avg		0.8	0.9	-	≥0.80	-
Initial carrier frequency tolerance		-	10	35	±75	kHz
Drift Rate		-	8	20	≤20	kHz/ 50μs
Drift (single slot packet)		-	9	20	≤25	kHz
Drift (five slot packet)		-	10	25	≤40	kHz
Emissions	**Frequency (GHz)**	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Emitted power in cellular bands measured at chip terminals Output power ≤4dBm	0.925-0.960[6]	-	-143	-138	-	dBMHz
	1.570-1.580[7]	-	-138	-135		
	1.805-1.880[6]	-	-131	-115		
	1.930-1.990[8]	-	-135	-125		
	1.930-1.990[6]	-	-135	-126		
	1.930-1.990[9]	-	-137	-130		
	2.110-2.170[9]	-	-132	-122		
	2.110-2.170[10]	-	-135	-127		

Notes:

Results shown are referenced to input of the RF balun

(1) Power at the chip pads

(2) Measured according to the Bluetooth specification v1.2

(3) The firmware maintains the transmit power to be within the Bluetooth specification v1.2 limits

(4) Class 2 RF transmit power range, Bluetooth specification v1.2

(5) Measured at F_0 = 2441MHz

(6) Integrated in 200kHz bandwidth

(7) Integrated in 1MHz bandwidth

(8) Integrated in 30kHz bandwidth

(9) Integrated in 1.2MHz bandwidth

(10) Integrated in 5MHz bandwidth

5.2 Receiver – Temperature +20°C

Radio Characteristics VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-84	-80	≤-70	dBm
	2.441	-	-85	-81		dBm
	2.480	-	-85	-81		dBm
Maximum received signal at 0.1% BER		0	3	-	≥-20	dBm
C/I co-channel		-	9	11	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1)		-	-4	0	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1)		-	-35	-30	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1)		-	-21	-20	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1)		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1)		-	-18	-9	≤-9	dB
Blocking	**Frequency (GHz)**	**Min**	**Typ**	**Max**	**Modulation**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (2) Measured at chip terminals	0.880-0.915	5	7	-	GSM	dBm
	1.710-1.785	3	6	-	GSM	
	1.850-1.910	1	5	-	GSM	
	1.920-1.980	-8	-6	-	W_CDMA	

Notes:

Results shown are referenced to input of the RF balun

(1) Measured at F_0 = 2441MHz

(2) For Bluetooth sensitivity of -67dBm with 0.1% BER

5.3 Power Consumption

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +4dBm		
Mode	**Average**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	21	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	21	mA
SCO connection HV3 (No Sniff Mode) (Slave)	28	mA
SCO connection HV1 (Slave)	42	mA
SCO connection HV1 (Master)	42	mA
ACL data transfer 115.2kbps UART no traffic (Master)	5	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	22	mA
ACL data transfer 720kbps UART (Master or Slave)	45	mA
ACL data transfer 720kbps USB (Master or Slave)	45	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	3.2	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.45	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.55	mA
Standby Mode (Connected to host, no RF activity)	47.0	µA
Reset (RESET high or RESETB low)	15.0	µA
DSP		
DSP core	0.12	mA/MIPs
DSP memory access	0.65	mA/MIPs
CODEC		
Microphone inputs and ADC / channel	0.85	mA
DAC and loudspeaker driver, no signal / channel	1.7	mA

6 Device Diagram

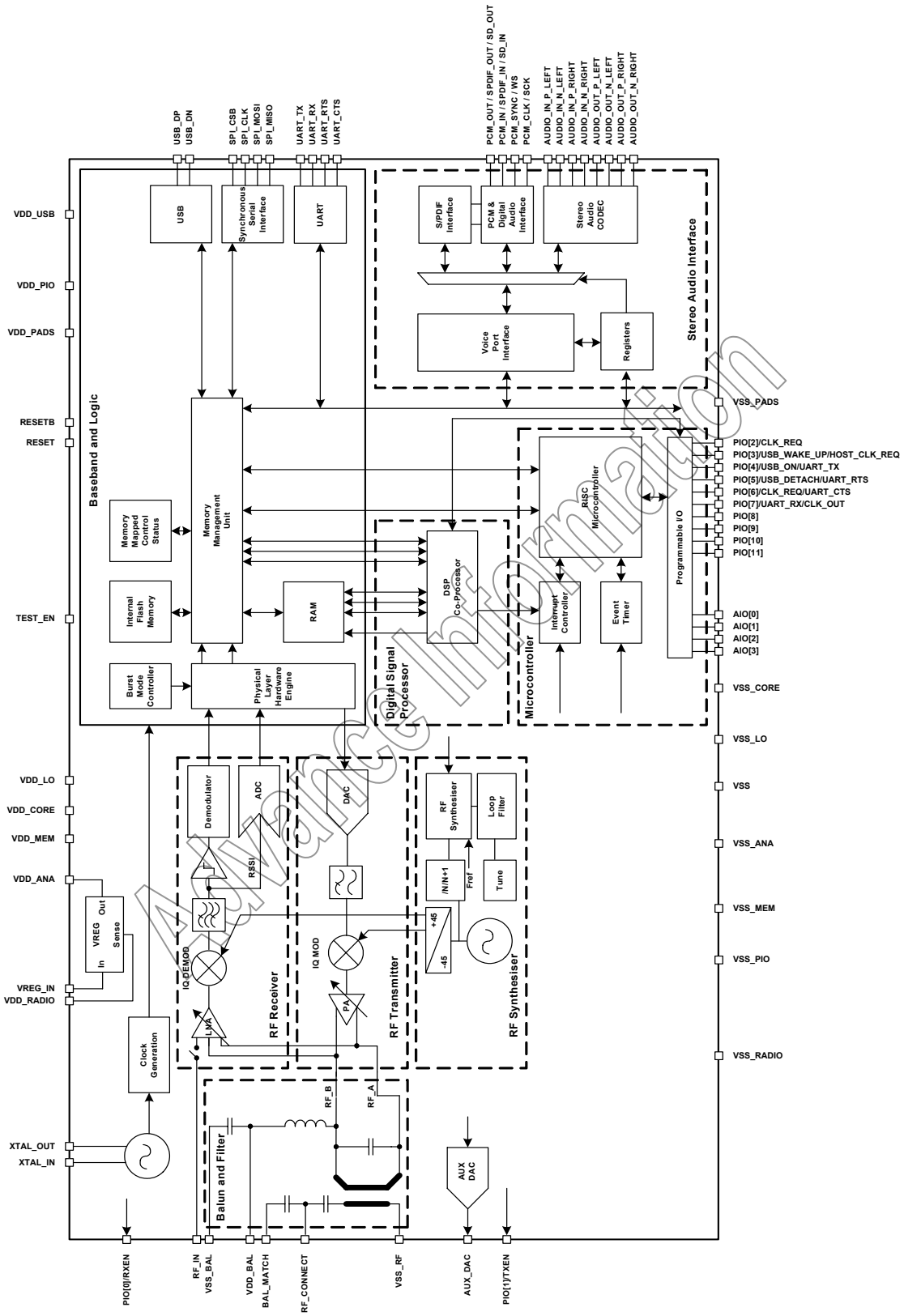


Figure 6.1: BlueCore3-Multimedia Device Diagram

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-Multimedia to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

7.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-Multimedia to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter.

7.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

7.5 Baseband and Logic

7.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

7.5.4 RAM

32Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.5.5 DSP RAM

Further on-chip RAM is provided to support the DSP co-processor as follows:

- 8K x 24-bit for data memory 1 (DM1)
- 8K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

7.5.6 FLASH Memory

8Mbits of internal Flash is available on the BC358239A. The Flash memory is provided for system firmware and the DSP co-processor code implementation.

7.5.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore3-Multimedia acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.5.8 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

7.5.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.6 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.6.1 Programmable I/O

BlueCore3-Multimedia has a total of 16 (12 digital and 4 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7.7 DSP Co-Processor

The DSP co-processor is an open platform DSP allowing signal processing functions to be performed on over air data or CODEC data in order to enhance audio applications. Figure 7.1 shows how the DSP interfaces to other functional blocks within BlueCore3-Multimedia.

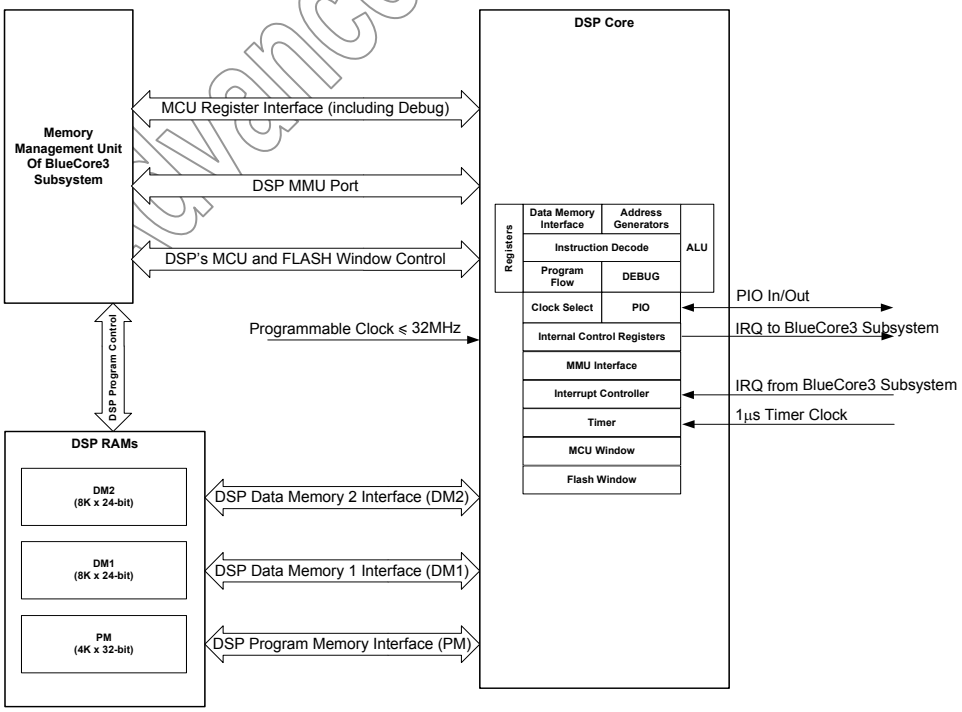


Figure 7.1: DSP Interface to Internal Functions

The key features of the DSP include:

- 32MIPs performance, 24-bit fixed point DSP Core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping and branching
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

7.8 Stereo Audio Interface

The stereo audio interface circuit consists of audio CODEC, dual audio inputs and outputs, and a PCM, I^2S or SPDIF configurable interface. Figure 7.2 outlines the functional blocks of the CODEC . The CODEC supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the CODEC contains two independent channels each. Any ADC or DAC channel can be run at its own independent sample rate.

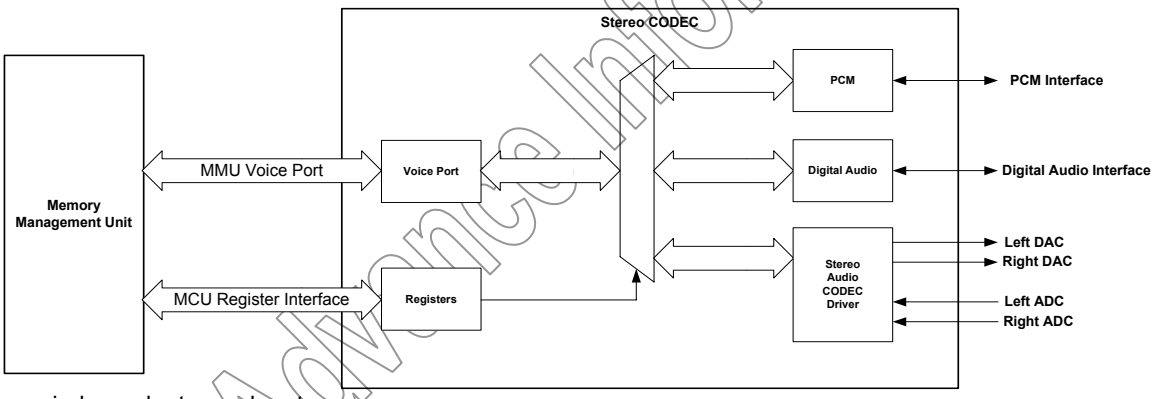


Figure 7.2: Audio Stereo Interface

7.8.1 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded voice data over Bluetooth. It also contains support for PCM master CODECs that require an external system clock. The interface shares the same pins as the digital audio interface see Table 9.1.

7.8.2 Audio Input

The audio input circuitry consists of a dual audio input that can be configured to be either single ended or fully differential and programmed for either microphone or line input. It has a programmable gain stage for optimisation of different microphones.

7.8.3 Audio Output

The audio output circuitry consists of a dual audio class A-B output stage.

7.8.4 Digital Audio Interface

The digital audio bus supports various digital audio bus standard, which include I^2S, and the interfaces contained within the IEC 60958 specification such as SPDIF and AES3.

8 CSR Bluetooth Software Stacks

BlueCore3-Multimedia is supplied with Bluetooth stack firmware, which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.2.

The BlueCore3-Multimedia software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

Running the upper stack on BlueCore3-Multimedia reduces (or eliminates, in the case of a virtual machine (VM) application) the need for host-side software and processing time. Running the upper layers on the host processor allows greater flexibility.

8.1 BlueCore HCI Stack

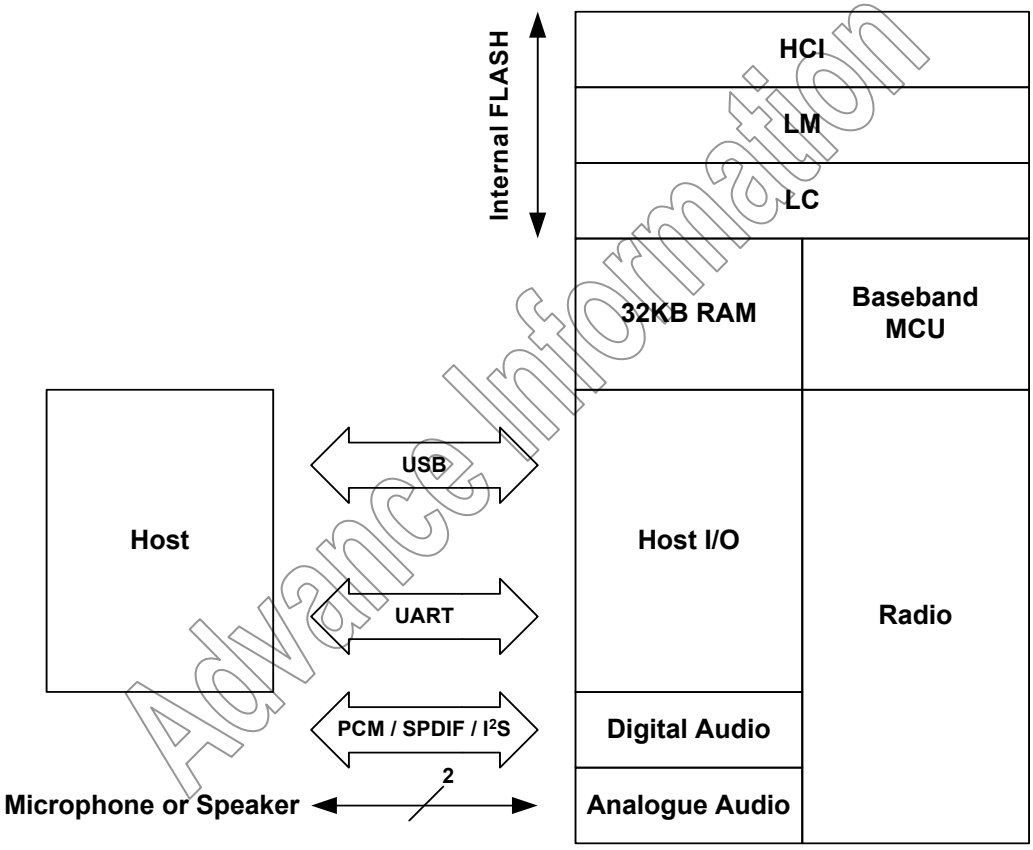


Figure 8.1: BlueCore HCI Stack

In the implementation shown in Figure 8.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers.

8.1.1 Key Features of the HCI Stack - Standard Bluetooth Functionality

New Bluetooth v1.2 Mandatory Functionality:

- Adaptive Frequency Hopping (AFH)
- Faster Connections
- Flow and Flush Time out
- LMP Improvements
- Parameter Ranges

Optional v1.2 functionality supported:

- Extended SCO (eSCO), HV3 +CRC, HV4, HV5
- Scatter mode
- LMP Absence Masks, Quality of Service and SCO handle
- L2CAP flow and error control
- Synchronisation

The firmware has been written against the Bluetooth Core Specification v1.2.

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard USB v1.1 and UART (H4) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2Kbps asymmetric(1)
- Operation with up to 7 active slaves(1)
- Operation as slave to one master while master of several slaves (Scatternet “2.0”)
- Page and Inquiry scanning while slave and master (Scatternet “2.5”)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice coding, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from http://www.csr.com.

Note:

(1) Maximum allowed by Bluetooth specification v1.2

(2) BlueCore3-Multimedia supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.2

8.1.2 Key Features of the HCI Stack - Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:
  - Access to the chip's general-purpose PIO port
  - Access to the chip's Bluetooth clock – this can help transfer connections to other Bluetooth devices
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location Piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a deep sleep state
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port (at the same time as routing up to two other SCO channels over HCI). [Future versions of the BlueCore3 firmware will be able to exploit the hardware's ability to route up to three SCO channels through the single PCM port.]

8.2 BlueCore RFCOMM Stack

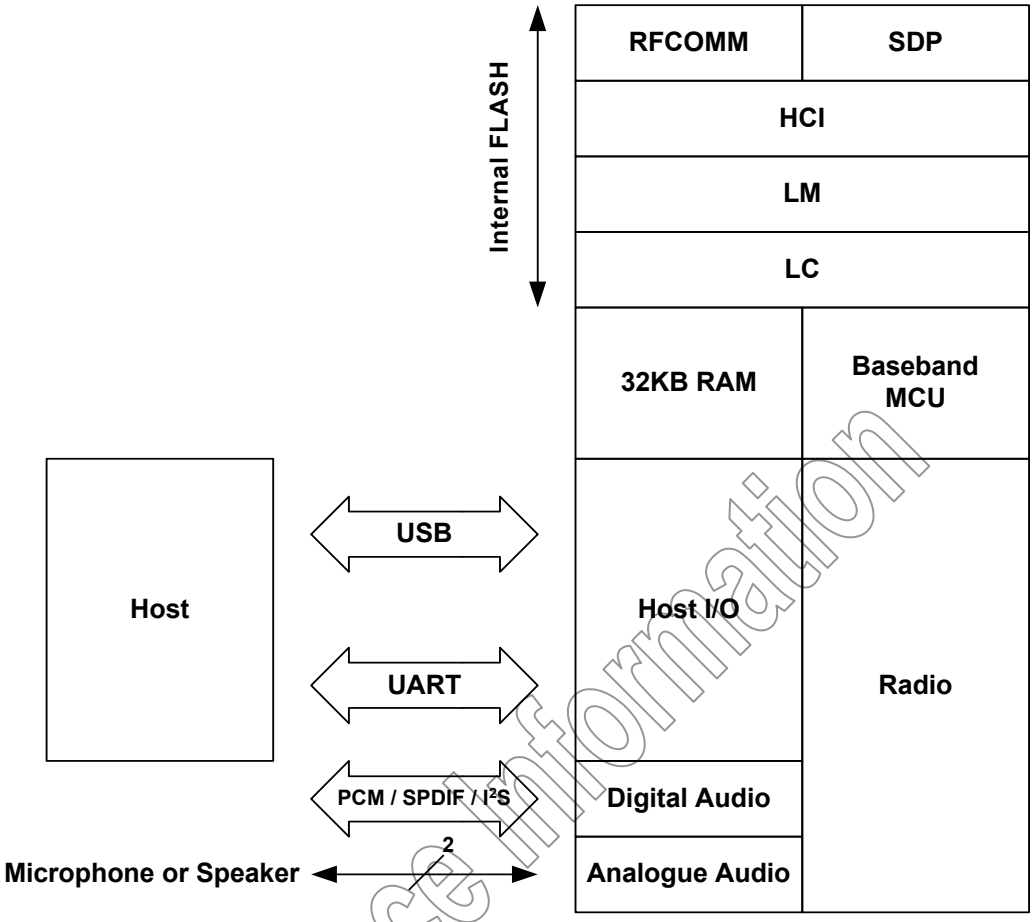


Figure 8.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 8.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.2.1 Key Features of the BlueCore3-Multimedia RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kbps

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

8.3 BlueCore Virtual Machine Stack

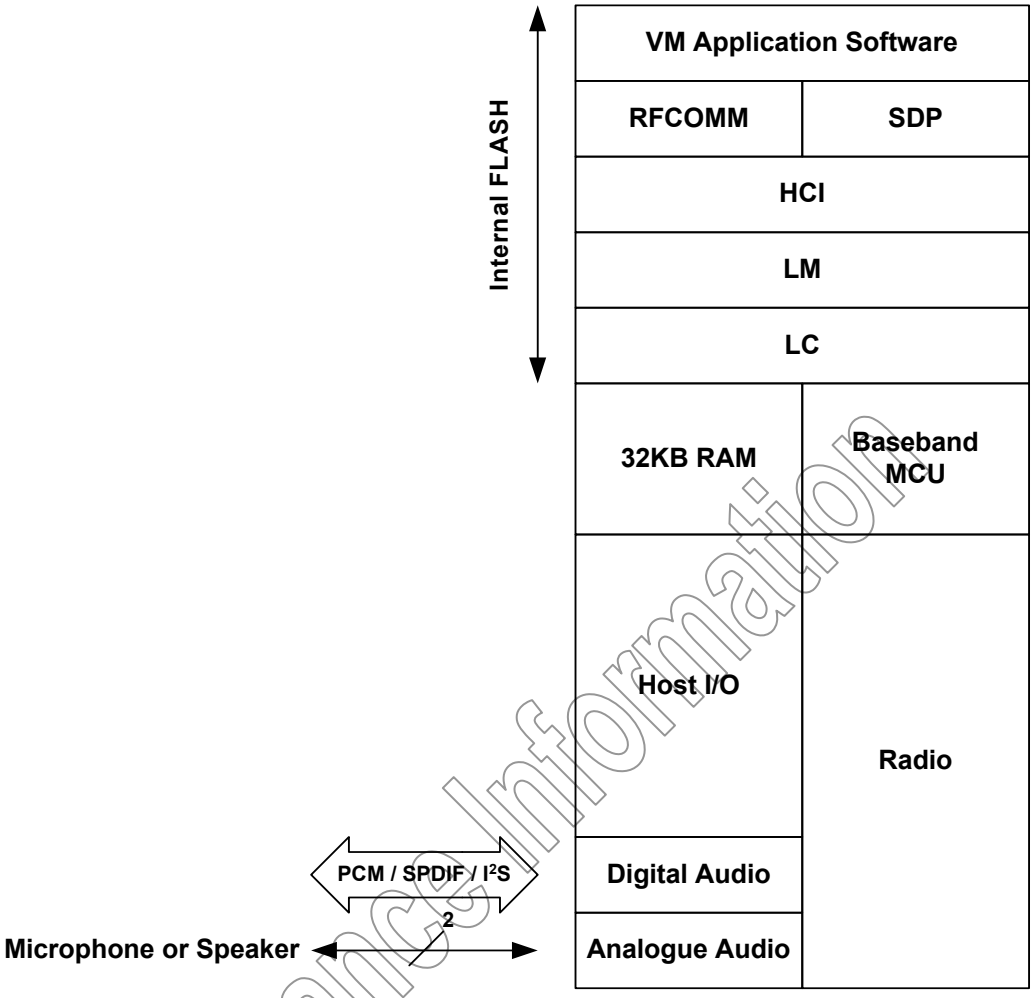


Figure 8.3: Virtual Machine

In Figure 8.3, this version of the stack firmware shown requires no host processor (but can use a host processor for debugging etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab Multimedia and Casira2 development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

8.4 BlueCore3-Multimedia and DSP Co-Processor Stack

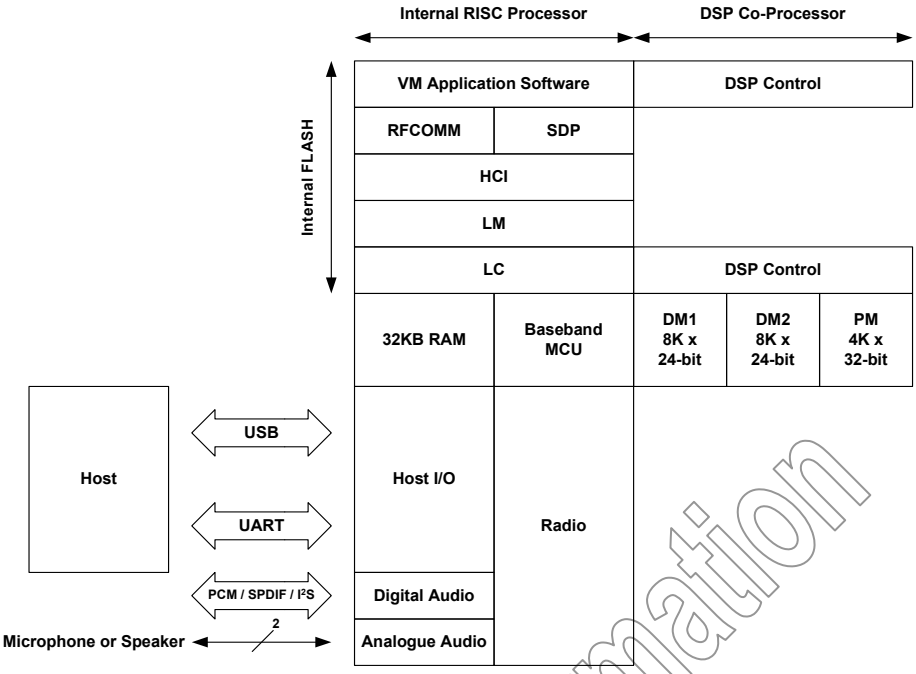


Figure 8.4: DSP Co-Processor Stack

In Figure 8.4, this version of the stack firmware requires no host processor. The software layers for the application software runs on the internal RISC processor in the VM and the DSP application code runs from the DSP program memory RAM.

8.5 Host-Side Software

BlueCore3-Multimedia can be ordered with companion host-side software:

BlueCore3-PC includes software for a full Windows®98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.

BlueCore3-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

8.6 Device Firmware Upgrade

BlueCore3-Multimedia is supplied with boot loader software, which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the Flash memory through BlueCore3-Multimedia's UART or USB ports.

8.7 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore3-Multimedia, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as ‘C’ source or object code.

8.8 CSR Development Systems

CSR’s BlueLab Multimedia and Casira2 development kits are available to allow the evaluation of the BlueCore3-Multimedia hardware and software, and as toolkits for developing on-chip and host software.

9 External Interfaces

9.1 Transmitter/Receiver Input and Output

For Class 1 operation the RF_IN ball is provided which is single-ended. A swing of up to 0.5V root mean squared (rms) can be tolerated at this terminal. An external antenna switch can be connected to RF_IN.

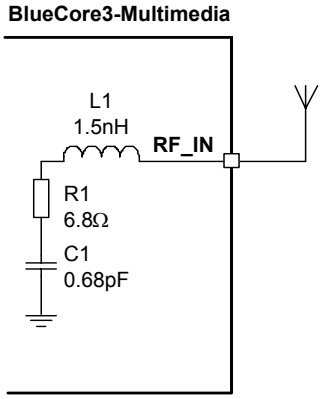


Figure 9.1: Circuit RF_IN

9.2 RF Plug 'n' Go

The 10 x 10 96-ball LFBGA package used on the BlueCore3-Multimedia device is a RF Plug 'n' Go package where the terminal RF_CONNECT forms an unbalanced ouput with a nominal 50Ω impedance. This terminal can be directly connected to an antenna requiring no impedance matching network as shown in Figure 9.2.

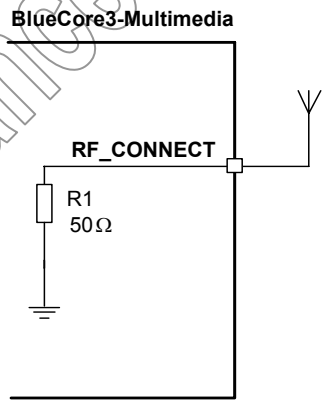


Figure 9.2: Circuit for RF_CONNECT

9.3 Asynchronous Serial Data Port (UART) and USB Port

UART_TX, UART_RX, UART_RTS and UART_CTS form a conventional asynchronous serial data port. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signalling levels are 0V and VDD_USB and are inverted with respect to the signalling on an RS232 cable. The interface is programmable over a variety of bit rates; no, even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in memory.

The maximum UART data rate is 1.5 MBaud. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and is active low. UART_CTS is an input and is active low. These signals operate according to normal industry convention.
The port carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API, SDP and device management. For the UART, these are combined into a robust tunnelling protocol, BlueCore Serial Protocol (BCSP), where each channel has its own software flow control and cannot block other data channels. In addition, the Bluetooth specification v1.2, HCI UART Transport Layer (part H4) format is supported.

Full speed USB (12Mbit/s) is supported in accordance with the Bluetooth specification v1.2, HCI USB Transport Layer (H2). USB_DP and USB_DN are available on dedicated terminals. Both Open Host Controller Interface (OHCI) and Universal Host Controller Interfaces (UHCI) are supported.

The firmware in Flash can be downloaded through the USB or UART ports by DFU if the CSR supplied boot loader is first programmed. Firmware shipped with BlueCore3-Multimedia includes security features to prevent misuse of this upgrade facility.

9.4 UART Bypass

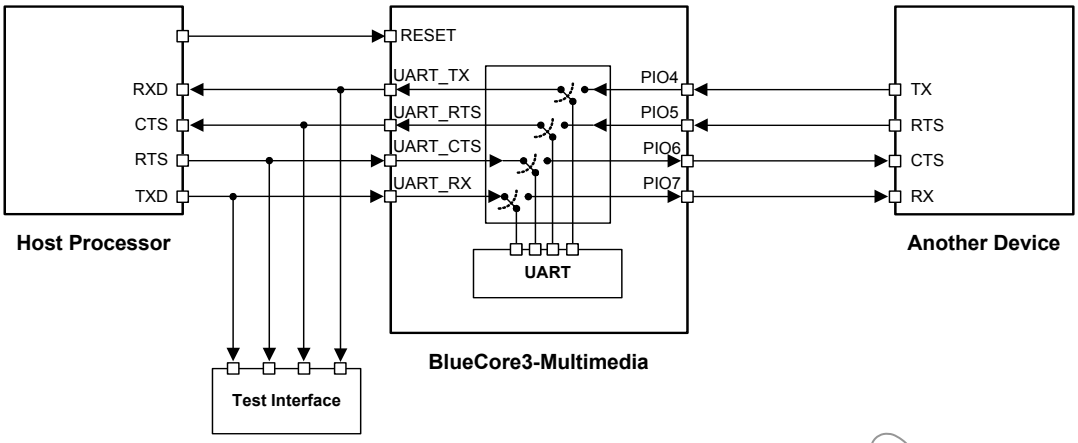


Figure 9.3: UART Bypass Architecture

9.4.1 UART Configuration While RESET is Active

The UART interface for BlueCore3-Multimedia while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore3-Multimedia reset is de-asserted and the firmware begins to run.

9.4.2 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore3-Multimedia can be used. The default state of BlueCore3-Multimedia after reset is de-asserted, this is for the host UART bus to be connected to the BlueCore3-Multimedia UART, thereby allowing communication to BlueCore3-Multimedia via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore3-Multimedia upon this, it will switch the bypass to PIO[7:4] as shown in Figure 9.3. Once the bypass mode has been invoked, BlueCore3-Multimedia will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore3-Multimedia, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

9.5 Stereo Audio Interface

The main features of the interface are that it supports the following functions:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I^2S
- Support for IEC-60958 standard stereo digital audio bus standards i.e. S/PDIF and AES3/EBU
- Support for PCM interfaces including PCM master CODECs that require an external system clock

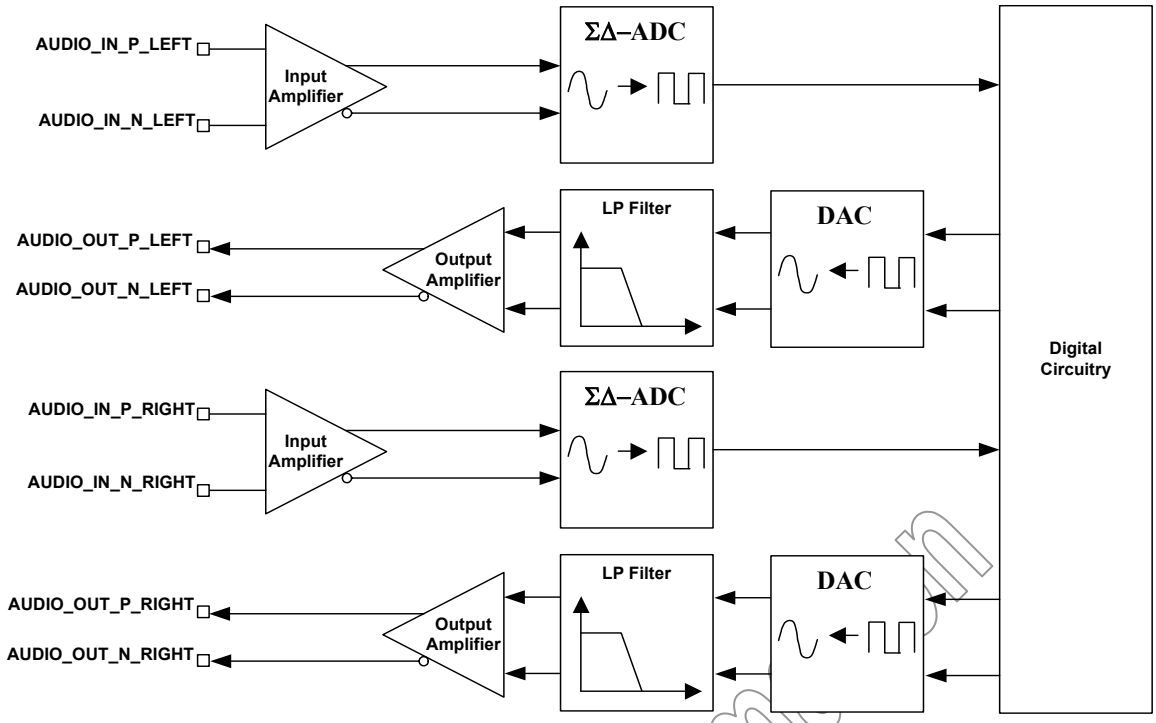


Figure 9.4: Stereo CODEC Audio Input and Output Stages

The stereo audio CODEC uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.8V and uses a minimum of external components.

The CODEC is based on a similar CODEC architecture used inside BlueCore2-Audio. With the input bandwidth and sample rates being modified to extend from the speech-band 0 – 3.4kHz to the whole audible band 0 - 20kHz. Also a second audio channel has been added for stereo input and output. Figure 9.4 shows the input and the output stage of the stereo audio channels.

9.5.1 PCM CODEC Interface

PCM_OUT, PCM_IN, PCM_CLK and PCM_SYNC carry up to three bi-directional channels of voice data, each at 8Ksps. The format of the PCM samples can be 8-bit A-law, 8-bit μ-law, 13-bit linear or 16-bit linear. The PCM_CLK and PCM_SYNC terminals can be configured as inputs or outputs, depending on whether BlueCore3-Multimedia is the Master or Slave of the PCM interface and can generate a clock on PIO[7] to supply to devices that require an external system clock.

BlueCore3-Multimedia interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- Xemics XE3005 16-bit sigma delta CODEC
- BlueCore3-Multimedia is also compatible with the Motorola SSI™ interface

9.5.2 Digital Audio Bus

The digital audio bus supports various digital audio bus standard, which include I^2S and the IEC 60958 interface specification. The interface for the digital audio bus shares the same pins as the PCM CODEC Interface described in Section 9.5.1 this means each of the audio busses are mutually exclusive in their usage. The pin out for the PCM interface with alternative pin descriptions can be seen in the device diagram shown in Figure 6.1 and Table 9.1 lists these alternative functions.

PCM Interface	SPDIF Interface	I^2S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

Table 9.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

9.5.3 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the two industry standards AES/EBU and the Sony and Philips interface specification SPDIF. The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins as shown in Figure 6.1. The input and output stages of the SPDIF pins can interface either 75Ω coaxial cable with an RCA connector or there is an option to use an optical link that uses Toslink optical components. Typical output and input stage interfaces for the coaxial solution interface is shown in Figure 9.5 and Figure 9.6 and the equivalent optical solution is shown in Figure 9.7 and Figure 9.8.

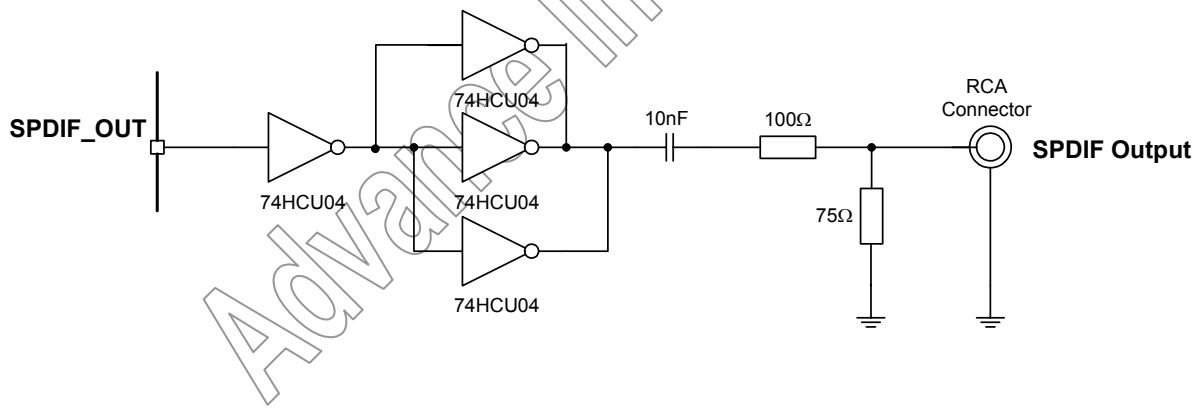


Figure 9.5: Example Circuit for SPDIF Interface with Coaxial Output

Note:

The 100Ω and 75Ω resistors are dependent on the supply voltage and therefore subject to change

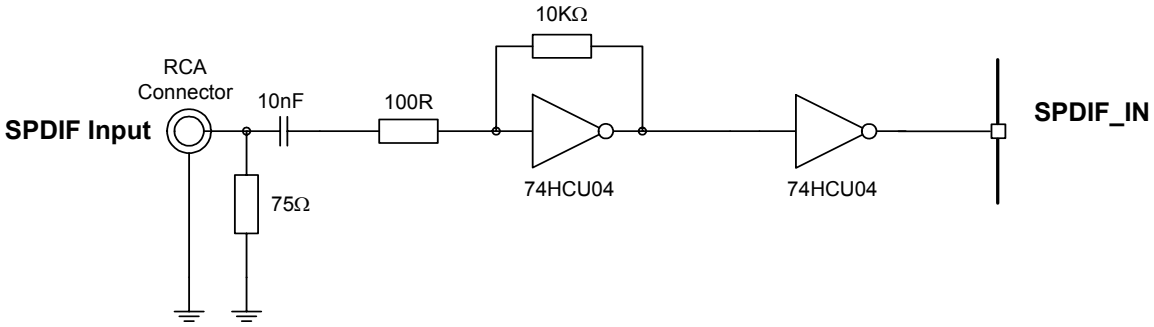


Figure 9.6: Example Circuit for SPDIF Interface with Coaxial Input

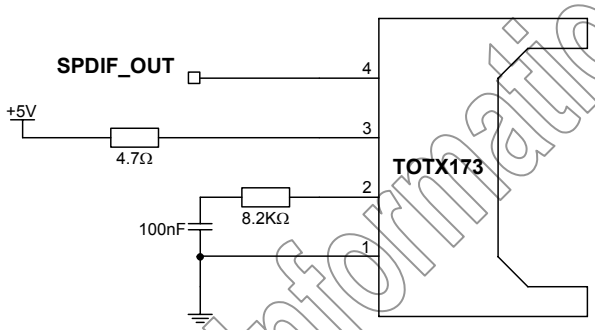


Figure 9.7: Example Circuit for SPDIF Interface with Optical Output

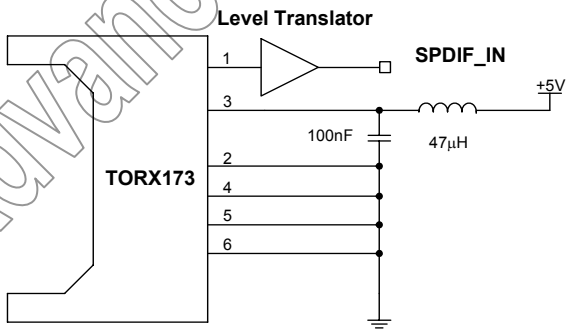


Figure 9.8: Example Circuit for SPDIF Interface with Optical Input

9.5.4 Audio Input Stage

The input stage of BlueCore3-Multimedia consists of a low noise input amplifier, which receives its analogue input signal from pins AUDIO[IN]_P_LEFT and AUDIO[IN]_N_LEFT to a second-order Σ-Δ ADC that outputs a 4MBit/sec single-bit stream into the digital circuitry. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

9.5.5 Microphone Input

The audio-input is intended for use from 1μA@94dB SPL to about 10μA@94dB SPL. With biasing-resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV. The microphone for each channel should be biased as shown in Figure 9.9.

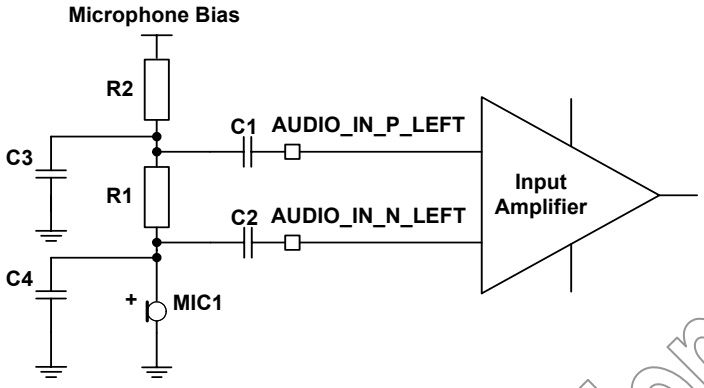


Figure 9.9: BlueCore3-Multimedia Microphone Biasing (Left Channel Shown)

The input impedance at AUDIO[IN]_N_LEFT, AUDIO[IN]_P_LEFT, AUDIO[IN]_N_RIGHT and AUDIO[IN]_P_RIGHT is typically 20kΩ. C1 and C2 should be 47nF. R1 sets the microphone load impedance and is normally in a range of 1 to 2 kΩ. R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required in the specification. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the AUX_DAC output (which is ground referenced and so provides good rejection of the supply), which maybe configured to provide bias only when the microphone is required.

9.5.6 Line Input

If the input gain is set to less than 21dB BlueCore3-Multimedia automatically selects line input mode. In this mode the input impedance at AUDIO[IN]_N_LEFT, AUDIO[IN]_P_LEFT, AUDIO[IN]_N_RIGHT and AUDIO[IN]_P_RIGHT are increased to 130kΩ typically. In line-input mode, the full-scale input signal is about 400mV rms. Figure 9.10 and Figure 9.11 show two circuits for line input operation and show connections for either differential or single ended inputs.

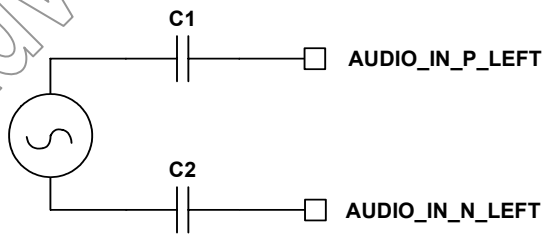


Figure 9.10: Differential Input (Left Channel Shown)

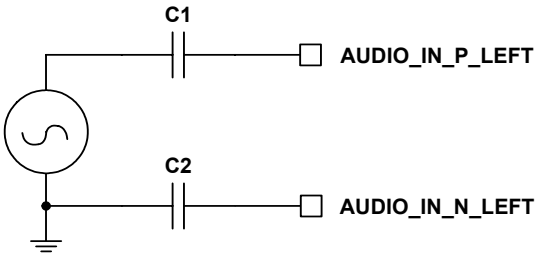


Figure 9.11: Single Ended Input (Left Channel Shown)

9.5.7 Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to an 8 MBits/sec bit stream, which is fed into the analogue output circuitry.

The output circuit comprises a digital to analogue converter with digital gain setting and an output amplifier. Its class-AB output-stage is capable of driving a current of up to 10mA into a load of 100Ω and 500pF with a typical distortion of less than –75dBc. The output is available as a differential signal between AUDIO[OUT]_N_LEFT and AUDIO[OUT]_P_LEFT for the left channel as shown in Figure 9.12; and between AUDIO[OUT]_N_RIGHT and AUDIO[OUT]_P_RIGHT for the right channel. The output is capable of driving a speaker directly if its impedance is greater than 8Ω.

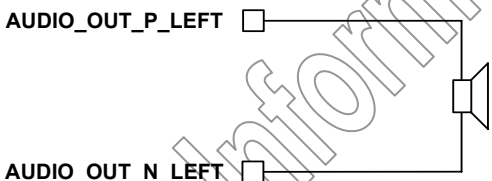


Figure 9.12: Speaker Output (Left Channel Shown)

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

In normal operating mode, the 8MBit/sec single bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz. It uses its high open loop gain in the closed loop application circuit to achieve low distortion while operating with low standing current.

9.6 Serial Peripheral Interface

BlueCore3-Multimedia is a slave device that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This interface is used for program emulation/debug and IC test. It is also the means by which the Flash memory may be programmed ‘in situ’ before any 'boot' program is loaded.

Note:

The designer should be aware that no security protection is built into the hardware or firmware associated with this port, so the terminals should not be permanently connected in a PC application.

9.7 I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [3:0] are powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO [2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore3-Multimedia is provided from a system application specific integrated circuit (ASIC).

BlueCore3-Multimedia has three general purpose analogue interface pins, AIO[0], AIO[1], AIO[2] and AIO[3]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals; 48, 24, 16, 8 MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

9.7.1 PIO Defaults for BTv1.2 HCI Level Bluetooth Stack

I/O Terminal	Description
PIO[0]	Pull high on boot up to select USB transport rather than BCSP Control output for external LNA after boot up completion
PIO[1]	Pull high on boot up to select 16MHz reference clock frequency rather than 26MHz Control output for external PA (Class 1 operation) after boot up completion
PIO[2]	Clock request output
PIO[3]	Clock request “OR” gate input
PIO[4]	UART Bypass (UART_TX)
PIO[5]	UART Bypass (UART_RTS)
PIO[6]	UART Bypass (UART_CTS) E^2SCL
PIO[7]	UART Bypass (UART_RX) E^2SDA
PIO[8]	E^2 write protect
AIO[0]	32kHz watchdog input
AIO[2]	Vref output. Must be decoupled

Table 9.2: PIO Defaults

Notes:

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode

CSR cannot guarantee that these terminal functions remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

9.8 I^2C Interface

PIO[8:6] can be used to form a Master I^2C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

9.9 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore3-Multimedia where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore3-Multimedia.

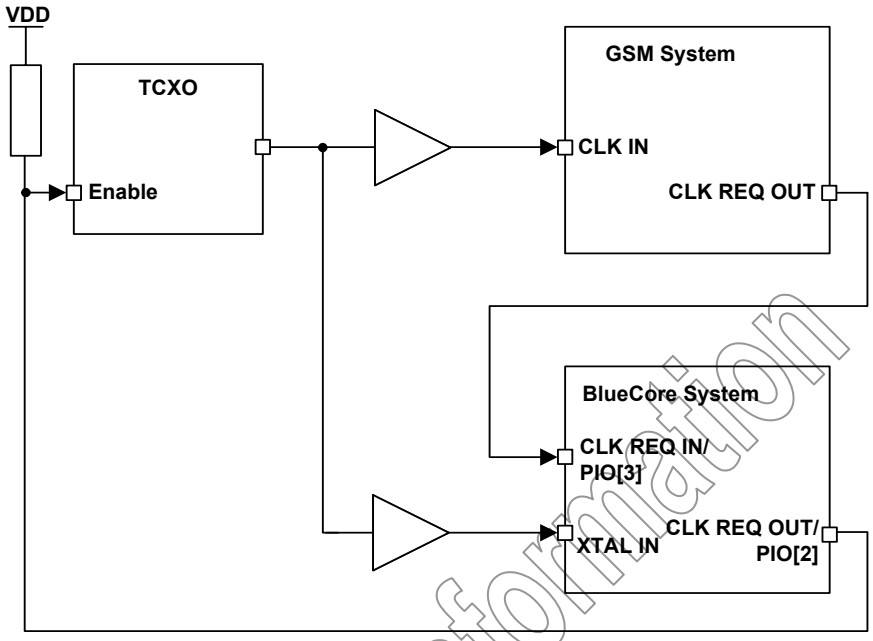


Figure 9.13: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

9.10 Reset

BlueCore3-Multimedia may be reset from several sources: RESET or RESETB pins, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is 'ORed' on chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

Following a reset, BlueCore3-Multimedia assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore-Multimedia is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore3-Multimedia free runs, again at a safe frequency.

9.11 Power Supply

9.11.1 Voltage Regulator

An on chip linear voltage regulator can be used to power the 1.8V dependent supplies. The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

9.11.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA be powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important. However if VDD_CORE is not present, all inputs have a weak pull-down irrespective of the reset state.

9.11.3 Sensitivity to Disturbances

It is recommended that if you are supplying BlueCore3-Multimedia from an external voltage source that VDD_VCO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this reduces transients put back onto the power supply rails

The transient response of the regulator is also important. At the start of a packet, power consumption will jump to high levels, see average current consumption section. The regulator should have a response time of 20μs or less, it is essential that the power rail recovers quickly.

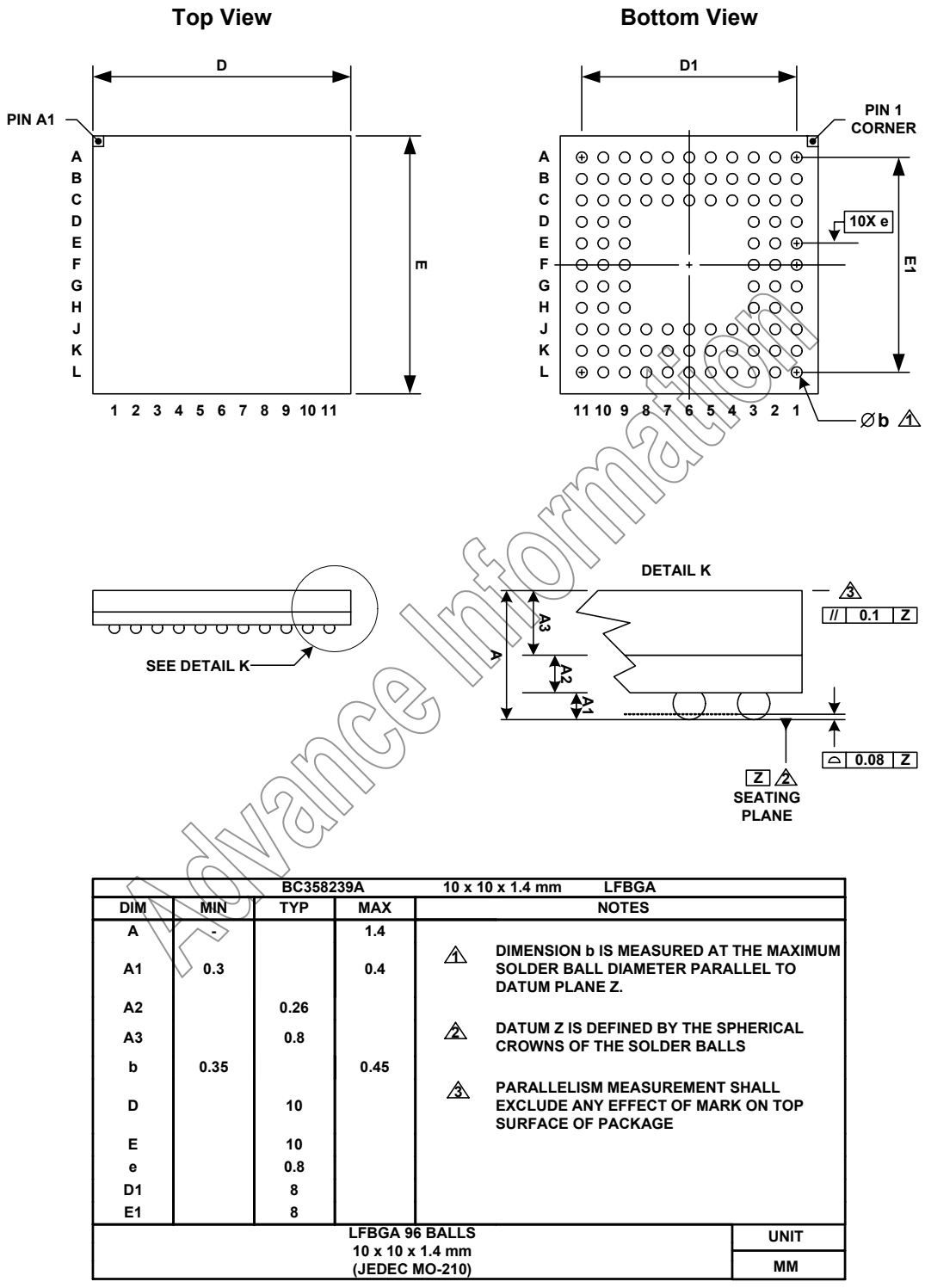
10 Schematic

TBD

Figure 10.1: Application Circuit for Radio Characteristics Specification with 10 x 10 LFBGA Package

11 Package Dimensions

11.1 10 x 10 LFBGA 96-Ball LFBGA Package



BC358239A 10 x 10 x 1.4 mm LFBGA				
DIM	MIN	TYP	MAX	NOTES
A	-		1.4	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.3		0.4	
A2		0.26		
A3		0.8		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
b	0.35		0.45	
D		10		3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE
E		10		
e		0.8		
D1		8		
E1		8		
LFBGA 96 BALLS 10 x 10 x 1.4 mm (JEDEC MO-210)				UNIT: MM

Figure 11.1: BlueCore3-Multimedia 96-Ball LFBGA Package Dimensions

12 Ordering Information

12.1 BlueCore3-Multimedia (Internal Flash)

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	96-Ball LFBGA	10 x 10 x 1.4mm	Tape and reel	BC358239A-BN-E4
UART and USB	96-Ball LFBGA (Pb free)	10 x 10 x 1.4mm	Tape and reel	BC358239A-NN-E4

Minimum Order Quantity

2kpcs Taped and Reeled

13 Contact Information

CSR U.S.
1651 N. Collins Blvd.
Suite 210
Richardson
TX75080
Tel: +1 (972) 238 2300
Fax: +1 (972) 231 1440
e-mail: sales@csr.com

CSR UK
Cambridge Science Park
Milton Road
Cambridge, CB4 0WH
United Kingdom
Tel: +44 (0) 1223 692 000
Fax: +44 (0) 1223 692 001
e-mail: sales@csr.com

CSR Denmark
Novi Science Park
Niels Jernes Vej 10
9220 Aalborg East
Denmark
Tel: +45 72 200 380
Fax: +45 96 354 599
e-mail: sales@csr.com

CSR Japan
CSR KK
9F Kojimachi KS Square 5-3-3,
Kojimachi,
Chiyoda-ku,
Tokyo 102-0083
Japan
Tel: +81-3-5276-2911
Fax: +81-3-5276-2915
e-mail: sales@csr.com

CSR Singapore
Blk 5, Ang Mo Kio
Industrial Park 2A,
AMK Tech II, #07-08
Singapore 567760
Tel: +65 6484 2212
Fax: +65 6484 2219
e-mail: sales@csr.com

CSR Korea
Rm. 1111 Keumgang Venturetel,
#1108 Beesan-dong,
Dong An-ku, Anyang-city,
Kyunggi-do 431-050,
Korea
Tel: +82 31 389 0541
Fax : +82 31 389 0545
e-mail: sales@csr.com

To contact a CSR representative, go to http://www.csr.com/contacts.htm

14 Document References

Document:	Reference, Date:
Specification of the Bluetooth system	v1.1, 22 February 2001
Universal Serial Bus Specification	v1.1, 23 September 1998

Acronyms and Definitions

BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
CSR	Cambridge Silicon Radio
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BMC	Burst Mode Controller
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
DSP	Digital Signal Processor
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LFBGA	Low profile Fine Ball Grid Array
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
μ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface

PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SPI	Serial Peripheral Interface
SSI	Signal Strength Indication
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)
www	world wide web

Status Information

The status of this Data Sheet is Advance Information.

The progression of CSR Product Data Sheets follows the following format:

Advance Information

Information for designers on the target specification for a CSR product in development.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications.

Trademarks, Patents and Licenses

BlueCore™, BlueLab™, Casira™, CompactSira™ and MicroSira™ are trademarks of CSR Ltd.

Bluetooth® and the Bluetooth logos are trademarks owned by Bluetooth SIG Inc, USA and licensed to CSR.

Windows™, Windows 98™, Windows 2000™, Windows XP™ and Windows NT™ are registered trademarks of the Microsoft Corporation.

I^2C™ is a trademark of Philips Corporation.

All other product, service and company names are trademarks, registered trademarks or service marks of their respective owners.

The publication of this information does not imply that any license is granted under any patent or other rights owned by CSR Ltd.

CSR Ltd reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Record of Changes

Date:	Revision	Reason for Change:
11 FEB 03	a	Original publication of this document. (CSR reference: BC358239A-ds-001Pa)
05 JUN 03	b	Pinout added and associated changes. Plus updates with respect to performance data of initial devices

BlueCore™3-Multimedia

Product Data Sheet

BC358239A-ds-001Pb

June 2003