Device Features

- **Fully qualified Bluetooth system**
- **Low power 1.8V operation**
- **Minimum external components**
- **Integrated 1.8V regulator**
- **15-bit linear audio CODEC**
- **Dual UART ports**
- **Available in TFBGA and LFBGA packages**
- **Also available in 'RF Plug and Go' package for low cost manufacture**

BlueCore™2-Flash

Single Chip Bluetooth™ System

Advance Information Data Sheet for

BC215159A
BC219159A

January 2003

BlueCore™2-Flash Product Data Sheet

General Description

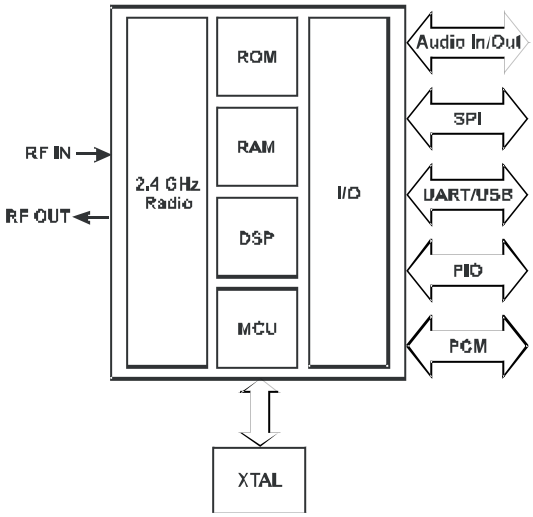
BlueCore2-Flash is a single chip radio and baseband IC for Bluetooth™ 2.4GHz systems. It is implemented in 0.18µm CMOS technology.

BlueCore2-Flash has the same pinout and electrical characteristics as available in BlueCore2-ROM to enable development of custom code before committing to ROM.

The integrated mono audio CODEC allows for more compact designs and low power consumption for battery powered applications.

Applications

- **Headsets**
- **Cellular Handsets**
- **Personal Digital Assistants**
- **Mice**
- **Keyboards**



BlueCore2-Flash System Architecture

BlueCore2-Flash has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth specification v1.1.

Contents

List of Figures

1 Key Features

Radio

- Operation with common TX/RX terminals simplifies external matching circuitry and eliminates external antenna switch
- Extensive built-in self-test minimises production test time
- No external trimming is required in production
- Full RF reference designs are available

Transmitter

- Up to +6dBm RF transmit power with level control from the on-chip 6-bit DAC over a dynamic range greater than 30dB
- Supports Class 2 and Class 3 radios without the need for an external power amplifier or TX/RX switch
- Supports Class 1 radios with an external power amplifier, provided by a power control terminal controlled by an internal 8-bit voltage DAC and an external RF TX/RX switch

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Digitised RSSI available in real time over the HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesizer; no external VCO varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with either sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down and wake up commands and an integrated low power oscillator for ultra-low power consumption during Park/Sniff/Hold modes
- Device can be used with an external Master oscillator and provides a ‘clock request signal’ to control external clock source
- On-chip linear regulator, producing 1.8V output from 2.2-4.2V input
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies is permitted

Auxiliary Features (continued)

- Uncommitted 8-bit ADC and 8-bit DAC are available to application programs

Baseband and Software

- Internal programmed 4Mbit ROM for complete system solution
- 32Kbyte on-chip RAM allows full speed Bluetooth data transfer, mixed voice and data, plus full 7 Slave piconet operation
- Dedicated logic for forward error correction, header error control, access code correlation, demodulation, cyclic redundancy check, encryption bitstream generation, whitening and transmit pulse shaping
- Transcoders for A-law, µ-law and linear voice from host and A-law, µ-law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable Baud rate up to 1.5Mbaud with an optional bypass mode
- Full speed USB interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Synchronous bi-directional serial programmable audio interface
- Optional I²C™ compatible interface

Bluetooth Stack Running on an Internal Microcontroller

CSR’s Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customer specific builds with embedded application code

Audio CODEC

- 15-bit resolution with 8kHz sampling frequency
- Designed for use in voice applications such as headsets and hands-free kits
- Integrated input/output amplifiers capable of driving a microphone and speaker with minimum external components

Package Options

- 84-ball TFBGA 6 x 6 x 1.2mm 0.5mm pitch
- 96-ball LFBGA 10 x 10 x 1.4mm 0.8mm pitch (RF Plug and GO package)

2 6 x 6 Package Information

2.1 BC215159A-HK and BC215159A-TK Pinout Diagram

Orientation from top of device

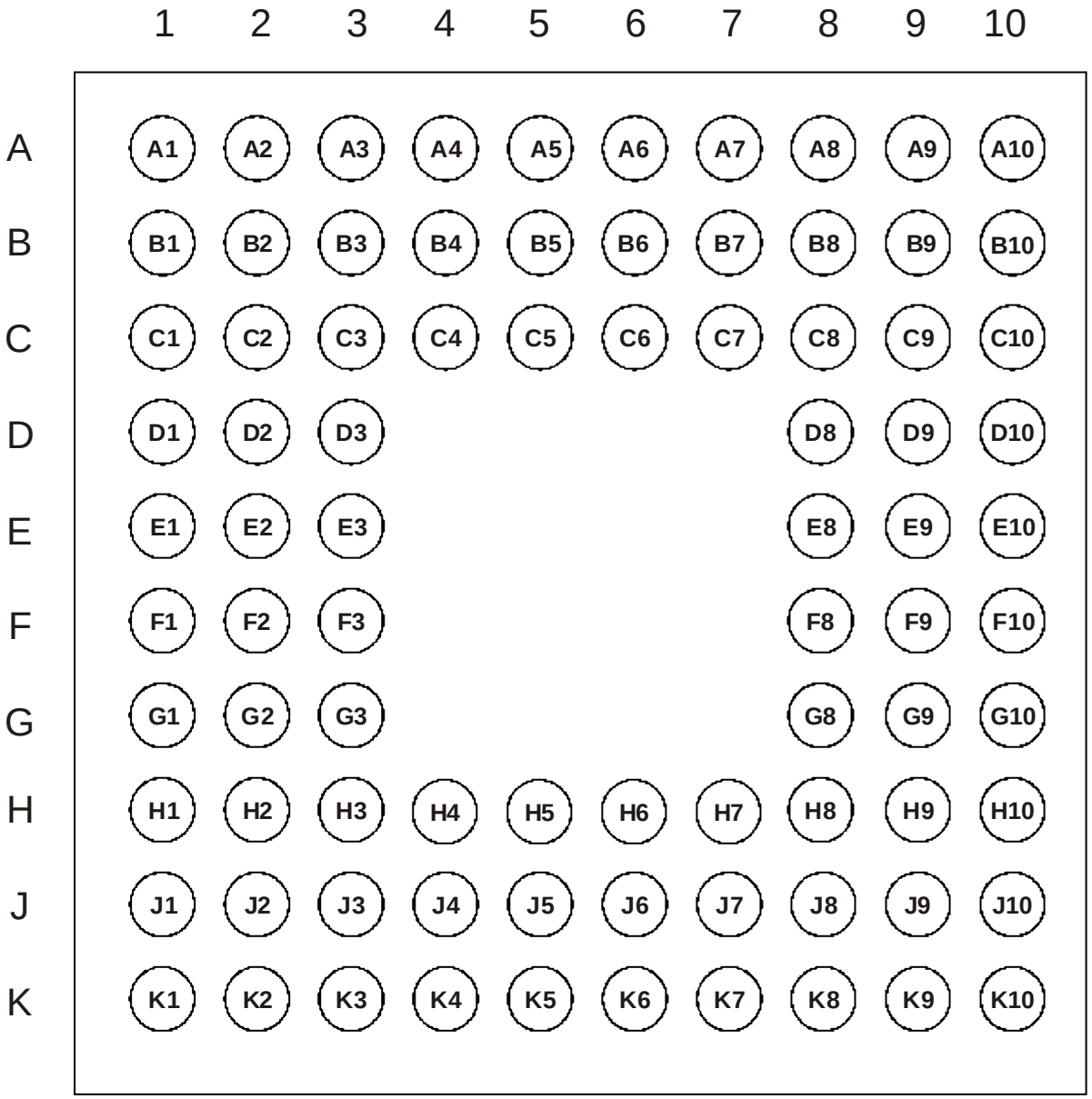


Figure 2.1: BlueCore2-Flash 6 x 6mm Packages (BC215159A-HK and BC215159A-TK)

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single ended receiver input
PIO[0]/RXEN	B1	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA, Class 1 only
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	D3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	K3	Analogue	For crystal or external clock input
XTAL_OUT	J3	Analogue	Drive for crystal
LOOP_FILTER	H2	Analogue	Connection to external PLL loop filter (Do not connect)

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G8	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	G9	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G10	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tristatable with weak internal pull-up	UART data output active high
UART_RX	H9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	H7	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	H8	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	J8	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	K8	Bi-directional	USB data minus

CODEC	Ball	Pad Type	Description
MIC_P	H3	Analogue	Microphone input positive
MIC_N	G3	Analogue	Microphone input negative
SPKR_P	J1	Analogue	Speaker output positive
SPKR_N	K1	Analogue	Speaker output negative

Test and Debug	Ball	Pad Type	Description
RESET	C7	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	D8	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C9	CMOS input with weak internal pull-up	Chip select for Serial Peripheral Interface, active low
SPI_CLK	C10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C8	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B9	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C6	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
FLASH_EN	B8	CMOS input with weak internal pull-down	Pull high to VDD_MEM

PIO Port	Ball	Pad Type	Description
PIO[2]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	E8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	F8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	F10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	F9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	C5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	C4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	H4	Bi-directional	Programmable input/output line
AIO[1]	H5	Bi-directional	Programmable input/output line
AIO[2]	J5	Bi-directional	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	K6	VDD	2.2-3.6V Voltage input
VDD_USB	K9	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC (1)
VDD_PADS	D10	VDD	Positive supply for all other digital input/output ports (2)
VDD_MEM	A6,A7, A9, H6, J6, K7	VDD	Positive supply for ROM memory and AIO ports
VDD_CORE	E10	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1, C2	VDD	Positive supply for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K4	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VSS_USB	J9, K10	VSS	Ground connections for UART/USB ports
VSS_PIO	A1, A2	VSS	Ground connections for PIO and AUX DAC
VSS_PADS	D9	VSS	Ground connection for input/output
VSS_MEM	A10, B5, B7, B10, J7	VSS	Ground connections for ROM memory and AIO ports
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry
VSS_RADIO	D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	J2, J4, K2	VSS	Ground connections for analogue circuitry
VSS	F3	VSS	Ground connection for internal package shield

Unconnected Terminals	Ball	Description
	A4, A5, A8, B6 and K5	Leave unconnected

Notes:

(1) Positive supply for PIO[3:0] and PIO[11:8].

(2) Positive supply for SPI/PCM ports and PIO[7:4].

3 10 x 10 Package Information

3.1 BC219159A-BN Pinout Diagram

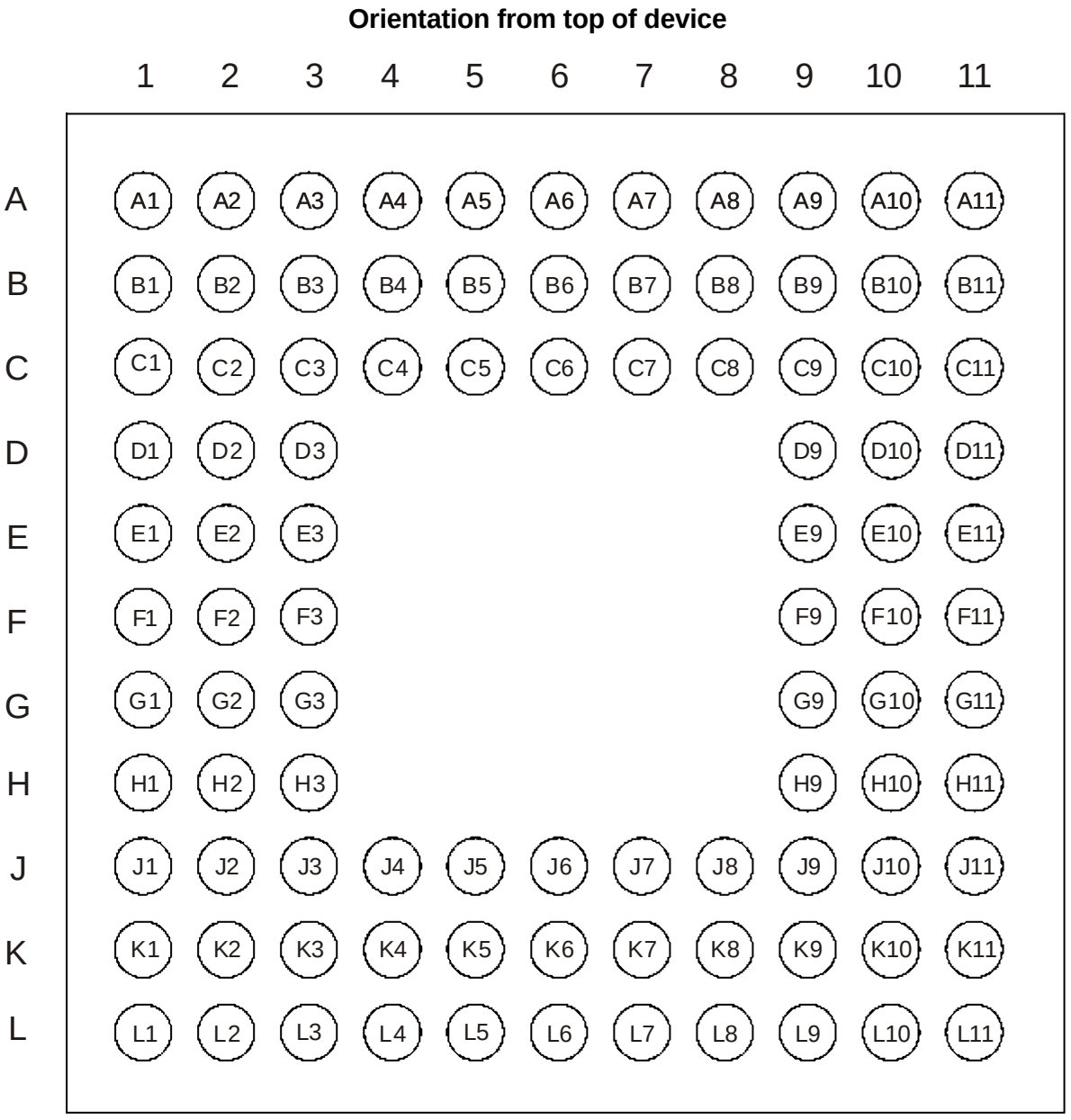


Figure 3.1: BlueCore2-Flash 10 x 10mm LFBGA Package (BC219159A-BN)

3.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D2	Analogue	Single ended receiver input
PIO[0]/RXEN	D3	Bi-directional with programmable strength internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C4	Bi-directional with programmable strength internal pull-up/down	Control output for external PA Class 1 only
BAL_MATCH	A1	Analogue	Tie to VSS_RADIO
RF_CONNECT	B1	Analogue	50O RF matched I/O
AUX_DAC	C2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L3	Analogue	For crystal or external clock input
XTAL_OUT	L4	Analogue	Drive for crystal
LOOP_FILTER	J2	Analogue	Connection to external PLL loop filter (Do not connect)

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G10	CMOS output, tristatable with weak internal pull-down	Synchronous data output
PCM_IN	H11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	G11	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H10	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	J10	CMOS output, tristatable with weak internal pull-up	UART data output active high
UART_RX	J11	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	L11	CMOS output, tristatable with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L9	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L8	Bi-directional	USB data minus

CODEC	Ball	Pad Type	Description
MIC_P	K2	Analogue	Microphone input positive
MIC_N	L2	Analogue	Microphone input negative
SPKR_P	J5	Analogue	Speaker output positive
SPKR_N	J4	Analogue	Speaker output negative

Test and Debug	Ball	Pad Type	Description
RESET	F9	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
RESETB	G9	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	C10	CMOS input with weak internal pull-up	Chip select for Synchronous Peripheral Interface, active low
SPI_CLK	D10	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	D11	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	C11	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	E9	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
FLASH_EN	B10	CMOS input with weak internal pull-down	Pull high to VDD_MEM

PIO Port	Ball	Pad Type	Description
PIO[2]	C3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[3]	B2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[4]	H9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[5]	J8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[6]	K8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[7]	K9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[8]	B3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	K5	Bi-directional	Programmable input/output line
AIO[1]	J6	Bi-directional	Programmable input/output line
AIO[2]	K7	Bi-directional	Programmable input/output line

PIO Port	Ball	Pad Type	Description
D[0]	B5	Bi-directional with weak internal pull-down	Programmable input/output line
D[1]	C6	Bi-directional with weak internal pull-down	Programmable input/output line
D[2]	B6	Bi-directional with weak internal pull-down	Programmable input/output line
D[3]	A7	Bi-directional with weak internal pull-down	Programmable input/output line
D[4]	A8	Bi-directional with weak internal pull-down	Programmable input/output line
D[5]	B8	Bi-directional with weak internal pull-down	Programmable input/output line
D[6]	A9	Bi-directional with weak internal pull-down	Programmable input/output line
D[7]	A10	Bi-directional with weak internal pull-down	Programmable input/output line
D[8]	C5	Bi-directional with weak internal pull-down	Programmable input/output line
D[9]	A6	Bi-directional with weak internal pull-down	Programmable input/output line
D[10]	C7	Bi-directional with weak internal pull-down	Programmable input/output line
D[11]	B7	Bi-directional with weak internal pull-down	Programmable input/output line
D[12]	C8	Bi-directional with weak internal pull-down	Programmable input/output line
D[13]	C9	Bi-directional with weak internal pull-down	Programmable input/output line
D[14]	B9	Bi-directional with weak internal pull-down	Programmable input/output line
D[15]	A11	Bi-directional with weak internal pull-down	Programmable input/output line

Power Supplies and Control	Ball	Pad Type	Description
VREG_IN	L7	VDD	2.2-3.6V Voltage input
VDD_USB	L10	VDD	Positive supply for UART/USB ports
VDD_PIO	A3	VDD	Positive supply for PIO and AUX DAC (1)
VDD_PADS	E11	VDD	Positive supply for all other digital input/output ports (2)
VDD_DIG	L6	VDD	Positive 1.8V supply for VDD_MEM and VDD_CORE
VDD_MEM	B11, K6	VDD	Positive supply for ROM memory and AIO and Extended PIO ports
VDD_CORE	F11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	E3	VDD	Positive supply for RF circuitry
VDD_ANA	L5	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VDD_BALUN	F1	VDD	Positive supply for balun
VSS_USB	K10	VSS	Ground connection for UART/USB ports
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_PADS	E10	VSS	Ground connection for input/output
VSS_MEM	D9, J9	VSS	Ground connections for ROM memory and AIO ports
VSS_CORE	F10	VSS	Ground connection for internal digital circuitry
VSS_RADIO	E2, F3, G2	VSS	Ground connections for RF circuitry
VSS_VCO	G3, H2, H3	VSS	Ground connections for VCO and synthesiser
VSS_ANA	K4	VSS	Ground connection for analogue circuitry
VSS_BAL	G1,J1, K1	VSS	Ground connections for balun

Unconnected Terminals	Ball	Description
	C1, D1, E1, F2, H1, J3, J7, K3 and L1	Leave unconnected

Notes:

(1) Positive supply for PIO[3:0] and PIO[11:8].

(2) Positive supply for SPI/PCM ports and PIO[7:4].

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE, VDD_MEM, VDD_BAL	-0.40V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	-0.40V	3.70V
Supply Voltage: VREG_IN	-0.40V	4.20V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range	-40°C	105°C
Guaranteed RF performance range (1)	-25°C	85°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE, VDD_MEM, VDD_BAL	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_USB	1.70V	3.60V
Supply Voltage: VREG_IN	2.20V	4.20V

Note:

(1) Typical figures are given for RF performance between -40°C and +105°C.

Input/Output Terminal Characteristics				
Linear Regulator	**Min**	**Typ**	**Max**	**Unit**
Normal Operation				
Output Voltage (Iload = 70mA / Vreg_IN = 3.0V)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	250	ppm/C
Output Noise(1)(2)	-	-	1	mV rms
Load Regulation (Iload < 100mA)	-	-	50	mV/A
Settling Time(1)(3)	-	-	50	µs
Line Regulation(1)(4)	-20	-	-	dB
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Input Voltage	-	-	3.6	V
Dropout Voltage (Iload = 70mA)	-	-	350	mV
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	µA
Low Power Mode(5)				
Quiescent Current (excluding load, Iload < 100µA)	4	7	10	µA
Disabled Mode(6)				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

(1) Regulator output connected to 47nF pure and 4.7mF 2.2W ESR capacitors.

(2) Frequency range 100Hz to 100kHz.

(3) 1mA to 70mA pulsed load.

(4) Frequency range 100Hz to 10MHz.

(5) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

(6) Regulator is disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

Input/Output Terminal Characteristics (Continued)				
Digital Terminals	**Min**	**Typ**	**Max**	**Unit**
Input Voltage Levels				
V_{IL} input logic level low (VDD=3.0V)	-0.4	-	0.8	V
(VDD=1.8V)	-0.4	-	0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=3.0V	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=1.8V	VDD-0.4	-	-	V
Input and Tristate Current with:				
Strong pull-up	-100	-20	-10	µA
Strong pull-down	10	20	100	µA
Weak pull-up	-5	-1	0	µA
Weak pull-down	0	1	5	µA
I/O pad leakage current	-1	0	1	µA
C_I Input Capacitance	1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.57VDD_USB	-	-	V
Input leakage current				
VSS_USB< V_{IN}< VDD_USB (1)	-1	-	1	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage levels To correctly terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size (2)	12.5	14.2	16.5	mV
Output Voltage		monotonic(2)		
Voltage range (I_O=0mA)	VSS_PIO	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-120	-	120	mV
Integral non-linearity (2)	-1.5	-	1.5	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency [3]	8.0	-	32.0	MHz
Digital trim range [4]	5.0	6.2	8.0	pF
Trim step size [4]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance [5]	870	1500	2400	Ω
External Clock				
Input frequency [6]	8.0	-	40.0	MHz
Clock input level [7]	0.4	-	VDD_ANA	V pk-pk
Phase noise (at zero crossing)	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Min**	**Typ**	**Max**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO, VDD_ANA, VDD_BAL and VDD_MEM are at 1.8V unless shown otherwise.

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise.

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

[1] Internal USB pull-up disabled.

[2] Specified for an output voltage between 0.2V and VDD_PIO -0.2V.

[3] Integer multiple of 250kHz.

[4] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[5] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

[6] Clock input can be any frequency between 8 and 40MHz in steps of 250kHz + CDMA/3G TCXO frequencies of 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[7] Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN.

Input/Output Terminal Characteristics (Continued)				
Audio CODEC, 15-bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Microphone Amplifier				
Input full scale at maximum gain	-	3	-	mV rms
Input full scale at minimum gain	-	350	-	mV rms
Gain resolution (1)	-	3	-	dB
Distortion at 1kHz	-	-	-78	dB
Input referenced rms noise (2)	-	5	-	µV rms
Bandwidth	-	20	-	kHz
Input impedance	-	20	-	kΩ
Analog to Digital Converter				
Input sample rate (3)	-	1	-	MSamples/s
Output sample rate (4)	-	8	-	KSamples/s
Distortion and noise at 1kHz (relative to full scale)	-	-78	-75	dB
Digital to Analog Converter				
Gain Resolution	-	3	-	dB
Min Gain (5)	-	-14	-	dB
Max Gain (5)	-	+6	-	dB
Loudspeaker Driver				
Output voltage full scale swing	-	2.0	-	V Pk-Pk
Output current drive (at full scale swing) (6)	10	20	40	mA
Output full scale current (at reduced swing) (7)	-	75	-	mA
Output –3dB bandwidth	-	18.5	-	kHz
Distortion and noise (relative to full scale)	-	-75	-	dB
Allowed Load: resistive	8	-	OC	Ω
Allowed Load: capacitive	-	-	500	pF

Notes:

(1) 42dB range of gain control (under software control)

(2) Noise in bandwidth from 100Hz to 4kHz gain setting >17dB

(3) Single bit, 2nd order Σ–Δ ADC clocked at 1MHz

(4) This is the decimated and filtered output at 15-bit resolution

(5) 21dB gain range (under software control)

(6) Output for 0.1% THD, signal level of 2V Pk-Pk

(7) Output for 1%THD, Signal level of 1V Pk-Pk

5 Radio Characteristics

BlueCore2-Flash meets the Bluetooth specification v1.1 when used in a suitable application circuit between -40°C and +105°C.

Radio Characteristics, VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-	≤-70	dBm
	2.441	-	-84	-		dBm
	2.480	-	-84	-		dBm
Maximum received signal at 0.1% BER	2.402	-	+3	-	≥-20	dBm
	2.441	-	+3	-		dBm
	2.480	-	+3	-		dBm
Maximum RF transmit power (1)	2.402	-	6.0	-	-6 to +4(2)	dBm
	2.441	-	6.0	-		dBm
	2.480	-	6.0	-		dBm
Initial carrier frequency tolerance	2.402	-	12	-	±75	kHz
	2.441	-	10	-		kHz
	2.480	-	9	-		kHz
20dB bandwidth for modulated carrier	2.402	-	879	-	≤1000	kHz
	2.441	-	816	-		kHz
	2.480	-	819	-		kHz
Drift (single slot packet)	2.402	-	9	-	≤25	kHz
	2.441	-	9	-		kHz
	2.480	-	9	-		kHz
Drift (five slot packet)	2.402	-	10	-	≤40	kHz
	2.441	-	10	-		kHz
	2.480	-	10	-		kHz
Drift Rate	2.402	-	8	-	20	kHz/50 µs
	2.441	-	8	-		kHz/50 µs
	2.480	-	8	-		kHz/50 µs
RF power control range		-	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Radio Characteristics, VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
$Df1_{avg}$ "Maximum Modulation"	2.402	-	165	-	140<$\Delta f1_{avg}$<175	kHz
	2.441	-	165	-		kHz
	2.480	-	165	-		kHz
$Df2_{max}$ "Minimum Modulation"	2.402	-	150	-	115	kHz
	2.441	-	150	-		kHz
	2.480	-	150	-		kHz
C/I co-channel		-	9	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ [3] [5]		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ [3] [5]		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ [3] [5]		-	-35	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ [3] [5]		-	-21	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ [3] [5]		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ [3] [5]		-	-45	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{image}$ [3] [5]		-	-18	-	≤-9	dB
Adjacent channel transmit power $F=F_0\pm2MHz$ [4] [5]		-	-35	-	≤-20	dBc
Adjacent channel transmit power $F=F_0\pm3MHz$ [4] [5]		-	-55	-	≤-40	dBc

Notes:

[1] BlueCore2-Flash firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits.

[2] Class 2 RF transmit power range, Bluetooth specification v1.1.

[3] Up to five exceptions are allowed in v1.1 of the Bluetooth specification.

[4] Up to three exceptions are allowed in v1.1 of the Bluetooth specification.

[5] Measured at F_0 = 2441MHz.

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +3dBm		
Mode	**Avg**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV3 (No Sniff Mode) (Slave)	32.0	mA
SCO connection HV1 (Slave)	43.0	mA
SCO connection HV1 (Master)	43.0	mA
ACL data transfer 115.2kbps UART no traffic (Master)	7.0	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	24.0	mA
ACL data transfer 720kbps UART (Master or Slave)	50.0	mA
ACL data transfer 720kbps USB (Master or Slave)	50.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	85.0	mA
Reset (RST high or RSTB low)	55.0	mA

6 Device Diagrams

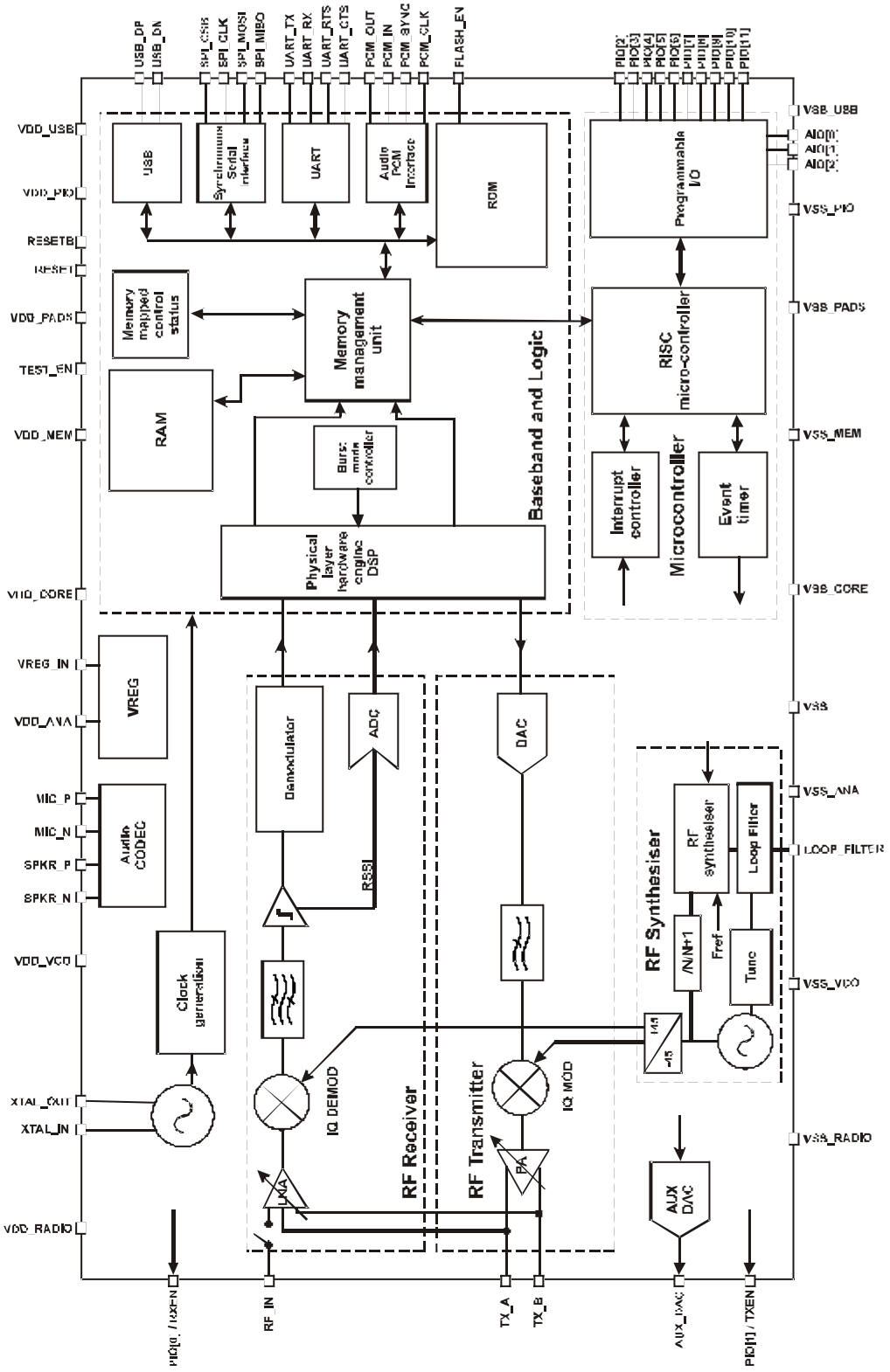


Figure 6.1: BlueCore2-Flash Device Diagram for 6 x 6mm TFBGA Package

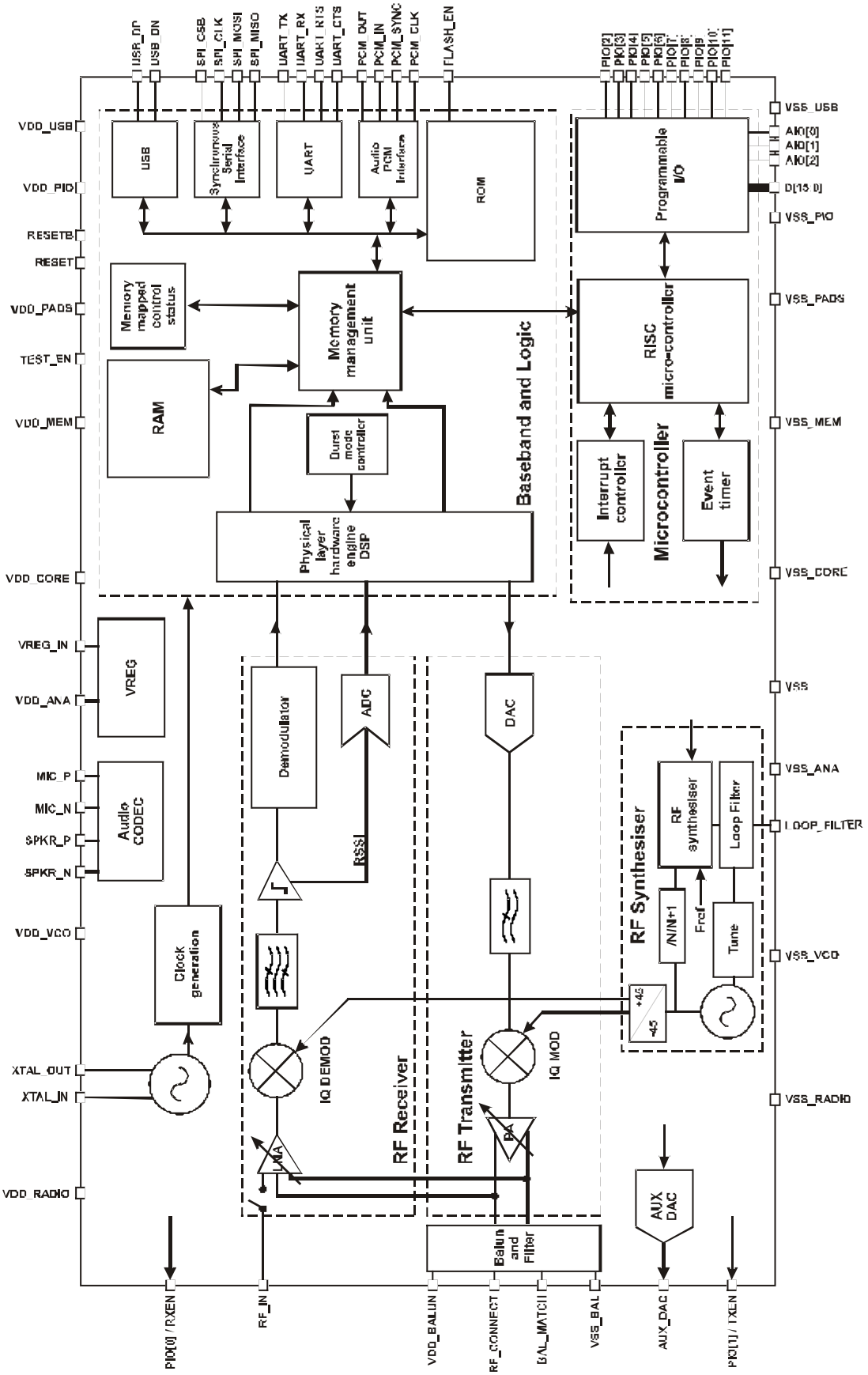


Figure 6.2: BlueCore2-Flash Device Diagram for 10 x 10mm LFBGA Package

7 Description of Functional Blocks

7.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore2-Flash to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

7.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation and differential mode is used for Class 2 operation.

7.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

7.2 RF Transmitter

7.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot which results in a controlled modulation index. A digital baseband transmit filter provides the required spectral shaping.

7.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore2-Flash to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

7.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

7.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes or LC resonators.

7.4 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

7.5 Baseband and Logic

7.5.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.5.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

7.5.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

7.5.4 RAM

32Kbytes of on-chip RAM is provided and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

7.5.5 Flash ROM

4Mbits of Flash ROM is provided for system firmware implementation in the BC215159A packages and 8Mbits is available in the BC219159A package.

7.5.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore2-Flash acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

7.5.7 Synchronous Serial Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging.

7.5.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

7.5.9 Audio PCM Interface

The Audio Pulse Code Modulation (PCM) Interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

7.6 Microcontroller

The microcontroller, interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit Reduced Instruction Set Computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

7.6.1 Programmable I/O

BlueCore2-Flash has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

7.6.2 Extended Programmable I/O Port

BC219159A-BN has an extra 16 I/O lines available. These are controlled by firmware running on the device. Normal functions running on PIO ports [11:0] should not be transferred to the extended ports. An example application for these extra lines could be keyboard scanning. Extended PIO lines can only be used for certain functions, please contact CSR for details.

7.6.3 Audio CODEC

BlueCore2-Flash has a 15-bit Audio CODEC that has a 8kHz sampling frequency. This has been designed for use in voice applications such as headsets and hands-free kits. The CODEC has integrated input/output amplifiers capable of driving a microphone and speaker with minimum external components.

8 CSR Bluetooth Software Stacks

BlueCore2-Flash is supplied with Bluetooth stack firmware which runs on the internal RISC microcontroller. This is compliant with the Bluetooth specification v1.1.

The BlueCore2-Flash software architecture allows Bluetooth processing overheads to be shared in different ways between the internal RISC microcontroller and the host processor. The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

Running the upper stack on BlueCore2-Flash reduces (or eliminates, in the case of a virtual machine (VM) application) the need for host-side software and processing time. Running the upper layers on the host processor allows greater flexibility.

8.1 BlueCore HCI Stack

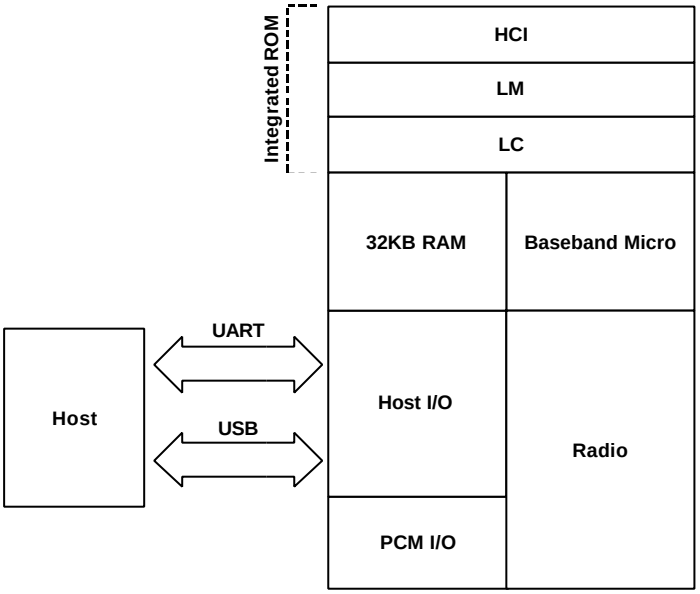


Figure 8.1: BlueCore HCI Stack

In this implementation the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). All upper layers must be provided by the Host processor.

8.1.1 Key Features of the HCI Stack

Standard Bluetooth Functionality

The firmware has been written against the Bluetooth Core Specification v1.1.

- Bluetooth components: Baseband (including LC), LM and HCI
- Standard USB v1.1 and UART (H4) HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kb/s asymmetric (1)
- Operation with up to 7 active slaves (1)
- Maximum number of simultaneous active ACL connections: 7 (2)
- Maximum number of simultaneous active SCO connections: 3 (2)
- Operation with up to 3 SCO links, routed to one or more slaves
- Role switch: can reverse Master/Slave relationship
- All standard SCO voice codings, plus “transparent SCO”
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes

The firmware’s supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

Notes:

(1) Maximum allowed by Bluetooth specification v1.1.

(2) BlueCore2-Flash supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.1.

Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth H4 UART Host Transport.
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:
  - Access to the chip's general-purpose PIO port
  - Access to the chip's Bluetooth clock – this can help transfer connections to other Bluetooth devices
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
  - Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code.
- A block of BCCMD commands provides access to the chip's "persistent store" configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a deep sleep state
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LED's via the chip's PIO port.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed over HCI (over BCSP). However, a single SCO channel can be routed over the chip's single PCM port (at the same time as routing up to two other SCO channels over HCI). [Future versions of the BlueCore2 firmware will be able to exploit the hardware's ability to route up to three SCO channels through the single PCM port].

8.2 BlueCore RFCOMM Stack

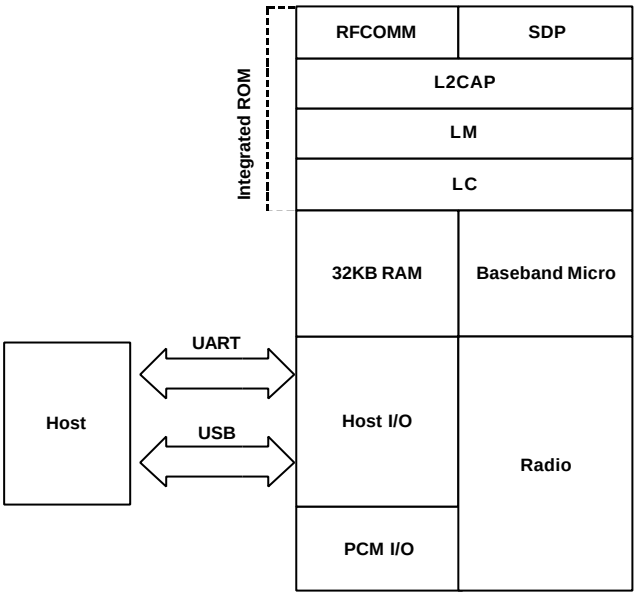


Figure 8.2: BlueCore RFCOMM Stack

In this version of the firmware the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

8.2.1 Key Features of the BlueCore2-Flash RFCOMM Stack

Interfaces to Host

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350Kb/s

Security

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

8.3 BlueCore Virtual Machine Stack

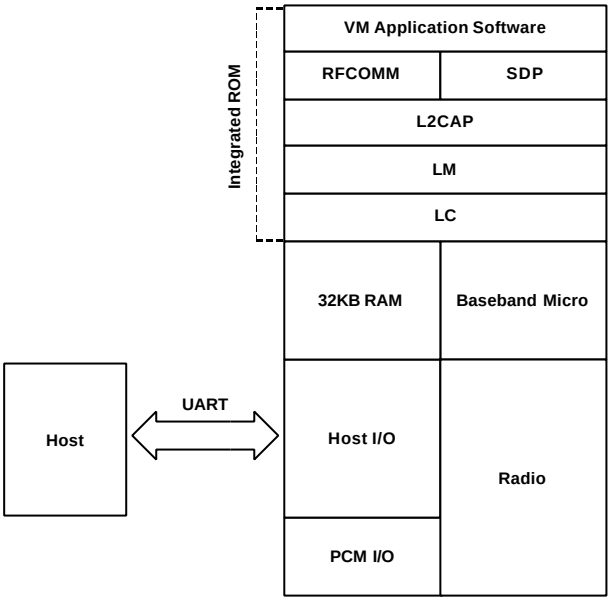


Figure 8.3: Virtual Machine

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

On successful completion of firmware development and testing using BlueCore2-Flash (BC215159A), CSR can commit the code to a mask set for mass production of the device. A Non Recurring Engineering (NRE) charge will be required.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

8.4 Host-Side Software

BlueCore2-Flash can be ordered with companion host-side software:

BlueCore2-PC includes software for a full Windows® 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.

BlueCore2-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

8.5 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore2-Flash, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as 'C' source or object code.

8.6 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore2 hardware and software, and as toolkits for developing on-chip and host software.

9 External Interfaces

9.1 Transmitter/Receiver Inputs and Outputs

Terminals TX_A and TX_B form a balanced current output. They require a DC path to VDD and should be connected through a balun to the antenna. The output impedance is capacitive and remains constant, irrespective of whether the transmitter is enabled or disabled. For Class 2 operation these terminals also act as differential receive input terminals with an internal TX/RX switch.

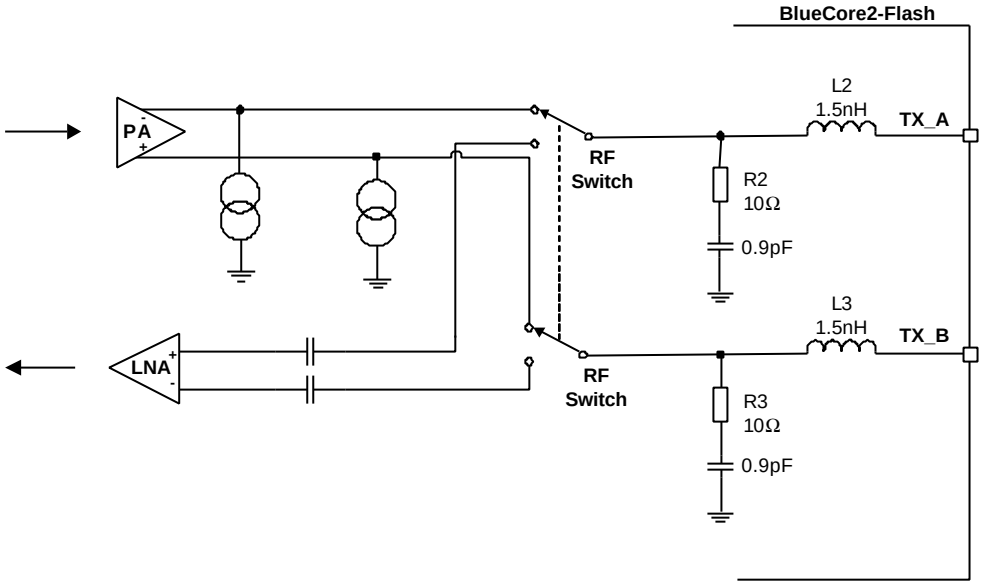


Figure 9.1: Circuit TX/RX_A and TX/RX_B

For Class 1 operation the RF_IN ball is provided which is single-ended. A swing of up to 0.5V root mean squared (rms) can be tolerated at this terminal. An external antenna switch can be connected to RF_IN.

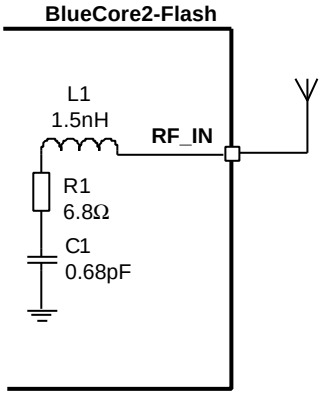


Figure 9.2: Circuit RF_IN

9.2 RF Plug and Go

For BC219159A-BN, terminal RF_CONNECT forms an unbalanced output/input with a nominally 50Ω impedance which means it can be directly connected to an antenna requiring no impedance matching networks.

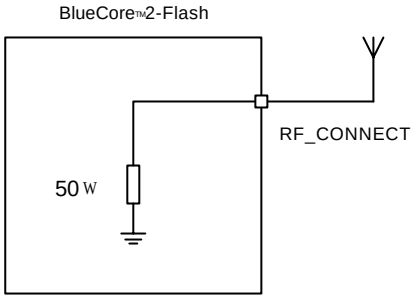


Figure 9.3: Circuit for RF_CONNECT

9.3 Asynchronous Serial Data Port (UART) and USB Port

UART_TX, UART_RX, UART_RTS and UART_CTS form a conventional asynchronous serial data port. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signalling levels are 0V and VDD_USB and are inverted with respect to the signaling on an RS232 cable. The interface is programmable over a variety of bit rates; no, even or odd parity; one or two stop bits and hardware flow control on or off. The default condition on power-up is pre-assigned in the ROM memory.

The maximum UART data rate is 1.5MBaud. Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and is active low. UART_CTS is an input and is active low. These signals operate according to normal industry convention.

The port carries a number of logical channels: HCI data (both SCO and ACL), HCI commands and events, L2CAP API, RFCOMM API, SDP and device management. For the UART, these are combined into a robust tunnelling protocol, BlueCore Serial Protocol (BCSP), where each channel has its own software flow control and cannot block other data channels. In addition, the Bluetooth specification v1.1, HCI UART Transport Layer (part H4) format is supported.

Full speed USB (12Mbit/s) is supported in accordance with the Bluetooth specification v1.1, HCI USB Transport Layer (H2). USB_DP and USB_DN are available on dedicated terminals. Both Open Host Controller Interface (OHCI) and Universal Host Controller Interfaces (UHCI) are supported.

9.4 UART Bypass

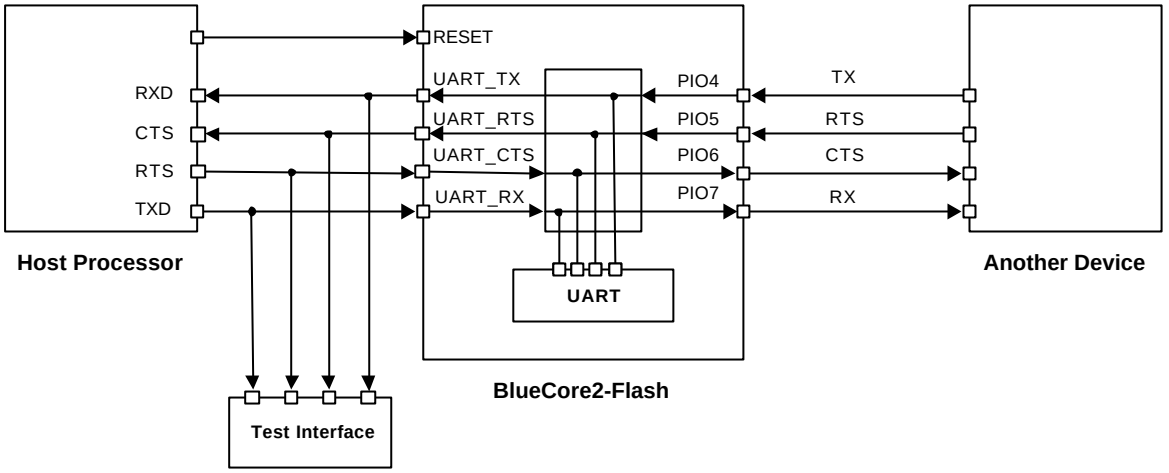


Figure 9.4: UART Bypass Architecture

9.4.1 UART Configuration while RESET is Active

The UART interface for BlueCore2-Flash while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore2-Flash reset is de-asserted and the firmware begins to run.

9.4.2 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore2-Flash can be used. The default state of BlueCore2-Flash after reset is de-asserted is for the host UART bus to be connected to the BlueCore2-Flash UART, thereby allowing communication to BlueCore2-Flash via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore2-Flash upon this, it will switch the bypass to PIO[7:4] as shown in Figure 9.4. Once the bypass mode has been invoked, BlueCore2-Flash will enter the deep sleep state indefinitely.

In order to re-establish communication with BlueCore2-Flash, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

9.5 PCM CODEC Interface

PCM_OUT, PCM_IN, PCM_CLK and PCM_SYNC carry up to three bi-directional channels of voice data, each at 8ksamples/s. The format of the PCM samples can be 8-bit A-law, 8-bit µ-law, 13-bit linear or 16-bit linear. The PCM_CLK and PCM_SYNC terminals can be configured as inputs or outputs, depending on whether BlueCore2-Flash is the Master or Slave of the PCM interface.

BlueCore2-Flash interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and µ-law CODEC
- Motorola MC145481 8-bit A-law and µ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

BlueCore2-Flash is also compatible with the Motorola SSI™ interface.

9.6 Serial Peripheral Interface

BlueCore2-Flash is a slave device that uses terminals SPI_MOSI, SPI_MISO, SPI_CLK and SPI_CSB. This interface is used for program emulation/debug and IC test.

Note:
The designer should be aware that no security protection is built into the hardware or firmware associated with this port, so the terminals should not be permanently connected in a PC application.

9.7 I/O Parallel Ports

Fifteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:8] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_MEM. Extended I/O lines D[15:0] are also powered from VDD_MEM.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

BlueCore2-Flash has three general purpose analogue interface pins, AIO[0], AIO[1] and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip bandgap reference voltage, the other two may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the bandgap reference voltage and a variety of clock signals ; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_MEM (1.8V).

9.7.1 PIO Defaults for BTv1.1 HCI level Bluetooth Stack

PIO[0]	Pull-high on boot to select USB transport rather than BCSP Control output for external LNA after boot up completion
PIO[1]	Pull-high on boot to select 16MHz reference clock frequency rather than 26MHz Control output for external PA (Class 1 operation) after boot up completion
PIO[2]	Clock request output
PIO[3]	Clock request “OR” gate input
PIO[4]	UART bypass (UART_TX)
PIO[5]	UART bypass (UART_RTS)
PIO[6]	UART bypass (UART_CTS) E^2 SCL
PIO[7]	UART bypass (UART_RX) E^2 SDA
PIO[8]	E^2 write protect
AIO[2]	Vref output. Must be decoupled

Notes:

PIO[7:6] are used for two purposes, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode.

CSR cannot guarantee that these terminal functions remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

9.8 I2C Interface

PIO[8:6] can be used to form a Master I^2C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO lines need to be pulled-up through 2.2kΩ resistor

For connection to EEPROM’s, Refer to Document bcore-an-008Pa for information on the type of devices which are currently supported.

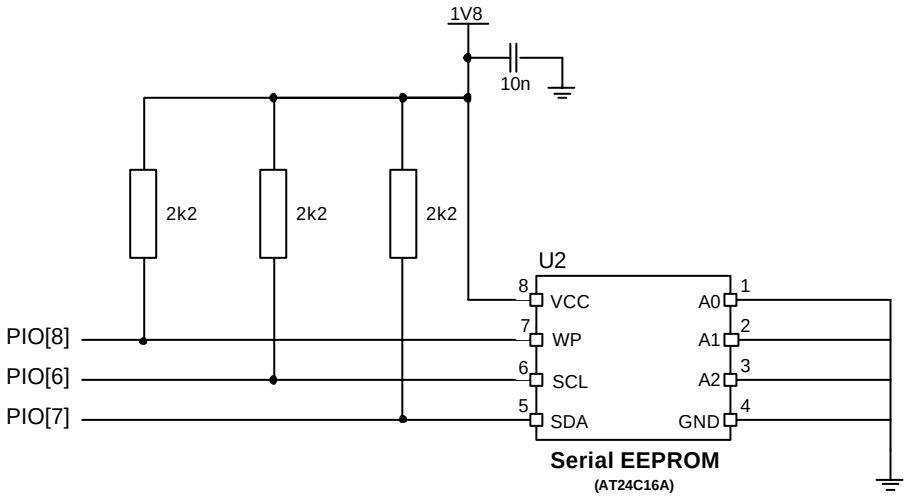


Figure 9.5: Example EEPROM Connection

9.9 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore2-Flash where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore2-Flash.

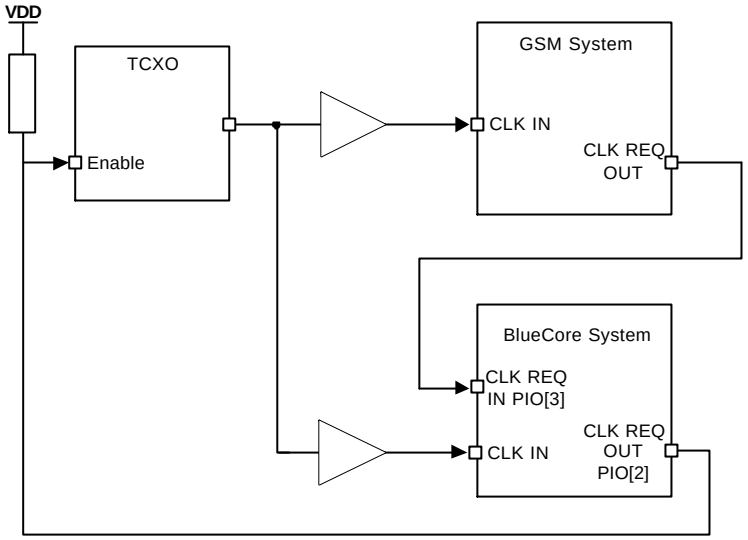


Figure 9.6: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470k resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

9.10 Reset

BlueCore2-Flash may be reset from several sources: RESET or RESETB pins, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET is applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is 'ORed' on chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

Following a reset, BlueCore2-Flash assumes the maximum XTAL_IN frequency which ensures that the internal clocks run at a safe (low) frequency until BlueCore-ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore2-Flash free runs, again at a safe frequency.

9.11 Power Supply

9.11.1 Voltage Regulator

An on-chip linear voltage regulator can be used to power the 1.8V dependant supplies. It is advised that a smoothing circuit using a 2.2µF low ESR capacitor and 2.2Ω resistor be placed on the output VDD_ANA.

The regulator is switched into a low power mode when the device is sent into deep sleep mode. When the on chip regulator is not required VDD_ANA is a 1.8V input and VREG_IN must be either open circuit or tied to VDD_ANA.

On the BC219159A-BN VDD_DIG is a filtered output for digital circuitry.

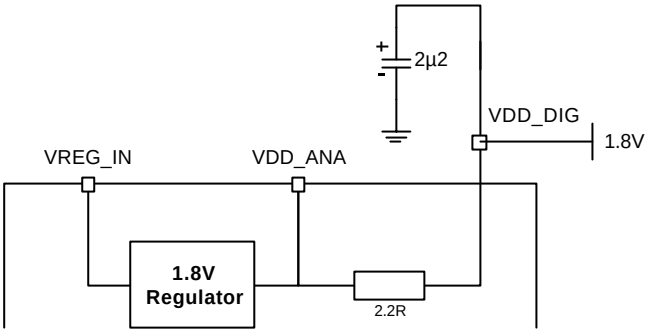


Figure 9.7: VDD_DIG Output Circuit

9.11.2 Sequencing

It is recommended that VDD_CORE, VDD_RADIO, VDD_VCO and VDD_MEM are powered at the same time. The order of powering supplies for VDD_CORE, VDD_PIO, VDD_PADS and VDD_USB is not important. However if VDD_CORE is not present, all inputs have a weak pull-down irrespective of the reset state.

9.11.3 Sensitivity to Disturbances

It is recommended that if you are supplying BlueCore2-Flash from an external voltage source that VDD_VCO, VDD_ANA and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided. A simple RC filter is recommended for VDD_CORE as this reduces transients put back onto the power supply rails.

The transient response of the regulator is also important as at the start of a packet, power consumption will jump to the levels defined in average current consumption section. It is essential that the power rail recovers quickly, so the regulator should have a response time of 20µs or less.

9.12 Audio CODEC

The BlueCore2-Flash audio CODEC is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8 Volt power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and a Σ-Δ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram is shown below.

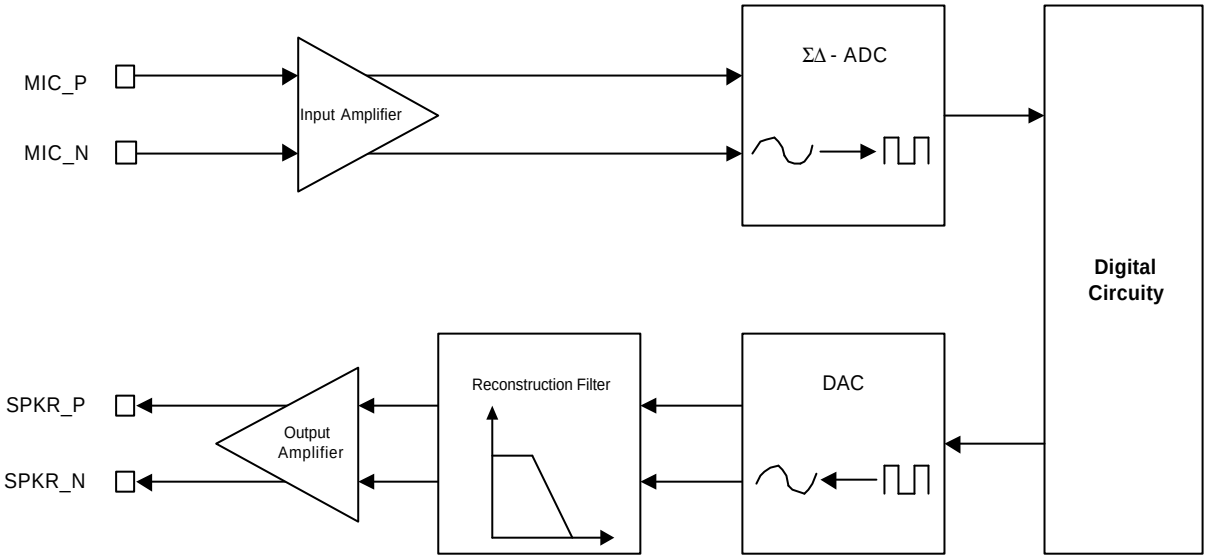


Figure 9.8: BlueCore2-Flash CODEC Diagram

9.12.1 Input Stage

A low noise variable gain amplifier amplifies the signal difference between inputs MIC_N and MIC_P. The input may be from either a microphone or line. The amplified signal is then digitised by a second order Σ-Δ ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via a PSKEY and has a 42dB range with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation with a microphone whereas the line input may be simply a.c. coupled. The following sections explain each of these modes. Single ended signals are supported by BlueCore2-Flash: a single ended signal may be driven into either MIC_N or MIC_P with the undriven input coupled to ground by a capacitor.

At the maximum gain the signal to noise ratio is better than 60dB and distortion is better than –75dB relative to a full-scale sine wave. At lower gain settings (such as used for line input) the signal to noise ratio improves to better than -75dB.

9.12.2 Microphone Input

The BlueCore2-Flash audio CODEC has been designed for use with microphones that have sensitivities between –60 and –40dBV. The sensitivity of –60dBV is equivalent to a microphone output of 1µA when presented with an input level of 94dB SPL and loaded with 1kΩ. The microphone should be biased as shown in Figure 9.9.

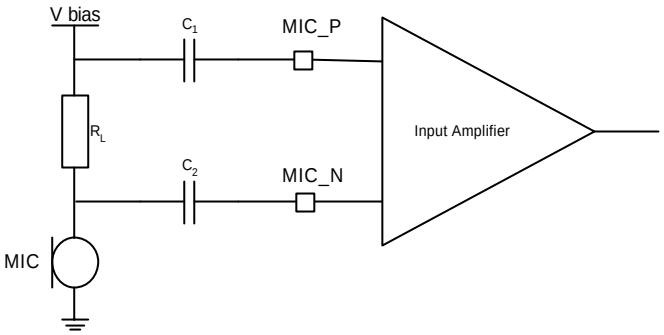


Figure 9.9: BlueCore2-Flash Microphone Biasing

The input impedance at MIC_N and MIC_P is typically 20kΩ. C1 and C2 should be 47nF. R_L sets the microphone load impedance and is normally between 1 and 2kΩ. V bias should be chosen to suit the microphone and have sufficient low noise. It may be obtained by filtering the output of a PIO line.

9.12.3 Line Input

If the input gain is set to less than 21dB BlueCore2-Flash automatically selects line input mode. In this mode the input impedance at MIC_N and MIC_P is increased to 130kΩ typical. At the minimum gain setting the maximum input signal level is 380 mV rms. Figures 9.11 and 9.12 show two circuits for line input operation and show connections for either differential or single ended inputs.

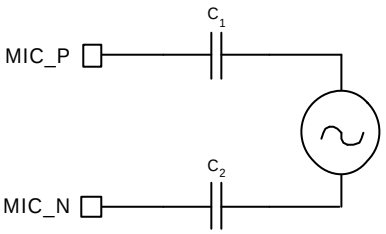


Figure 9.11: Differential Microphone Input

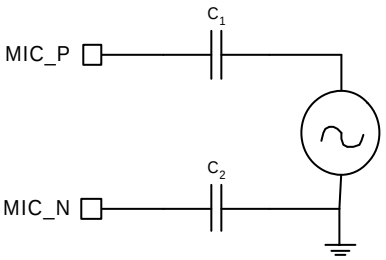


Figure 9.12: Single-ended Microphone Input

Note:

C_1 and C_2 should be 15nF.

9.12.4 Output stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR_P and SPKR_N. The output amplifier is capable of driving a speaker directly if its impedance is greater than or equal to 8Ω. The amplifier is stable with capacitive loads up to 500pF.

The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700 mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than –75dB.

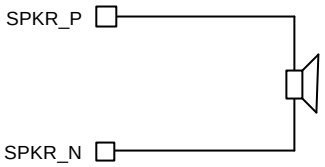


Figure 9.13: Speaker Output

10 Application Schematic

10.1 6 x 6 TFBGA 84-Ball Package

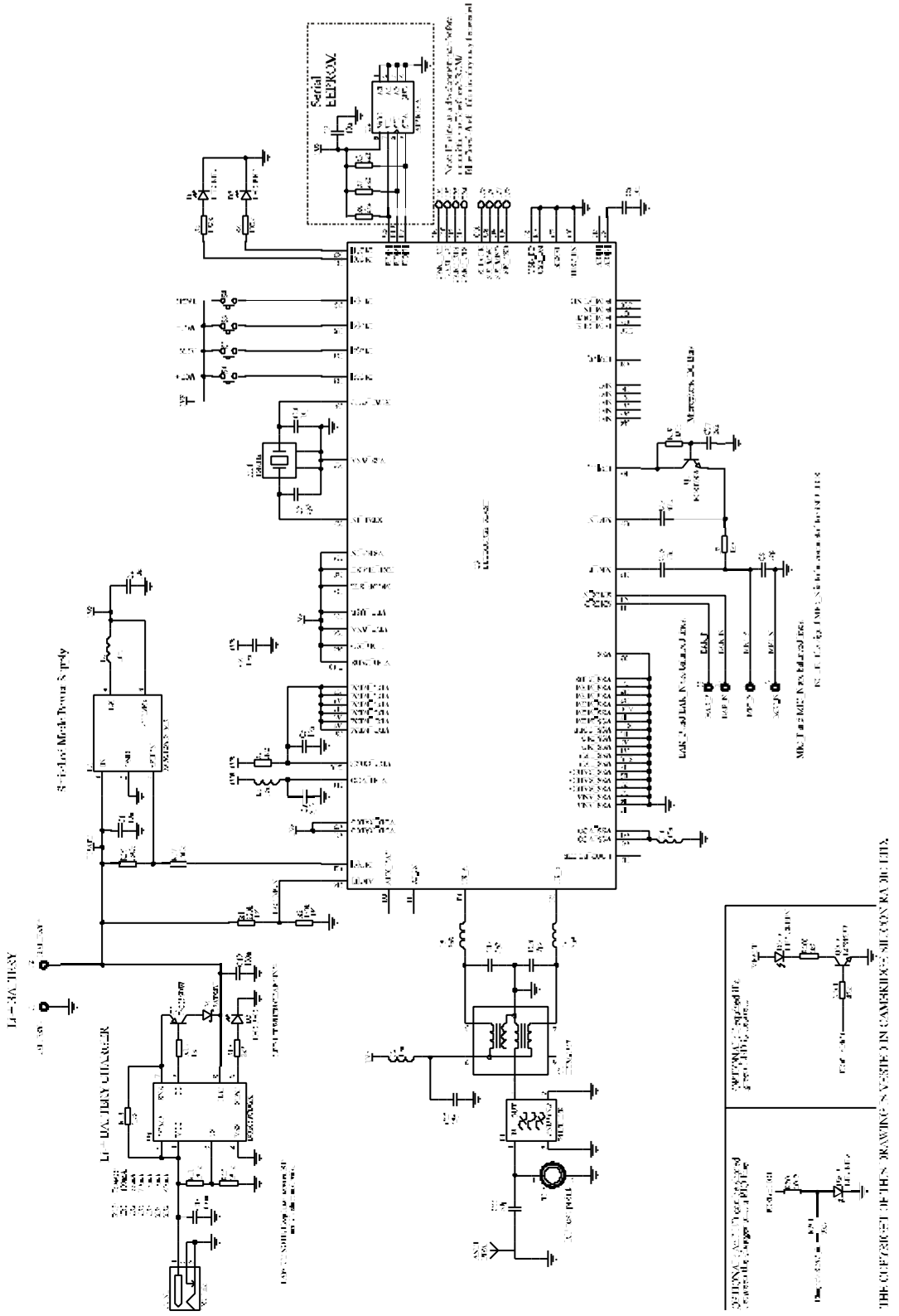


Figure 10.1: Example of a Headset Design for 6 x 6 TFBGA Package

10.2 10 x 10 LFBGA 96-Ball Package

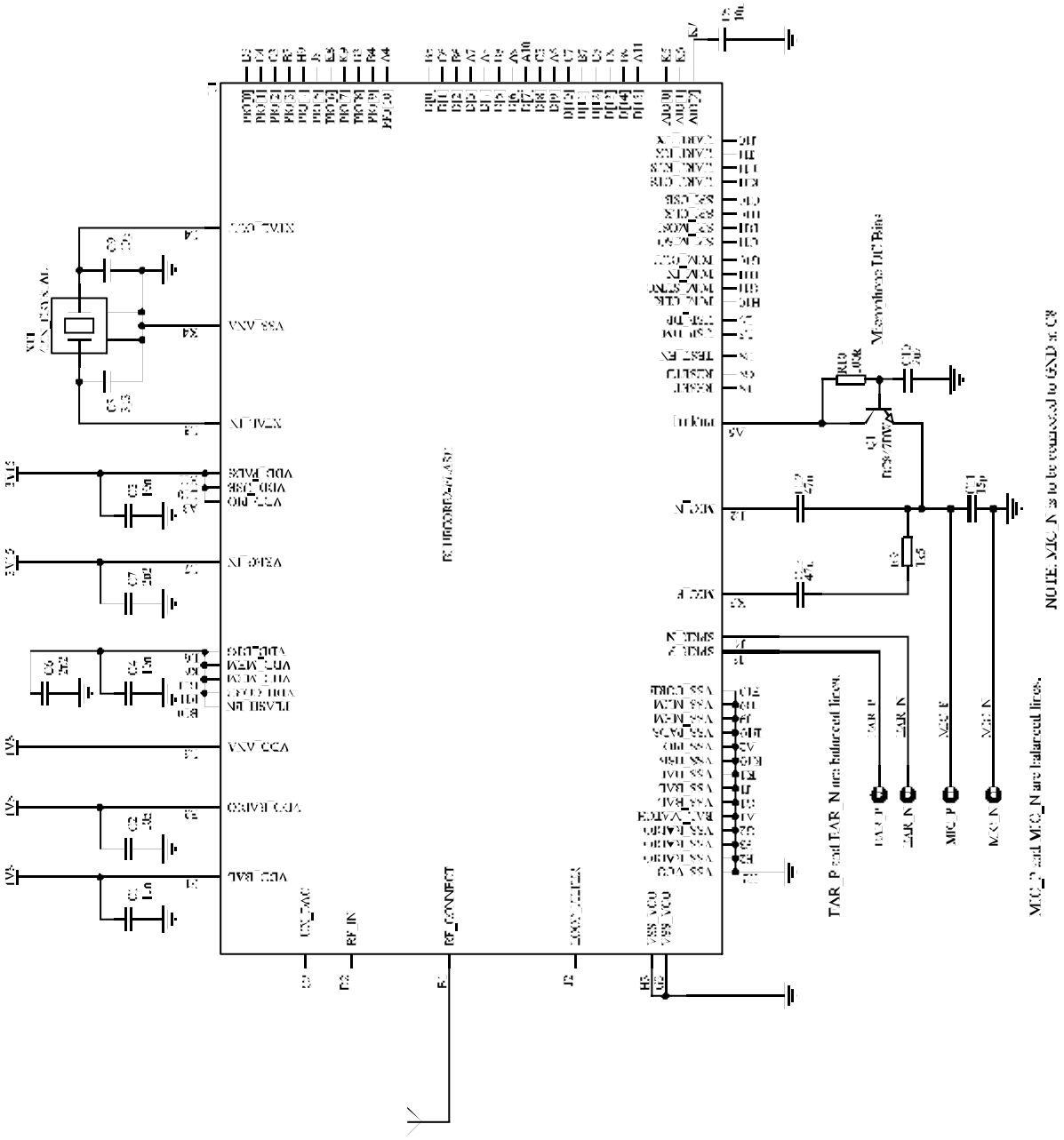
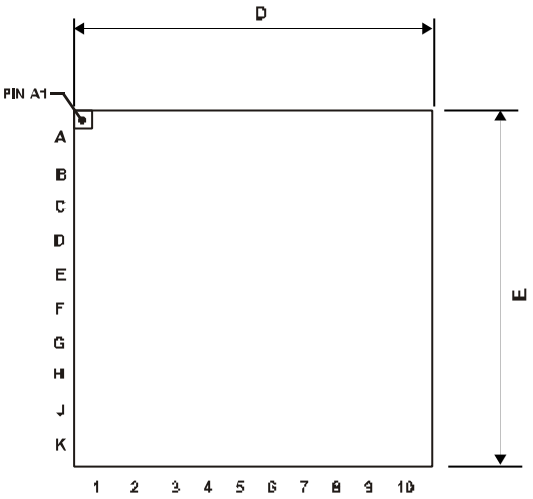


Figure 10.2: Application Circuit for Radio Characteristics Specification 10 x 10 LFBGA Package

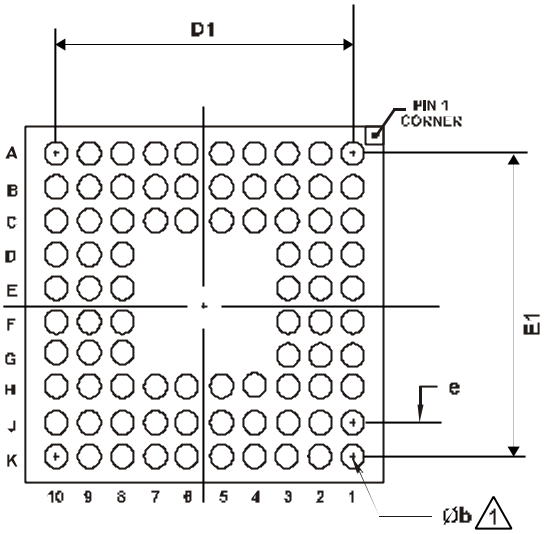
11 Package Dimensions

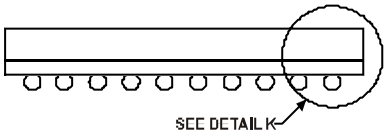
11.1 6 x 6 TFBGA 84-Ball Package

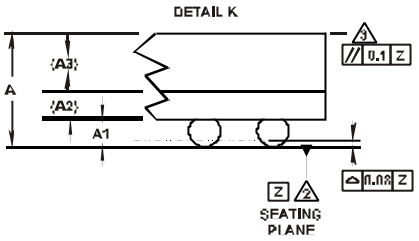
Top View



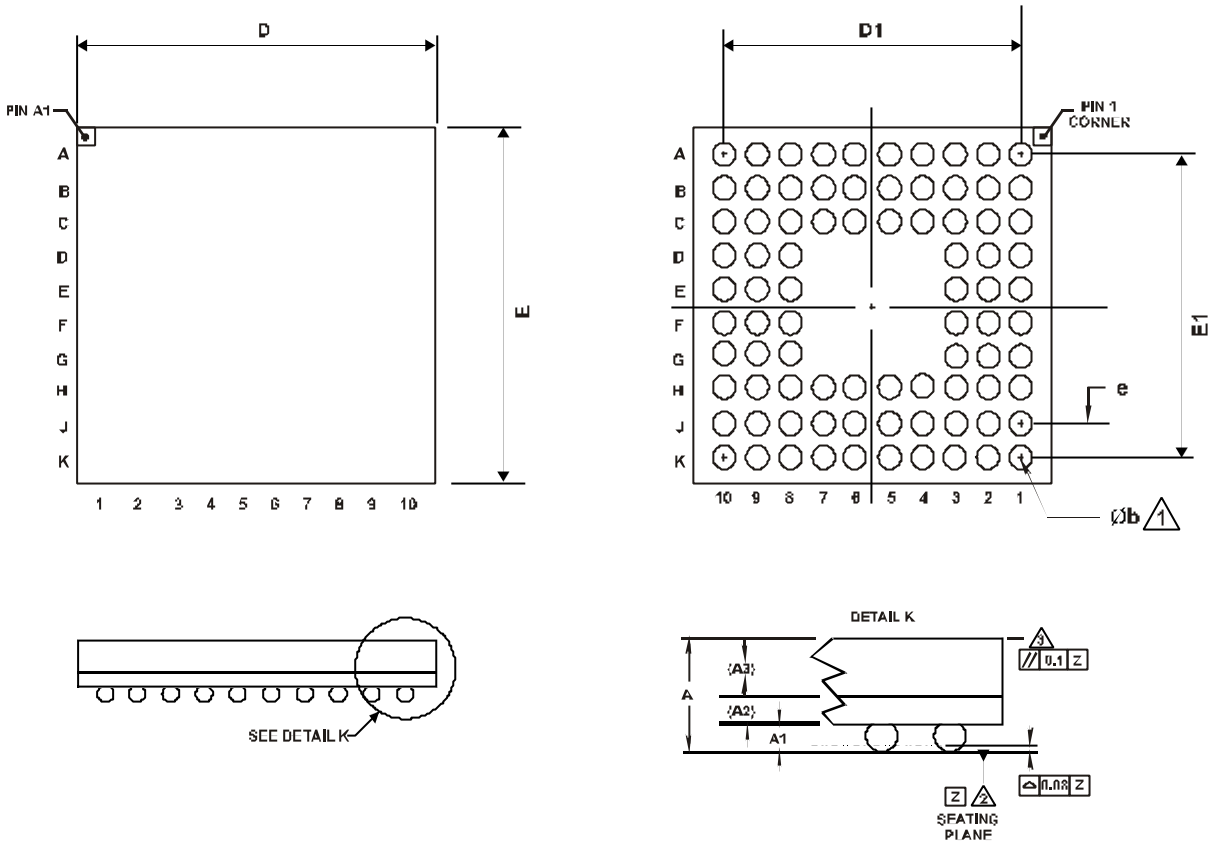
Bottom View







BC215159A-HK and BC215159A-TK 84-Ball 6x6x1.2mm TFBGA				
DIM	MIN	TYP	MAX	NOTES
A	0.8		1.2	1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A1	0.2		0.3	
A2		0.22		
A3		0.45		2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
b	0.25	0.30	0.35	
D		6		3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
E		6		
e		0.50		
D1		4.50		
E1		4.50		
84-Ball TFBGA 6X6X1.2 mm (JEDEC MO-216)				UNIT: MM



BC213159AXX-EK and BC213159AXX-RK 84-Ball 6x6x1mm VFBGA				
DIM	MIN	TYP	MAX	NOTES
A	0.8		1	
A1	0.2		0.3	
A2		0.22		
A3		0.45		
b	0.25	0.30	0.35	
D		6		
E		6		
e		0.50		
D1		4.50		
E1		4.50		

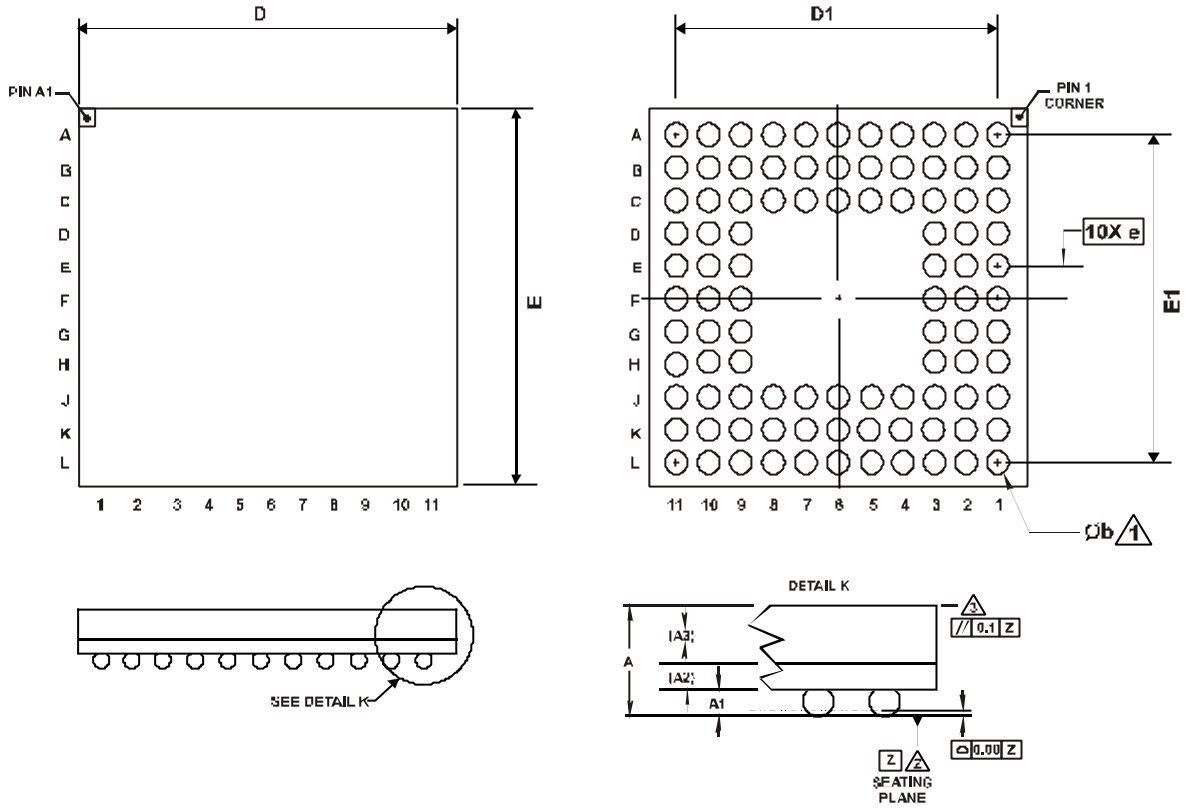
1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
2. DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

84-Ball VFBGA 6X6X1 mm (JEDEC MO-225)	UNIT
	MM

Figure 11.1: BlueCore2-Flash TFBGA Package Dimensions

11.2 10 x 10 LFBGA 96-Ball Package

Top View **Bottom View**



BC213159AXX-BN 10x10x1.4mm LFBGA				
DIM	MIN	TYP	MAX	NOTES
A	—		1.4	
A1	0.3		0.4	⚠1 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM PLANE Z.
A2		0.25		
A3		0.8		⚠2 DATUM Z IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
b	0.35		0.45	
D		10		⚠3 PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
E		10		
e		0.8		
D1		8		
E1		8		
LFBGA 96 BALLS 10X10X1.4mm (JEDEC MO-210)				UNIT: MM

Figure 11.2: BlueCore2-Flash LFBGA Package Dimensions

12 Ordering Information

12.1 BlueCore2-Flash

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	84-Ball TFBGA	6x6x1.2mm	Tape and reel	BC215159A-HK-E4
	84-Ball TFBGA (Pb free)	6x6x1.2mm	Tape and reel	BC215159A-TK-E4
	96-Ball LFBGA	10x10x1.4mm	Tape and reel	BC219159A-BN-E4

Minimum Order Quantity

2kpcs Taped and Reeled

13 Contact Information

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Fax: +82 31 389 0545
e-mail: sales@csr.com

To contact a CSR representative, go to www.csr.com/contacts.htm

14 Document References

Document References	Version
Specification of the Bluetooth system	v1.1, 22 February 2001
Universal Serial Bus Specification	v1.1, 23 September 1998
I2C EEPROMS for use with BlueCore	bcore-an-008Pa October 2002

15 Acronyms and Definitions

Term:	Definition:
BlueCore	Group term for CSR's range of Bluetooth chips.
Bluetooth	A set of technologies providing audio and data transfer over short-range radio connections
ACL	Asynchronous Connection-Less. A Bluetooth data packet.
AC	Alternating Current
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BGA	Ball Grid Array
BIST	Built-In Self-Test
BOM	Bill of Materials. Component part list and costing for a product
BMC	Burst Mode Controller
C/I	Carrier Over Interferer
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CPU	Central Processing Unit
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
FSK	Frequency Shift Keying
GCI	General Circuit Interface. Standard synchronous 2B+D ISDN timing interface
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HV	Header Value
IQ Modulation	In-Phase and Quadrature Modulation
IAC	Inquiry Access Code
IF	Intermediate Frequency
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksamples/s	kilosamples per second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LGA	Land Grid Array
LNA	Low Noise Amplifier
LSB	Least-Significant Bit
µ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface

PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation. Refers to digital voice data
PDA	Personal Digital Assistant
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
ROM	Read Only Memory
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SMS	Short Message Service
SOC	System On Chip
SPI	Serial Peripheral Interface
SPP	Serial Port Profile
SRAM	Static Random Access Memory
SS	Supplementary Services
SSI	Signal Strength Indication
SSL	Secure Sockets Layer
SUT	System Under Test
SW	Software
SWAP	Shared Wireless Access Protocol
TA	Terminal Adaptor
TAE	Terminal Adaptor Equipment
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)
www	world wide web

Status of Information

The progression of CSR Product Data Sheets follows the following format:

Advance Information

Information for designers on the target specification for a CSR product in development.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Final pinout and mechanical dimensions. All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

The status of this Data Sheet is **Advance Information.**

Life Support Policy and Use in Safety-Critical Applications

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16 Record of Changes

Date:	Revision:	Reason for Change:
JANUARY 2002	a	Latest information for BlueCore2-Flash
JANUARY 2003	b	Latest release of new package information

BlueCore™2-Flash Product Data Sheet

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