VGA to NTSC/PAL Encoder

Features

- Enhanced bandwidth and signal-to-noise ratio for higher video performance
- Integrated triple video rate 8-bit analog to digital converters for input RGB
- 3-line digital vertical filtering with pin-programmable characteristics for optimum anti-flicker and resolution
- On-chip phase-locked loop generates sampling clock from VGA horizontal sync
- Enhanced power management for selective circuit power-down
- Simultaneous composite/S-video output
- Horizontal and vertical position control
- Pin-programmable underscan/overscan mode
- On-chip reference generation and loop filter
- CMOS technology in 44-pin PLCC
- 5V supply

Description

Chrontel's CH7001C VGA to NTSC/PAL encoder is a stand-alone integrated circuit that converts analog VGA inputs directly into 525-line (M) NTSC or 625-line (B, D, G, H, I) PAL composite video and S-video outputs.

This circuit integrates a digital NTSC/PAL encoder with 8-bit ADC and DAC interfaces, a 3-line vertical filter and low-jitter phase-locked loop to create outstanding quality video with 24-bits-per-pixel processing throughout the entire signal path.

A high level of integration and performance makes the CH7001C ideal for a variety of stand-alone and system-level integration solutions, including notebook computers and PC add-on graphics cards.

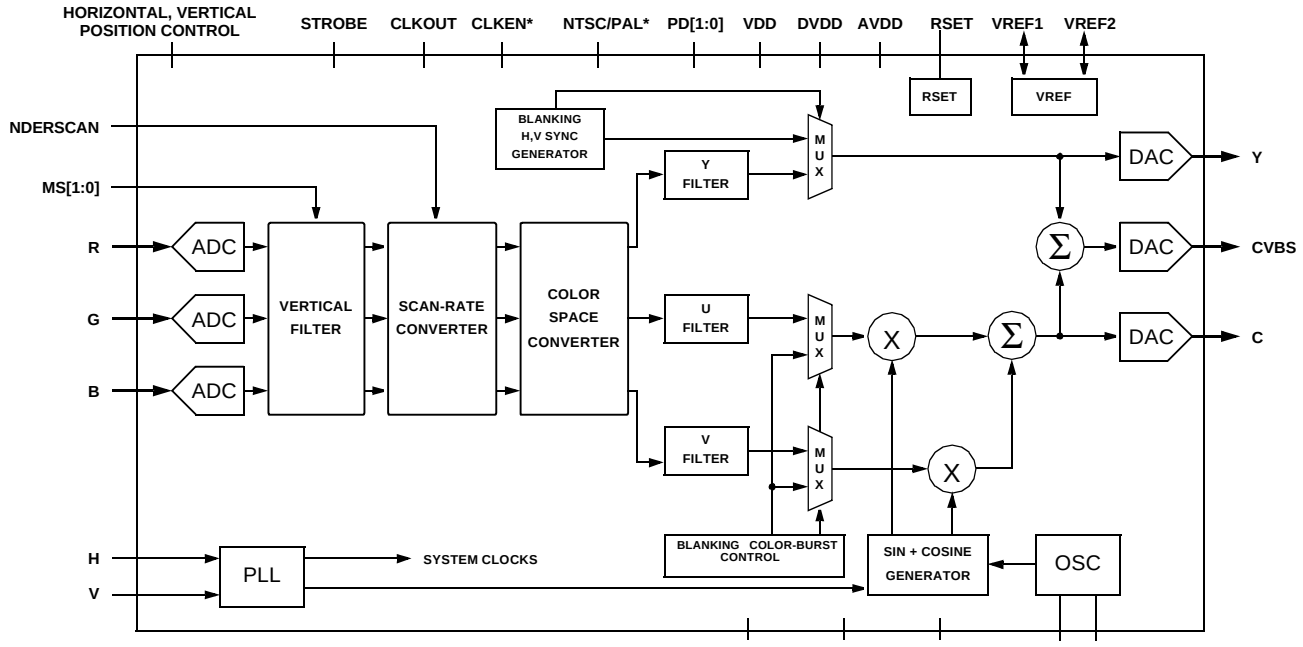


Figure 1: Functional Block Diagram

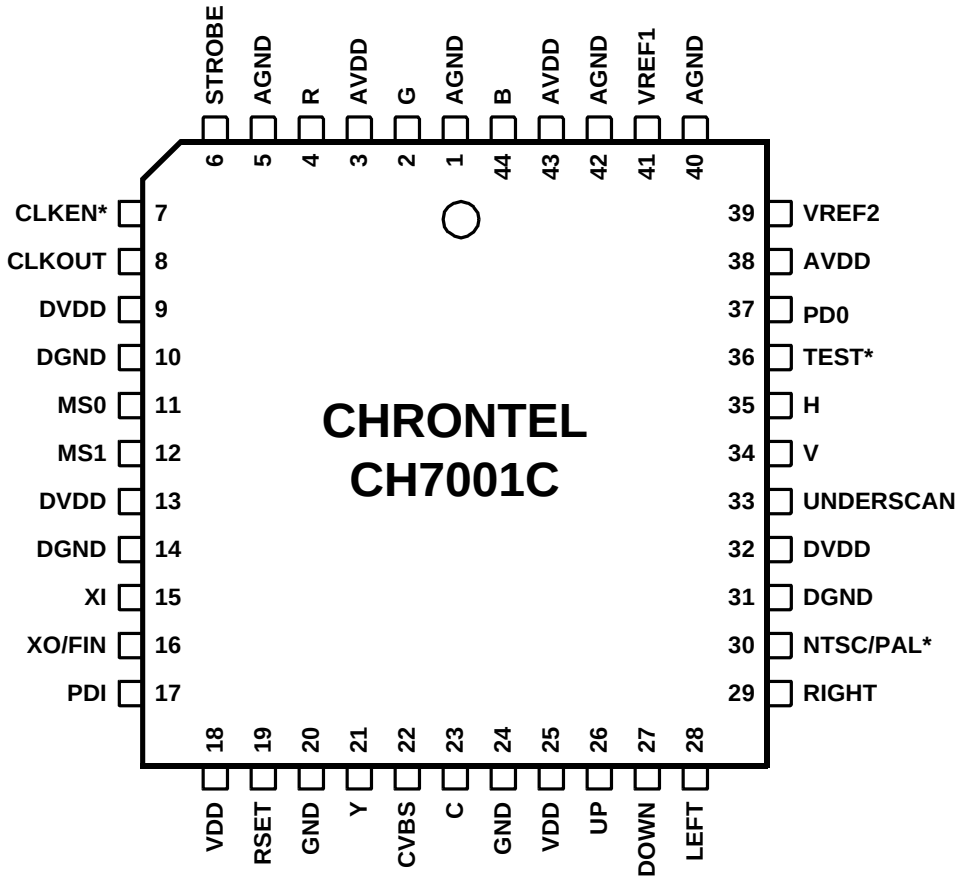


Figure 2: 44-pin PLCC

Table 1 • Pin Description

Pin	Type	Symbol	Description
1, 5, 40, 42	Power	AGND	**Analog ground** These pins provide the ground reference for the analog section of CH7001C, and MUST be connected to the system ground to prevent latchup. Please refer to **Application Note AN-11** for information on proper supply decoupling.
2, 4, 44	In	G, R, B	**VGA Inputs [1]** These pins should be terminated with 75Ω resistors and isolated from switching digital signals and video output pins.
3, 38, 43	Power	AVDD	**Analog Supply Voltage** These pins supply the 5V power to the analog section of the CH7001C. For information on proper supply decoupling, please refer to **Application Note AN-11**.
6	In	STROBE	**Strobe Input (active high, internal pull-up)** A logical HIGH input to this pin keeps chip mode pins (CLKEN*, UNDERSCAN, MS[1:0], UP, DOWN, LEFT, and RIGHT) active. These input signals are internally sampled on the high-to-low transition of the STROBE signal. This allows the chip state to be maintained while rendering these mode pins inactive.
7	In	CLKEN*	**Clock Enable (active low, internal pull-up)** A logical LOW input to this pin enables CLKOUT. CLKEN* should be hardwired to ground to enable CLKOUT. Otherwise, CLKEN* should be left unconnected or connected to VDD.
8	Out	CLKOUT	**Clock Output** This pin defaults to 14.31818 MHz upon power-up. Further toggling of the CLKEN* pin causes CLKOUT to output other internal test clocks. When disabled (i.e., CLKEN*=1), this output is a logic LOW. Setting the PD* pin low also causes CLKOUT to be logic LOW.
9, 13, 32	Power	DVDD	**Digital Supply Voltage** These pins supply the 5V power to the digital section of CH7001C. For information on proper supply decoupling, please refer to **Application Note AN-11**.
10, 14, 31	Power	DGND	**Digital Ground** These pins provide the ground reference for the digital section of CH7001C, and MUST be connected to the system ground to prevent latchup. For information on proper supply decoupling, please refer to **Application Note AN-11**.
11, 12	In	MS0, MS1	**Anti-flicker Mode Select Pins** These two pins are used to select one of four possible anti-flicker vertical filter modes.
15	In	XI	**Crystal Input [2]** A 14.31818 MHz parallel resonance (± 50 ppm) crystal should be attached between XI and XO/FIN. However, if an external CMOS clock is attached to XO/FIN, XI should be connected to ground.
16	In	XO/FIN	**Crystal Output or External FREF Input [2]** A 14.31818 MHz (± 50 ppm) crystal may be attached between XO/FIN and XI. An external CMOS compatible clock can be connected to XO/FIN as an alternative.

Note: **1** The **Typical Connection Diagram** (**Figure 4** on page 6) shows the VGA input configured for applications that do not require RGB buffering before the monitor. In this configuration, 75 Ω input termination must be guaranteed either by termination by the monitor connection, by discrete 75 Ω resistors on the PCB, or by a dummy 75 Ω termination connector. The total RGB trace on the PCB must be kept as short as possible to avoid cable reflection problems. For further information, request a copy of **Application Note AN-11, "PC Board Layout Considerations for CH7001C.** "

2 Please refer to crystal manufacturer specifications for proper load capacitances. The optional variable tuning capacitor is required only if the crystal oscillation frequency cannot be controlled to the required accuracy. The capacitance value for the tuning capacitor should be obtained from the crystal manufacturer. For further information, request a copy of **Application Note AN-19, "Tuning Clock Outputs.** "

Table 1 • Pin Description (continued)

Pin	Type	Symbol	Description
17, 37	In	PDI, PD0	**Power Down Inputs (active low, internal pull-up)** Asserting these signals place CH7001C into different power-down states. (Refer to section on Power Management). Note: Use of these pins is optional. Leaving these two pins floating will maintain normal operating mode.
18, 25	Power	VDD	**DAC Power Supply** These pins supply power to CH7001C's internal DACs. Please refer to **Application Note AN-11** for information on proper supply decoupling.
19	In	RSET	**Reference Resistor** A 330Ω resistor with short and wide traces should be attached between RSET and ground. No other connections should be made to this pin.
20, 24	Power	GND	**DAC Ground** These pins provide the ground reference for CH7001C's internal DACs. For information on proper supply decoupling, please refer to **Application Note AN-11**.
21	Out	Y	**Luminance Output** A 75Ω termination resistor with short traces should be attached between Y and ground for optimum performance. An optional low pass filter circuit, shown in **Figure 3** on page 5, may be used as an alternative to the ferrite bead shown in **Figure 4** on page 6.
22	Out	CVBS	**Composite Output** A 75Ω termination resistor with short traces should be attached between CVBS and ground for optimum performance. An optional low pass filter circuit shown in **Figure 3** on page 5, may be used as an alternative to the ferrite bead shown in **Figure 4** on page 6.
23	Out	C	**Chrominance Output** A 75Ω termination resistor with short traces should be attached between C and ground for optimum performance. An optional low pass filter circuit shown in **Figure 3** on page 5, may be used as an alternative to the ferrite bead shown on **Figure 4** on page 6.
26	In	UP	**Up Position Control (active low, internal pull-up)** UP allows the screen display position to be moved up incrementally for every toggle of this pin to ground. An internal schmitt trigger minimizes switch bounce problems. UP may be connected directly to the power supply or ground.
27	In	DOWN	**Down Position Control (active low, internal pull-up)** DOWN allows the screen display position to be moved down incrementally for every toggle of this pin to ground. An internal schmitt trigger minimizes switch bounce problems. DOWN may be connected directly to the power supply or ground.
28	In	LEFT	**Left Position Control (active low, internal pull-up)** LEFT allows the screen display position to be moved to the left incrementally for every toggle of this pin to ground. An internal schmitt trigger minimizes switch bounce problems. LEFT may be connected directly to the power supply or ground.
29	In	RIGHT	**Right Position Control (active low, internal pull-up)** RIGHT allows the screen display position to be moved to the right incrementally for every toggle of this pin to ground. An internal schmitt trigger minimizes switch bounce problems. RIGHT may be connected directly to the power supply or ground.
30	In	NTSC / PAL*	**NTSC/PAL Mode Select Input (internal pull-up)** A logical HIGH input NTSC/PAL* pin selects NTSC operation. A logical LOW input to NTSC/PAL* selects PAL operation. NTSC/PAL* accepts CMOS logic level inputs and may be connected directly to the power supply or ground.

Table 1 • Pin Description (continued)

Pin	Type	Symbol	Description
33	In	UNDERSCAN	**Underscan Enable Pin (active high, internal pull-up)** A logical HIGH input to UNDERSCAN results to an output screen that has approximately 12.5% horizontal underscan. This pin may be connected directly to the power supply or ground.
34	In	V	**Vertical Sync Input** This pin accepts the vertical sync output from the VGA card. The capacitive loading on this pin should kept to a minimum.
35	In	H	**Horizontal Sync Input** This pin accepts the horizontal sync output from the VGA card. The capacitive loading on this pin should kept to a minimum. Please refer to **Application Note 11 "PC Board Layout Considerations for CH7001C.**"
36	—	TEST*	**Test Pin (active low, internal pull-up)** Connect a capacitor in the range of 2.2uF - 4.7uF from this pin to GND to ensure proper functionality of the UNDERSCAN/ OVERSCAN feature.
39	In	VREF2	**Internal Voltage Reference** VREF2 provides a typical 2.5V reference that is used as an internal bias to the ADCs. A 0.1 µF decoupling capacitor should be connected between VREF2 and ground.
41	In	VREF1	**ADC Voltage Reference Input / Output** VREF1 provides a typical 1.235V reference that sets the RGB input full scale at 0.75V. A 0.1 µF decoupling capacitor should be connected between VREF1 and ground. VREF1 may also be forced by external reference.

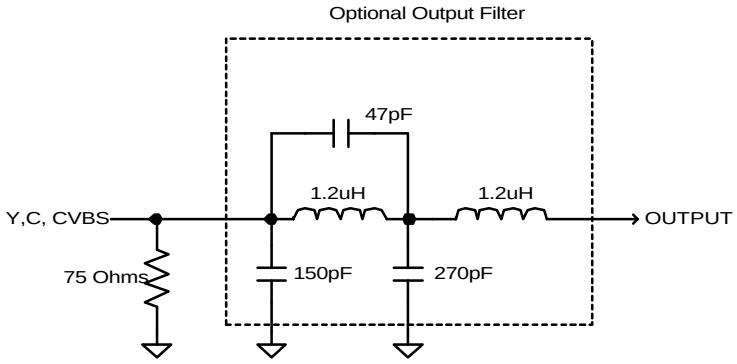


Figure 3: Optional Output Filter

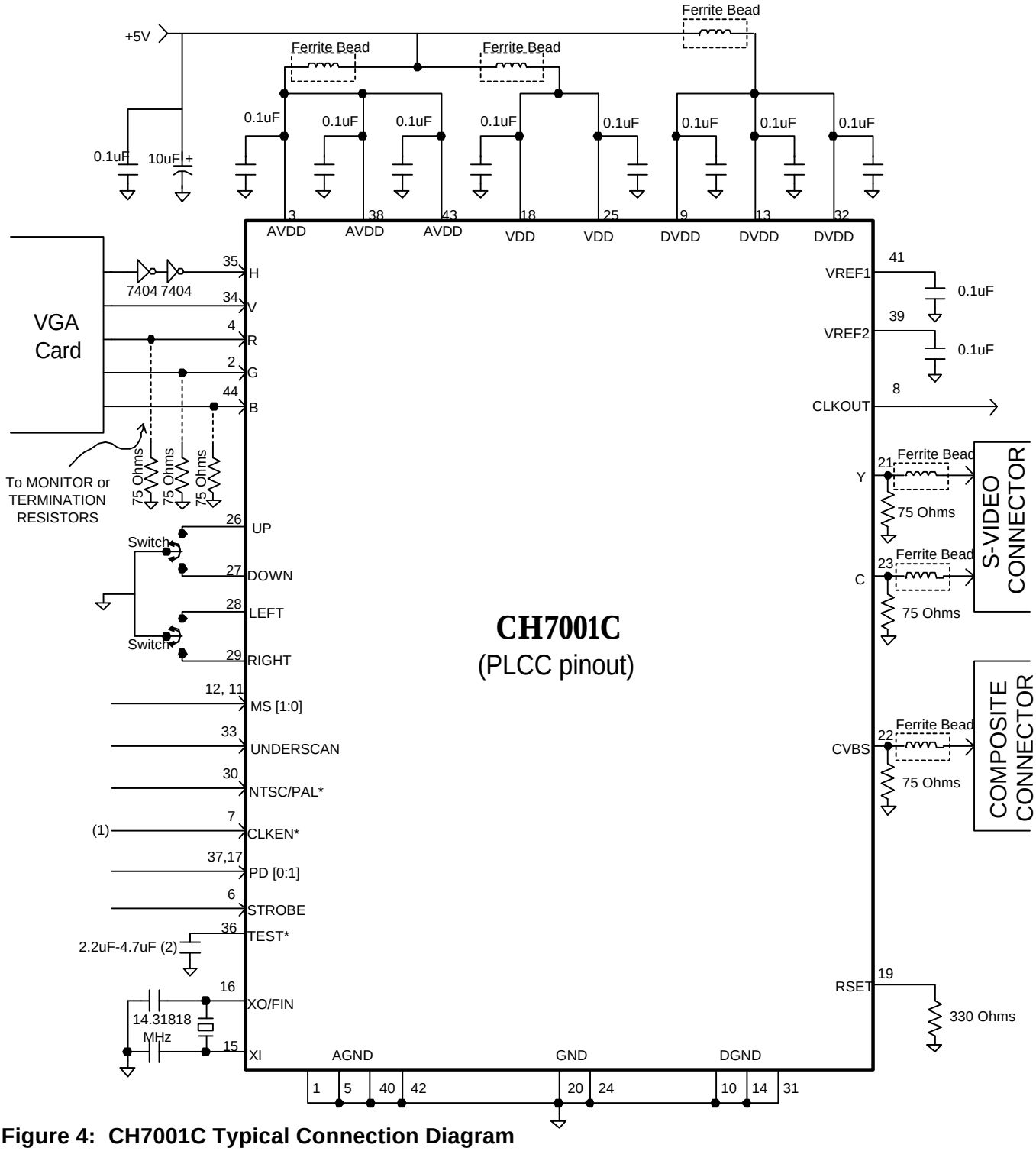


Figure 4: CH7001C Typical Connection Diagram

Note: 1 If the CLKOUT signal is not used, either connect CLKEN* to VDD, or leave it unconnected.

Note: 2 An external pull-up resistor should not be connected to the TEST* pin.

General Description

The CH7001C is a fully integrated solution for converting analog RGB and synchronization signals from a standard VGA source into high-quality NTSC or PAL video signals. All essential circuitry for this conversion (memory, memory control, PLL, ADC, DAC, digital filters, digital NTSC/PAL encoder) are present in this IC. All internal signal processing, including NTSC/PAL encoding, is performed using digital techniques to ensure that the high-quality video signals are not affected by drift issues associated with analog components. No additional adjustment is required during manufacturing.

CH7001C is ideal for stand-alone VGA to NTSC/PAL applications, where a minimum of discrete support components (passive components, 14.31818 MHz crystal) are required for full operation. The CH7001C easily integrates into notebook computers and PC add-on graphics cards.

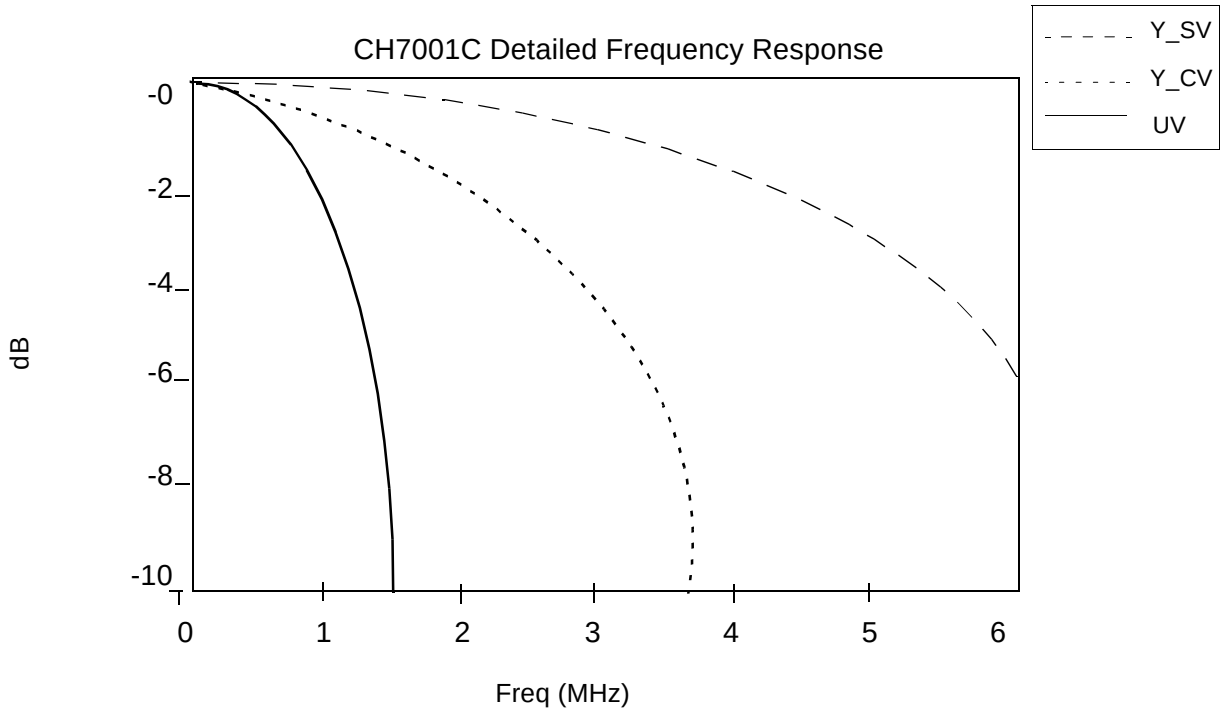
Functional Description

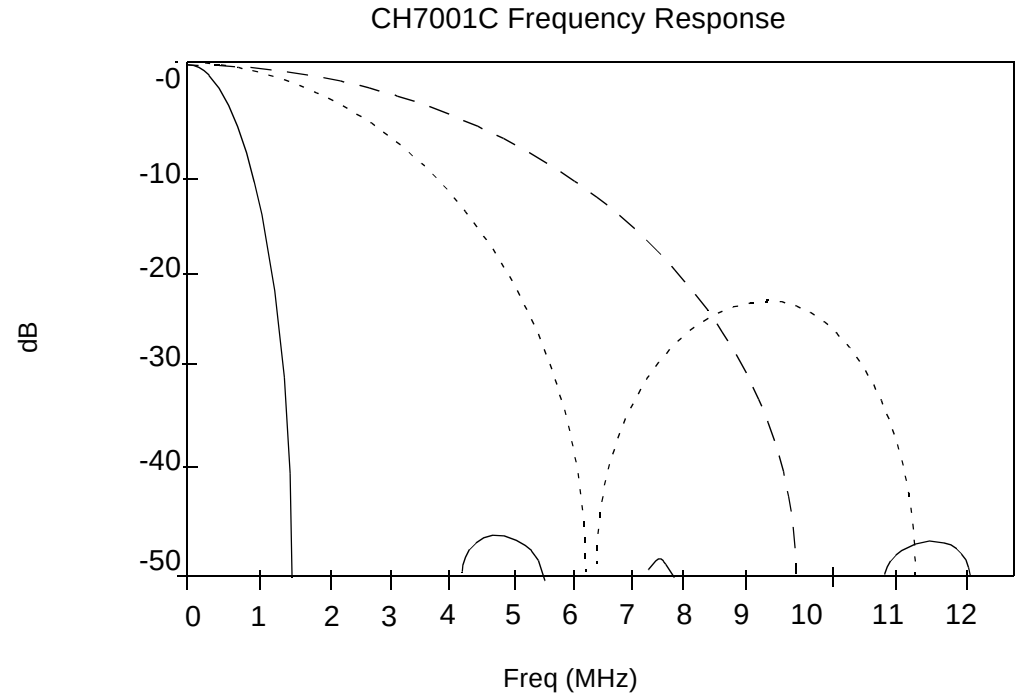
The analog RGB inputs are digitized on a pixel-by-pixel basis by three 8-bit video A/D converters. The digitized RGB inputs are fed to a block where scan-rate conversion and programmable 3-line vertical filtering are performed. The vertical filter eliminates flicker at the output, while the scan-rate converter transforms the VGA horizontal scan-rate to either NTSC or PAL scan-rates.

The digitized RGB inputs are encoded into luminance (Y) and color-difference (U,V) signals through the color space converter. The resulting YUV signals are filtered through digital filters to minimize aliasing problems (the frequency response is shown in **Figure 5** on page 8). The digital encoder receives the filtered signals and transforms them to composite and S-video outputs, which are converted by the three 8-bit DACs into analog outputs. High-quality video is ensured by using 24 bits per pixel processing throughout the entire signal path.

General Description (continued)

Figure 5: U,V, and Y Filter Response



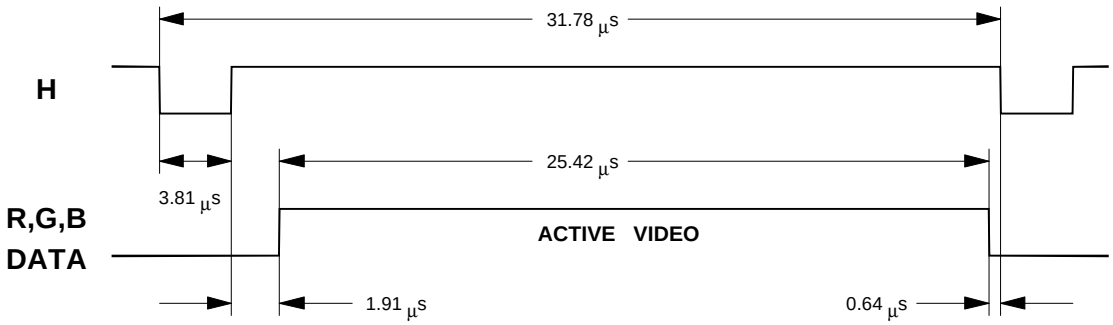


General Description (continued)

Clock Generation and Video Timing

All clock signals of the CH7001C are generated from the VGA synchronization inputs by a low-jitter, PLL circuit. The VGA input and sync timing are illustrated in **Figures 6** and **7** below. The VGA pixel clock is generated internally, using the VGA horizontal sync signal, and is used for sampling the RGB inputs pixel-by-pixel, which aids in preventing aliasing artifacts.

All synchronization and color burst envelope pulses are internally generated using only the timing signals provided by the VGA synchronization inputs.



Note: The timing diagram shown is for 640 x 480, 60 Hz VGA mode

Figure 6: Typical VGA Input Timing

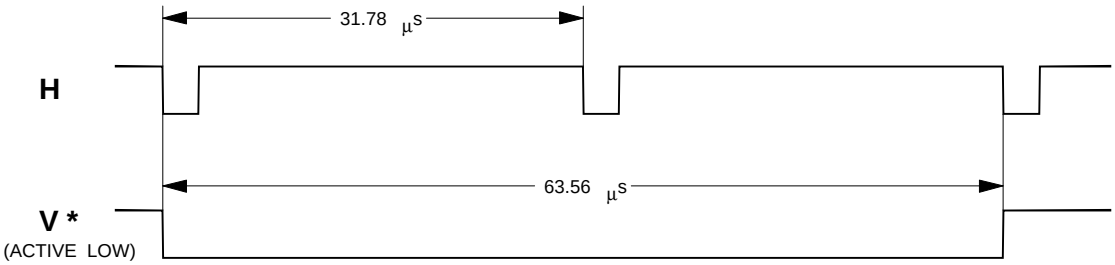


Figure 7: VGA Horizontal and Vertical Sync Timing

Internal Voltage Reference

The on-chip generated ADC voltage references are brought out to pins VREF1 and VREF2 for decoupling purposes. VREF1 and VREF2 should each have a 0.1 µF decoupling capacitor between each pin and ground. VREF2 provides a typical 2.5V reference, used for setting the internal bias to the ADCs, and VREF1 provides a typical 1.235V reference, used for setting the RGB input full scale at 0.75V. VREF1 can be forced by an external voltage reference in order to accommodate different RGB input ranges. An additional on-chip bandgap circuit is used in the DAC to generate a reference voltage which, in conjunction with a reference resistor at pin RSET, sets the output ranges of the DACs.

General Description (continued)

Strobing

The CH7001C programmable pins (MS[1:0], UNDERSCAN, NTSC/PAL*, LEFT, RIGHT, UP, and DOWN) may be connected to shared signal lines and then strobed in using the STROBE pin. By asserting the STROBE pin high, the state of the programmable pins is internally sampled during the STROBE signal's high-to-low transition. A logical low input to the STROBE pin allows the chip state to be maintained, while rendering the programmable pins inactive.

Power Management

The CH7001C supports four operating states including Normal (On), Power Down, S-Video Off, and Composite Off) in order to provide optimal power consumption for the application involved. Using pins PD0 and PD1, the CH7001C ay be placed in either Normal state or any of the three power managed states as listed below:

PD1	PD0	Operating State	Functional Description
1	1	Normal (On)	All functions and pins are active (default state with inputs floating.)
0	1	Power Down	Most pins and cicruitry are disabled. This reduces power to only 1% of normal operating power.
1	0	S-Video Off	Power is shut off to the unused DACs associated with Y and C outputs. This reduces power to 81% of normal operating power.
0	0	Composite Off	Power is shut off to the unused DAC associated with CVBS output. This reduces power to 89% of normal operating power.

Color Burst Accuracy*

The CH7001C employs a proprietary technique for generating the color sub-carrier frequency. This method allows the sub-carrier frequency to be accurately generated from a 14.31818 MHz crystal oscillator, leaving the accuracy of the sub-carrier frequency independent of the sampling rate. As a result, the CH7001C is compatible with any VGA card, since the CH7001C sub-carrier frequency is not dependent on the pixel rates of VGA card manufacturers. This feature is a significant benefit, since even a ± 0.01% sub-carrier frequency variation may be enough to cause some television monitors to lose color lock.

Programmability

All operational modes of the CH7001C are accessed directly through the package pins, making the CH7001C programmable without the use of an additional microcontroller. Some of the programmable features are: horizontal overscan/underscan control, NTSC or PAL operation, selectable anti-flicker filter modes, and adjustable horizontal and vertical display positioning capabilities.

Horizontal Overscan/Underscan

Horizontal underscan mode is enabled via the UNDERSCAN pin. By setting this pin high, the resulting output screen experiences a 12.5% horizontal underscan.

The CH7001C also implements an overscan/underscan mode that is controllable through the PC. Software control is available only when the underscan input is inactive (i.e., UNDERSCAN = 0) and is accomplished by programming the length (in VGA line periods) of the vertical sync pulse.

When the CH7001C detects the vertical sync pulse as having fewer than eight VGA line periods, the device operates in overscan mode; when it detects the vertical sync pulse as having more than eight VGA line periods, it operates in underscan mode. The CH7001C determines the number of VGA line periods through an internal circuitry that continuously analyzes the width of the VGA vertical sync input.

Software control is overridden if the underscan input is set high.

NTSC or PAL Operation

Composite and S-video outputs are supported in either NTSC or PAL format, as shown in **Figures 8** through **10**. These outputs can be conveniently switched to either format via the NTSC/PAL* pin. If the NTSC/PAL* pin is set low, PAL output format is selected. If the NTSC/PAL* is set high, NTSC output format is selected. See **Figures 11** through **16** on pages 14 through 16 for illustrations of the composite and S-video output waveforms.

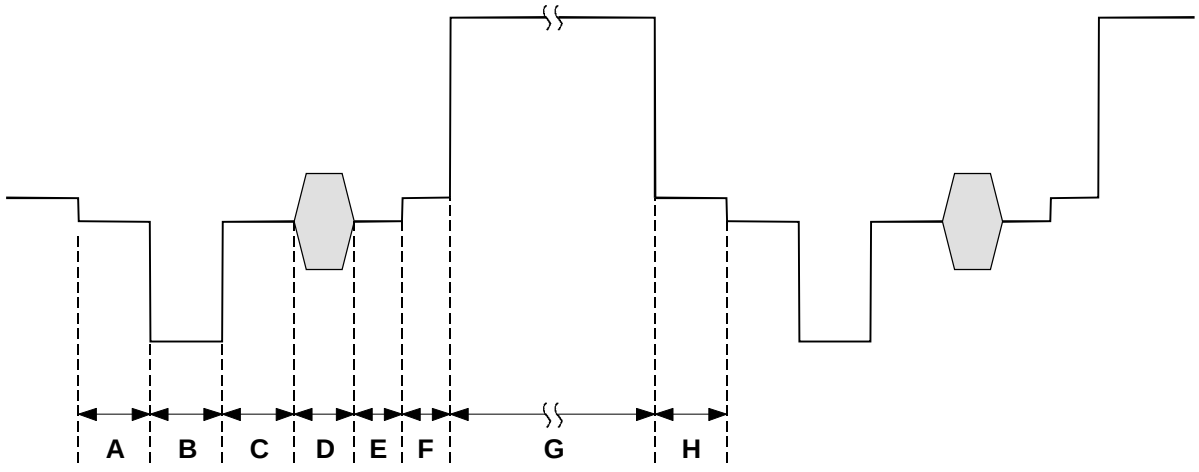


Figure 8: NTSC / PAL Composite Output

General Description (continued)

Table 2 • NTSC/PAL Composite Output Timing Parameters (in μS)

Symbol	Description	NTSC		PAL	
		OVERSCAN	UNDERSCAN	OVERSCAN	UNDERSCAN
A	Front Porch	1.35	1.20	1.35	1.20
B	Horizontal Sync	4.69	4.70	4.69	4.70
C	Breezeway	0.64	0.57	0.56	0.49
D	Color Burst	2.66	2.37	2.39	2.12
E	Back Porch	1.47	1.31	1.83	1.63
F	Black	2.38	5.10	2.37	5.11
G	Active Video	50.51	45.19	50.51	45.19
H	Black	0.00	3.12	0.00	3.12

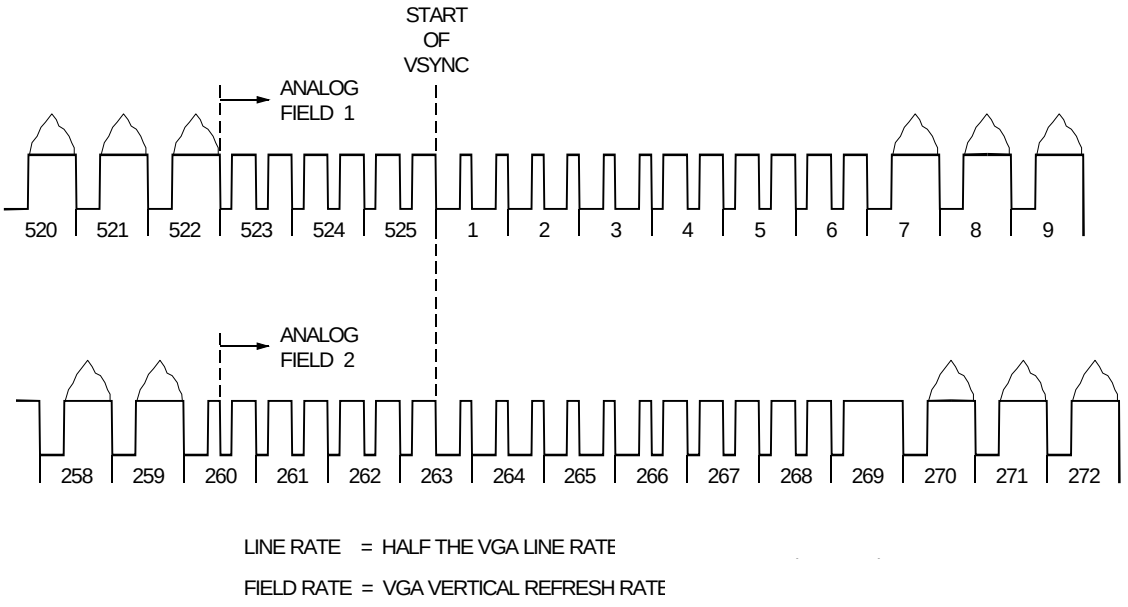


Figure 9: Interlaced NTSC Video Timing

General Description (continued)

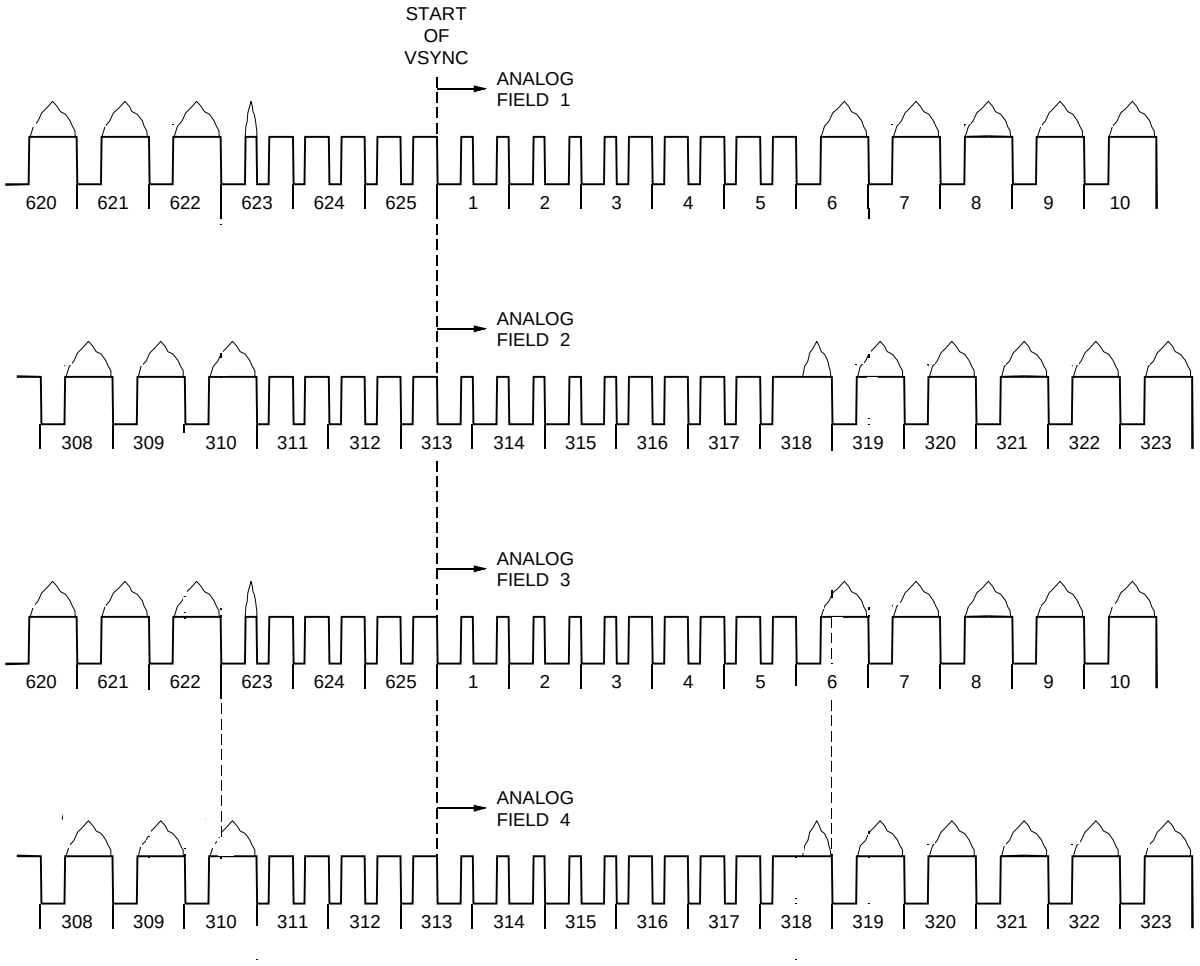
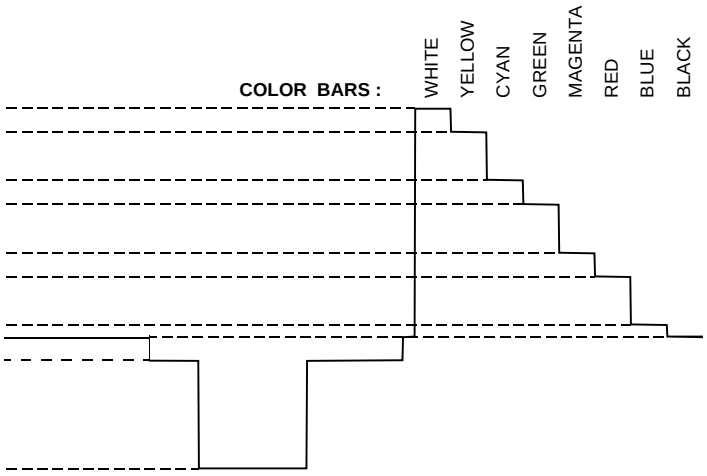


Figure 10: Interlaced PAL Video Timing

Color / Level	mA	V
White	27.48	1.030
Yellow	25.41	0.953
Cyan	22.08	0.828
Green	20.01	0.750
Magenta	16.99	0.637
Red	14.93	0.560
Blue	11.59	0.435
Black	9.69	0.363
Blank	8.26	0.310
Sync	0.640	0.024

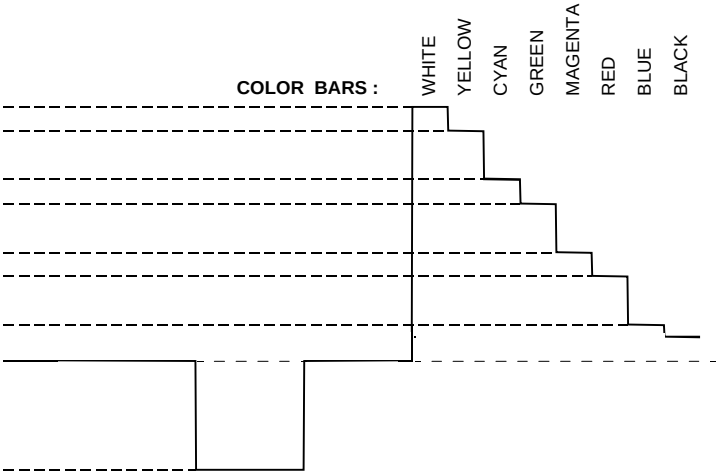


Note: 100% amplitude, 100% saturation color bars are shown

Note: VREF1 = 1.235V, RSET = 330Ω, 75Ω doubly terminated load.

Figure 11: NTSC Y (Luminance) Output Waveform

Color / Level	mA	V
White	26.05	0.977
Yellow	24.00	0.900
Cyan	20.67	0.775
Green	18.59	0.697
Magenta	15.57	0.584
Red	13.52	0.507
Blue	10.19	0.382
Blank	8.26	0.310
Sync	0.640	0.024

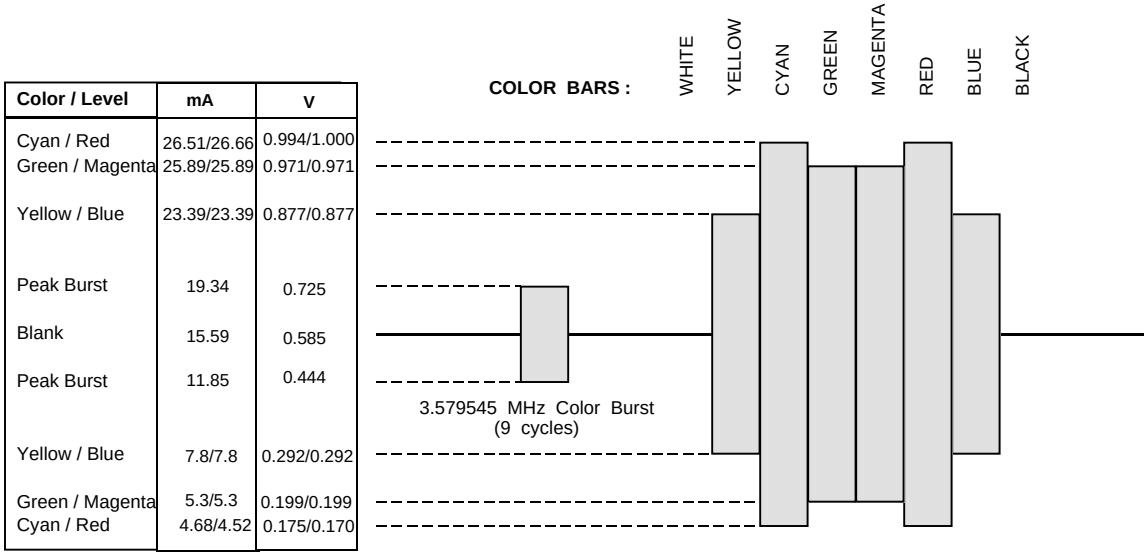


Note: 100% amplitude, 100% saturation color bars are shown

Note: VREF1 = 1.235V, RSET = 330Ω, 75Ω doubly terminated load.

Figure 12: PAL Y (Luminance) Video Output Waveform

General Description (continued)

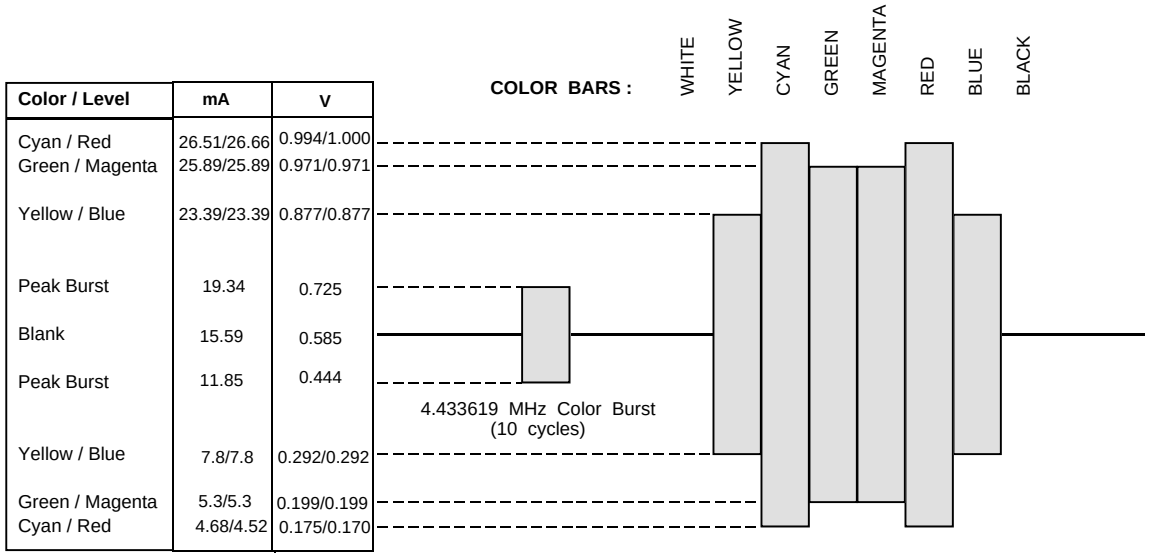


Color / Level	mA	V
Cyan / Red	26.51/26.66	0.994/1.000
Green / Magenta	25.89/25.89	0.971/0.971
Yellow / Blue	23.39/23.39	0.877/0.877
Peak Burst	19.34	0.725
Blank	15.59	0.585
Peak Burst	11.85	0.444
Yellow / Blue	7.8/7.8	0.292/0.292
Green / Magenta	5.3/5.3	0.199/0.199
Cyan / Red	4.68/4.52	0.175/0.170

Note: 1 100% amplitude, 100% saturation color bars are shown

Note: 2 VREF1 = 1.235V, RSET = 330Ω, 75Ω doubly terminated load.

Figure 13: NTSC C (Chrominance) Video Output Waveform



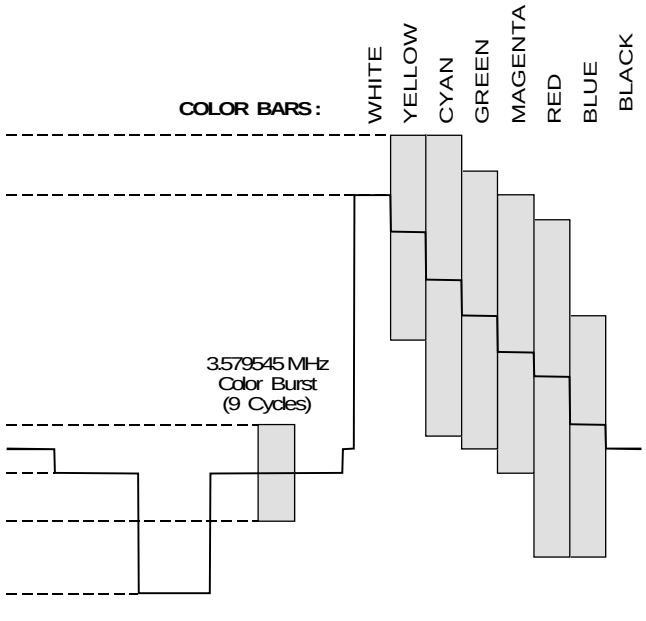
Color / Level	mA	V
Cyan / Red	26.51/26.66	0.994/1.000
Green / Magenta	25.89/25.89	0.971/0.971
Yellow / Blue	23.39/23.39	0.877/0.877
Peak Burst	19.34	0.725
Blank	15.59	0.585
Peak Burst	11.85	0.444
Yellow / Blue	7.8/7.8	0.292/0.292
Green / Magenta	5.3/5.3	0.199/0.199
Cyan / Red	4.68/4.52	0.175/0.170

Note: 1 100% amplitude, 100% saturation color bars are shown

Figure 14: PAL C (Chrominance) Video Output Waveform

General Description (continued)

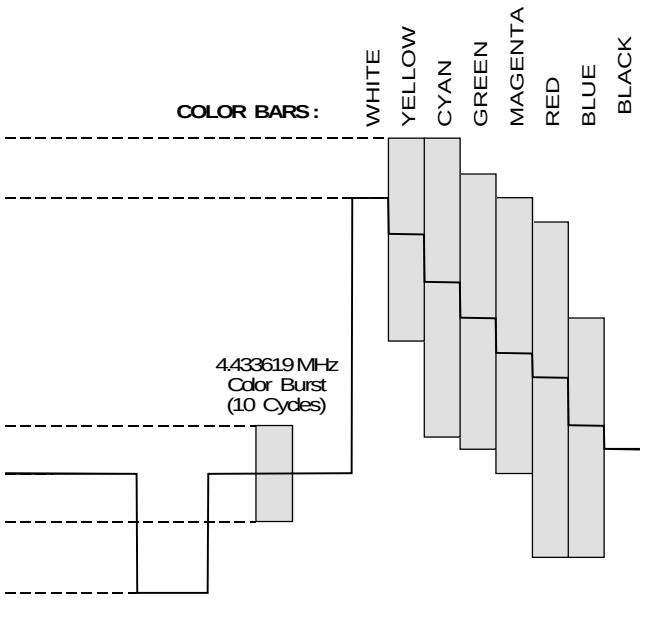
Color / Level	mA	V
Peak Chroma	33.23	1.246
White	27.47	1.030
Peak Burst	12.03	0.451
Black	9.68	0.363
Blank	8.27	0.310
Peak Burst	4.53	0.170
Sync	0.640	0.024



Note: VREF1=1.235V, RSET=330Ω, 75Ω, doubly terminated load.

Figure 15: Composite NTSC Video Output Waveform

Color / Level	mA	V
Peak Chroma	31.81	1.193
White	26.05	0.977
Peak Burst	12.03	0.451
Blank/Black	8.26	0.310
Peak Burst	4.53	0.170
Sync	0.643	0.024



Note: VREF1=1.235V, RSET=330W, 75W, doubly terminated load.

Figure 16: Composite PAL Video Output Waveform

General Description (continued)

Anti-Flicker Filter Modes

The CH7001C integrates a 3-line vertical filter circuitry to help eliminate the flicker associated with interlaced displays. The CH7001C provides four anti-flicker filter modes programmable via the anti-flicker mode select pins MS[1:0]. For a list of the filter modes available, please refer to **Table 3** below.

Table 3 • Anti-Flicker Filter Modes

MS1	MS0	Filter Modes
0	0	0:1:0 averaging
0	1	1:3:1 averaging
1	0	1:2:1 averaging
1	1	1:1:1 averaging

Programmability

Display Position Control

UP, DOWN, LEFT, and RIGHT are dedicated inut pins controlling the NTSC or PAL display position. Upon power up, the internal position registers for a typical VGA input center the display on the television screen. With each toggle of any position pin to ground, the display will shift four pixels in the respective direction. For example, if the LEFT pin is toggled to ground once, the screen display will move four pixels to the left. Similarly, if the RIGHT pin is toggled to ground once, the screen display will move four pixels to the right. The shift of the display occurs during the low-to-high transition of the position pin. Toggling conflicting pins, such as the LEFT and RIGHT pins for example, simultaneously is not allowed. The minimum time required for the display position pins to be held low is 40 ns.Electrical Specifications

Table 4 • Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD relative to GND	- 0.5		7.0	V
	Input voltage of all digital pins[1]	GND - 0.5		V_{DD} + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	- 55		125	° C
T_{STOR}	Storage temperature	- 65		150	° C
T_J	Junction temperature			150	° C
T_{VPS}	Vapor phase soldering (one minute)			220	° C
P_{MAX}	Maximum Power dissipation			TBD	W

Note: 1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of device at these or any other conditions above those indicated under the normal operating conditions section of this specification is not recommended, Exposure to absolute maximum rating conditions for extended periods may affect relaibility.

The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

Table 5 • Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	DAC power supply voltage	4.75	5.00	5.25	V
AVDD	Analog supply voltage		5.00		
DVDD	Digital supply voltage		5.00		
T_A	Ambient operating temperature	0	25	70	° C
R_L	Output load to DAC outputs		37.5		Ω
VREF1	ADC voltage reference input/output	1.20	1.235	1.32	V
VREF2	Internal voltage reference		2.5		V

Table 6 • Electrical Characteristics (Operating Conditions: T_A = 0– 70° C, V_{DD} = 5V ± 5%)

Symbol	Description	Min	Typ	Max	Unit
	Video D/A resolution	8	8	8	Bits
	Full scale output current		33.89		mA
	Video level error using external reference using internal reference			 5 10	 % %
IREF1	VREF1 input current (VREF1 = 1.235V)		10		µA
	Total Current Consumption (both S-video & composite outputs are On)		340		mA

Note: As applied to Tables 4, 5, and 6, Recommended Operating Conditions are used as test conditions unless otherwise specified.

Table 7 • Digital Inputs / Outputs

Symbol	Description	Test Condition @ T_A = 25	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = - 400 µA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.2 mA			0.4	V
V_{IH}	Input high voltage		2.0		V_{DD} + 0.5	V
V_{IL}	Input low voltage		GND - 0.5		0.8	V
I_{PU}	Input internal pull-up current		5		25	µA
I_{LK}	Input leakage current		-10		10	µA
CD_{IN}	Input capacitance	f = 1 MHz, V_{IN} = 2.4V		7		pF
CD_{OUT}	Output capacitance			10		pF

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7001C-V	PLCC	44	5V