

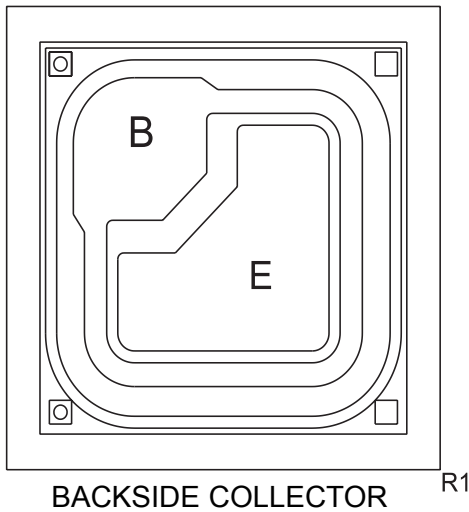
**PROCESS CP188**  
**Small Signal Transistor**  
NPN - Low Noise Amplifier Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



**GROSS DIE PER 4 INCH WAFER**

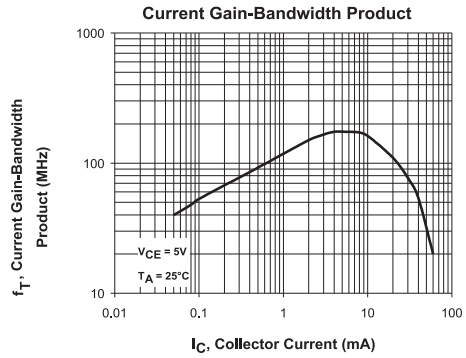
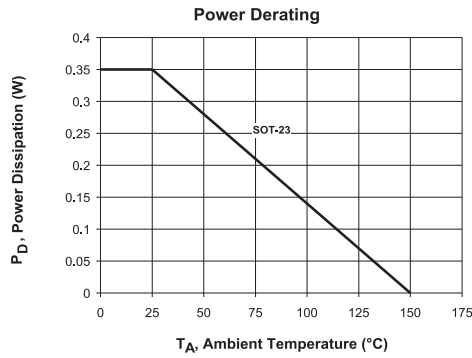
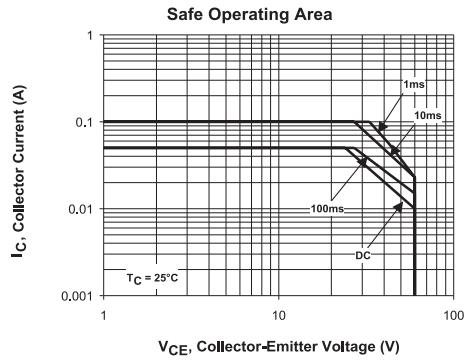
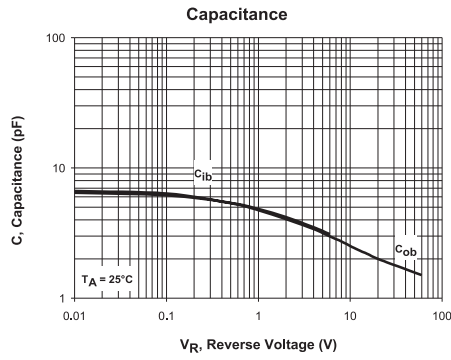
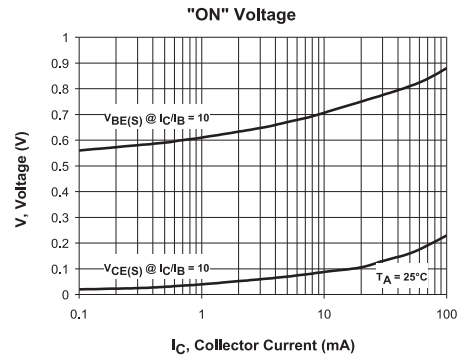
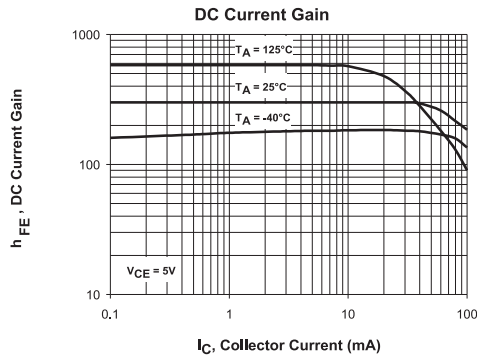
53,730

**PRINCIPAL DEVICE TYPES**

CMPT2484  
CMPT5088  
CMPT5089  
CMPT6428  
CMPT6429  
2N2484

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