PROCESS CP117

Power Transistor

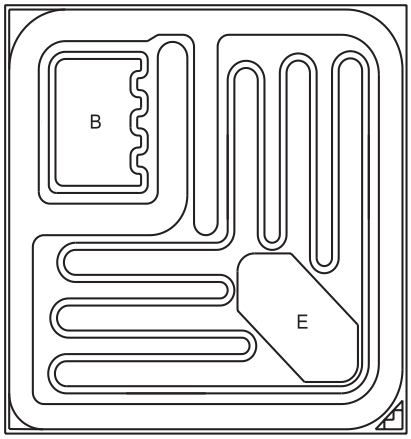
NPN - Darlington Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL BASE
Die Size	111 X 111 MILS
Die Thickness	10 MILS
Base Bonding Pad Area	20 X 30 MILS
Emitter Bonding Pad Area	20 X 26 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au/Cr/Ni/Au - Ni-6,000Å, Au-6,000Å

GEOMETRY



BACKSIDE COLLECTOR

R1

GROSS DIE PER 5 INCH WAFER

910

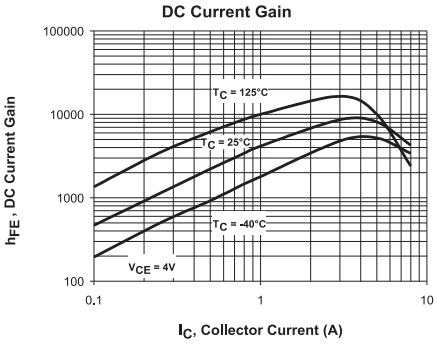
PRINCIPAL DEVICE TYPES

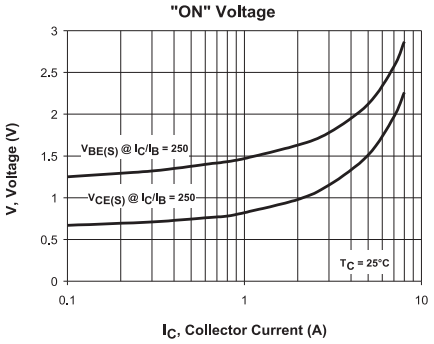
2N6043
2N6044
2N6045
2N6301

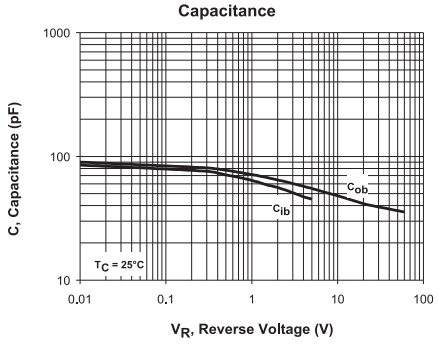
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

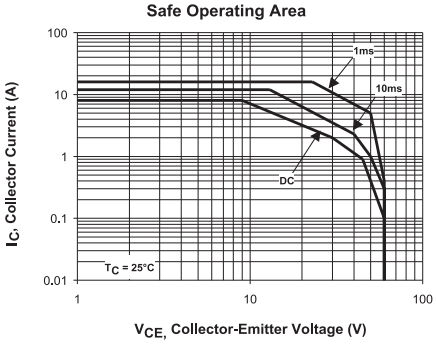
R6 (1 -August 2002)

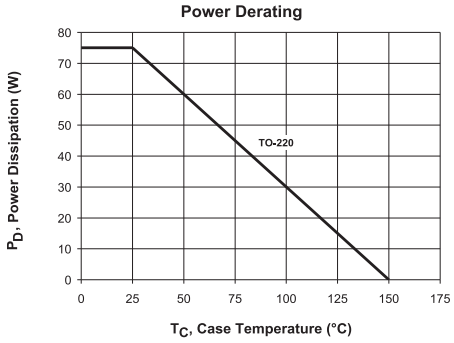
Typical Electrical Characteristics

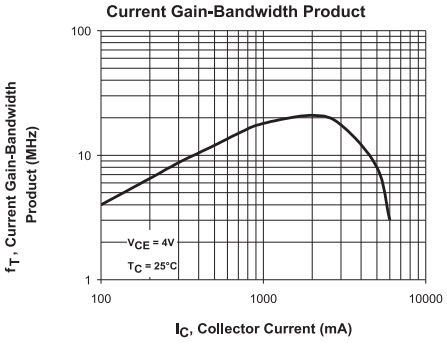












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