5V and 3.3V Supply Voltage Monitor and Reset Circuit

FEATURES

- **Selectable reset voltage tolerance**
  - **— CAT1232LP for 5V supply**
  - **— CAT1832 for 3.3V supply**
- **Selectable watchdog period: 150ms, 600ms or 1.2 sec**
- **Two reset outputs**
  - **— Active high, push-pull reset output**
  - **— Active low, open-drain reset output (CAT1232LP)**
  - **— Active low, push-pull reset output (CAT1832)**
- **Debounced manual push-button reset**
- **Compact SOIC and MSOP packages**

APPLICATIONS

- **Microprocessor Systems**
- **Portable Equipment**
- **Controllers**
- **Single Board Computers**
- **Instrumentations**
- **Telecommunications**

DESCRIPTION

The CAT1232LP and CAT1832 microprocessor supervisors can halt and restart a “hung-up” or “stalled” microprocessor, restart a microprocessor after a power failure, and debounce a manual/push-button microprocessor reset switch. The devices are drop in replacements for the Maxim/Dallas Semiconductor DS1232LP and DS1832 supervisors

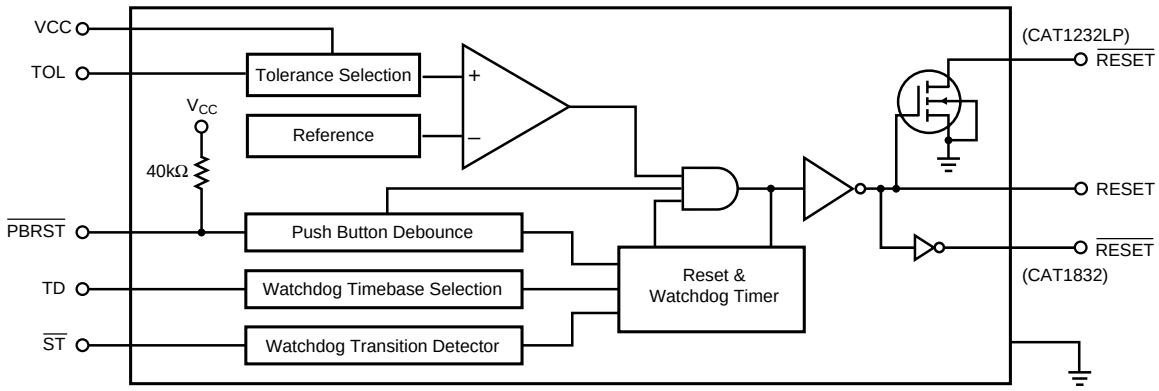
Precision reference and comparator circuits monitor the 5V or 3.3V system power supply voltage, V_{CC}. During power-up or when the power supply falls outside selectable tolerance limits, both the RESET and $\overline{\text{RESET}}$ become active. After the power supply voltage rises above the RESET threshold voltage, the reset signals remain active for a minimum of 250ms, allowing the power supply and system processor to stabilize. The trip-point tolerance input, TOL, selects the trip level tolerance to be either 5% or 10% for the CAT1232LP 5V supply and 10% or 20% for the CAT1832 3.3V supply.

Each device has a push-pull, active HIGH reset output. The CAT1232LP also has an open drain, active LOW reset output while the CAT1832 also has a push-pull, active LOW reset output.

A debounced manual reset input activates the reset outputs and holds them active for a minimum period of 250ms after being released.

Also included is a watchdog timer to reset a microprocessor that has stopped due to a software or hardware failure. Three watchdog time-out periods are selectable: 150ms, 600ms and 1.2sec. If the $\overline{\text{ST}}$ input is not strobed low before the watchdog time out period expires, the reset signals become active for a minimum of 250ms.

FUNCTIONAL DIAGRAM

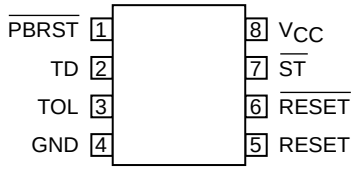


ORDERING INFORMATION

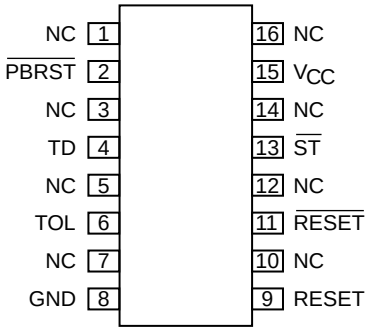
Solder Plate Lead Finish	Green Sn Lead Finish	Green NiPdAu Lead Finish				
Ordering Part Number	**Ordering Part Number**	**Ordering Part Number**	**Package**	**Parts per Tube**	**Parts Per Reel**	**Reel Size (inch)**
CAT1232LP	CAT1232LPL	CAT1232LPGL	8-lead, DIP	50	—	—
CAT1232LPS	CAT1232LPW	CAT1232LPGW	16-lead, SOIC	47	—	—
CAT1232LPS-2	CAT1232LPV	CAT1232LPGV	8-lead, SOIC	100	—	—
CAT1232LPU	CAT1232LPZ	CAT1232LPGZ	MSOP	100	—	—
CAT1232LPS-T13	CAT1232LPW-T13	CAT1232LPGW-T13	16-lead, SOIC	—	2,000	13
CAT1232LPS-2T13	CAT1232LPV-T13	CAT1232LPGV-T13	8-lead, SOIC	—	2,000	13
CAT1232LPU-T13	CAT1232LPZ-T13	CAT1232LPGZ-T13	MSOP	—	2,500	13
CAT1832	CAT1832L	CAT1832GL	8-lead, DIP	50	—	—
CAT1832S	CAT1832V	CAT1832GW	8-lead, SOIC	100	—	—
CAT1832U	CAT1832Z	CAT1832GZ	MSOP	100	—	—
CAT1832S-T13	CAT1832V-T13	CAT1832GW-T13	8-lead, SOIC	—	2,000	13
CAT1832U-T13	CAT1832Z-T13	CAT1832GZ-T13	MSOP	—	2,500	13

PIN CONFIGURATION

8-Lead SOIC/MSOP/DIP



16-Lead SOIC



PIN DESCRIPTION

Pin Number 8-Lead Package	Pin Number 16-Lead Package	Name	Function
1	2	$\overline{\text{PBRST}}$	Debounced manual pushbutton reset input
2	4	TD	Watchdog typical time delay selection: a) t_{TD} = 150ms for TD = GND b) t_{TD} = 600ms for TD = Open c) t_{TD} = 1200ms for TD = V_{CC}
3	6	TOL	CAT1232LP TOL selects 5% (TOL = GND) or 10% (TOL = V_{CC}) trip point tolerance. CAT1832 TOL selects 10% (TOL = GND) or 20% TOL = V_{CC}) trip point tolerance.
4	8	GND	Ground
5	9	RESET	Active HIGH reset output. RESET is active 1. If V_{CC} falls below the reset voltage trip point 2. If $\overline{\text{PBRST}}$ is low 3. If $\overline{\text{ST}}$ is not strobed low before the timeout period set by TD expires. 4. During power-up.
6	11	$\overline{\text{RESET}}$	Active LOW reset output. (See RESET)
7	13	$\overline{\text{ST}}$	Strobe Input
8	15	V_{CC}	Power Supply
	1, 3. 5, 7, 10, 12, 14, 16	NC	No internal connection

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} ..... -0.5V to 7.0V
Voltage on $\overline{ST}$ and TD ..... -0.5V to V_{CC} + 0.5V
Voltage on $\overline{PBRST}$, $\overline{RESET}$ and RESET ..... -0.5V to V_{CC} + 0.5V

Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (10 sec) ..... 300°C
Operating Temperature Range ..... -40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, 1.0V ≤ V_{CC} ≤ 5.5V and over the operating temperature range of -40°C to +85°C. All voltages are referenced to ground.

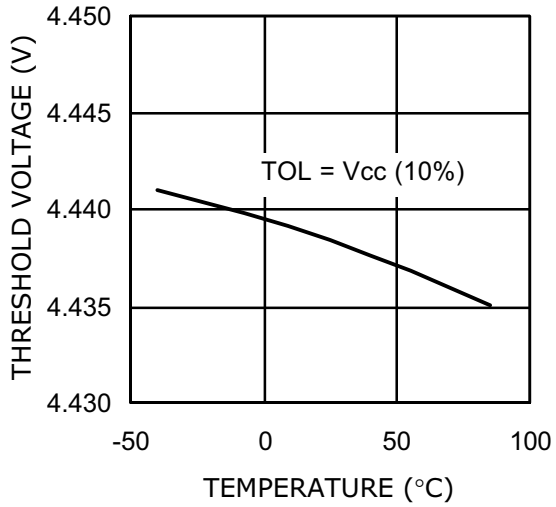
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.0		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.5V, CAT1232LP		35	50	µA
		V_{CC} = 3.6V, CAT1832		20	35	
V_{IH}	$\overline{ST}$ and $\overline{PBRST}$ Input High Level	(5)	2		V_{CC} + 0.3V	V
		(6)	V_{CC} - 0.4V			
V_{IL}	$\overline{ST}$ and $\overline{PBRST}$ Input Low Level	V_{CC} = 5.5V, CAT1232LP	– 0.3		0.8	V
		V_{CC} = 3.6V, CAT1832			0.5	
V_{CCTP}	V_{CC} Trip Point (TOL = GND)	CAT1232LP	4.50	4.62	4.74	V
V_{CCTP}	V_{CC} Trip Point (TOL = V_{CC})	CAT1232LP	4.25	4.37	4.49	V
V_{CCTP}	V_{CC} Trip Point (TOL = GND)	CAT1832	2.80	2.88	2.97	V
V_{CCTP}	V_{CC} Trip Point (TOL = V_{CC})	CAT1832	2.47	2.55	2.64	V
t_{TD}	Watchdog Time-Out Period	TD = GND	62.5	150	250	ms
t_{TD}	Watchdog Time-Out Period	TD = V_{CC}	500	1200	2000	ms
t_{TD}	Watchdog Time-Out Period	TD floating	250	600	1000	ms
V_{OH}	Output Voltage	I = – 500µA(3)	V_{CC} - 0.5V	V_{CC} - 0.1V		V
I_{OH}	Output Current	Output = 2.4V(2)		– 350		µA
I_{OL}	Output Current	Output = 0.4V,	10			mA
I_{IL}	Input Leakage	(1)	– 1.0		1.0	µA
R_{PU}	Internal Pull-Up Resistor	(1)	32	40	55	kΩ
C_{IN}	Input Capacitance				5	pF
C_{OUT}	Output Capacitance				7	pF
t_{PB}	$\overline{PBRST}$ Manual Reset Minimum Low Time	$\overline{PBRST}$ = V_{IL}	20			ms
t_{RST}	Reset Active Time		250	600	1000	ms
t_{ST}	$\overline{ST}$ Pulse Width	(4)	20			ns
t_{RPD}	V_{CC} Fail Detect to RESET or $\overline{RESET}$			5	8	µs
t_F	V_{CC} Slew Rate		20			µs
t_{PDLY}	$\overline{PBRST}$ Stable LOW to RESET and $\overline{RESET}$ Active				20	ms
t_{RPU}	V_{CC} Detect to RESET or $\overline{RESET}$ Inactive	t_{RISE} = 5µs	250	600	1000	ms
t_R	V_{CC} Slew Rate	4.25V to 4.75V	0			ns

Notes:
(1) $\overline{PBRST}$ is internally pulled HIGH to V_{CC} through a nominal 40kΩ resistor (R_{PU}).
(2) $\overline{RESET}$ is an open drain output on the CAT1232LP.
(3) RESET remains within 0.5V of V_{CC} on power-down until V_{CC} falls below 2V. RESET remains within 0.5V of ground on power-down until V_{CC} falls below 2.0V.
(4) Must not exceed the minimum watchdog time-out period (t_{TD}). The watchdog circuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed.
(5) Measured with V_{CC} ≥ 2.7V.
(6) Measured with V_{CC} < 2.7V.

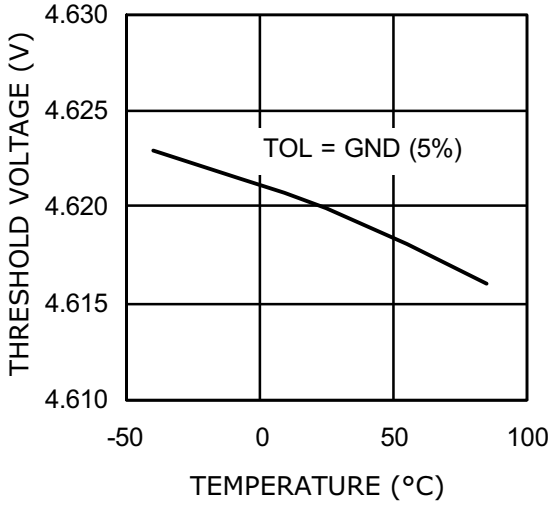
TYPICAL CHARACTERISTICS

For the CAT1232LP, V_{CC} = 5V and T_{AMB} = 25°C unless otherwise stated.

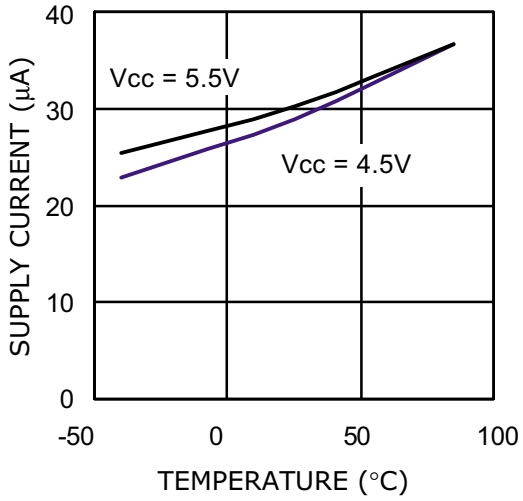
Threshold Voltage vs. Temperature (10% TOL)



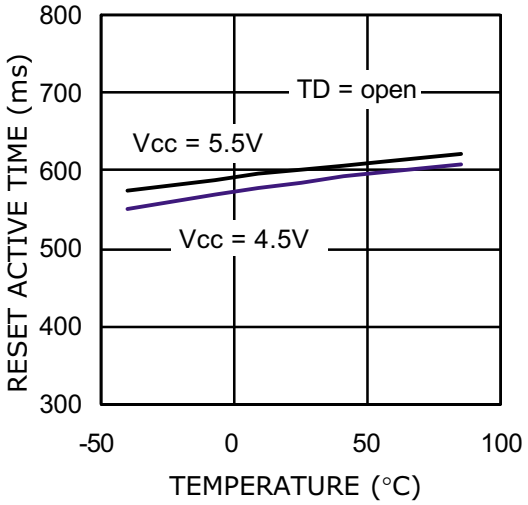
Threshold Voltage vs. Temperature (5% TOL)



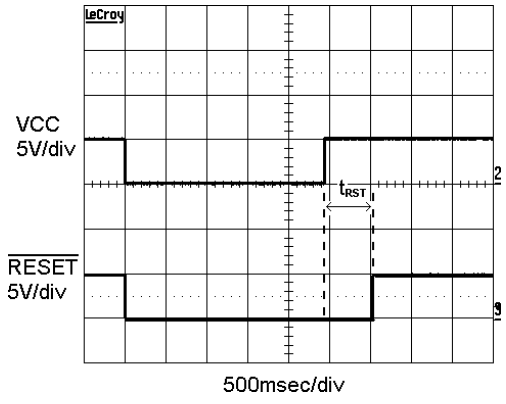
Supply Current vs. Temperature



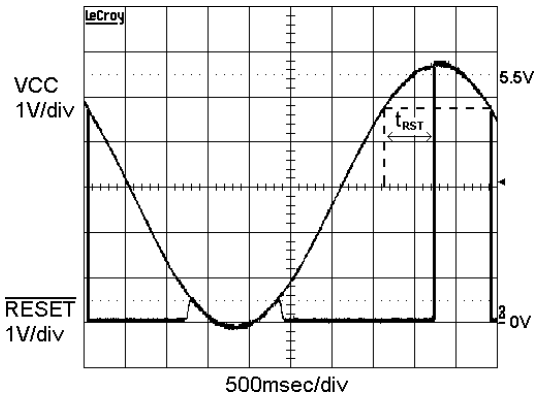
Reset Active Time vs. Temperature



Reset Active Time Waveform



Transient Response



APPLICATION INFORMATION

SUPPLY VOLTAGE MONITOR

Reset Signal Polarity and Output Stage Structure

$\overline{\text{RESET}}$ is an active LOW signal. It is developed with an open drain driver in the CAT1232LP. A pull-up resistor is required, typical values are 10kΩ to 50kΩ. The CAT1832 uses a CMOS push-pull output stage for the $\overline{\text{RESET}}$.

RESET is an active High signal developed by a CMOS push-pull output stage and is the logical opposite to $\overline{\text{RESET}}$.

Trip Point Tolerance Selection

The TOL input is used to select the V_{CC} trip point threshold. This selection is made connecting the TOL input to ground or V_{CC}. Connecting TOL to Ground makes the V_{CC} trip threshold 4.62V for the CAT1232LP and 2.88V for the CAT1832.

Connecting TOL to VCC makes the VCC trip threshold 4.37V for the CAT1232LP and 2.55V for the CAT1832.

After V_{CC} has risen above the trip point set by TOL, RESET and $\overline{\text{RESET}}$ remain active for a minimum time period of 250ms.

On power-down, once V_{CC} falls below the reset threshold the RESET outputs will remain active and are guaranteed valid down to a V_{CC} level of 1.0V.

Tolerance Select Voltage	Trip Point Tolerance	Trip Point Voltage (V)		
		MIN	NOMINAL	MAX
CAT1232LP TOL = V_{CC}	10 %	4.25	4.37	4.49
CAT1232LP TOL = GND	5 %	4.50	4.62	4.74
CAT1832 TOL = V_{CC}	20 %	2.47	2.55	2.64
CAT1832 TOL = GND	10 %	2.80	2.88	2.97

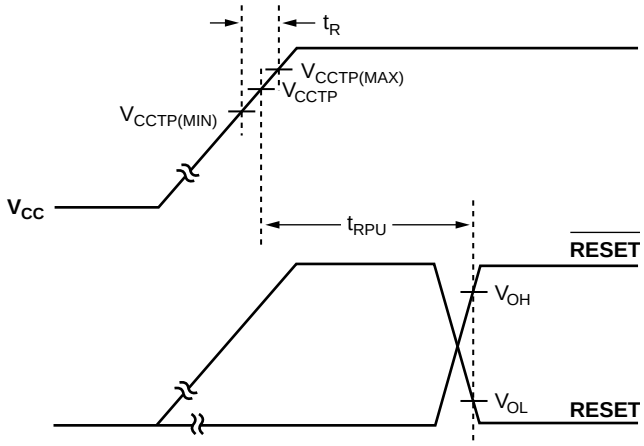


Figure 1. Timing Diagram: Power Up

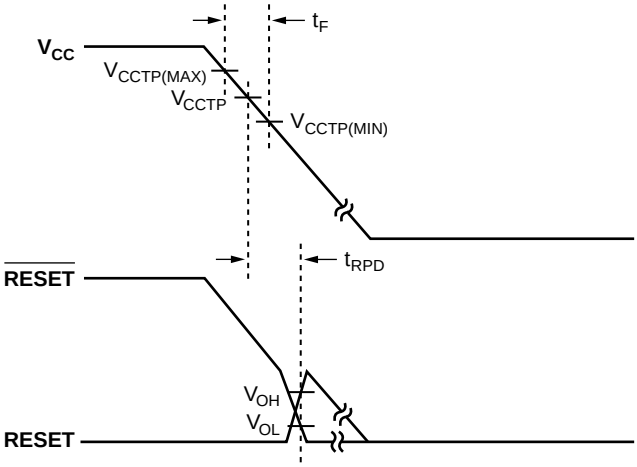


Figure 2. Timing Diagram: Power Down

Manual Reset Operation

Push-button input, $\overline{\text{PBRST}}$, allows the user to issue reset signals. The pushbutton input is debounced and is pulled high through an internal 40kΩ resistor.

When $\overline{\text{PBRST}}$ is held low for the minimum time of 20 ms, both resets become active and remain active for a minimum time period of 250ms after $\overline{\text{PBRST}}$ returns high.

No external pull-up resistor is required, since $\overline{\text{PBRST}}$ is pulled high by an internal 40kΩ resistor.

$\overline{\text{PBRST}}$ can be driven from a TTL or CMOS logic line or short-ed to ground with a mechanical switch.

WATCHDOG TIMER AND $\overline{ST}$ INPUT

A watchdog timer stops and restarts a microprocessor that has stopped proper operation or become “hung”. The watchdog performs this function by monitoring the $\overline{ST}$ input. After the reset outputs go inactive the $\overline{ST}$ input must be strobed with a high-to-low signal transition prior to the minimum watchdog timeout period. However if the $\overline{ST}$ input is not strobed with a high-to-low signal transition prior to a watchdog timeout the reset outputs will become active for T_{RST} reseting and restarting the microprocessor. Once the resets return to the inactive state the watchdog timer restarts the process.

The TD input allows the user to select from three predetermined watchdog timeout periods. Always use the minimum timeout period to determine the required frequency of $\overline{ST}$ high-to-low transitions and the maximum to determine the time prior to the reset outputs becoming active. $\overline{ST}$ pulse widths must be 20ns or greater.

The watchdog timer cannot be disabled. It must be strobed with a high-to-low signal transition to avoid a watchdog timeout and subsequent reset.

TD Voltage Level	Watchdog Time-out Period (ms)		
	MIN	NOMINAL	MAX
GND	62.5	150	250
Floating	250	600	1000
V_{CC}	500	1200	2000

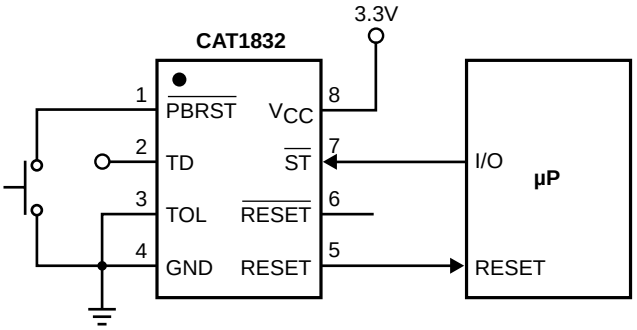


Figure 4. CAT1832 Application Circuit: Pushbutton Reset

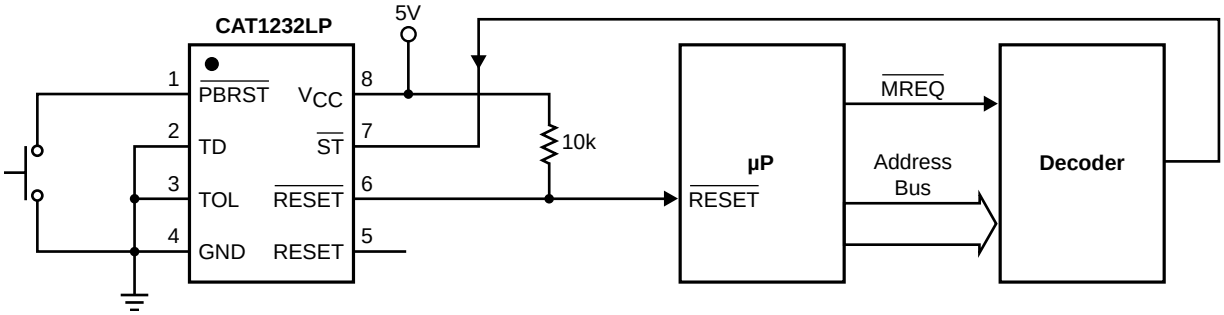


Figure 5. CAT1232LP Application Circuit: Watchdog Timer

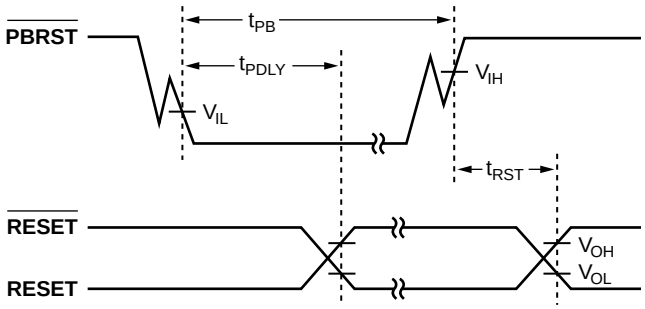
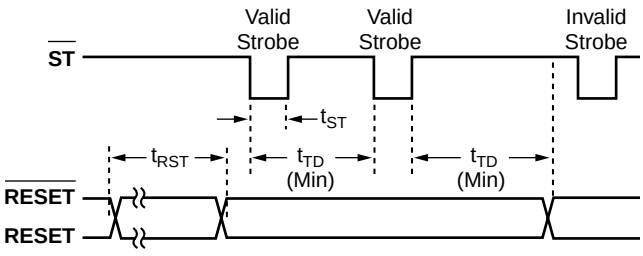


Figure 6. Timing Diagram: Pushbutton Reset

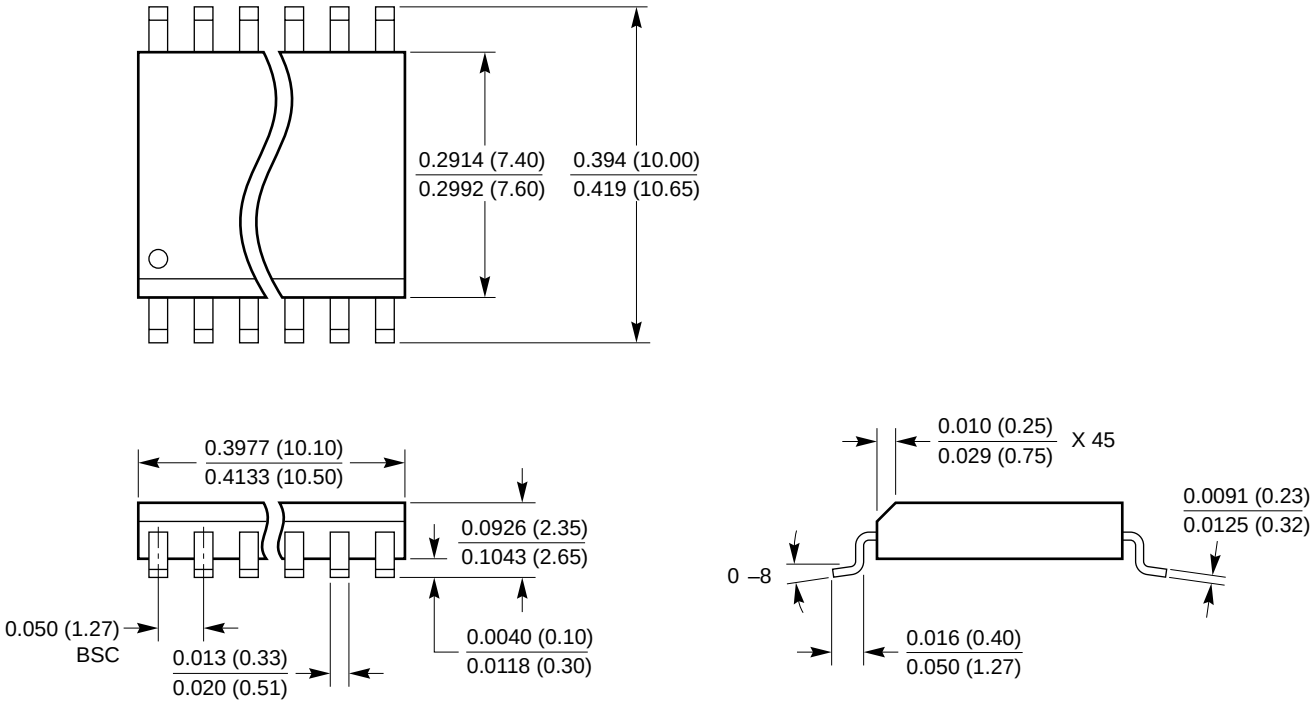


Note: $\overline{ST}$ is ignored whenever a reset is active.

Figure 7. Timing Diagram: Strobe Input

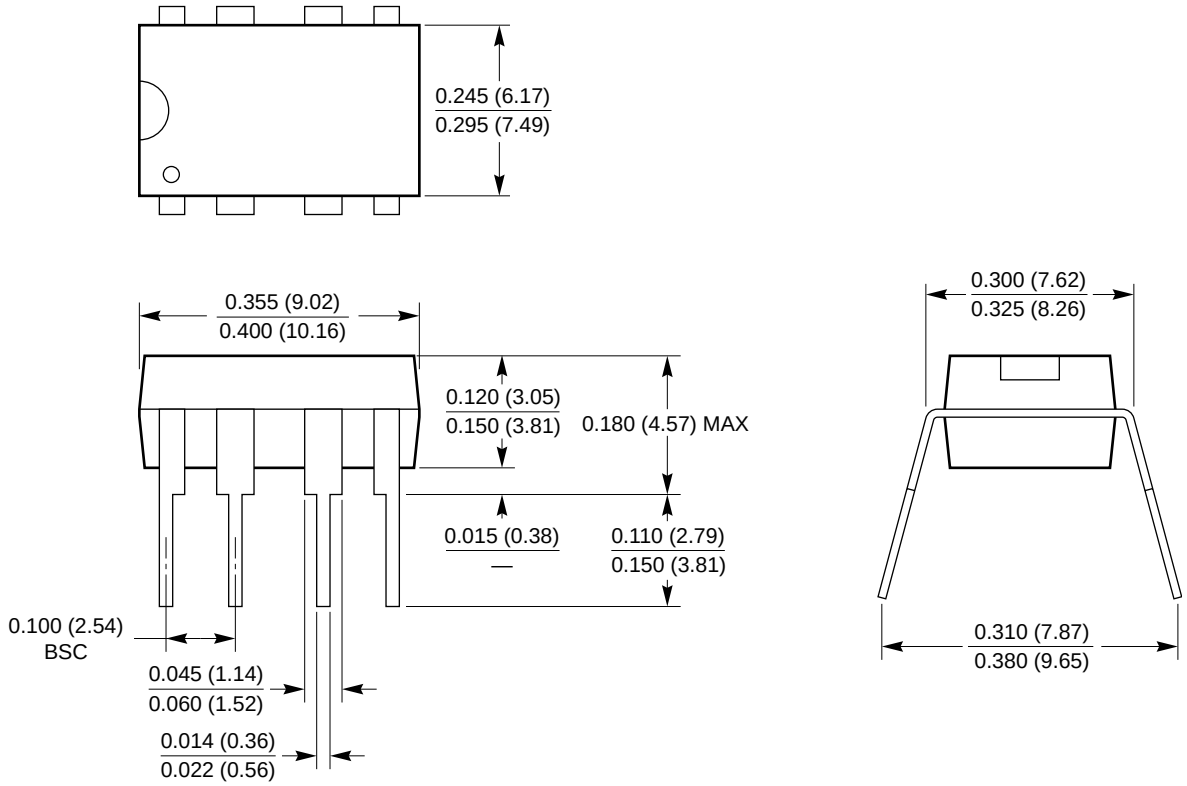
PACKAGE MECHANICAL

16-LEAD WIDE BODY SOIC (300mil)



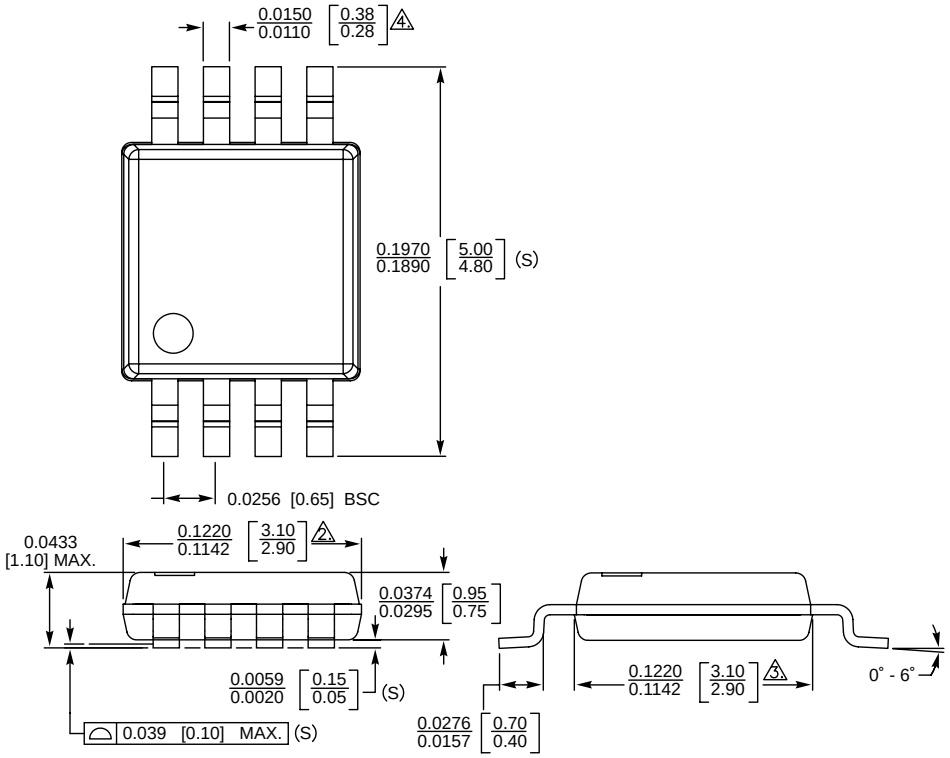
Notes:
1. Complies with JEDEC publication 95 MS-013 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.

8-LEAD DIP (300mil)

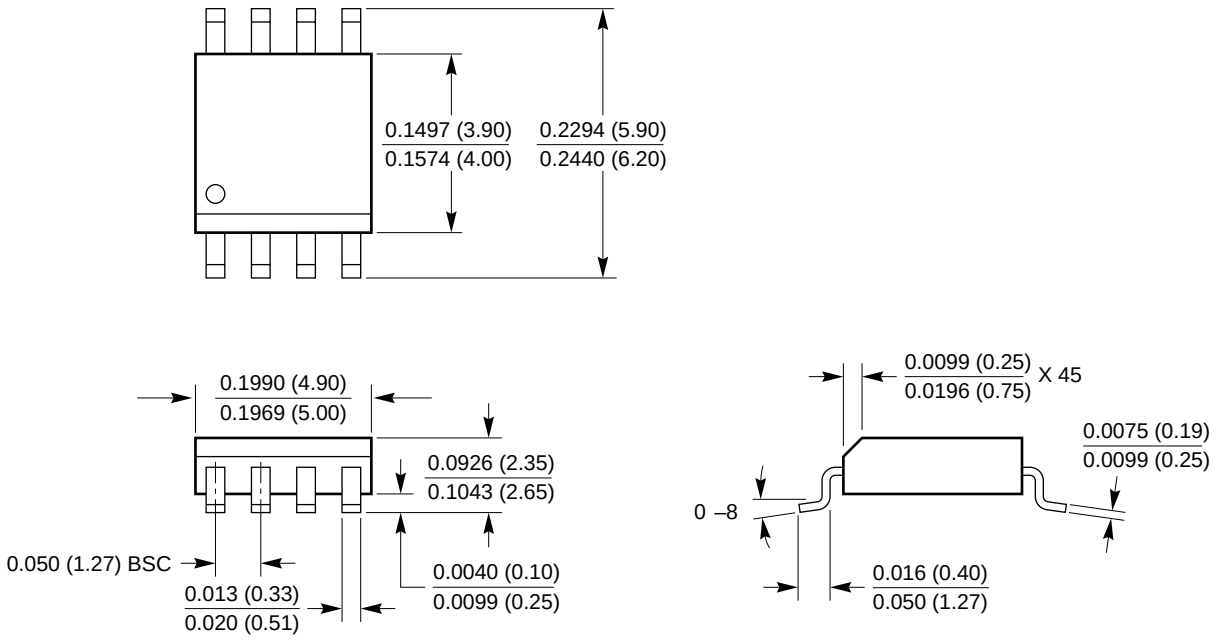


PACKAGE MECHANICAL

8-LEAD MSOP



8-LEAD Narrow Body SOIC (150mil)



REVISION HISTORY

Date	Revision	Comments
06/13/2005	00	Initial Issue
07/26/2005	A	Update Electrical Characteristics Add Typical Characteristics

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Publication #: 25089
Revison: A
Issue date: 07/26/05