AL4CE211
AL4CE221
AL4CE231
AL4CE241
AL4CE251

Data Sheets

Version 1.0

Amendments

04-05-02 Preliminary Version 1.0

02-20-03 Company Contact Information updated

AL4CE211/AL4CE221/AL4CE231/AL4CE241 /AL4CE251 (512 x9, 1k x9, 2k x9, 4k x9, 8k x9) Enhanced Synchronous FIFO

Contents:

1.0 Description

The AL4CE211/AL4CE221/AL4CE231/AL4CE241/AL4CE251 series memory products are high-performance, low-power 9-bit read/write FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of communication applications, such as optical disk controllers, Local Area Networks (LANs), SONET (Synchronous Optical Network).

The input data is synchronous with a free-running clock (WCLK), and input-enable pins (/WEN). Data is written into the FIFO on every clock when enable pins are asserted. The output is synchronous with the other free-running clock (RCLK) and enables (/REN). An Output Enable pin (/OE) is provided at the read port for tri-state control of the output port. The FIFOs can output two fixed flags, Empty Flag(/EF) and Full Flag (/FF), and two programmable flags, Almost-Empty (/PAE) and Almost-Full (/PAF). The offsets of the /PAE and /PAF flags are loaded when Load pin (/LD) goes low.

The AL4CE211/AL4CE221/AL4CE231/AL4CE241/AL4CE251 series are enhanced version of the AL4CS211/AL4CS221/AL4CS231/AL4CS241/AL4CS251 series with Retransmit function supported which allows data to be reread from the FIFO more than once.

2.0 Features

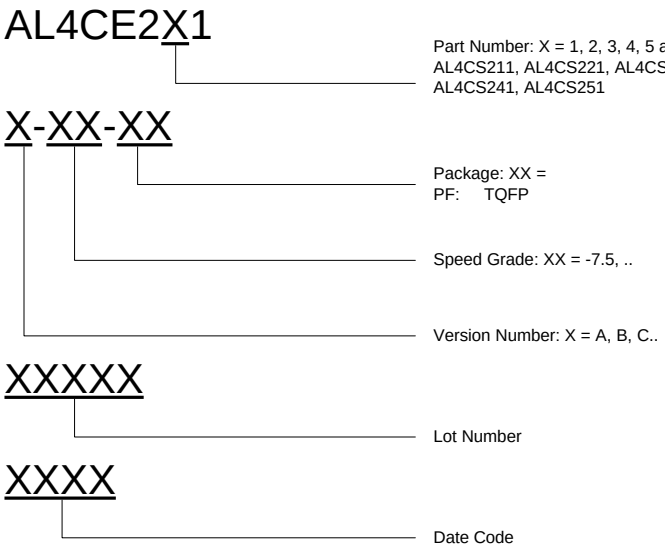
- 512 x9-bit cell array (AL4CE211)
- 1,024 x9-bit cell array (AL4CE221)
- 2,048 x9-bit cell array (AL4CE231)
- 4,096 x9-bit cell array (AL4CE241)
- 8,192 x9-bit cell array (AL4CE251)
- 133 MHz Operation
- 7.5 ns read/write cycle time
- Independent Read and Write operations
- Retransmit the data (reread the data)
- Empty and Full flags support
- Programmable Almost-Empty and Almost-Full flags
- Output enable (data skipping)
- 3.3V power supply with 5V signal tolerant input
- Available in a 32-pin Thin Quad Flat Pack (TQFP) packages

3.0 Applications

- Routers
- ATM switches
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- Time base correction (TBC)

4.0 Chip Information

4.1 Marking Information



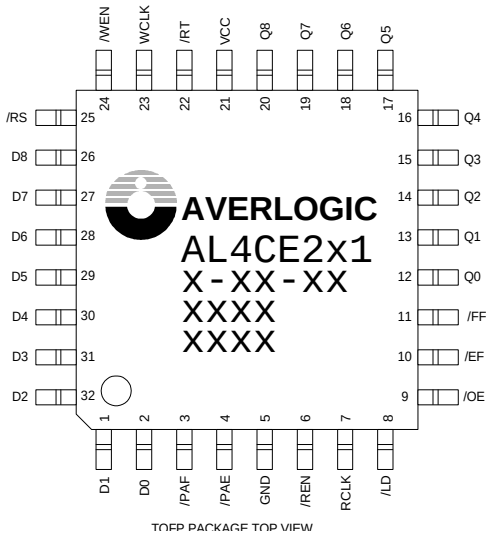
4.2 Ordering Information

The ordering information for AL4CE211/AL4CE221/AL4CE231/AL4CE241/AL4CE251 are:

Part number	Package	Power Supply	Status
AL4CE211/221/231/241/251(A-7.5-PF)	32-pin plastic TQFP(7x7mm)	+3.3V±10%	Sample in Aug., 2001

5.0 Pin-out Diagram

The AL4CE211/AL4CE221/AL4CE231/AL4CE241/AL4CE251 pin-out diagram is following:



6.0 Block Diagram

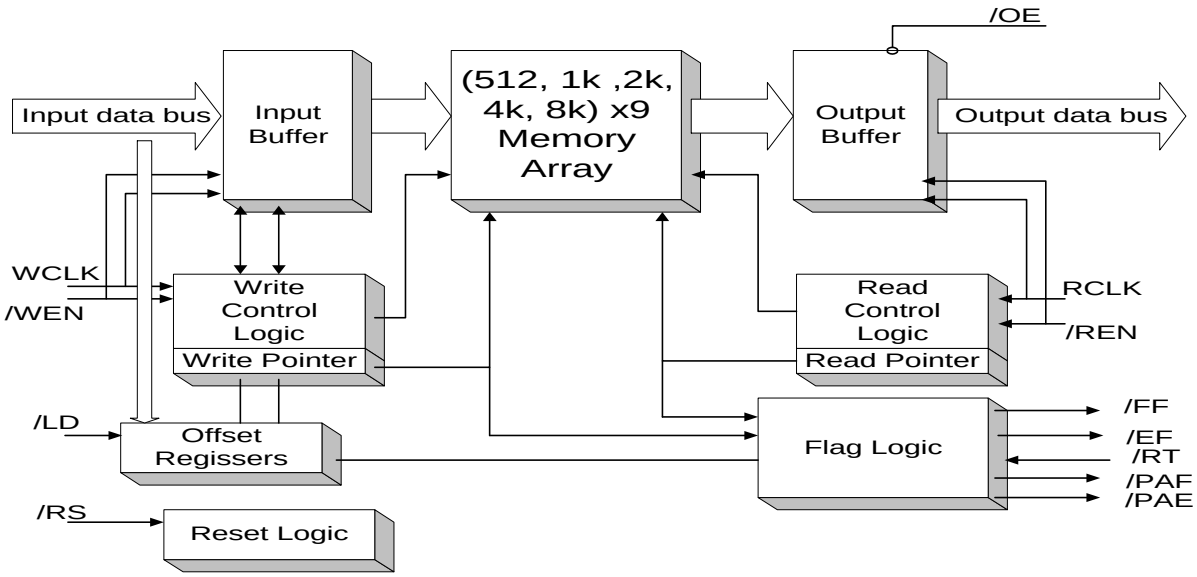


Figure 1. AL4CE2x1 FIFO Block Diagram

The internal structure of the AL4CE211/AL4CE221/AL4CE231/AL4CE241/AL4CE251 consists of Input/Output buffers, Read/Write Control Logic and main (512, 1k, 2k, 4k, 8k) x9 different configuration memory cell array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.

7.0 Pin Definition and Description

The pin-out definition and function are described as following:

Write Bus Signals

Pin Symbol	Pin name	TQFP Pin no.	I/O Typ	Description
D[8:0]	Data Inputs	[26:32], 1, 2	I	9-bit input data bus.
/WEN	Write Enable	24	I	When /WEN is LOW, data is written into the FIFO on every rising edge of WCLK. When /WEN is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the /FF is LOW.
WCLK	Write Clock	23	I	Data is written into the FIFO on a rising edge of WCLK when the Write Enable(s) are asserted. Data will not be written into FIFO if /FF is not LOW.

Read Bus Signals

Pin symbol	Pin name	TQFP Pin no.	I/O typ	Description
Q[8:0]	Data Outputs	[20:12]	O	9-bit output data bus.
/REN	Read Enable	6	I	When both /REN are LOW, data is read from the FIFO on every rising edge of RCLK. Data will not be read from the FIFO if the /EF is LOW.
/OE	Output Enable	9	I	When /OE is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in high-impedance.
RCLK	Read Clock	7	I	Data is read from the FIFO on a rising edge of RCLK when /REN is LOW, and if the FIFO is not empty.

Miscellaneous & Flags Signals

Pin Symbol	Pin name	TQFP Pin no.	I/O typ	Description
/RS	Reset	25	I	When /RS is set LOW, internal read and write pointers are set to the first location of the RAM array, /FF and /PAF go HIGH, and /PAE and /EF go LOW. A reset is required before an initial WRITE after power-up.
/LD	Load	8		When /LD is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the rising edge of the WCLK, when /WEN is LOW. When /LD is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the rising edge of the RCLK, when /REN is LOW.
/RT	Retransmit	22		/RT asserted on the rising edge of RCLK initialized the READ pointer to zero, sets the /EF flag to LOW and does not affect the write pointer, programming
/FF	Full Flag	11	O	/FF indicates whether or not the FIFO memory is full.
/EF	Empty Flag	10	O	/EF indicates whether or not the FIFO memory is empty.
/PAE	Programmable Almost-Full Flag	4	O	When /PAE is LOW, the FIFO is Almost-Empty based on the offset programmed into the FIFO.
/PAF	Programmable Almost-Full Flag	3	O	When /PAF is LOW, the FIFO is Almost –Full based on the offset programmed into the FIFO.

Power/Ground Signals

Pin Symbol	Pin name	TQFP Pin no.	I/O typ	Description
VCC	Power	21	-	3.3V ± 10% power supply
GND	Ground	5	-	Ground.

8.0 Memory Operations

8.1 Inputs and Outputs

8.1.1 DATA INPUTS (D8 ~ D0)

D8 ~ D0 are 9-bit wide of input data port.

8.1.2 DATA OUTPUTS (Q8-Q0)

Q8 ~ Q0 are 9-bit wide of output data port.

8.2 Controls

8.2.1 Reset (/RS)

Reset takes place when the Reset (/RS) input is LOW. During reset, both internal read and write pointers are set to the staring position. A reset is required to initial internal logic after power-up. The Full Flag (/FF) and Programmable Almost-Full Flag (/PAF) will be reset to HIGH after t_{RSF}. The Empty Flag (/EF) and Programmable Almost-Empty Flag (/PAE) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

8.2.2 Write Clock (WCLK)

A write cycle is initiated on the rising edge of the Write Clock (WCLK). Data setup and hold times must be met with respect to the rising edge of WCLK. The Full Flag (/FF) and Programmable Almost-Full Flag (/PAF) are synchronized with respect to the rising edge of the Write Clock (WCLK).

The Write and Read Clocks can be asynchronous or coincident.

8.2.3 Write Enable1 (/WEN)

When Write Enable (/WEN) is low, data can be written into the input register and memory array on the rising edge of every Write Clock (WCLK). Data is stored in the memory array sequentially and independently of any on going read operation. When Write Enable (/WEN) is HIGH, the input holds the previous data and no new data can be written into the memory array. To prevent data overflow, the Full Flag (/FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag (/FF) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable(s) are ignored when the FIFO is full.

8.2.4 Read Clock (RCLK)

Data can be read on the outputs on the rising edge of the Read Clock (RCLK), when all the output controls /REN, Output Enable (/OE) are set LOW. The Empty Flag (/EF) and Programmable Almost-

Empty Flag (/PAE) are synchronized with respect to the rising edge of the Read Clock (RCLK). The Write and Read Clocks can be asynchronous or coincident.

8.2.5 Read Enable (/REN)

When Read Enables (/REN) is LOW, data is read from the memory array to the output register on the rising edge of the Read Clock (RCLK) if the FIFO is not empty. When Read Enable (/REN) is HIGH, the output register holds the previous data and no new data can to be loaded into the register. When all the data has been read from the FIFO, the Empty Flag (/EF) will go LOW, inhibiting further read operations. Once a valid write operation has been done, the Empty Flag (/EF) will go HIGH after t_{REF} and a valid read can begin. The /EF flag is updated on the rising edge of RCLK. The Read Enables (/REN) are ignored when the FIFO is empty.

8.2.6 Output Enable (/OE)

When Output Enable (/OE) is enabled (LOW), the parallel output buffers receive data from the output register. When /OE is disabled (HIGH), the Q8 ~ Q0 output data bus is in a high-impedance state.

8.2.7 Load (/LD)

The AL4CE211/221/231/241/251 devices contain four 8-bit offset registers, which can be loaded with data on the inputs, or read from the outputs. See following table for details of the size of the registers and the default values.

	1st word	2nd word	3rd word	4th word
AL4CE211	[7:0] Empty Offset (LSB)	[0] Empty Offset (MSB)	[7:0] Full Offset (LSB)	[0] Full Offset (MSB)
	Default = 07h	Default = 0b	Default = 07h	Default = 0b
AL4CE221	[7:0] Empty Offset (LSB)	[1:0] Empty Offset (MSB)	[7:0] Full Offset (LSB)	[1:0] Full Offset (MSB)
	Default = 07h	Default = 00b	Default = 07h	Default = 00b
AL4CE231	[7:0] Empty Offset (LSB)	[2:0] Empty Offset (MSB)	[7:0] Full Offset (LSB)	[2:0] Full Offset (MSB)
	Default = 07h	Default = 000b	Default = 07h	Default = 000b
AL4CE241	[7:0] Empty Offset (LSB)	[3:0] Empty Offset (MSB)	[7:0] Full Offset (LSB)	[3:0] Full Offset (MSB)
	Default = 07h	Default = 0000b	Default = 07h	Default = 0000b
AL4CE251	[7:0] Empty Offset (LSB)	[4:0] Empty Offset (MSB)	[7:0] Full Offset (LSB)	[4:0] Full Offset (MSB)
	Default = 07h	Default = 00000b	Default = 07h	Default = 00000b

When the Write Enable1 (/WEN) and Load (/LD) are set LOW, data on the inputs D8 ~ D0 is written into the Empty (Least Significant Bit) Offset register on the first rising edge of the Write Clock (WCLK). Data is written into the Empty (Most Significant Bit) Offset register on the second rising edge of the Write Clock (WCLK), into the Full (Least Significant Bit) Offset register on the third transition, and into the Full (Most Significant Bit) Offset register on the fourth transition. The fifth transition of the Write Clock (WCLK) again writes to the Empty (Least Significant Bit) Offset register.

However, writing all offset registers does not have to occur consecutively. The FIFO can return to normal read/write operation by bringing the Load (/LD) pin HIGH after one or two offset registers can be written. When the Load (/LD) pin is set LOW again, and Write Enable (/WEN) is LOW, the next offset register in sequence is written.

8.2.8 Retransmit (/RT)

The Retransmit operation can do multiple data read. The Retransmit operation occurs when a /RT low is sampled at the rising edge of the RCLK. The read pointer will be reset to first location of the memory and /EF will be brought to low (if /EF was HIGH before setup), and then the data can be read out from the memory, starting at the beginning of the memory.

8.3 Flags

8.3.1 Full Flag (/FF)

The Full Flag (/FF) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset (/RS), the Full Flag (/FF) will go LOW after 512 writes for the AL4CE211, 1,024 writes for the AL4CE221, 2,048 writes for the AL4CE231, 4,096 writes for the AL4CE241 and 8,192 writes for the AL4CE251. The Full Flag (/FF) is synchronized with respect to the rising edge of the Write Clock (WCLK).

8.3.2 Empty Flag (/EF)

The Empty Flag (/EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty. The Empty Flag (/EF) is synchronized with respect to the rising edge of the Read Clock (RCLK).

8.3.3 Programmable Almost- Full Flag (/PAF)

The Programmable Almost-Full flag (/PAF) will go LOW when the FIFO reaches the almost-full condition. If no reads are performed after Reset (/RS), the Programmable Almost-Full flag (/PAF) will go LOW after (512-m) writes for the AL4CE211, (1,024-m) writes for the AL4CE221, (2,048-m) writes for the AL4CE231, (4,096-m) writes for the AL4CE241 and (8,192-m) writes for the AL4CE251. The offset “m” is defined in the Full Offset registers. If there is no full offset specified, the Programmable Almost-Full flag (/PAF) will go LOW at Full-7 words. The Programmable Almost-Full flag (/PAF) is synchronized with respect to the rising edge of the Write Clock (WCLK).

8.3.4 Programmable Almost-Empty Flag (/PAE)

The Programmable Almost-Empty flag (/PAE) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset registers. If no reads are performed after Reset the Programmable Almost-Empty flag (/PAE) will go HIGH after "n+1" for the AL4CE211/221/231/241/251. If there is no empty offset specified, the Programmable Almost-Empty flag (/PAE) will go LOW at Empty+7 words. The Programmable Almost-Empty flag (/PAE) is synchronized with respect to the rising edge of the Read Clock (RCLK).

9.0 Multiple Devices Bus Expansion and Cascading

9.1 Width Expansion Configuration

Simply connecting the corresponding input controls signals of multiple devices may increase data bus width. A composite flag should be created for each of the end-point status flags (/EF and /FF). The

partial status flags (/PAE and /PAF) can be detected from any one device. Figure 15 demonstrates an 18-bit word width data bus by using two AL4CE211/221/231/241/251s. Any word width expansion can be attained by adding additional AL4CE211/221/231/241/251s.

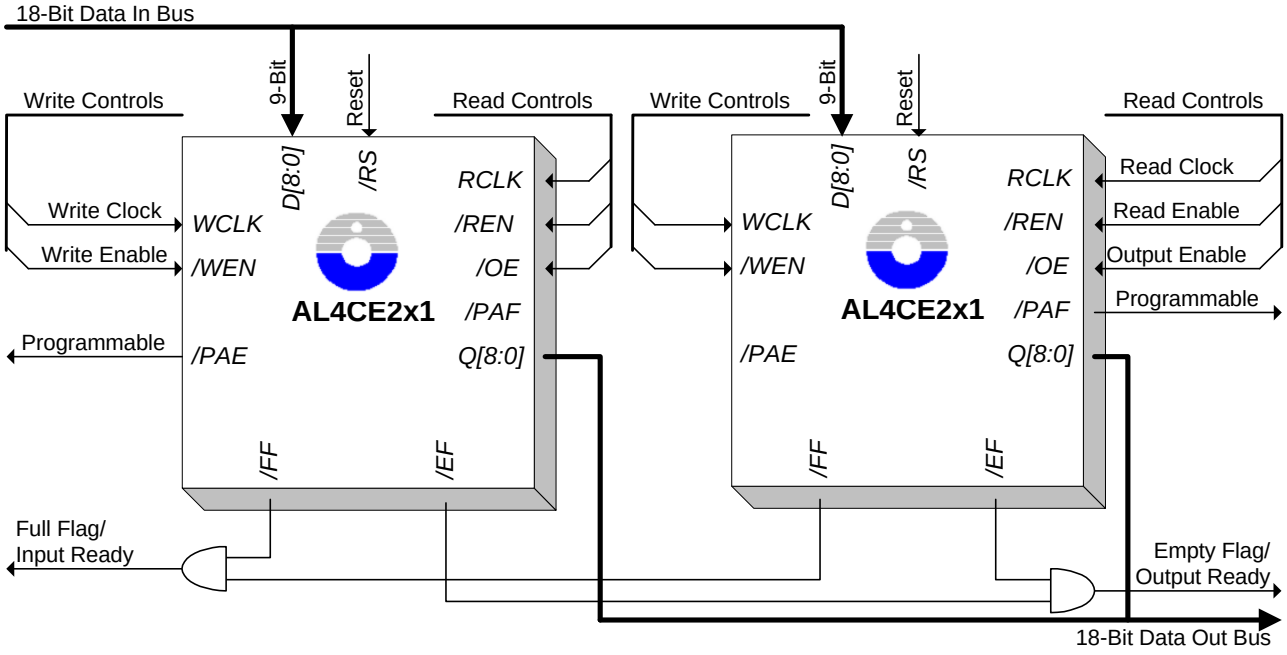


Figure 2. Multiple FIFO memory in bus width expansion

10.0 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

10.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V

10.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
I_{DD}	Operating Current @20MHz	-	-	16	mA
I_{DDS}	Standby Current	-	1.8	5	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-2	-	+2	μA
I_{LO}	Output Leakage Current	-10	-	+10	μA

Note: The Operating Current is tested at RCLK=WCLK=20MHz and data inputs switch at 10MHz

10.4 AC Electrical Characteristics

(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

		133Mhz		
Symbol	Parameter	Min	Max	Unit
t_S	Clock Cycle Frequency	-	133	MHz
t_A	Data Access Time	2	5	ns
t_{CLK}	Clock Cycle Time	7.5	-	ns
t_{CLKH}	Clock HIGH Time	3.5	-	ns
t_{CLKL}	Clock LOW Time	3.5	-	ns
t_{DS}	Data Setup Time	2.5	-	ns
t_{DH}	Data Hold Time	0.5	-	ns
t_{ENS}	Enable Setup Time	2.5	-	ns
t_{ENH}	Enable Hold Time	0.5	-	ns
t_{RS}	Reset Pulse Width	7.5	-	ns
t_{RSS}	Reset Setup Time	6	-	ns
t_{RSR}	Reset Recovery Time	6	-	ns
t_{RSF}	Reset to Flag and Output Time	-	9	ns
t_{OLZ}	Output Enable to Output in Low-Z	0	-	ns
t_{OE}	Output Enable to Output Valid	-	5	ns
t_{OHZ}	Output Enable to in High-Z	-	5	ns
t_{WFF}	Write Clock to Full Flag	-	5	ns
t_{REF}	Read Clock to Empty Flag	-	5	ns
t_{AF}	Write Clock to Almost-Full Flag	-	5	ns
t_{AE}	Read Clock to Almost-Empty Flag	-	5	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for /FF & /EF	3	-	ns
T_{SKEW2}	Skew time between Read Clock & Write Clock for /PAE and /PAF	8	-	ns

10.5 Timing Diagrams

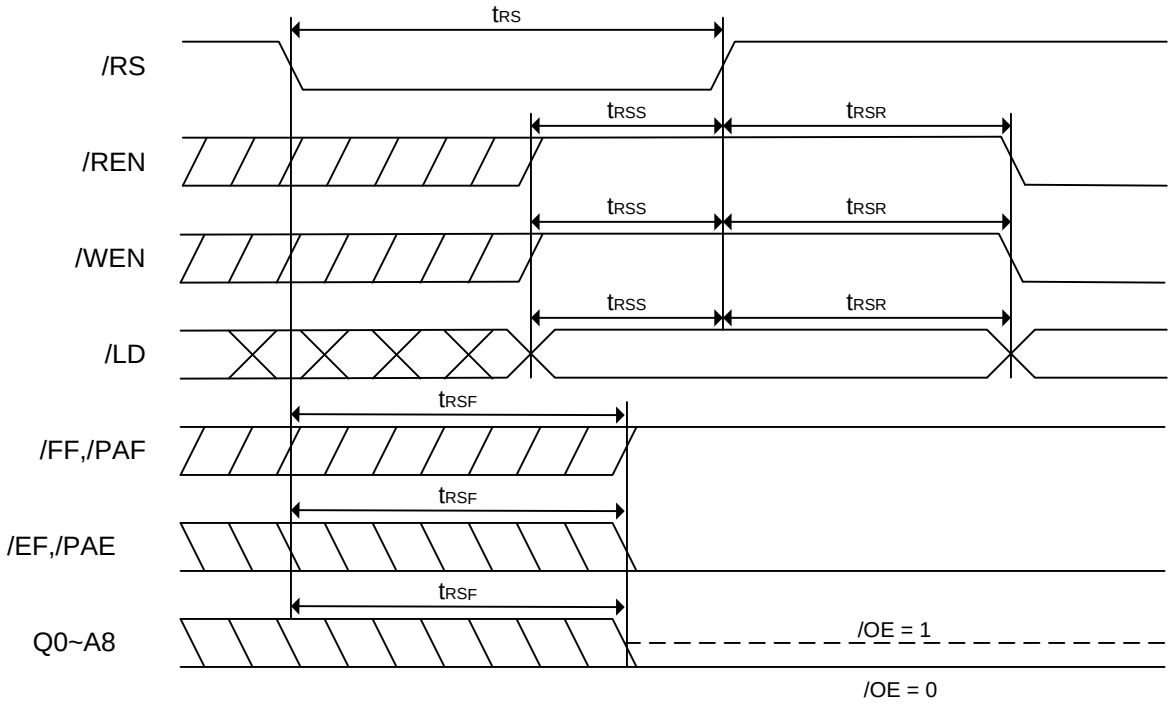


Figure 3. Reset Timing

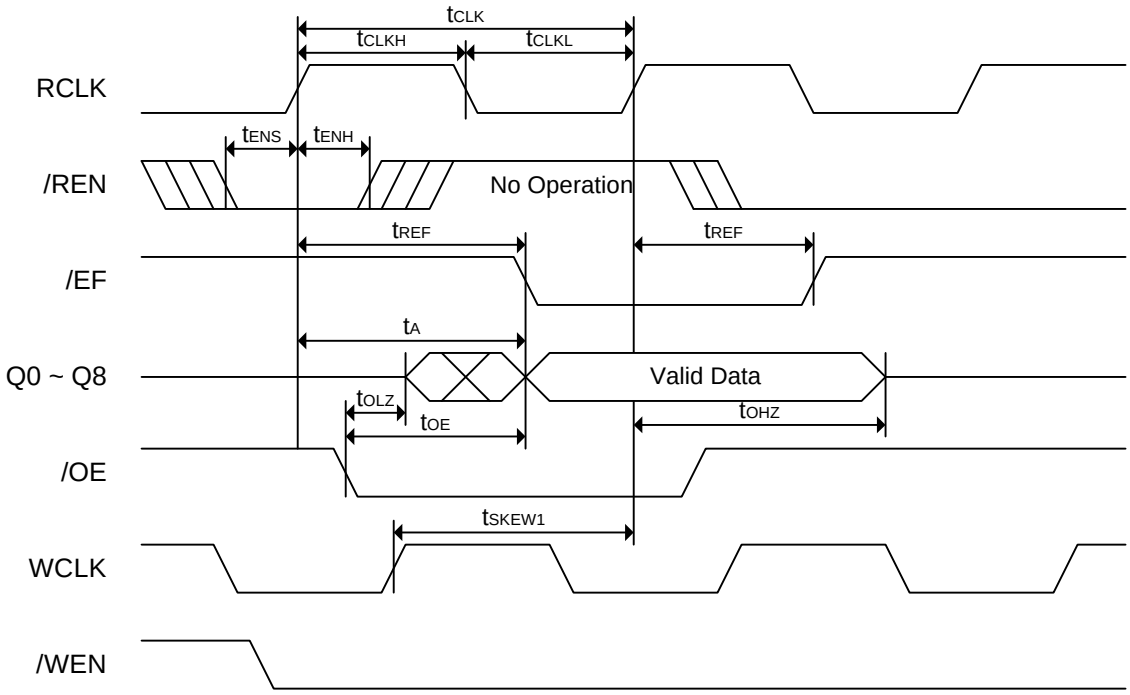


Figure 4. Read Cycle Timing

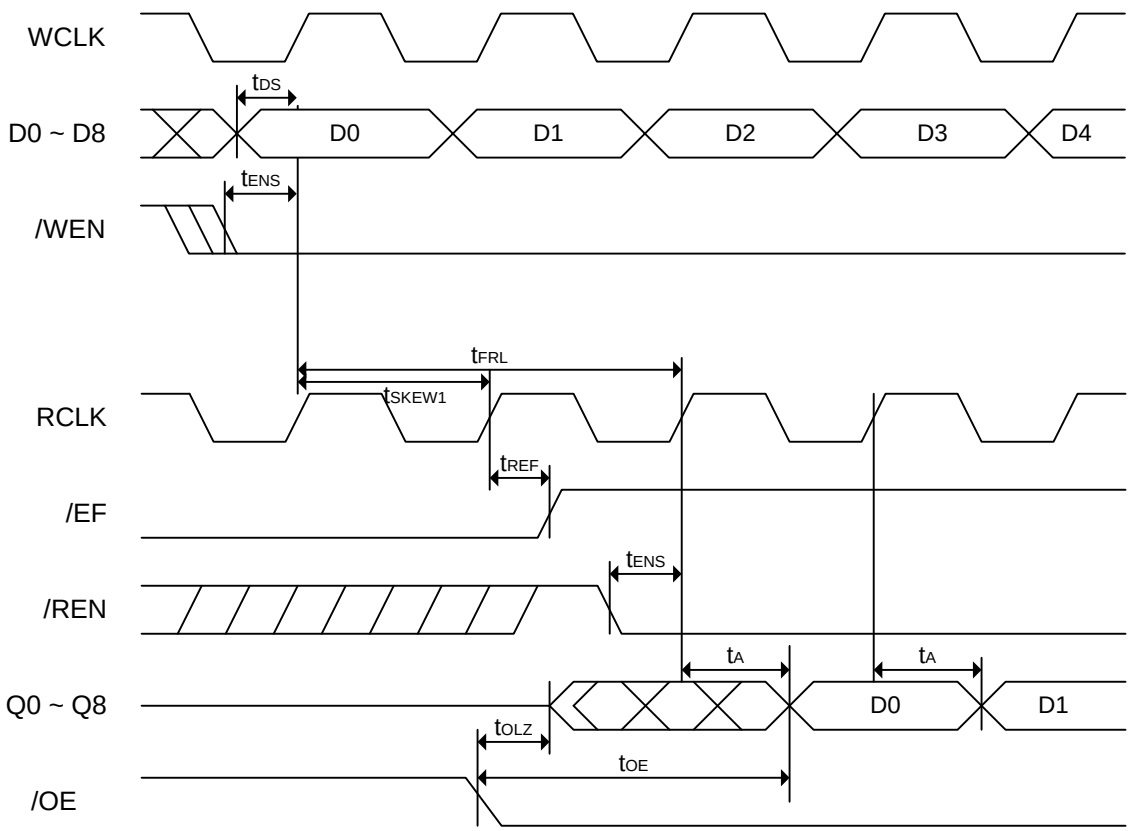


Figure 5. First Data Word Latency Timing

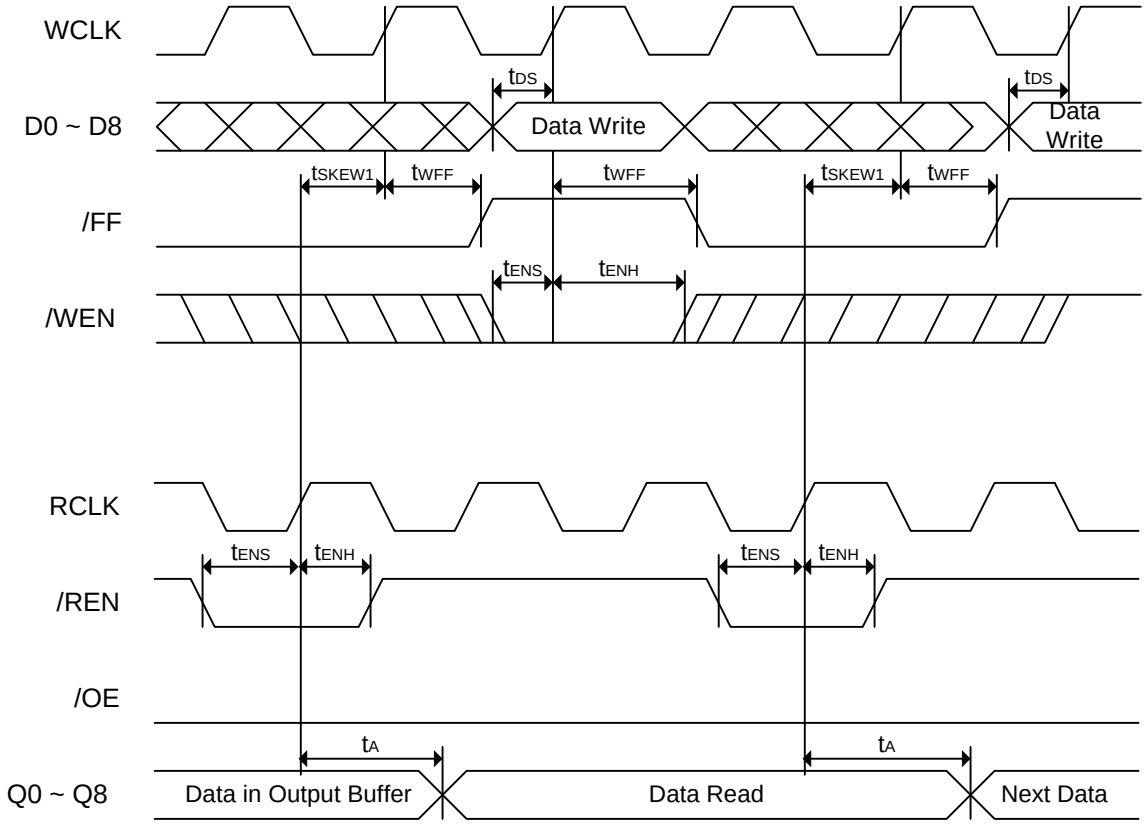


Figure 6. Full Flag Timing

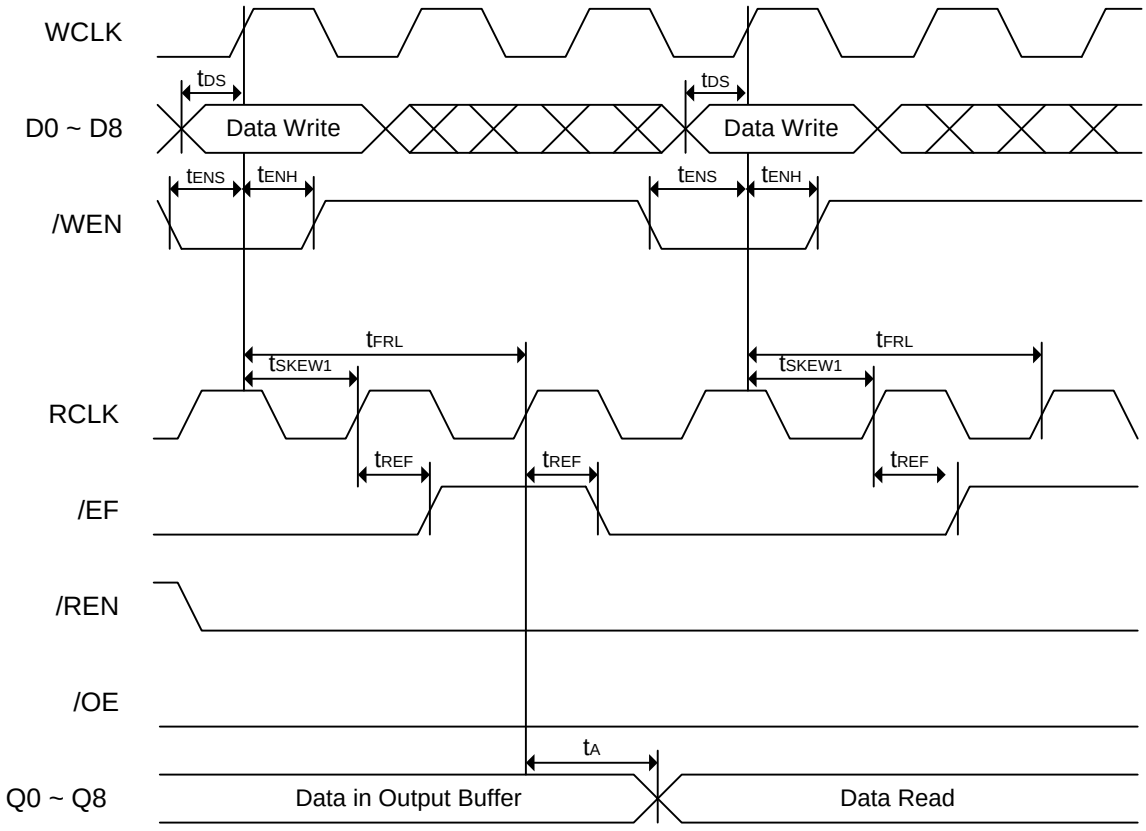


Figure 7. Empty Flag Timing

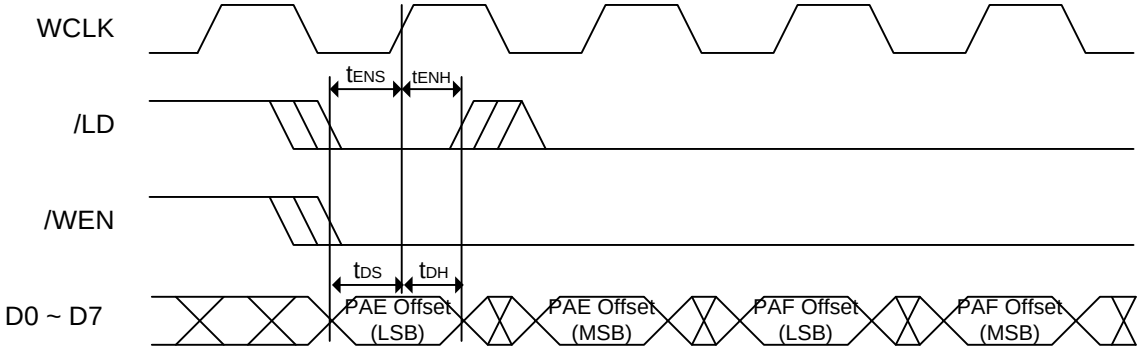


Figure 8. Write Offset Registers

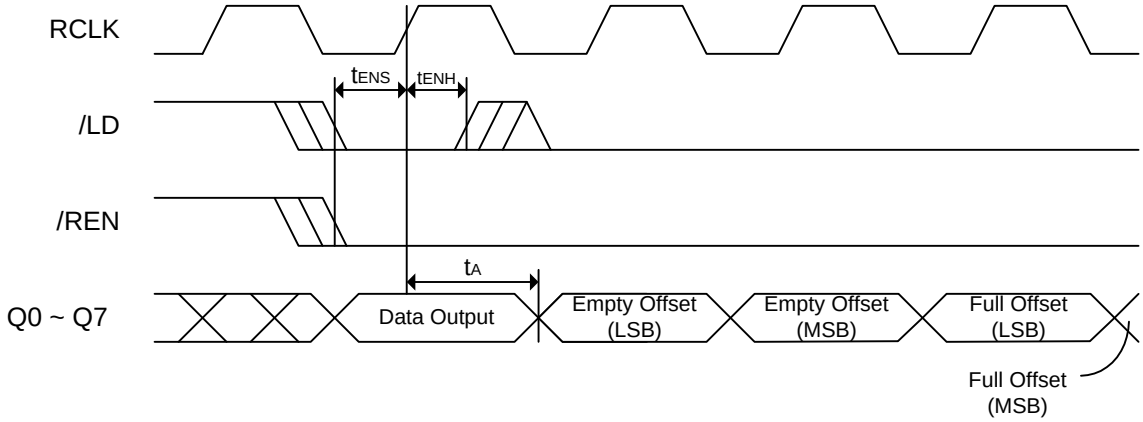


Figure 9. Read Offset Registers Timing

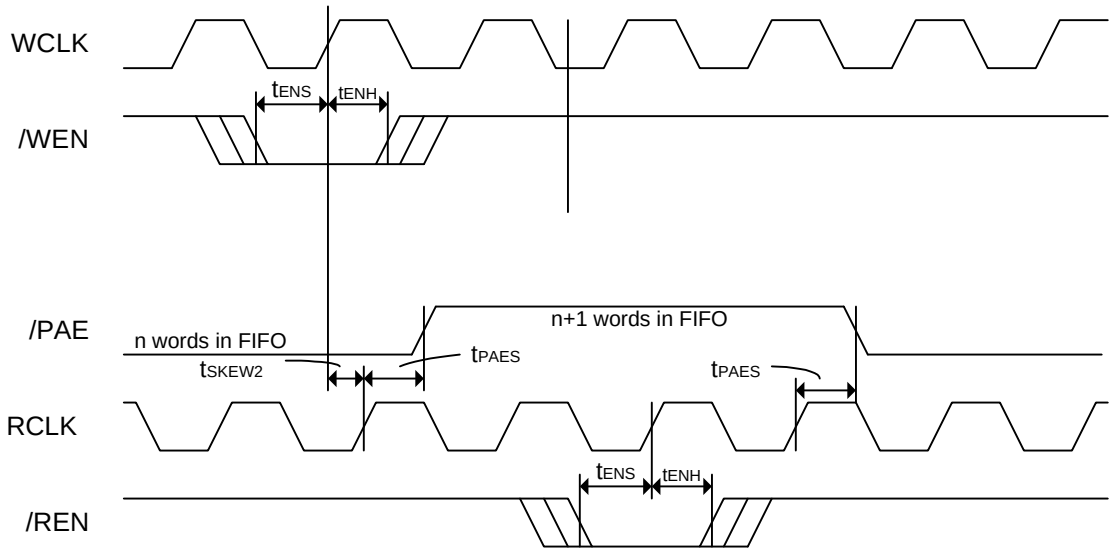


Figure 10. Programmable Empty Flag Timing

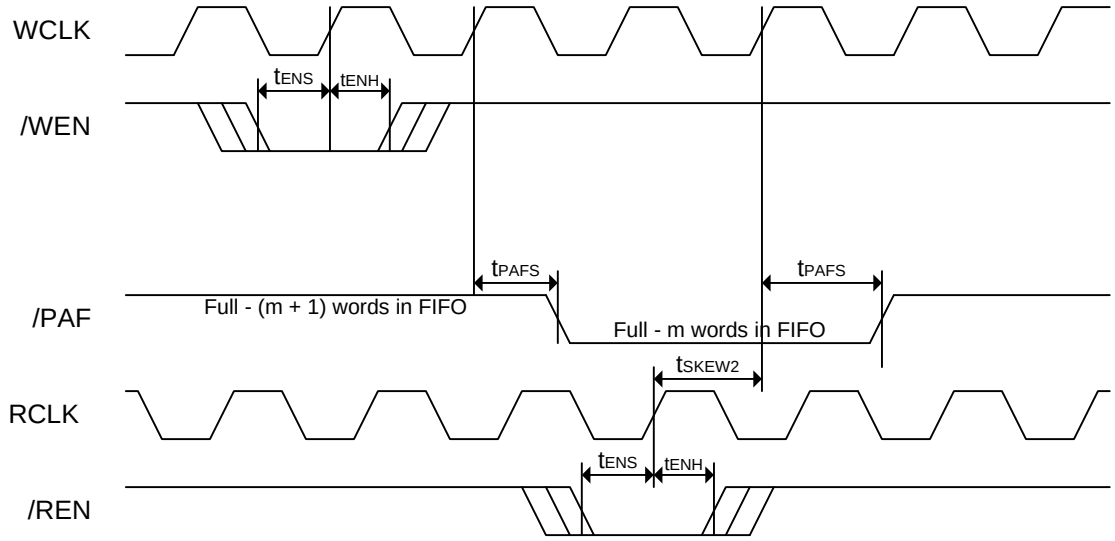
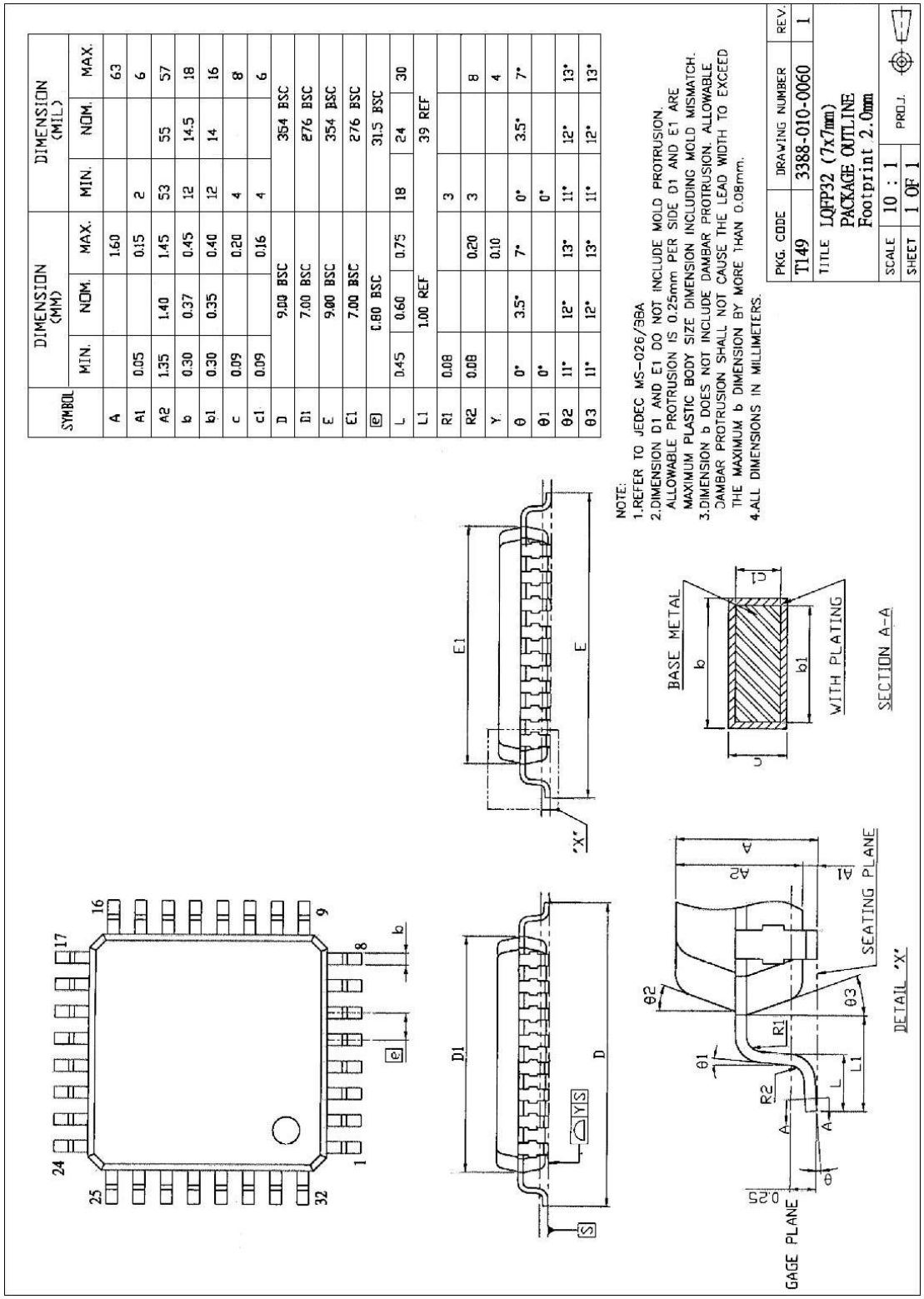


Figure 11. Programmable Full Flag Timing

11.0 Mechanical Drawing

11.1 7x7mm 32-pin TQFP Package



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