AL4CE205
AL4CE215
AL4CE225
AL4CE235
AL4CE245

Data Sheets

Version 1.01

Amendments

01-04-02 Version 1.0

04-05-02 Update speed grade information

02-20-03 Company Contact Information updated

AL4CE205/AL4CE215/AL4CE225/AL4CE235 /AL4CE245 (256 x 18, 512 x18, 1k x 18, 2k x 18, 4k x 18) Enhanced Synchronous FIFO

Contents:

1.0 Description

The AL4CE205/AL4CE215/AL4CE225/AL4CE235/AL4CE245 series products are high-performance, low-power 18bit read/write synchronous FIFO (First-In-First-Out) memory chips. They are specially designed to buffer high speed streaming data for a wide range of multimedia and communication applications, such as optical disk controllers, Local Area Networks (LANs), SONET (Synchronous Optical Network).

The input data is synchronous with a free-running clock (WCLK), and an input enable pin (/WEN). Data is written into the FIFO on every write clock when /WEN is low. The output data is synchronous with the other free-running clock (RCLK) and enable pin (/REN). Data is read out from the FIFO on every read clock when both /REN and /OE are low. An Output Enable pin (/OE) can control the output port becoming tri-state. The FIFOs provide 3 fixed flags, Empty Flag<Output Ready> (/EF</OR>), Full Flag<Input Ready> (/FF/<IR>) and Half-Full flag (/HF), and two programmable flags, Almost-Empty (/PAE) and Almost-Full (/PAF). The offsets of the /PAE and /PAF flags are loaded when Load pin (/LD) goes low. A Half-Full flag (/HF) is available in a single device configuration.

Bus-Matching feature can flexibly configure input and output bus width. The chip can automatically convert the input data bus width to match up output data bus width by packing or unpacking the data. A Big-Endian/Little-Endian data word format is provided to invert the read-in bytes sequence for output. And the Retransmit function allows data to be reread from the FIFO more than once.

2.0 Features

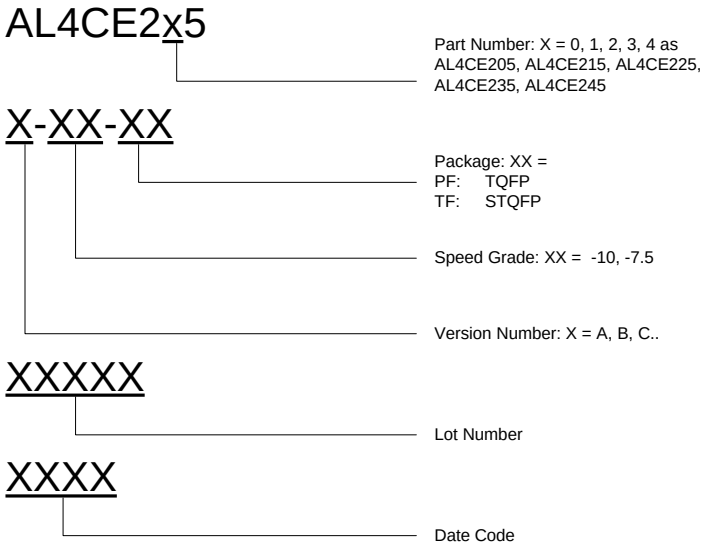
- 256 x18-bit memory array (AL4CE205)
- 512 x18-bit memory array (AL4CE215)
- 1,024 x18-bit memory array (AL4CE225)
- 2,048 x18-bit memory array (AL4CE235)
- 4,096 x18-bit memory array (AL4CE245)
- 133 MHz Operation
- 7.5 ns read/write cycle time
- Independent Read and Write operations
- Retransmit the data (reread the data)
- User selectable input and output bus width
  - x9 in to x9 out
  - x9 in to x18 out
  - x18 in to x19 out
  - x18 in to x18 out
- Big-Endian/Little-Endian word format selectable
- Double register-buffered Empty and Full flags
- Programmable Almost-Empty and Almost-Full flags
- Half-Full flag
- Output enable (data skipping)
- 3.3V power supply with 5V input tolerant
- Available in a 64-lead thin quad flat pack (TQFP/STQFP)

3.0 Applications

- Routers
- ATM switches
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- Time base correction (TBC)

4.0 Chip Information

4.1 Marking Information



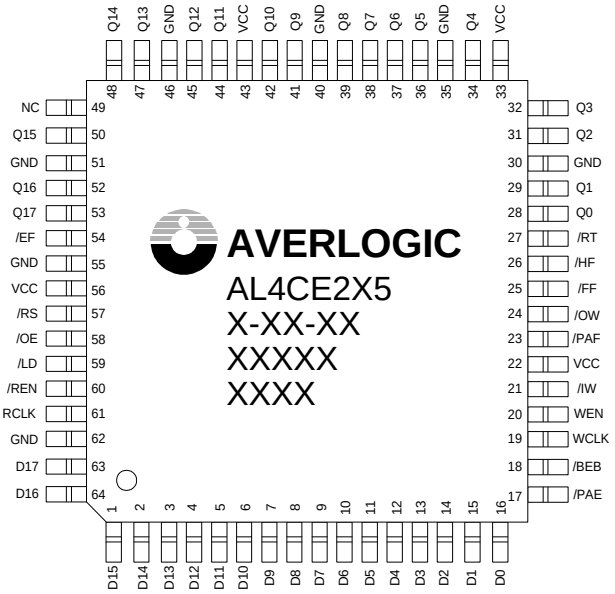
4.2 Ordering Information

Two packages are available for AL4CE205/AL4CE215/AL4CE225/AL4CE235/AL4CE245.

Part number	Package	Power Supply	Status
AL4CE205/215/225/235/245 (A-7.5-PF)	64-pin plastic TQFP(14x14mm)	+3.3V±10%	Sample in Nov.,2001
AL4CE205/215/225/235/245 (A-7.5-TF)	64-pin plastic STQFP(10x10mm)	+3.3V±10%	Sample in Nov., 2001

5.0 Pin Diagram

The AL4CE205/AL4CE215/AL4CE225/AL4CE235/AL4CE245 pin-out diagram is following:



TQFP, STQFP PACKAGE TOP VIEW

6.0 Block Diagram

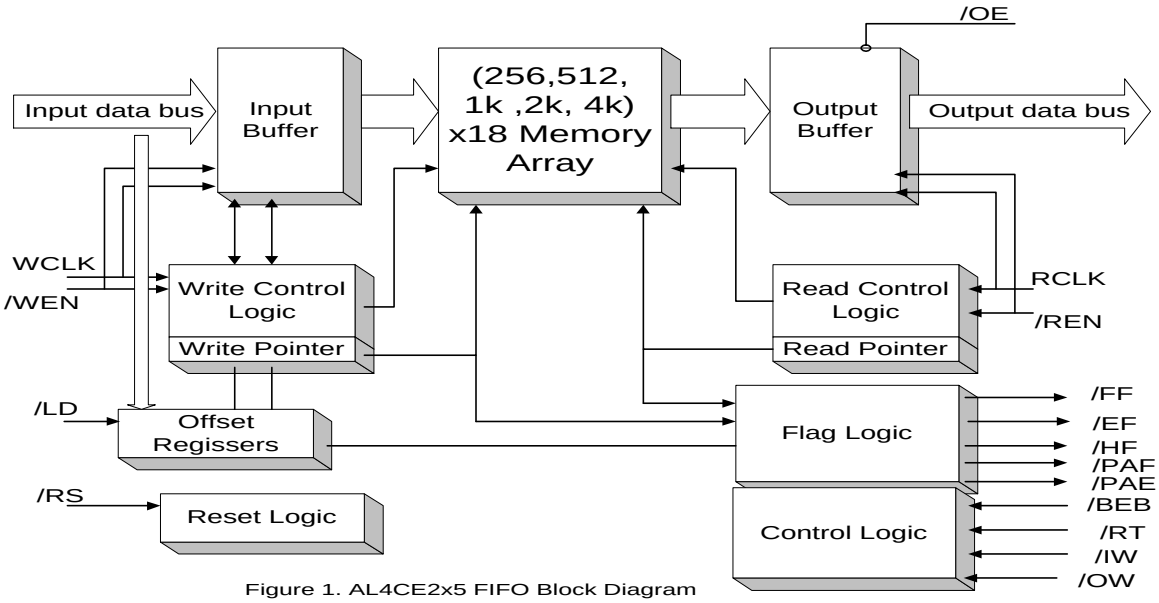


Figure 1. AL4CE2x5 FIFO Block Diagram

The internal structure of the AL4CE205/AL4CE215/AL4CE225/AL4CE235/AL4CE245 consists of Input/Output buffers, Read/Write Control Logic and main (256, 512, 1k, 2k, 4k) x18 configuration

memory array and state-of-the-art logic design that takes care of addressing and controlling the read/write data.

7.0 Pin Definition and Description

The pin-out definition and function are described as following:

Write Bus Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
D[17:0]	Data Inputs	63,64, [1:16]	I	18-bit or 9-bit Input data bus. During Reset, if IW is LOW, the Input port will be configured to 18-bit mode and D17 ~ D0 are used. If IW is HIGH, the Input port will be configured to 9-bit mode and D8 ~ D0 are used.
/WEN	Write Enable	20	I	When /WEN is LOW, data is written into the FIFO on every rising edge of WCLK. When /WEN is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the /FF is LOW.
WCLK	Write Clock	19	I	When /WEN is LOW, data is written into the FIFO on a rising edge of WCLK, if the FIFO is not full.

Read Bus Signals

Pin symbol	Pin name	Pin number	I/O type	Description
Q[17:0]	Data Outputs	53,52,50,48, 47,45,44,42, 41,39,38,37, 36,34,32,31, 29,28	O	18-bit or 9-bit Output data bus. During Reset, if OW is LOW, the Output port will be configured to 18-bit mode and Q17 ~ Q0 are used. If IW is HIGH, the Output port will be configured to 9-bit mode and Q8 ~ Q0 are used.
/REN	Read Enable	60	I	When /REN is LOW, data is read from the FIFO on every rising edge of RCLK. When /REN is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the /EF is LOW.
/OE	Output Enable	58	I	When /OE is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in high-impedance.
RCLK	Read Clock	61	I	When /REN is LOW, data is read from the FIFO on a rising edge of RCLK, if the FIFO is not empty.

Miscellaneous & Flags Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
/RS	Reset	57	I	When /RS is set LOW, internal read and write pointers are set to the first location of the RAM array, /FF and /PAF go HIGH, and /PAE and /EF go LOW. A reset is required before an initial WRITE after power-up.
/LD	Load	59	I	When /LD is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the rising edge of the WCLK, when /WEN is LOW. When /LD is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the rising edge of the RCLK, when /REN is LOW.
/BEB	Big-Endian /Little-Endian	18	I	During Reset, a LOW on /BEB will select Big-Endian operation. A HIGH on /BEB during Reset will select Little-Endian format
IW	Input Bus Width	21	I	This pin is to configure the bus width of the write port. During Reset, the write port will be configured to x18 bus width if IW is LOW and to x9 bus width if IW is HIGH.
OW	Output Bus Width	24	I	This pin is to configure the bus width of the read port. During Reset, the read port will be configured to x18 bus width if OW is LOW and to x9 bus width if OW is HIGH.
/FF	Full Flag	25	O	/FF indicates whether or not the FIFO memory is full.
/EF	Empty Flag	54	O	/EF indicates whether or not the FIFO memory is empty.
/PAE	Programmable Almost-Full Flag	17	O	When /PAE is LOW, the FIFO is Almost-Empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for AL4CS, 63 from empty for AL4CE215 and 127 from empty for AL4CE225/235/245.
/PAF	Programmable Almost-Full Flag	23	O	When /PAF is LOW, the FIFO is almost –full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for AL4CE205, 63 from full for AL4CE215 and 127 from full for AL4CE225/235/245.
/HF	Half-Full Flag	26	O	When data are buffered more than half full /HF flag will go LOW.
/RT	Retransmit	27	I	/RT asserted on the rising edge of RCLK initialized the READ pointer to zero, sets the /EF flag to LOW and does not affect the write pointer, programming

				method, existing timing mode or programmable flag settings.

Power/Ground Signals

Pin Symbol	Pin name	Pin number	I/O type	Description
VCC	Power	22,33,43,56	-	3.3V ± 10% power supply.
GND	Ground	30,35,40,46 ,51,55,62	-	Ground.
NC	-	49	-	No Connect.

8.0 Function Description

8.1 Operating Timing

The AL4CE205/215/225/235/245 data Write/Read is controlled by clock, enable and reset signals respectively. A write operation, which consists of a LOW Write-Enable (/WE) and a rising Write-Clock (WCLK) edge, will write the word from input port to the internal memory. A read operation, which consists of a LOW Read-Enable (/REN) and a rising Read-Clock (RCLK) edge, will load the word from internal memory to the data output port.

8.2 Flags Status

The behavior of status flags, /FF, /PAF, /HF, /PAE, and /EF refer to the Table 1.

Table 1: Status Flags

/FF	/PAF	/HF	/PAE	/EF	AL4CE205	AL4CE215	AL4CE225	AL4CE235	AL4CE245
H	H	H	L	L	0	0	0	0	0
H	H	H	L	H	1~n	1~n	1~n	1~n	1~n
H	H	H	H	H	(n+1)~128	(n+1)~256	(n+1)~512	(n+1)~1024	(n+1)~2048
H	H	L	H	H	129~(256-(m+1))	257~(512-(m+1))	513~(1024-(m+1))	1025~(2048-(m+1))	2049~(4096-(m+1))
H	L	L	H	H	(256-m)~255	(512-m)~511	(1024-m)~1023	(2048-m)~2047	(4096-m)~4095
L	L	L	H	H	256	512	1024	2048	4096

Notes:
1. n = Empty Offset (Default: 31 for AL4CE205, 63 for AL4CE215 and 127 for AL4CE225/235/245.
2. m = Full Offset (Default: 31 for AL4CE205, 63 for AL4CE215 and 127 for AL4CE225/235/245.

Data at input port, D[17:0], will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK) when Write Enable (/WEN) is LOW. The Empty Flag (/EF) will go HIGH after the first write. The Programmable Almost-Empty flag (/PAE) will go HIGH after n + 1 words have been written into the FIFO, where n is the preset empty offset value. The value of empty offset for each

chip is user programmable and the default value is remarked in the footnote of Table1. When the unread data accumulated to haft way of the total FIFO size, the Half-Full Flag (/HF) would toggle to LOW once the 129th (AL4CE205), 257th (AL4CS 215), 513th (AL4CS 225), 1,025th (AL4CS 235), and 2,049th (AL4CS 245) word respectively was written into the FIFO. Continuing to write data into the FIFO will cause the Programmable Almost-Full Flag (/PAF) to go LOW. Again, if no reads are performed, the /PAF will go LOW after (256-m) writes for the AL4CE205, (512-m) writes for the AL4CE215, (1,024-m) writes for the AL4CE225, (2,048-m) writes for the AL4CE235 and (4,096–m) writes for the AL4CE245. The offset "m" is the full offset value. This parameter is also user programmable. If there is no full offset specified, the /PAF will go LOW when the device is 31 away from completely full for the AL4CE205, 63 for the AL4CE215, and 127 for the AL4CE225/235/245. When the FIFO is full, the Full Flag (/FF) will go LOW to prevent further write operations. If no reads are performed after a reset, /FF will go LOW after D writes to the FIFO. D = 256 writes for the AL4CE205, 512 for the AL4CE215, 1,024 for the AL4CE225, 2,048 for the AL4CE235 and 4,096 for the AL4CE245, respectively.

If the FIFO is full, the first read operation will cause /FF to go HIGH. Likewise, subsequent read operations will cause /PAF and the Half-Full Flag (/HF) to go HIGH at the conditions described in Table 1. If further read operations occur, without write operations, the Programmable Almost-Empty Flag (/PAE) will go LOW when there are n words in the FIFO, where n is the empty offset value. If there is no empty offset specified, the /PAE will be LOW when the device is 31 away from completely empty for AL4CE205, 63 for AL4CE215, and 127 for AL4CE225/235/245. Continuing read operations will cause the FIFO to be empty.

8.3 Programmable Flag Loading

Full and Empty flag offset values for the AL4CE205/ 215/225/235/245 are user programmable and are stored into the internal registers. Default settings are stated in the footnotes of Table 1 and Table 2. Offset values are loaded into the FIFO using the data input lines D0-D11. To load the offset registers, the Load (/LD) pin and /WEN pin must be kept LOW. Data present on D0-D11 will be transferred into the Empty Offset register on the first rising edge of WCLK. By continuing to hold the /LD and /WEN pin low, data present on D0-D11 will be transferred into the Full Offset register on the next rising edge of the WCLK. The third rising edge of WCLK again writes to the Empty Offset register. Writing all offset registers does not have to occur consecutively. The FIFO can be returned to normal read/write operation by bringing the /LD pin HIGH after one or two offset registers being programmed. When the /LD pin and /WEN are again set LOW, the next offset register in sequence is programmed.

The contents of the offset registers can be read back on the data output lines Q0-Q11 when the /LD pin is set LOW and /REN is set LOW. Data can then be read on the next rising edge of RCLK. The first transition of RCLK will present the empty offset value to the data output lines and full offset value is the next.

8.5 Register-Buffered Flag and Synchronous Programmable Flag Timing

The AL4CE205/215/ 225/235/245 support Double Register-Buffered Empty/Full Flags and Synchronous timing for /PAE and /PAF flags. In Synchronous timing mode, the /PAE is asserted and

updated on the rising edge of RCLK. Likewise, /PAF is asserted and updated on the rising edge of WCLK. For detail operation timing, please refer timing diagram.

9.0 Memory Operations:

9.1 Inputs and Outputs:

9.1.1 Data Input (D17 – D0)

D17 ~ D0 are 9-bit or 18-bit wide of input data port. During Reset, if IW is LOW, the Input port will be configured to 18-bit mode and D17 ~ D0 are used. If IW is HIGH, the Input port will be configured to 9-bit mode and D8 ~ D0 are used.

9.1.2 Data Outputs (Q17-Q0)

Q0-Q17 are data outputs for 18-bit wide data. During Reset, if OW is LOW, the Output port will be configured to 18-bit mode and Q17 ~ Q0 are used. If IW is HIGH, the Output port will be configured to 9-bit mode and Q8 ~ Q0 are used.

9.2 Controls:

9.2.1 Reset (/RS)

Reset is asserted whenever the Reset (/RS) input becomes LOW. During reset, both internal read and write pointers are reset to the first location. A reset is required after power-up before a write operation can take place. The Half-Full Flag (/HF) and Programmable Almost-Full Flag (/PAF) will be reset to HIGH after t_{RSF}. The Programmable Almost-Empty Flag (/PAE) will be reset to LOW after t_{RSF}. The Full Flag (/FF) will reset to HIGH. The Empty Flag (/EF) will reset to LOW. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

9.2.2 Write Clock (WCLK)

A write cycle is initiated on the rising edge of the Write Clock (WCLK). Data setup and hold times must be met with respect to the rising edge of WCLK. The Write and Read Clocks can be asynchronous or coincident.

9.2.3 Write Enable (/WEN)

When the /WEN input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the memory array sequentially and independently of any ongoing read operation. When /WEN is HIGH, no new data is written in the memory array on each WCLK cycle. To prevent data overflow, /FF will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, /FF will go HIGH allowing a write to occur. The /FF flag is updated on the rising edge of WCLK. /WEN is ignored when the FIFO is full.

9.2.4 Read Clock (RCLK)

Data can be read on the outputs on the rising edge of the Read Clock (RCLK), when Output Enable (/OE) is set LOW. The Write and Read Clocks can be asynchronous or coincident.

9.2.5 Read Enable (/REN)

When Read Enable (/REN) is LOW, data is loaded from the memory array into the output register on the rising edge of every RCLK cycle if the device is not empty. When the /REN input is HIGH, the

output register holds the previous data and no new data is loaded into the output register. The data outputs Q0-Q17 maintain the previous data value.
Every word accessed at output port, including the first word written to an empty FIFO, must be requested using /REN. When the last word has been read from the FIFO, the Empty Flag (/EF) will go LOW, inhibiting further read operations. /REN is ignored when the FIFO is empty. Once a write is performed, /EF will go HIGH allowing a read to occur. The /EF flag is updated on the rising edge of RCLK.

9.2.6 Output Enable (/OE)

When Output Enable (/OE) is enabled (LOW), the parallel output buffers receive data from the output register. When /OE is disabled (HIGH), the Q output data bus is in a high-impedance state.

9.2.7 Load (/LD)

The AL4CE205/4CS215/4CS225/4CS235/4CS245 devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load (/LD) pin is set LOW and /WEN is set LOW, data on the inputs D0-D11 is written into the Empty Offset register on the first rising edge of the Write Clock (WCLK). When the /LD pin and /WEN are held LOW then data is written into the Full Offset register on the second rising edge of WCLK. The third transition of WCLK again writes to the Empty Offset register. However, the offset registers programming does not have to occur consecutively. The FIFO can be returned to normal read/write operation by bringing the /LD pin HIGH after one or two offset registers being programmed. When the /LD pin is set LOW, and /WEN is LOW again, the next offset register in sequence is programmed.

Empty Offset Register:

17 .. 12	11 .. 0
No use	Offset value

Note: Default value are 001Fh for AL4CE205, 003Fh for AL4CE215, 007Fh for AL4CE225/AL4CE235/AL4CE245. Any bits of the offset register not being programmed should be set to zero.

Full Offset Register:

17 .. 12	11 .. 0
No use	Offset value

Note: Default value are 001Fh for AL4CE205, 003Fh for AL4CE215, 007Fh for AL4CE225/AL4CE235/AL4CE245. Any bits of the offset register not being programmed should be set to zero.

When the /LD pin is LOW and /WEN is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write. The contents of the offset registers can be read on the output lines when the /LD pin is set LOW and /REN is set LOW; then, data can be read on the rising edge of the Read Clock (RCLK). The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently). Offset register content can be read out, but a read and a write should not be performed simultaneously to the offset registers.

9.2.8 Big-Endian/Little-Endian (/BEB)

During Reset, a LOW on /BEB will select Big-Endian operation. A HIGH on /BEB during Reset will select Little-Endian format. If Big-Endian mode is selected, the most significant byte of the word written into the FIFO will be read out of the FIFO first, followed by the least significant byte. If Little0Endian format is selected, the least significant byte of the word written into the FIFO will be read out first, followed by the most significant byte.

9.2.9 Input Bus Width (IW)

This pin is to configure the bus width of the write port. During Reset, the write port will be configured to x18 bus width if IW is LOW and to x9 bus width if IW is HIGH.

9.2.10 Output Bus Width (OW)

This pin is to configure the bus width of the read port. During Reset, the read port will be configured to x18 bus width if OW is LOW and to x9 bus width if OW is HIGH.

Table 2: Bus-Matching and Endian Support Configuration

IW	OW	/BEB	Input Bus		Output		Configuration
			D17 ~ D9	D8 ~ D0	Q17 ~ Q9	Q8 ~ Q0	
L	L	L	A	B	A	B	x18 Input to x18 Output – Big Endian
L	L	H	A	B	B	A	x18 Input to x18 Output – Little Endian
L	H	L	A	B	X	A (1^{ST}) B (2^{ND})	x18 Input to x9 Output – Big Endian
L	H	H	A	B	X	B (1^{ST}) A (2^{ND})	x18 Input to x9 Output – Little Endian
H	L	L	X	A (1^{ST}) B (2^{ND})	A	B	x9 Input to x18 Output – Big Endian
H	L	H	X	A (1^{ST}) B (2^{ND})	B	A	x9 Input to x18 Output – Little Endian

Notes: In x9 in to x9 output configuration, Big-Endian/Little-Endian (/BEB) does not affect byte sequence.

9.2.11 Retransmit (/RT)

The Retransmit operation can do multiple data read. The Retransmit operation occurs when a /RT low is sampled at the rising edge of the RCLK. The read pointer will be reset to first location of the memory and /EF will be brought to low (if /EF was HIGH before setup), and then the data can be read out from the memory, starting at the beginning of the memory.

9.3 Flags Control:

9.3.1 Full Flag (/FF)

When the FIFO is full, /FF will go LOW, inhibiting further write operations. When /FF is HIGH, the FIFO is not full. If no reads are performed after a reset, /FF will go LOW after D writes to the FIFO where D = 256 writes for the AL4CE205, 512 for the AL4CE215, 1,024 for the AL4CE225, 2,048 for

the AL4CE235 and 4,096 for the AL4CE245. /FF is synchronous and updated on the rising edge of WCLK.

9.3.2 Empty Flag (/EF)

When the FIFO is empty, /EF will go LOW, inhibiting further read operations. When /EF is HIGH, the FIFO is not empty. /EF is synchronous and updated on the rising edge of RCLK.

9.3.3 Programmable Almost-Full Flag (/PAF)

The Programmable Almost-Full Flag (/PAF) will go LOW when FIFO reaches the almost-full condition. If no read is occurred after Reset (/RS), the /PAF will go LOW after (256-m) writes for the AL4CE205, (512-m) writes for the AL4CE215, (1,024-m) writes for the AL4CE225, (2,048–m) writes for the AL4CE235 and (4,096–m) writes for the AL4CE245. The offset “m” is defined in the Full Offset register (refers Table 1 for “m” default values). The /PAF is updated on the rising edge of WCLK.

9.3.4 Programmable Almost-Empty Flag (/PAE)

The /PAE flag will go LOW when the FIFO reaches the almost-empty condition. The /PAE will go LOW when there are “n” words or less in the FIFO. The offset "n" is defined as the empty offset. The default values for “n” are noted in Table 1. If there is no empty offset specified, the Programmable Almost-Empty Flag (/PAE) will be LOW when the device is 31 away from completely empty for AL4CE205, 63 away from completely empty for AL4CE215, and 127 away from completely empty for AL4CE225/4CS235/4CS245. The /PAE is updated on the rising edge of RCLK.

9.3.5 Half-Full Flag (/HF)

The /HF output acts as an indication of a half-full memory. After half of the memory is filled, and at the rising edge of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (/HF) is then reset to HIGH by the rising edge of the Read Clock (RCLK). The /HF is asynchronous.

11.0 Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage temperature	-40 ~ +125	°C

11.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V

11.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V Rating			Unit
		Min	Typ	Max	
I_{DD}	Operating Current @20MHz	-	-	25	mA
I_{DDS}	Standby Current	-	1	5	mA
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-2	-	+2	μA
I_{LO}	Output Leakage Current	-10	-	+10	μA

Note: The Operating Current is tested at RCLK=WCLK=20MHz and data inputs switch at 10Mhz

11.4 AC Electrical Characteristics

(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

		133Mhz		
Symbol	Parameter	Min	Max	Unit
t_S	Clock Cycle Frequency	-	133	MHz
t_A	Data Access Time	1	5	ns
t_{CLK}	Clock Cycle Time	7.5	-	ns
t_{CLKH}	Clock HIGH Time	3.5	-	ns
t_{CLKL}	Clock LOW Time	3.5	-	ns
t_{DS}	Data Setup Time	2.5	-	ns
t_{DH}	Data Hold Time	0.5	-	ns
t_{ENS}	Enable Setup Time	2.5	-	ns
t_{ENH}	Enable Hold Time	0.5	-	ns
t_{RS}	Reset Pulse Width	7.5	-	ns
t_{RSS}	Reset Setup Time	6	-	ns
t_{RSR}	Reset Recovery Time	6	-	ns
t_{RSF}	Reset to Flag and Output Time	-	9	ns
t_{OLZ}	Output Enable to Output in Low-Z	0	-	ns
t_{OE}	Output Enable to Output Valid	-	5	ns
t_{OHZ}	Output Enable to in High-Z	-	5	ns
t_{WFF}	Write Clock to Full Flag	-	5	ns
t_{REF}	Read Clock to Empty Flag	-	5	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	-	13	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	-	5	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	-	13	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	-	5	ns
t_{HF}	Clock to Half-Full Flag	-	13	ns
t_{XO}	Clock to Expansion Out	-	5	ns
t_{XI}	Expansion In Pulse Width	3	-	ns
t_{XIS}	Expansion In Set-Up Time	3	-	ns

t_{SKEW1}	Skew time between Read Clock & Write Clock for /FF</IR> & /EF</OR>	4	-	ns
T_{SKEW2}	Skew time between Read Clock & Write Clock for /PAE and /PAF	8	-	ns

11.5 Timing Diagrams

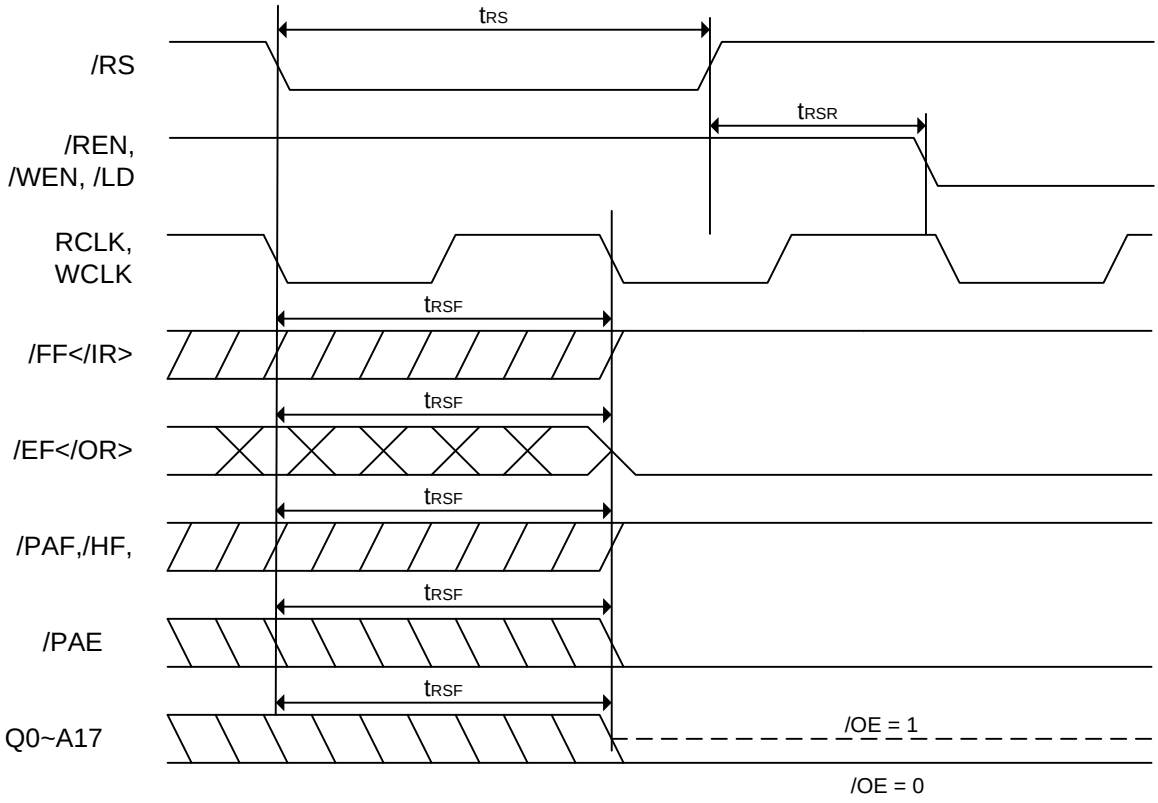


Figure 2. Reset Timing

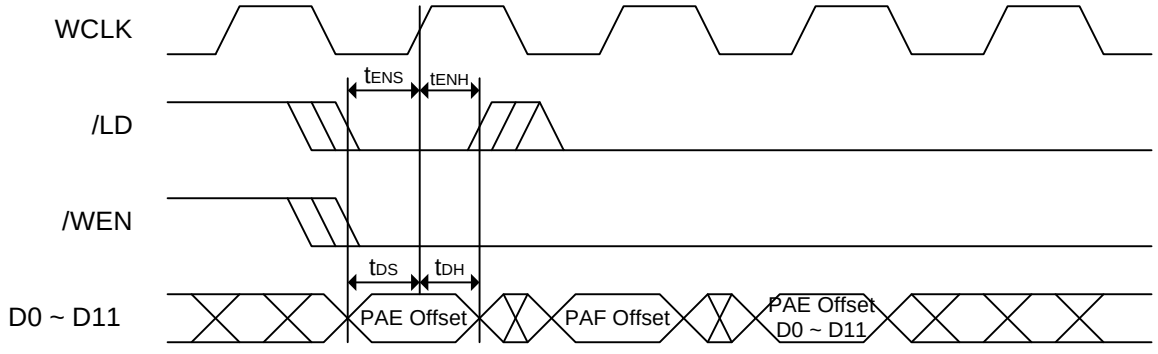


Figure 3. Write Programmable Registers

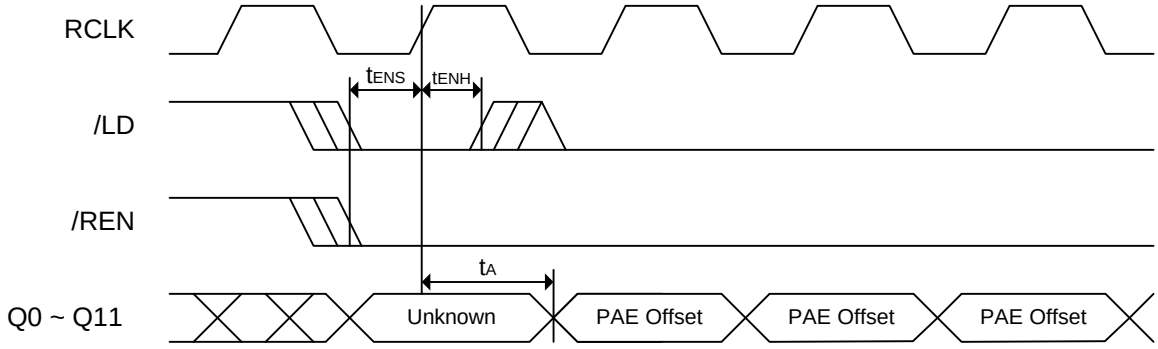


Figure 4. Read Programmable Registers

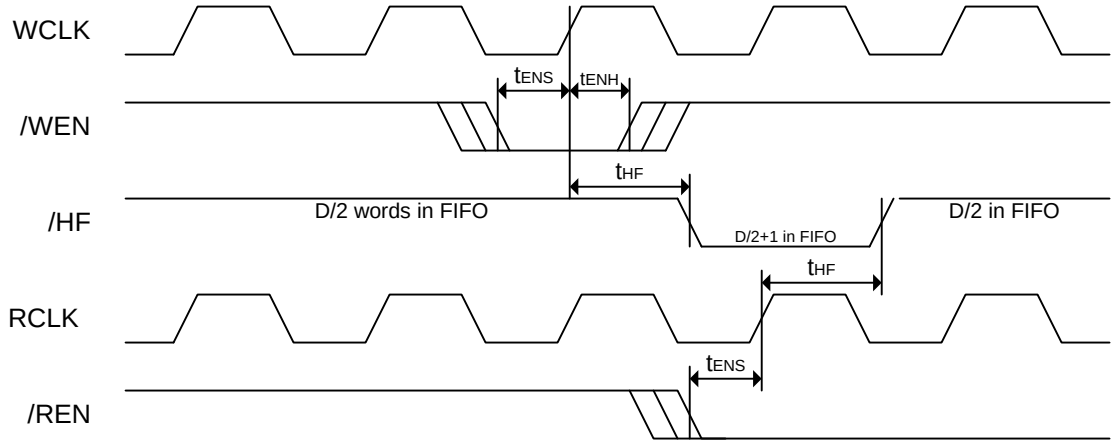


Figure 5. Half-Full Flag Timing

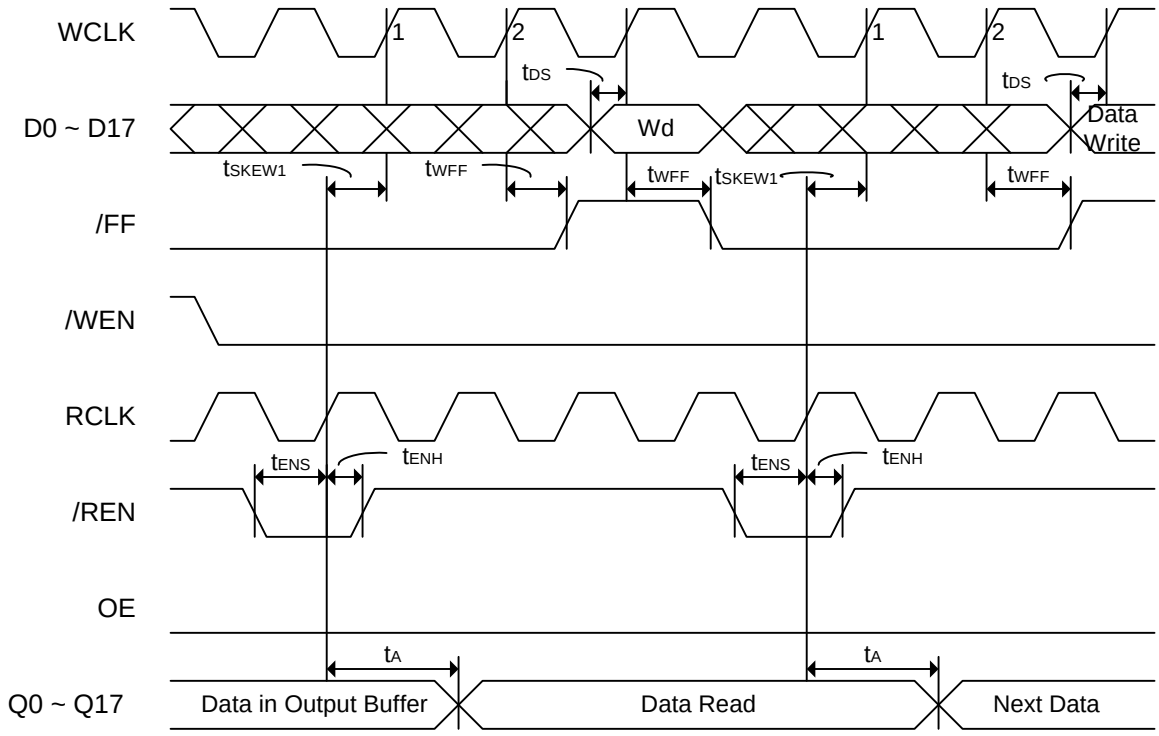


Figure 6. Double Register-Buffered Full Flag Timing

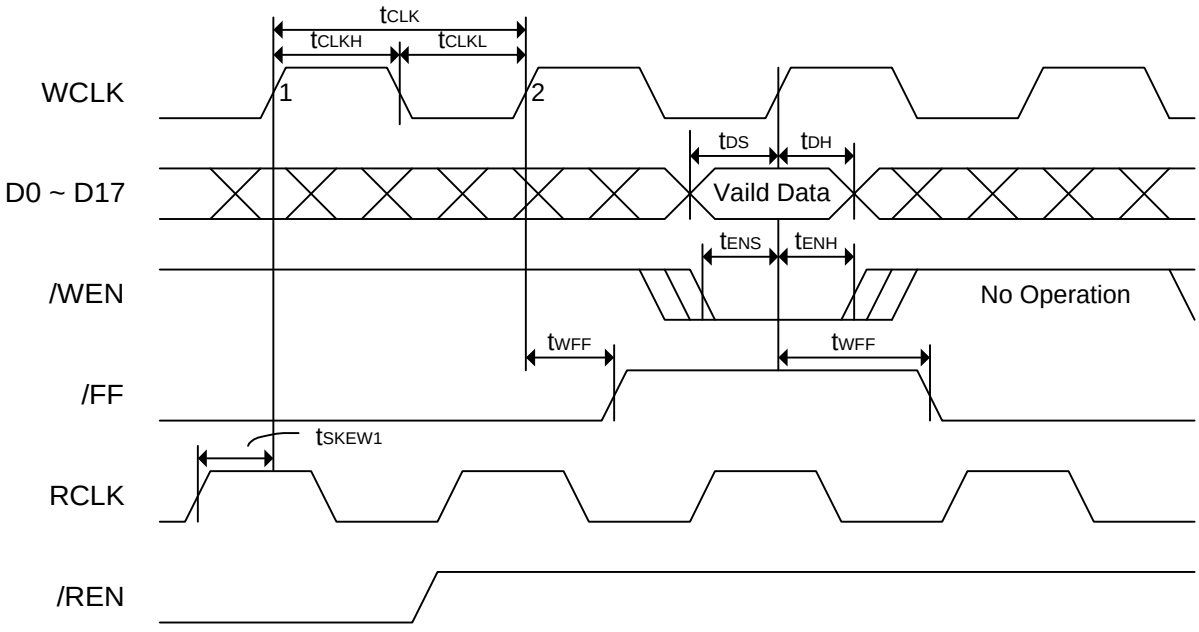


Figure 7. Write Cycle Timing with Double Register-Buffered /FF

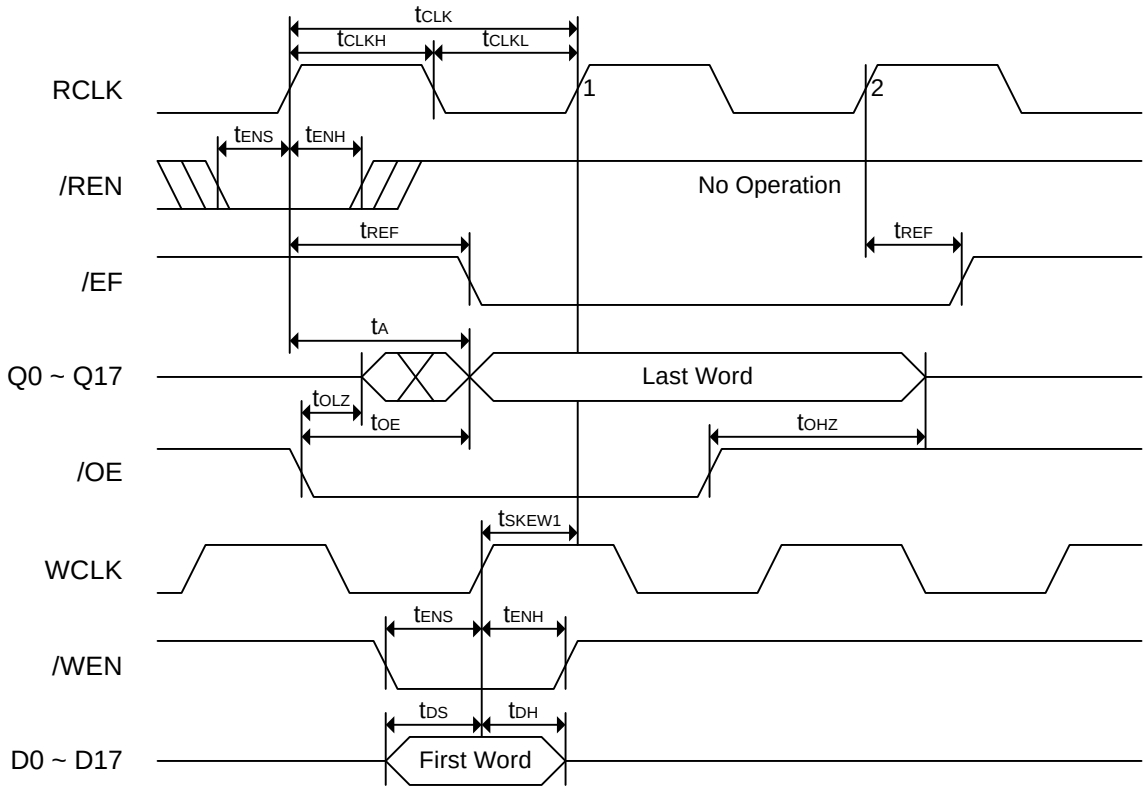


Figure 8. Read Cycle Timing with Double Register-Buffered /EF

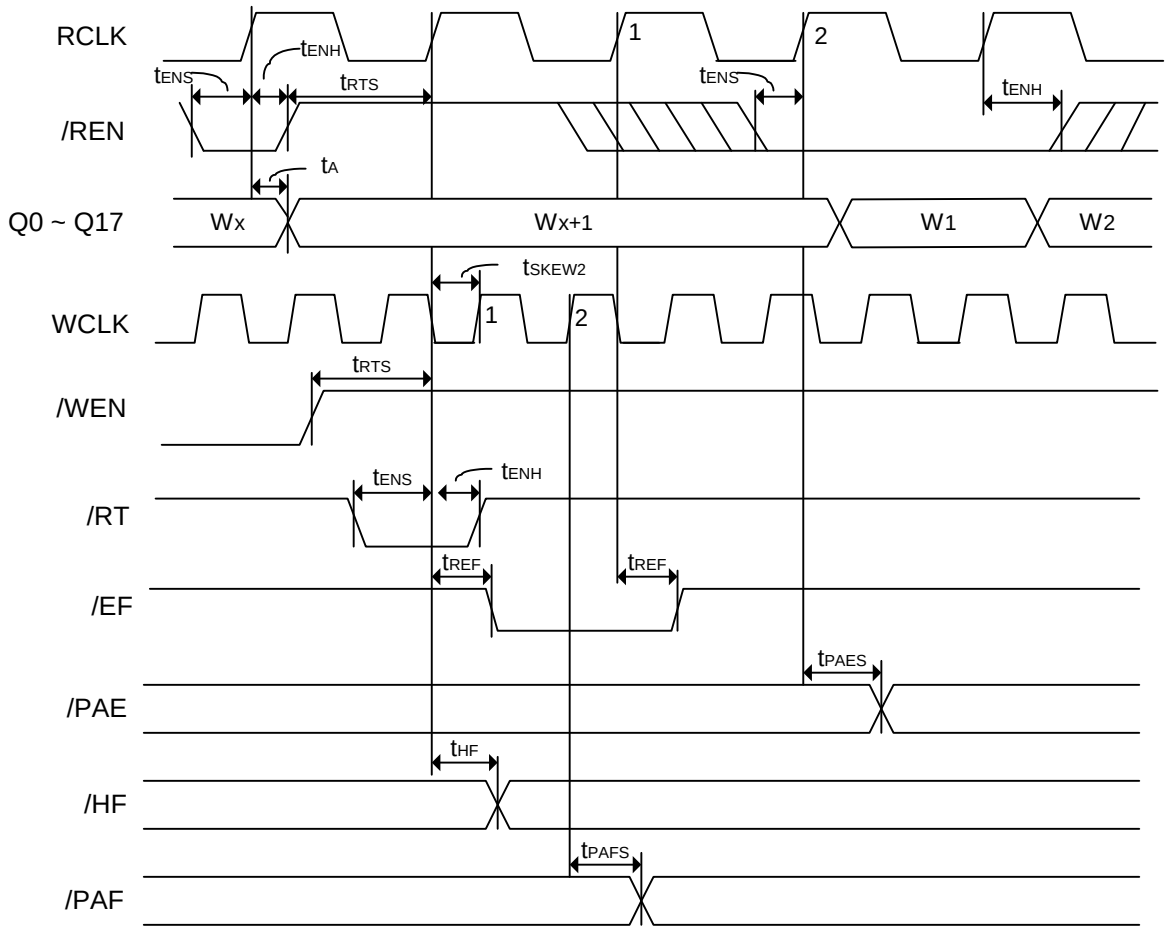


Figure 9. Retransmit Timing

12.0 Mechanical Drawing

12.1 10x10mm 64-Pin STQFP Package

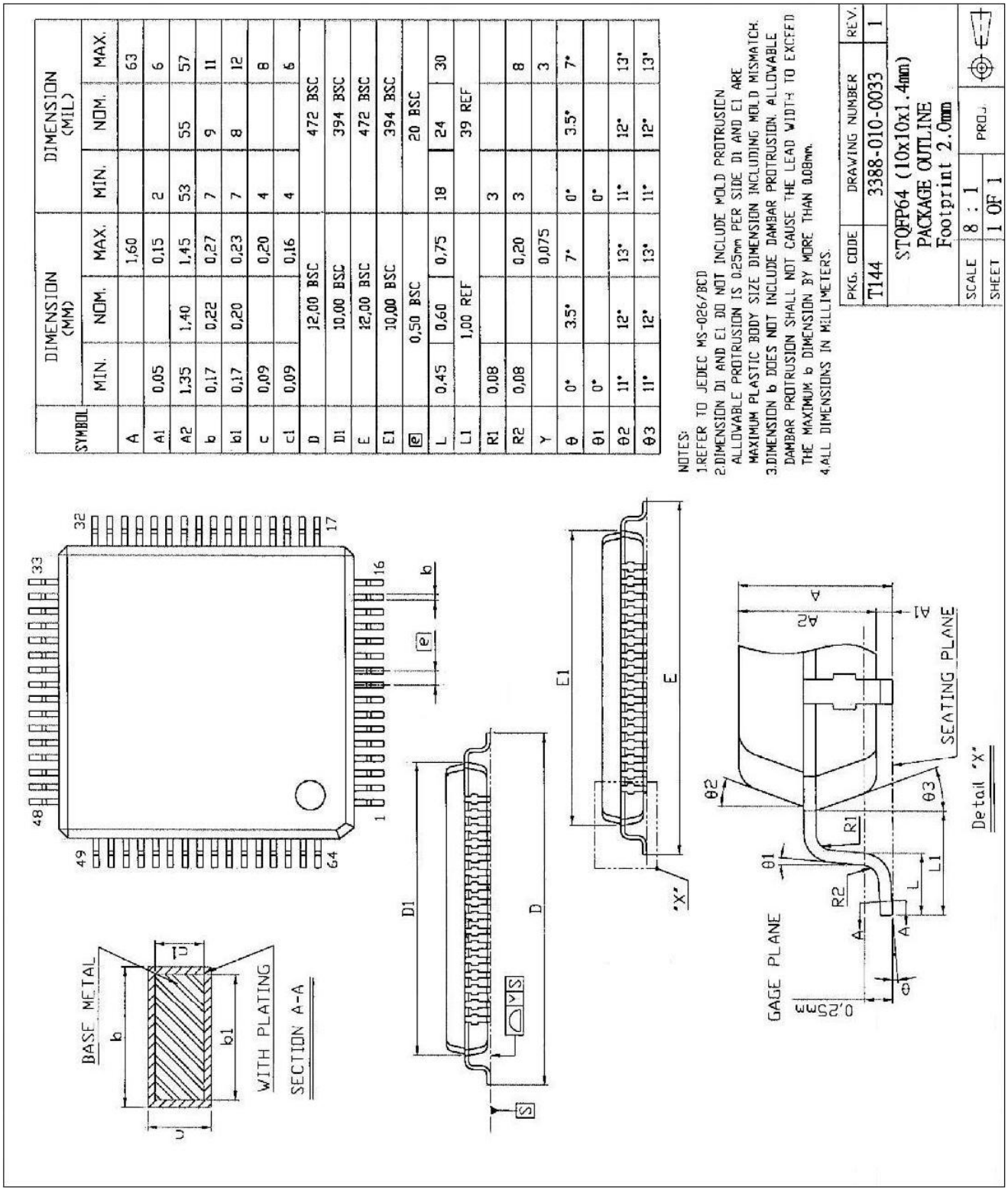
SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1,60			63
A1	0,05		0,15	2		6
A2	1,35	1,40	1,45	53	55	57
b	0,17	0,22	0,27	7	9	11
b1	0,17	0,20	0,23	7	8	12
c	0,09		0,20	4		8
c1	0,09		0,16	4		6
D		12,00 BSC			472 BSC	
D1		10,00 BSC			394 BSC	
E		12,00 BSC			472 BSC	
E1		10,00 BSC			394 BSC	
e		0,50 BSC			20 BSC	
L	0,45	0,60	0,75	18	24	30
L1		1,00 REF			39 REF	
R1	0,08			3		
R2	0,08		0,20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTES:
1.REFER TO JEDEC MS-026/BCD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

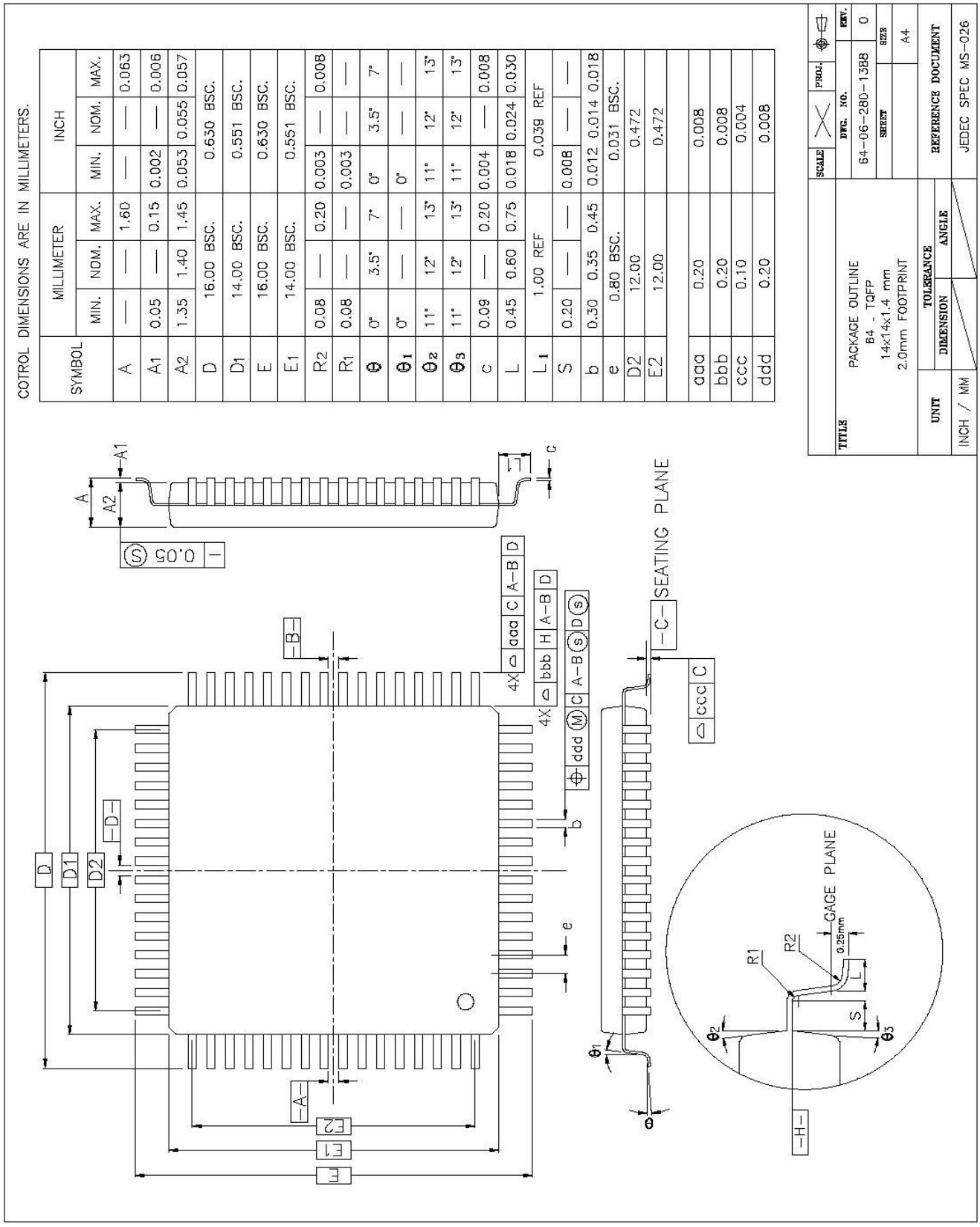
PKG. CODE	DRAWING NUMBER	REV.
T144	3388-010-0033	1

STQFP64 (10x10x1.4mm)
PACKAGE OUTLINE
Footprint 2.0mm

SCALE 8 : 1 PROJ.
SHEET 1 OF 1



12.2 14x14mm 64-pin TQFP Package



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC.			0.031 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.20			0.008		

TITLE: PACKAGE OUTLINE 64 - TQFP 14x14x1.4 mm 2.0mm FOOTPRINT
SCALE: X
PROJ.
DWG. NO.: 64-06-280-1388
REV.: 0
SHEET
SIZE: A4
UNIT: INCH / MM
TOLERANCE: DIMENSION, ANGLE
REFERENCE DOCUMENT: JEDEC SPEC MS-026

CONTACT INFORMATION

Averlogic Technologies Corp.
4F, No. 514, Sec. 2, Cheng Kung Rd., Nei-Hu Dist., Taipei, Taiwan
Tel: +886 2-27915050
Fax: +886 2-27912132
E-mail: sales@averlogic.com.tw
URL: http://www.averlogic.com.tw

Averlogic Technologies, Inc.
90 Great Oaks Blvd. #204, San Jose, CA 95119
USA
Tel: 1 408 361-0400
Fax: 1 408 361-0404
E-mail: sales@averlogic.com
URL: http://www.averlogic.com