Features

- **All Functions and Channel Selections are Controlled by Serial Bus**

RF Part

- **All Oscillators and PLL Integrated**
- **IF Converter**
- **FM Demodulator**
- **RSSI**

Low Frequency Part

- **Asymmetrical Input of Microphone Amplifier**
- **Asymmetrical Output of Earpiece Amplifier**
- **Compander**
- **Power Supply Management**
- **Serial Bus**

Application

- **CT0 Standard**
- **Narrowband Voice and Data Transmitting/Receiving Systems**

Description

The programmable single-chip multichannel cordless phone IC includes all necessary low frequency parts such as microphone- and earphone amplifier, compander, power-supply management as well as all RF parts such as IF converter, FM demodulator, RSSI, oscillators and PLL. Several gains and mutes in transmit and receive direction are controlled by the serial bus. The compander can be bypassed.

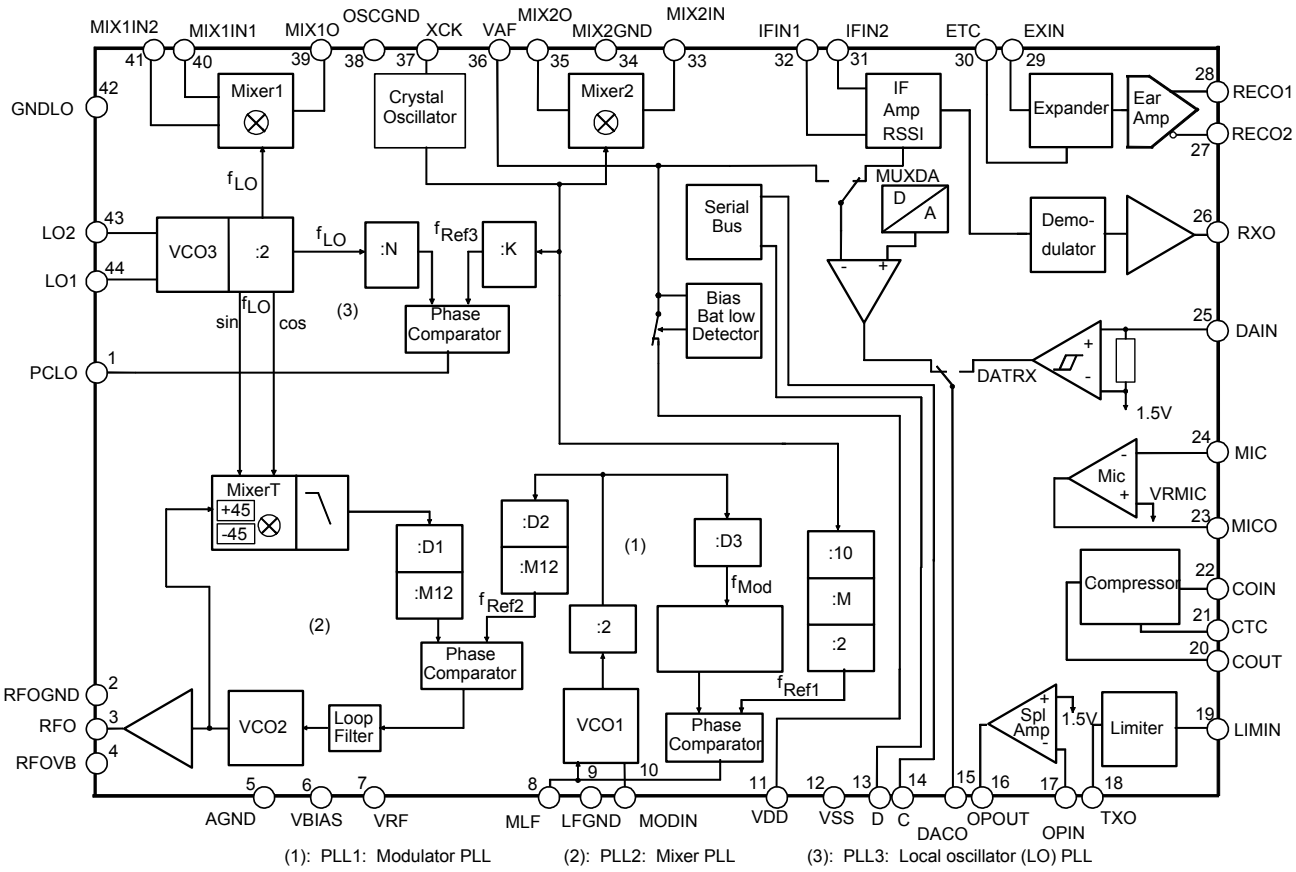
Single-chip Cordless Telephone IC

U3600BM

Preliminary

Rev. 4516C–CT0–08/02

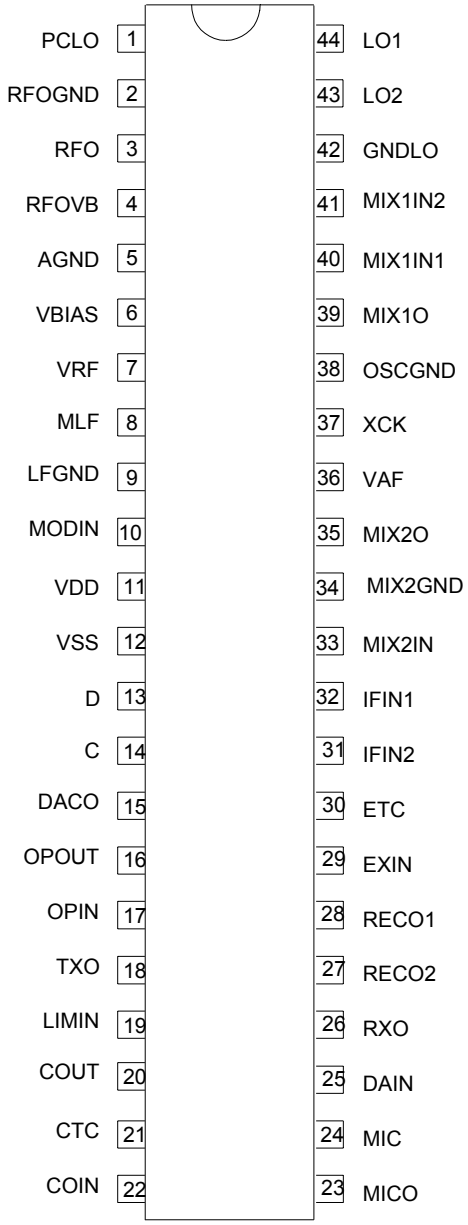
Figure 1. Block Diagram



(1): PLL1: Modulator PLL (2): PLL2: Mixer PLL (3): PLL3: Local oscillator (LO) PLL

Pin Configuration

Figure 2. Pinning SSO44



Pin Description

Pin	Symbol	Function
1	PCLO	Phase comparator local oscillator
2	RFOGND	RF transmit output ground
3	RFO	RF transmit output
4	RFOVB	Power supply input of RF transmit output buffer
5	AGND	Analog ground for RF part
6	VBIAS	Decoupling capacitor of current reference
7	VRF	Supply voltage for RF part
8	MLF	Modulator loop filter
9	LFGND	Modulator loop filter ground
10	MODIN	Modulator input
11	VDD	Supply voltage output for peripherals and internal supply of digital part
12	VSS	Ground for LF analog and digital
13	D	Data input of serial bus
14	C	Clock input of serial bus
15	DACO	D/A and data comparator output
16	OPOUT	Operational amplifier output
17	OPIN	Operational amplifier input (inverting)
18	TXO	Output of limiter amplifier
19	LIMIN	Limiter input
20	COUT	Compressor output
21	CTC	Compressor time constant control analog output
22	COIN	Compressor input
23	MICO	Microphone amplifier output
24	MIC	Inverting input of microphone amplifier
25	DAIN	Data comparator input
26	RXO	Output of demodulator
27	RECO2	Symmetrical output of receive amplifier
28	RECO1	
29	EXIN	Expander input
30	ETC	Expander time constant control analog output
31	IFIN2	Symmetrical input of IF amplifier
32	IFIN1	
33	MIX2IN	Input of Mixer2
34	MIX2GND	IF amplifier and Mixer2 ground
35	MIX2O	Mixer2 output
36	VAF	Supply voltage for AF/IF parts
37	XCK	Crystal oscillator input 11.15 MHz
38	OSCGND	Oscillator ground
39	MIX1O	Output of Mixer1
40	MIX1IN1	Symmetrical input of MIxer1
41	MIX1IN2	
42	GNDLO	Ground of LO
43	LO2	Tank elements for LO are connected to these pins
44	LO1	

System Description

Radio frequency IC for analog cordless telephone application in 26/50 MHz band (CTO standard). The IC performs full duplex communication. The transmitting and receiving frequency are depending on whether the IC is used in the handset or in the base station.

Frequency converter comprise an FM transmitter with switchable output power and first receiver mixer in the same unit. A two-wire bus interface can be used for the frequency control as well as for switching the transmitter power amplifier and the receiver. Fine frequency adjust of reference quartz oscillator is programmable.

The receive part is designed for a double conversion architecture. The incoming radio frequency signal will be filtered and amplified before reaching the first mixer. At this stage the RF signal will be converted down to the first intermediate frequency (10.7 MHz) by using a crystal oscillator (LO1).

The transmit part contains two PLL controlled VCOs. The frequency modulation is accomplished by super-posing the incoming audio signal on the PLL control voltage. Final frequency is a product of mixing VCO1 with first local oscillator of receiver part (VCO3). The FM modulated carrier is amplified by externals power amplifier before entering the output filter and the antenna connector.

Adjustments for VCO1 and VCO2

To be able to use a wide frequency range for the VCOs (i.e., VCO2 26.3 MHz to 49.9 MHz) the two internal VCOs (VCO1 and VCO2, i.e., the VCOs of the transmit part) have a rough adjust and a fine adjust to increase the frequency range given by the phase comparator.

The rough adjusts for these VCOs are correlated with the country setting. For every country there are two sets of VCO rough adjust settings, one for the base and one for the handset. See tables at channels frequencies and dividers.

To compensate the variation in production there is a fine adjust for each of the VCOs. The fine adjusts of the internal VCOs could be set manually (for test purposes) or set by the automatic mode. Theoretically the sign of the changing (increase/ decrease when the voltage of the phase comparator is to high) is selectable, but we need value 1 () in all cases.

Setting VCO1 (VCO2) under normal conditions:

EAFA1 (EAFA2) = 1, automatic fine adjust VCO1(VCO2) enabled
SAFA1 (SAFA2) = 1, sign of auto fine adjustment of VCO1 (VCO2) = 1.

Adjustment for VCO3

In order to increase the adjustment range of VCO3 with fixed external tank elements and/or for “band switching”, especially for US frequencies, VCO3 has programmable capacitors inside. These capacitors can be added by serial bus (FA3 [4:0]) between LO1 and LO2. There are 31 steps available, every step adding a capacitor of 0.5pF.

Speed-up of the Loop Filter of PLL1 (“Modulator PLL”)

To have a fast locking time for the modulator loop there is a precharge and a speed-up mode for the external loop filter.

During receive mode (VCO3 enabled, VCO1 disabled) the modulator loop filter is precharged to about half of the internally regulated 2.5 V charge-pump voltage.

During the first 30 ms after enabling VCO1 the modulator phase comparator is in speed-up mode. In this mode the current of the pase comparator which charges the loop filter is much larger than in normal mode. Additionally to the automatically switched 30 ms speed-up mode, the speed-up can be activated for any time by setting the bit SU1.

Speed-up of the Loop Filter of PLL3 (“1st. LO.”)

Similiar to PLL1, there is also a possibility to increase the locking speed of PLL3. This can be done by setting the bit SU3. Having done this, the charge pump at the output of the phase comparator has a bigger current capability and therefore charges the external capacitors faster.

Adjustment of the Modulator Gain

To fulfil the different requirements of the different countries three conversion gains of the modulator are selectable by the bits GMOD [1:0] (R6: D2, D3).

Country settings see tables at channel frequencies and dividers. Ranges see electrical characteristics at RF transmitter.

Modulator PLL

The fractional divider has been chosen to increase the reference frequency of the modulator PLL.

$$557.5\ \text{kHz} = f_{Mod} / \left(P_1 + \frac{Q_1}{223}\right)$$

P_1: integer part of the fractional divider (M = 1)
Q_1: fractional part of the fractional divider (M = 1)

$$Q_1 = 223 \times \left(\frac{f_{Mod}}{557.5\ \text{kHz}} - P_1\right)$$

$$223 = \frac{557.5\ \text{kHz}}{2.5\ \text{kHz}}$$

The frequency step 2.5 kHz is a fraction of the reference frequency 557.5 kHz.
In fact, the fractional divider divides Q_1 times by (P_1 + 1) and (223 - Q_1) times by P_1 during 223 cycles.

$$\rightarrow \frac{Q_1 \times (P_1 + 1) + (223 - Q_1)P_1}{223} = P_1 + \frac{Q_1}{223}$$

For each comparison cycle (f_{Ref1} = 557.5 kHz), the accumulator content is incremented by the Q_1 value and the divider divides by the P_1 value. When the accumulator value reaches or exceeds 223, the divider divides by the value (P_1 + 1). Then, the accumulator holds the excess value (accumulator value - 223). After 223 cycles, the correct division is executed.

Serial Bus Interface

The circuit is remoted by an external microcontroller through the serial bus.

The data is a 12-bit word:

A0 - A3: address of the destination register (0 to 15)

D7 - D0: contents of register

The data line must be stable when the clock is high and data must be serially shifted.

After 12 clock periods, the transfer to the destination register is (internally) generated by a low to high transition of the data line when the clock is high.

Figure 3. Serial Bus

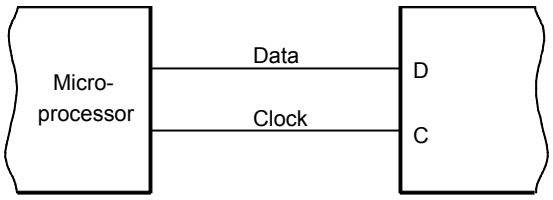


Figure 4. Serial Bus Transmission

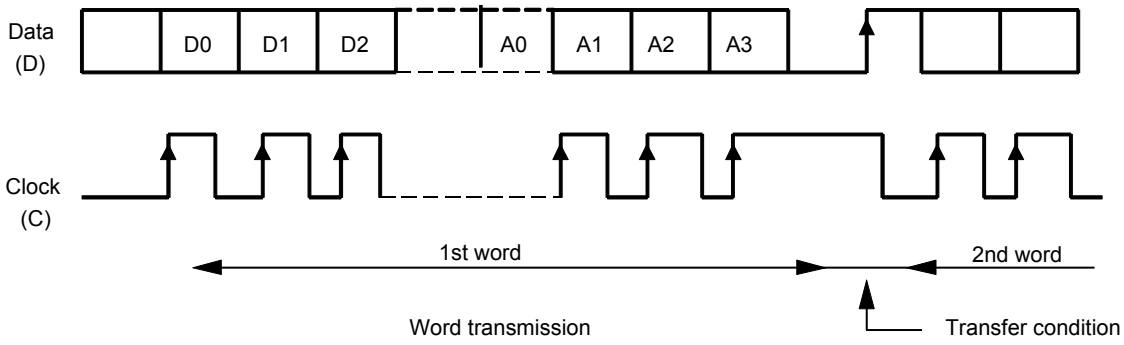


Figure 5. Serial Bus Structure

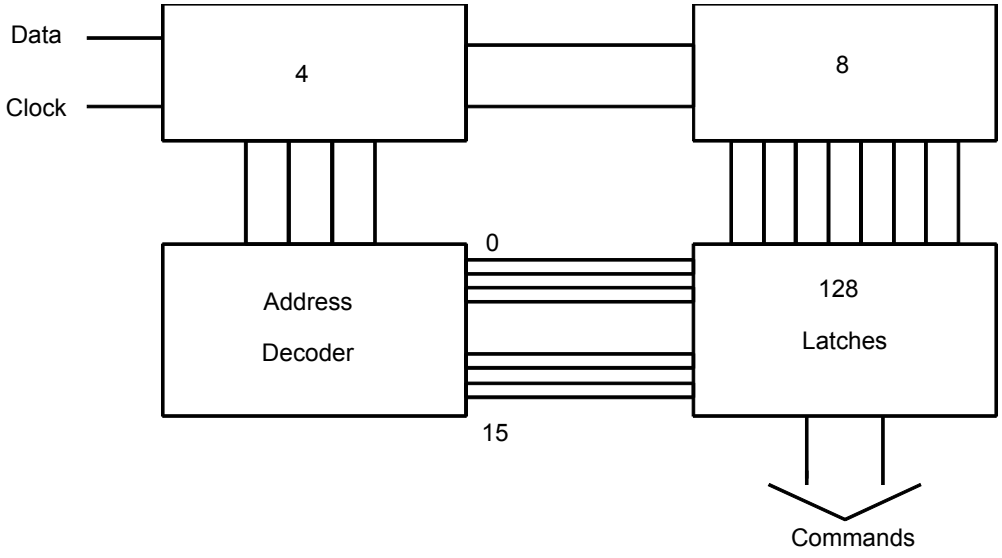
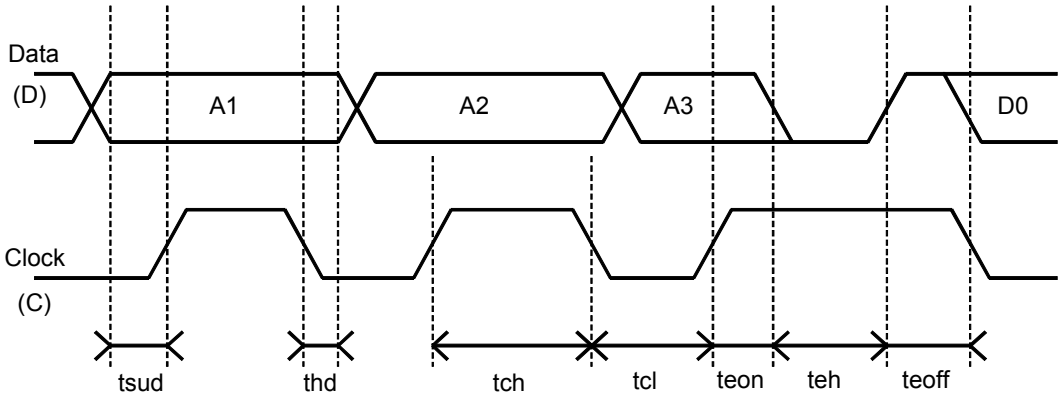


Figure 6. Serial Bus Timing Diagram



Content of Internal Registers

The registers have the following structure

D7	D6	D5	D4	D3	D2	D1	D0

R0: Reference for D/A converter

MUXDA	DA6	DA5	DA4	DA3	DA2	DA1	DA0

MUXDA: D/A multiplexing VBAT / RSSI
DA(0:6): Reference voltage D/A

R1: Gain of earpeace amplifier and demodulator

GEA4	GEA3	GEA2	GEA1	GEA0	GDEM	free	free

GEA[0:4]: Gain of earpeace amplifier; “0” is LSB, “4” is MSB
GDEM: Demodulator gain (1 = low gain)

R2: Switches and mutes for receive and data reception

DATRX	BEXP	EEA	ERXO	ERX1	ERXHF	MRX	ERX2

DATRX: Switch data comparator output to “DACO”-pin
BEXP: Bypass expander
EEA: Enable earpiece amplifier
ERXO: Enable RXO output driver
ERX1: Enable RX low frequency part 1
ERXHF: Enable Mixer2 and IF-amplifier
MRX: Mute RX low frequency path (expander) keeping circuit enabled
ERX2: Enable RX low frequency part 2 (expander)

R3: Switches and mutes for transmit and power managemant

PDVDD	RBAT	free	free	free	free	MTX	ETX

PDVDD: Enable pull-down transistor in power-down mode
RBAT: Battery detection high/low range
MTX: Mute TX low frequency path (compressor) keeping circuit enabled
ETX: Enable TX low frequency part

R4: free (not used, for future extensions)

free	free	free	free	free	free	free	free

R5: Gain VCO2

free	free	KV23	KV22	KV21	M12	free	free

KV2[1:3]: Gain of VCO2
M12: Double phase comparator frequency of PLL2

R6: Miscellaneus settings in synthesizer part

ETXO	M1CP	FRMT	IMIXI	GMOD1	GMOD0	SU1	(TM)

ETXO: Enable HF-transmit output
M1CP: Changes 1 dB compression point and current consumption of Mixer1 ("0" –> high, "1" –> low)
FRMT: Output frequency range of MixerT
IMIXI: Invert inputs of phase comparator in PLL2
GMOD[0:1]: Modulation gain of VCO1
SU1: Speed-up phase comparator for PLL1
(TM): Enable the internal test mode. It is mandatory that TM is kept to "0"! (if not 0, the circuit will not work as expected or described here in this paper)

R7: PLL1 setting

DR1I1	DR1I0	RA11	RA10	DV1I3	DV1I2	DV1I1	DV1I0

DR1I[0:1]: Additional divider reference frequency PLL1
RA1[0:1]: Rough adjustment VCO1
DV1I[0:3]: Divider setting PLL1 integer part; "0" is LSB, "3" is MSB

R8: Divider PLL1 fractional part

DV1F7	DV1F6	DV1F5	DV1F4	DV1F3	DV1F2	DV1F1	DV1F0

DV1F[0:7]: Divider setting PLL1 fractional part; "0" is LSB, "7" is MSB

R9: Divider PLL3 LSBs

DV3I7	DV3I6	DV3I5	DV3I4	DV3I3	DV3I2	DV3I1	DV3I0

R10: Divider PLL3 MSBs and MSB of VCO3 fine adjustment

FA34	DV3I14	DV3I13	DV3I12	DV3I11	DV3I10	DV3I9	DV3I8

FA34: Fine adjustment VCO3 (frequency reduction) MSB
DV1I[0:14]: Divider setting PLL3 integer part; "0" is LSB, "14" is MSB

R11: Setting PLL2 and VCO3

FA33	FA32	FA31	FA30	AMIX2	AMIX1	RA21	RA20

FA3[0:4]: Fine adjustment of VCO3 (frequency reduction); “0” is LSB, “4” is MSB
AMIX[1:2]: Lengthening antibacklash signal PLL2
RA2[1:0]: Rough adjustment VCO2

R12: Divider for country setting, fine adjustment oscillator

FAOS2	FAOS1	FAOS0	D31	D30	D20	D11	D10

FAOS[0:2]: Fine adjustment of crystal oscillator (frequency reduction);
“0” is LSB, “2” is MSB
D3[0:1]: Setting divider D3
D20: Setting divider D2
D1[0:1]: Setting divider D1

R13: VCO1 enable and fine adjustment

EVCO1	SAFA1	EAFA1	FA14	FA13	FA12	FA11	FA10

EVCO1: Enable VCO1
SAFA1: Sign for automatic fine adjustment of VCO1
EAFA1: Enable automatic fine adjustment of VCO1
FA1(0:4): Manual fine adjustment of VCO1 (frequency reduction);
“0” is LSB, “4” is MSB

R14: VCO2 enable and fine adjustment

EVCO2	SAFA2	EAFA2	FA24	FA23	FA22	FA21	FA20

EVCO2: Enable VCO2 and MixerT
SAFA2: Sign for automatic fine adjustment of VCO2
EAFA2: Enable automatic fine adjustment of VCO2
FA2(0:4): Manual fine adjustment of VCO2 (frtequency reduction);
“0” is LSB, “4” is MSB

R15: VCO3 enable, speed-up and referencq frequency, crystal oscillator enable

EVCO3	EOSC	SU3	E25K	E12K5	E10K	E6K25	E5K

EVCO3: Enable VCO3 and Mixer1
EOSC: Enable crystal oscillator (11.15 MHz)
SU3: Speed-up phase comparator for PLL3
E25K: Selection phase comparator frequency for PLL3: f_{Ref3} = 25 kHz
E12K5: Selection phase comparator frequency for PLL3: f_{Ref3} = 12.5 kHz
E10K: Selection phase comparator frequency for PLL3: f_{Ref3} = 10 kHz
E6K25: Selection phase comparator frequency for PLL3: f_{Ref3} = 6.25 kHz
E5K: Selection phase comparator frequency for PLL3: f_{Ref3} = 5 kHz
E5K, E6K25, E10K, E15K5, E25K = 0:
Selection phase comparator frequency for PLL3: f_{Ref3} = 2.5 kHz

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	V_{Batt}, V_{DD}	5.5	V
Junction temperature	T_j	+125	°C
Ambient temperature	T_{amb}	–25 to +75	°C
Storage temperature	T_{stg}	–50 to +125	°C
Power dissipation T_{amb} = 60°C	P_{tot}	0.9	W

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO44	R_{thJA}	70	K/W

Electrical Characteristics

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified.
Test circuit, see Figure 7. Crystal specifications, see table “Crystal Specifications”.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Supply						
Operating voltage range			3.1	3.6	5.2	V
Current Consumption						
Operating current in inactive mode (low voltage)	VRF = VAF = RFOVB = 2.9 V VDD = 0 V		30	65	85	µA
Operating current in standby mode	VRF = VAF = RFOVB = 3.6 V		30	100	350	µA
Operating current in RX mode “waiting for RSSI”	ERXHF = EVCO3 = EOSC = 1			7.5	10.4	mA
Operating current in RX mode “receiving data”	ERXHF = EVCO3 = EOSC = ERX1 = ERXO = 1			8.5	11.5	mA
Operating current in conversation mode: all blocks enabled	ERXHF = EVCO3 = EOSC = ERX1 = ERXO = ERX2 = EEA = EVCO2 = ETXO = 1 no load at RFO Pin 3			20	29	mA
Charge Pump of LL1						
Charge pump output voltage	Output high		2.38	2.5	2.63	V
Precharge voltage at the loop filter	SB127 = 1, SB119 = 0		1.15	1.4	1.65	V
Charge pump output current in speed-up mode	VMLF = 1.25 V, output low		190		400	µA
	VMLF = 1.25 V, output high		-400		-190	µA
Charge pump output current	VMLF = 1.25 V, output low		4.3	6.2	8	µA
	VMLF = 1.25 V, output high		-8	-6.2	-4.3	µA
Charge pump leakage current	VMLF = 1.25 V, output tristate		-150		+150	nA
Charge Pump of PLL3						
Charge pump output voltage	Output high		2.38	2.5	2.63	V
Charge pump output current in speed-up mode	VPCLO = 1.25 V, output low		220		420	µA
	VPCLO = 1.25 V, output high		-420		-220	µA

Electrical Characteristics (Continued)

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified.
Test circuit, see Figure 7. Crystal specifications, see table “Crystal Specifications”.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Charge pump output current	VPCLO = 1.25 V, output low		80		160	µA
	VPCLO = 1.25 V, output high		-160		-80	µA
Charge pump leakage current	VPCLO = 1.25 V, output tristate		-50		+50	nA
Receiver Input Mixer (Mixer1) EVCO3 = EOSC = 1						
Input frequency range			20		50	MHz
Output frequency				10.7		MHz
Input resistance	MIX1IN1 / MIX1IN2 to GND			3.0		kΩ
Input capacitance	MIX1IN1 / MIX1IN2 to GND			3.5		pF
Output impedance	MIX1O		210	330	390	Ω
Voltage gain	MIX1IN1/2 -> MIX1O “Loaded” (330 Ω with serial capacitance) “Unloaded”			 11.5 17.5		 dB dB
Input noise voltage				9		nV $Hz^{-1/2}$
Input 1-dB compression point	“Loaded” (330 Ω with serial capacitance) M1CP=0 M1CP=1 “unloaded” M1CP=1			 140 40 100		 mV mV mV
Third order input intercept point	“Loaded” (330 Ω with seial capacitance) M1CP=0			 430		 mV
IF Mixer (Mixer2) EOSC = ERXHF = 1; input frequency: 10.7 MHz						
Input resistance	MIX2IN to GND		2.0	3.0	4.0	kΩ
Input capacitance	MIX2IN to GND		2.5	3	3.5	pF
Output impedance	MIX2O		1200	1500	1800	Ω
Voltage gain	MIX2IN -> MIX2O “Loaded” (1500 Ω with serial capacitance)		13	15	17	dB
Input 1-dB compression point	“Loaded” (1500 Ω with serial capacitance)		32			mV
Third order input intercept point	“Loaded” (1500 Ω with serial capcitance)		80			mV
IF Amplifier and Demodulator ERXHF=1, ERX1=1, ERXO=1; Input signal: 450 kHz, 500 µV, FM-modulation frequency = 1 kHz						
Recovered audio at RXO, demodulator gain	GDEM=0 GDEM=1			180 90		mV/kHz mV/kHz
AM rejection ratio	30% AM, 2.5 kHz FM			35		dB
Expander ERX2 = 1; 470 nF from ETC to GND (VSS)						
Gain reference level = G.R.L. (gain = 0 dB)			70	80	90	mVrms
Gain versus input signal level (“gain tracking”)	VEXIN = 10 dB less than G.R.L. VEXIN = 20 dB less than G.R.L. VEXIN = 30 dB less than G.R.L.		 –11 –21 –35	 –10 –20 –30	 –9 –19 –25	 dB dB dB
Attack time	VEXIN = step 25 mV –> 50 mV measure time after step, when output voltage has 0.75 times of final value			16		ms

Electrical Characteristics (Continued)

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified.
Test circuit, see Figure 7. Crystal specifications, see table “Crystal Specifications”.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Release time	VEXIN = step 50 mV –> 25 mV measure time after step, when output voltage has 1.5 times of final value			16		ms
Input resistance			9.5		15	kΩ
Earpiece Amplifier EEA = 1, ERX2 = 1, BEXP = 1; apply input voltage to EXIN; measure differentially at RECO1/2						
Minimum gain	GEA[4:0]=0		0	1	2	dB
Medium gain	GEA[4:0]=16		16	17	18	dB
Maximum gain	GEA[4:0]=31		31	32	33	dB
Gain adjust step			0.8	1	1.2	dB
Output voltage swing	Maximum gain; 1 kΩ load; increase input voltage until distortion ≈ 5%		4.8	5		Vpp
Input resistance			7.3		12.5	kΩ
IF Amplifier: RSSI						
Input frequency	ERXHF=1			450		kHz
Input resistance			1.6	2.0	2.5	kΩ
RSSI sensitivity	VIF = 0 µV starting from 0 increase RSSI-level until mean of sampled signal at DACO is ≥ 0.5. RSSI-level = ION0 VIF = 25.4 µV, f = 450 kHz increase RSSI level again until mean of sampled signal at DACO is ≥ 0.5. RSSI-level = ION1 RSSI-sensitivity = ION1-ION0			1		
RSSI input voltage dynamic range				65		dB
RSSI level number of programmable steps (see folowing table “RSSI Level Programming (Typical Values)				127		dB
RSSI level step size in the logarithmic region			0.35	0.46	0.6	dB

RSSI Level Programming (Typical Values)

Input Voltage VIF (µV)	RSSI Level (Decimal)
0	5
25.4	8
42.4	14
424	54
4240	97
42400	111

Electrical Characteristics (Continued)

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified. Test circuit, see Figure 7.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Data Comparator ERX1 = DATRX = 1						
Hysteresis				50		mV
Threshold voltage				1.5		V
Input impedance	DAIN			100		kΩ
Output high voltage	DACO, without load (CMOS-output –> full swing)			3.5		V
Output low voltage	DACO, without load (CMOS-output –> full swing)			0.1		V
Output impedance	DACO			6		kΩ
Battery Switch						
“Off” threshold	Decrease VBAT until internal switch between VBAT and VDD becomes high ohmic (“off”)		2.85	2.95	3.1	V
“On” threshold	Increase VBAT until internal switch between VBAT and VDD becomes low ohmic (“on”)		3.1	3.2	3.35	V
Hysteresis	Difference between on and off threshold			250		mV
“Off”-leakage current					10	µA
Switch “On”-resistance					50	Ω
Battery Management MUXDA = 1						
Maximum bat low	DA[6:0] = 127, RBAT = 1		3.7	3.95	4.1	V
Minimum bat low over switch	DA[6:0] = 27, RBAT = 1		3.05	3.2	3.35	V
Maximum bat high	DA[6:0] = 127, RBAT = 0		4.75	5.05	5.25	V
Minimum bat high	DA[6:0] = 0, RBAT = 0		3.83	4.1	4.27	V
Adjust step			3.5	7.5	11.5	mV
Maximum - Minimum			852.5	952.5	1052.5	mV
Microphone Amplifier ETX=1						
Open loop gain				80		dB
Gain bandwidth product				3		MHz
Input noise voltage, BW = 300 Hz to 3.4 kHz, psophometrically weighted				0.8	2	µVrmsp
Compressor ETX = 1; 470 nF from CTC to GND (VSS)						
Gain reference level = G.R.L. (gain = 0 dB)			298	316	340	mVrms
Gain versus input signal level (“gain tracking”)	VCOIN = 20 dB less than G.R.L. VCOIN = 40 dB less than G.R.L. VCOIN = 50 dB less than G.R.L. VCOIN = 60 dB less than G.R.L		9 19 22	10 20 25 30	11 21 28	dB
Attack time	VCOIN = step 31.6 mV –> 126 mV, (-30 dBV –> –18 dBV) measure time after step, when output voltage has 1.5 times of final value			3.5		ms

Electrical Characteristics (Continued)

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified. Test circuit, see Figure 7.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Release time	VCOIN = step 126 mV –> 31.6 mV (-18 dBV –> -30 dBV) measure time after step, when output voltage has 0.75 times of final value			14.4		ms
Input resistance			14	19.5	26	kΩ
Splatter Amplifier ETX = 1						
Open loop gain				90		dB
Gain bandwidth product				150		kHz
Maximum output voltage swing			2.4			Vpp
Limiter Amplifier ETX = 1, Tj = 25°C						
Gain for signals below limitation	LIMIN –> TXO, 20 mV_{RMS} applied to LIMIN (AC coupled)			26		dB
Distortion for signals below limitation	LIMIN –> TXO, 20 mV_{RMS} applied to LIMIN (AC coupled)				2	%
Maximum output voltage swing (above limitation, clipping)			1.8	2.1	2.35	V_{pp}
Input resistance at LIMIN			15	20	25	kΩ
Remark: The gain and maximum output voltage swing of the limiter amplifier changes with temperature to compensate the temperature dependancy of MODIN (“tx conversion gain” of RF transmit part), fundamentally determined by the structure of the circuitry.						
RF Transmitter ETXO = EVCO1 = EVCO2 = EVCO3 = EOSC = 1; T_j = 25°C						
MODIN input impedance			70	100	130	kΩ
RFO output impedance	Load = 200 ø		230	300	390	Ω
RFO output voltage level	ETXO = 0; no load				0.3	V
Highest operating frequency	USA Base Channel 9 (US1b9)			49.9900		MHz
TX conversion gain MODIN - RFO	For the complete programming see “Channel Frequencies, Dividers and Country Settings” on page 19“ USA1: GMOD[1:0] = 00; fMod = ~7.6 MHz USA2: GMOD[1:0] = 01; fMod = ~5.7 MHz France: GMOD[1:0] = 01; fMod = 4.3 MHz GMOD[1:0] = 00; fMod = 4.3 MHz Spain/Netherlands: GMOD[1:0] = 10; fMod = 1.8 MHz			 5.2 5.2 3.8 2.7 7.9		 kHz/V kHz/V kHz/V kHz/V kHz/V
Demodulated distortion THD MODIN - RFO	Modulation frequency: 1 kHz US: ΔF = 4.0 kHz France: ΔF = 2.5 kHz			1.5	5	%

Electrical Characteristics (Continued)

T_{amb} = +25°C, VRF = VAF = RFOVB = 3.6 V, all bits set to “0”, unless otherwise specified. Test circuit, see Figure 7.

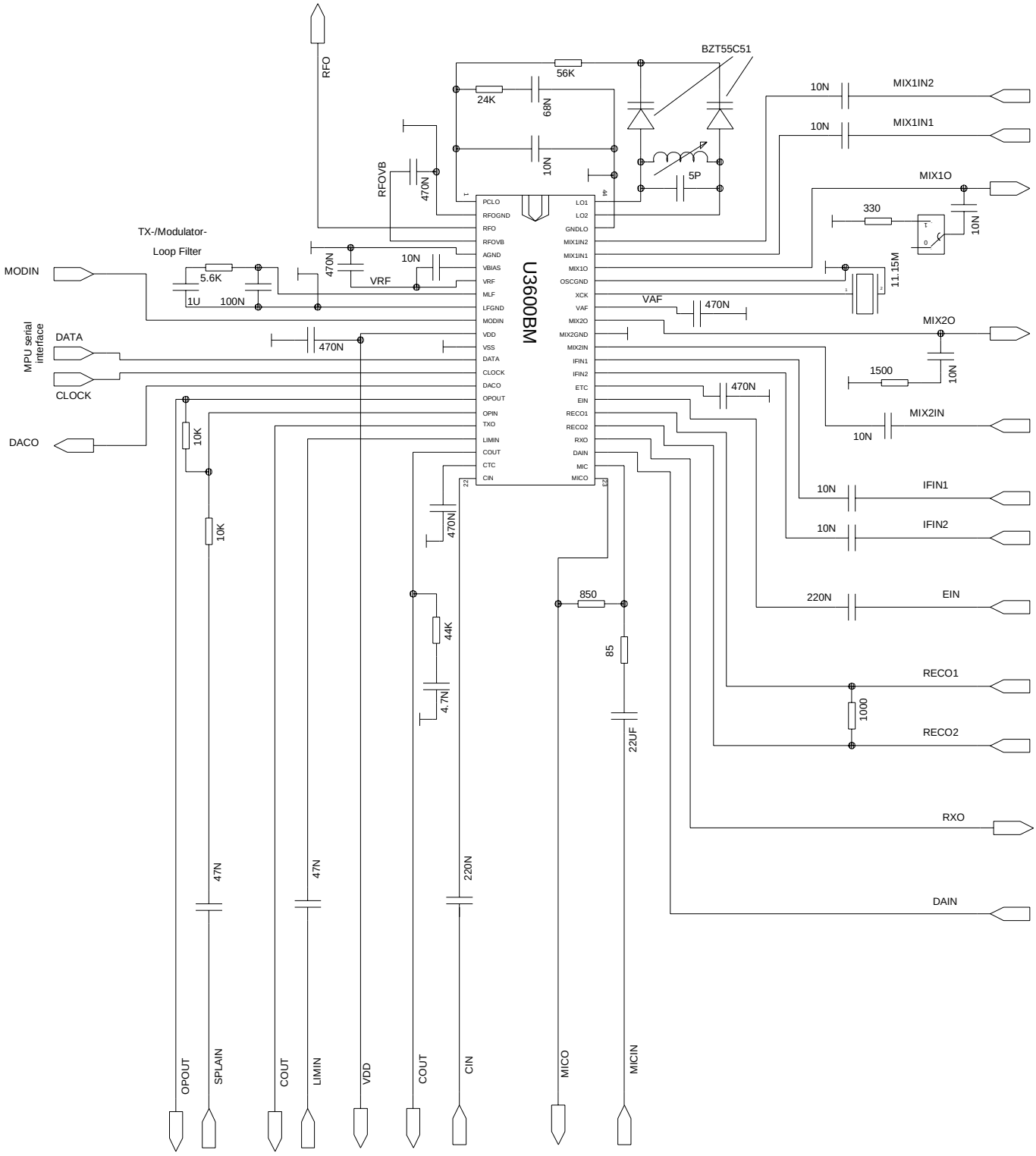
Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Remark: The tx conversion gain of the RF transmitter is somehow dependent on temperature. This is determined by the fundamental principle of this circuitry. Means have been taken inside the limiter amplifier, being in the signal path before MODIN, which are able to completely compensate this temperature behavior.						
Logical Part						
Inputs: C, D Low voltage input High voltage input Input leakage current (0 < VI < VDD)		 Vil Vih Ii	 $0.8 \times V_{DD}$ –1		 $0.2 \times V_{DD}$ +5	 µA
Input leakage current Pin XCK (0 < VI < VDD)			–5		+5	µA
Serial bus (Figure 8) Data set-up time Data hold time Clock low time Clock high time Hold time before transfer condition Data low pulse on transfer condition Data high pulse on transfer condition		 tsud thd tcl tch teon teh teoff	 0.1 0 2 2 0.1 0.2 0.2			 µs µs µs µs µs µs µs

Fine Adjustment of the Oscillator Frequency

To set the frequency of the oscillator exact to 11.15 MHz, the frequency is adjustable in 8 steps, by adding 3 different internal capacities the frequency could be reduced.

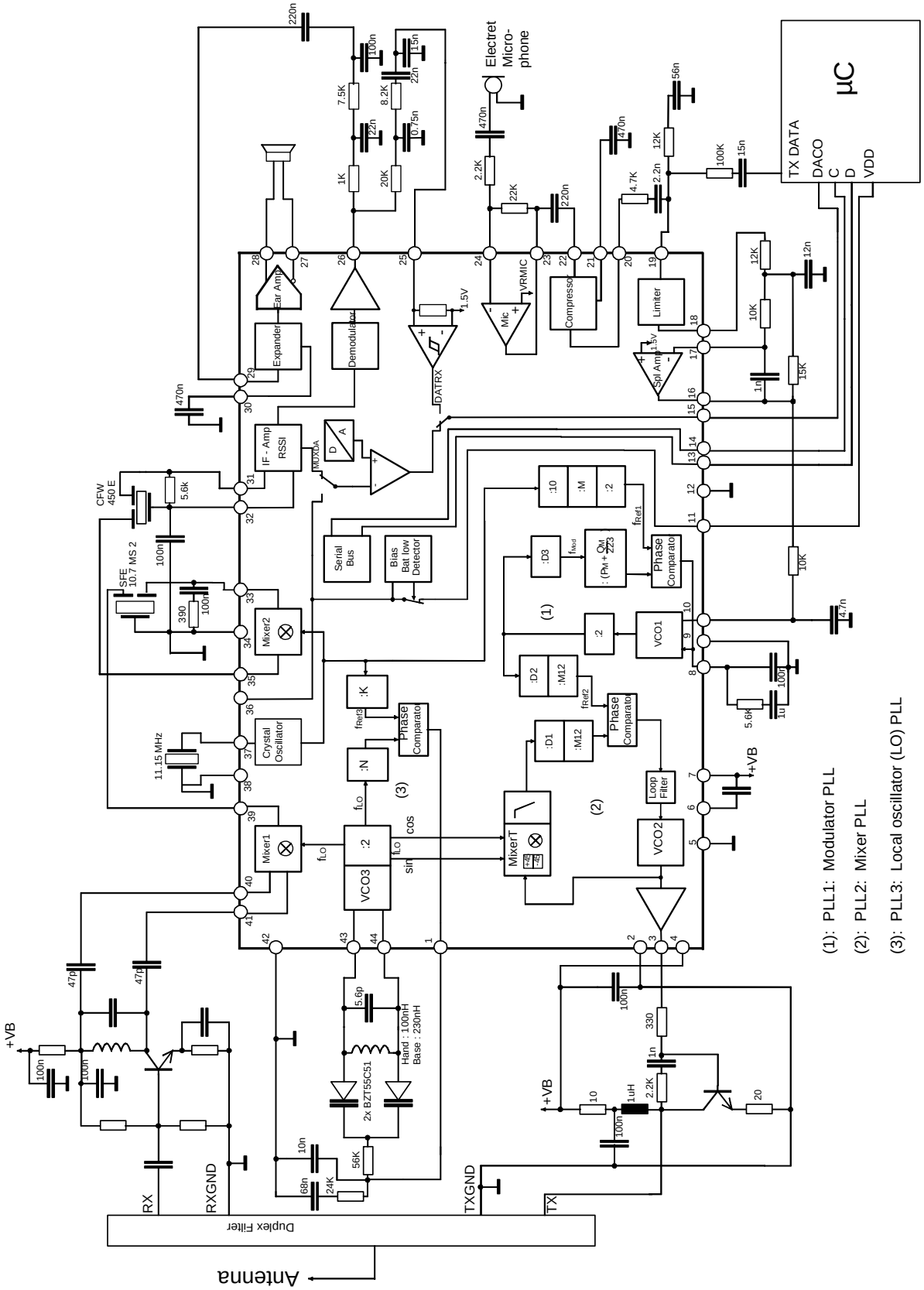
Parameters	Test Conditions / Pins	Min.	Typ.	Max.	Unit
Oscillator frequency without reduction	FAOS (0:2) = 0		11.15 +Δ		MHz
Changing of oscillator frequency with FOSC reduction	FAOS2 FAOS1 FAOS0 0 0 1 0 1 0 1 0 0 1 0 1		 140 280 560 700		 Hz

Figure 7. Test Circuit



NOTE: This schematics is only a basic(simplified) representation of the current production test circuit

Figure 8. Application Circuit



Channel Frequencies, Dividers and Country Settings

To meet all requirements of various countries – France (F), Spain (E), Netherlands (NL), USA, Portugal (P), Taiwan, New Zealand and Korea – and modes – base (b), handset (h) – several bits have to be set which do not change for the different channels. These settings are called country settings.

- The country-setting bits contain:
- Rough adjustments for 2 VCOs
- Setting three integer divider in the mixer PLL and modulator PLL
- Conversion gain adjustment of mixer PLL
- Modulator gain
- Setting of the pulling direction of PLL2 (value dependent, if TX frequency is higher or lower than LO frequency)
- Demodulator gain

Name Register	Function	Notes	Number of Positions
RA1[1:0]	Rough adjust VCO1	00: is the highest frequency	3
RA2[1:0]	Rough adjust VCO2	00: is the highest frequency	4
D1[1:0]	Integer divider D1	Division by 2, 4, 6, 8	4
D20	Integer divider D2	Division by 6, 8	2
M12	Integer divider M12	Doubles reference frequency of PLL2 when set to “1”	2
D3[1:0]	Integer divider D3	Division by 1, 2, 4	3
KV[3:1]	Conversion gain VCO2		6
GMOD[1:0]	Modulator gain	00: gain minimal	3
IMIXI	Reverse inputs of PC of PLL	0: if fVCO2 lower than fVCO3	2
DR1[1:0]	Additional divider M for reference frequency f_{Ref1}	“0” means no reduction, >0 only necessary in E, NL, Portugal	4
FRMT	Frequency range Mixer T	0: output frequency < 5 MHz	2
GDEM	Demodulator gain	0: high gain 1: low gain	2

Note: Setting the fractional dividers:
For N, Q_M, send the binary equivalent of the numbers given below.
For P_M (integer part of modulator PLL), send the D2 complement ($16 – P_M$)
i.e., Fb1 ($P_M = 7$, $Q_M = 159$ => integer: send $16 – P_M = 9$, fractional: send 159)

Tables for Programming of the Dividers (Refer to Block Diagram)

Divider D1 for PLL2:

D11 (bit)	D10 (bit)	Decimally	D1 (Block Diagram),if M12 = 0	D1 (Block Diagram),if M12 = 1
0	0	0	2	1
0	1	1	8	4
1	0	2	6	3
1	1	3	4	2

Divider D2 between PLL1 and PLL2:

D20 (bit)	Decimally	D2 (Block Diagram),if M12 = 0	D2 (Block Diagram),if M12 = 1
0	0	6	3
0	1	8	4

Divider D3 for PLL1:

D31 (bit)	D30 (bit)	Decimally	D3 (Block Diagram)
0	0	0	1
0	1	1	2
1	0	2	6
1	1	3	4

Divider M for Reference Frequency of PLL1:

There are several countries like Spain, the Netherlands and Portugal with relatively low modulator frequencies fMod. In case of modulation there will be a big maximum time shift between pulses coming from fractional divider and pulses coming from reference frequency divider. As a consequence the phase comparator enters an undesired operation mode. To avoid entering this operation mode the reference frequency f_{Ref1} has to be reduced by a factor M. Simultaneously, keeping f_{Mod} constant, the factors of fractional dividers have to be changed as well.

The connection between the additional reference frequency divider M and the factors P_M and Q_M of fractional divider is given below. The subscript M denotes which value of M refers to the factors P_M and Q_M of fractional divider. The formulas take into account that the numerator of the fraction $Q_M/223$ must not exceed 223.

$P_M = P_1 \times M + \text{integer} (Q \times M/223)$

$Q_M = Q_1 \times M - 223 \times \text{integer} (Q_1 \times M/223)$

France Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	00	11	11	1	01	100	01 (1)	0	00	0	0
Value	max	min	D1 = 4	D2 = 8	D3 = 2			supra	M = 1	low	high gain

Note: 1. Alternatively, GMOD[1:0] could be set to “00”. This reduces the TX conversion gain (MODIN –> RFO) from about 3.8 kHz/V to about 2.7 kHz/V, a value, which should be still sufficient for a maximum Δf of ~2.5 kHz that is useful in the French case.

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel (MHz)	Rx Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	26.3125	41.3125	30.6125	4898
2	26.3250	41.3250	30.6250	4900
3	26.3375	41.3375	30.6375	4902
4	26.3500	41.3500	30.6500	4904
5	26.3625	41.3625	30.6625	4906
6	26.3750	41.3750	30.6750	4908
7	26.3875	41.3875	30.6875	4910
8	26.400	41.4000	30.7000	4912
9	26.4125	41.4125	30.7125	4914
10	26.4250	41.4250	30.7250	4916
11	26.4375	41.4375	30.7375	4918
12	26.4500	41.4500	30.7500	4920
13	26.4625	41.4625	30.7625	4922
14	26.4750	41.4750	30.7750	4924
15	26.4875	41.4875	30.7875	4926

France Modulation Loop Frequency and Divider

f_{Mod} = 4.3 MHz, P_M = 7, Q_M = 159, M = 1

France Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	00	01	11	1	01	101	01 (1)	1	00	0	0
Value	max		D1 = 4	D2 = 8	D3 = 2			infra	M = 1	low	high gain

Note: 1. Alternatively, GMOD[1:0] could be set to “00”. This reduces the TX conversion gain (MODIN –> RFO) from about 3.8 kHz/V to about 2.7 kHz/V, a value, which should be still sufficient for a maximum Δf of ~2.5 kHz that is useful in the French case.

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	$f_{LO} = 1/2\ f_{VCO3}$ (MHz)	DV3I[14:0] = N
1	41.3125	26.3125	37.0125	5922
2	41.3250	26.3250	37.0250	5924
3	41.3375	26.3375	37.0375	5926
4	41.3500	26.3500	37.0500	5928
5	41.3625	26.3625	37.0625	5930
6	41.3750	26.3750	37.0750	5932
7	41.3875	26.3875	37.0875	5934
8	41.4000	26.4000	37.1000	5936
9	41.4125	26.4125	37.1125	5938
10	41.4250	26.4250	37.1250	5940
11	41.4375	26.4375	37.1375	5942
12	41.4500	26.4500	37.1500	5944
13	41.4625	26.4625	37.1625	5946
14	41.4750	26.4750	37.1750	5948
15	41.4875	26.4875	37.1875	5950

France Modulation Loop Frequency and Divider

f_{Mod} = 4.3 MHz, P_M = 7, Q_M = 159, M = 1

Spain Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	10	00	1	11	001	10	1	11	1	1
Value			D1 = 2	D2 = 8	D3 = 4			infra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	31.025	39.925	29.225	4676
2	31.050	39.950	29.250	4680
3	31.075	39.975	29.275	4684
4	31.100	40.000	29.300	4688
5	31.125	40.025	29.325	4692
6	31.150	40.050	29.350	4696
7	31.175	40.075	29.375	4700
8	31.200	40.100	29.400	4704
9	31.250	40.150	29.450	4712
10	31.275	40.175	29.475	4716
11	31.300	40.200	29.500	4720
12	31.325	40.225	29.525	4724

Spain Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

Spain Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	01	00	1	11	100	10	0	11	1	1
Value		high	D1 = 2	D2 = 8	D3 = 4		high	supra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	39.925	31.025	41.725	6676
2	39.950	31.050	41.750	6680
3	39.975	31.075	41.775	6684
4	40.000	31.100	41.800	6688
5	40.025	31.125	41.825	6692
6	40.050	31.150	41.850	6696
7	40.075	31.175	41.875	6700
8	40.100	31.200	41.900	6704
9	40.150	31.250	41.950	6712
10	40.175	31.275	41.975	6716
11	40.200	31.300	42.000	6720
12	40.225	31.325	42.025	6724

Spain Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

Netherlands Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	10	00	1	11	001	10	1	11	1	1
Value		low	D1 = 2	D2 = 8	D3 = 4		high	infra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	31.0375	39.9375	29.2375	4678
2	31.0625	39.9625	29.2625	4682
3	31.0875	39.9875	29.2875	4686
4	31.1125	40.0125	29.3125	4690
5	31.1375	40.0375	29.3375	4694
6	31.1625	40.0625	29.3625	4698
7	31.1875	40.0875	29.3875	4702
8	31.2125	40.1125	29.4125	4706
9	31.2375	40.1375	29.4375	4710
10	31.2625	40.1625	29.4625	4714
11	31.2875	40.1875	29.4875	4718
12	31.3125	40.2125	29.5125	4722

Netherlands Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

Netherlands Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	01	00	1	11	001	10	0	11	1	1
Value		high	D1 = 2	D2 = 8	D3 = 4		high	supra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	39.9375	31.0375	41.7375	6678
2	39.9625	31.0625	41.7625	6682
3	39.9875	31.0875	41.7875	6686
4	40.0125	31.1125	41.8125	6690
5	40.0375	31.1375	41.8375	6694
6	40.0625	31.1625	41.8625	6698
7	40.0875	31.1875	41.8875	6702
8	40.1125	31.2125	41.9125	6706
9	40.1375	31.2375	41.9375	6710
10	40.1625	31.2625	41.9625	6714
11	40.1875	31.2875	41.9875	6718
12	40.2125	31.3125	42.0125	6722

Netherlands Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

U.K. Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	10	00	1	11	001	10	1	11	1	1
Value		low	D1 = 2	D2 = 8	D3 = 4		high	infra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	31.0375	39.9375	29.2375	4678
2	31.0625	39.9625	29.2625	4682
3	31.0875	39.9875	29.2875	4686
4	31.1125	40.0125	29.3125	4690

U.K. Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

U.K. Handset

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	01	00	1	11	001	10	0	11	1	1
Value		high	D1 = 2	D2 = 8	D3 = 4		high	supra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	39.9375	31.0375	41.7375	6678
2	39.9625	31.0625	41.7625	6682
3	39.9875	31.0875	41.7875	6686
4	40.0125	31.1125	41.8125	6690

U.K. Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.8 MHz/4,P_M = 12,Q_M = 204, M = 4

USA Base

Country Setting Channels (Channel 1 – 10, USA1):

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	100	00	1	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1		low	infra	M = 1	high	low gain

Country Setting New Channels (Channel 11 – 25, USA2):

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	01	01	10	0	00	110	01	1	00	0	1
Value		high	D1 = 6	D2 = &	D3 = 1			infra	M = 1	low	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 5 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	46.610	49.670	38.970	7794
2	46.630	49.845	39.145	7829
3	46.670	49.860	39.160	7832
4	46.710	49.770	39.070	7814
5	46.730	49.875	39.175	7835
6	46.770	49.830	39.130	7826
7	46.830	49.890	39.190	7838
8	46.870	49.930	39.230	7846
9	46.930	49.990	39.290	7858
10	46.970	49.970	39.270	7854

New Channel

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
11	43.720	48.760	38.06	7612
12	43.740	48.840	38.14	7628
13	43.820	48.860	38.16	7632
14	43.840	48.920	38.22	7644
15	43.920	49.020	38.32	7664
16	43.960	49.080	38.38	7676
17	44.120	49.100	38.40	7680
18	44.160	49.160	38.46	7692
19	44.180	49.200	38.50	7700
20	44.200	49.240	38.54	7708
21	44.320	49.280	38.58	7716
22	44.360	49.360	38.66	7732
23	44.400	49.400	38.70	7740
24	44.460	49.460	38.76	7752
25	44.480	49.500	38.80	7760

USA Hand

Country Setting Channels (Channel 1 – 10, USA1):

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	100	00	0	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			supra	M = 1	high	low gain

Country Setting New Channels (Channel 11 – 25, USA2):

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	01	00	10	0	00	110	01	0	00	0	1
Value		high	D1 = 6	D2 = &	D3 = 1			supra	M = 1	low	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 5 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	49.670	46.610	57.31	11462
2	49.845	46.630	57.33	11466
3	49.860	46.670	57.37	11474
4	49.770	46.710	57.41	11482
5	49.875	46.730	57.43	11486
6	49.830	46.770	57.47	11494
7	49.890	46.830	57.53	11506
8	49.930	46.870	57.57	11514
9	49.990	46.930	57.63	11526
10	49.970	46.970	57.67	11534

New channel

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
11	48.760	43.720	54.42	10884
12	48.840	43.740	54.44	10888
13	48.860	43.820	54.52	10904
14	48.920	43.840	54.54	10908
15	49.020	43.920	54.62	10924
16	49.080	43.960	54.66	10932
17	49.100	44.120	54.82	10964
18	49.160	44.160	54.86	10972
19	49.200	44.180	54.88	10976
20	49.240	44.200	54.90	10980
21	49.260	44.320	55.02	11004
22	49.360	44.360	55.06	11012
23	49.400	44.400	55.10	11020
24	49.460	44.460	55.16	11032
25	49.500	44.480	55.18	11036

USA Modulation Loop Frequencies and Dividers

N Channel	P_M	Q_M	f_{Mod} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700

New Channel

N Channel	P_M	Q_M	f_{Mod} (MHz)
11	10	34	5.66
12	10	10	5.60
13	10	34	5.66
14	10	18	5.62
15	10	10	5.60
16	10	2	5.58
17	10	58	5.72
18	10	50	5.70
19	10	42	5.68
20	10	34	5.66
21	10	66	5.74
22	10	50	5.70
23	10	50	5.70
24	10	50	5.70
25	10	42	5.68

Portugal Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	01	10	00	1	11	001	10	1	11	1	1
Value			D1 = 2	D2 = 8	D3 = 4			infra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	27.550	37.000	26.300	4208
2	27.575	37.025	26.325	4212
3	27.600	37.050	26.350	4216
4	27.625	37.075	26.375	4220
5	27.650	37.100	26.400	4224
6	27.675	37.125	26.425	4228
7	27.700	37.150	26.450	4232
8	27.725	37.175	26.475	4236
9	27.750	37.200	26.500	4240
10	27.775	37.225	26.525	4244
11	27.800	37.250	26.550	4248
12	27.825	37.275	26.575	4252

Portugal Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.25 MHz/4,P_M = 8,Q_M = 216, M = 4

Portugal Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	01	01	00	1	11	001	10	0	11	1	1
Value			D1 = 2	D2 = 8	D3 = 4			supra	M = 4	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	37.000	27.550	38.250	6120
2	37.025	27.575	38.275	6124
3	37.050	27.600	38.300	6128
4	37.075	27.625	38.325	6132
5	37.100	27.650	38.350	6136
6	37.125	27.675	38.375	6140
7	37.150	27.700	38.400	6144
8	37.175	27.725	38.425	6148
9	37.200	27.750	38.450	6152
10	37.225	27.775	38.475	6156
11	37.250	27.800	38.500	6160
12	37.275	27.825	38.525	6164

Portugal Modulation Loop Frequency and Divider

f_{Ref1} = 557.5 kHz/4, f_{Mod} = 1.25 MHz/4,P_M = 8,Q_M = 216, M = 4

Taiwan Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	110	01	1	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			infra	M = 1	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	45.2500	48.2500	37.5500	6008
2	45.2750	48.2750	37.5750	6012
3	45.3000	48.3000	37.6000	6016
4	45.3250	48.3250	37.6250	6020
5	45.3500	48.3500	37.6500	6024
6	45.3750	48.3750	37.6750	6028
7	45.4000	48.4000	37.7000	6032
8	45.4250	48.4250	37.7250	6036
9	45.4500	48.4500	37.7500	6040
10	45.4750	48.4750	37.7750	6044

Taiwan Modulation Loop Frequency and Divider

f_{Mod} = 7.7 MHz, P_M = 13,Q_M = 181, M = 1

Taiwan Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	110	00	0	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			supra	M = 1	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	48.2500	45.2500	55.9500	8952
2	48.2750	45.2750	55.9750	8956
3	48.3000	45.3000	56.0000	8960
4	48.3250	45.3250	56.0250	8964
5	48.3500	45.3500	56.0500	8968
6	48.3750	45.3750	56.0750	8972
7	48.4000	45.4000	56.1000	8976
8	48.4250	45.4250	56.1250	8980
9	48.4500	45.4500	56.1500	8984
10	48.4750	45.4750	56.1750	8988

Taiwan Modulation Loop Frequency and Divider

f_{Mod} = 7.7 MHz, P_M = 13,Q_M = 181, M = 1

China Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	110	01	1	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			infra	M = 1	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	45.0000	48.0000	37.3000	5968
2	45.0250	48.0250	37.3250	5972
3	45.0500	48.0500	37.3500	5976
4	45.0750	48.0750	37.3750	5980
5	45.1000	48.1000	37.4000	5984
6	45.1250	48.1250	37.4250	5988
7	45.1500	48.1500	37.4500	5992
8	45.1750	48.1750	37.4750	5996
9	45.2000	48.2000	37.5000	6000
10	45.2250	48.2250	37.5250	6004
11	45.2500	48.2500	37.5500	6008
12	45.2750	48.2750	37.5750	6012
13	45.3000	48.3000	37.6000	6016
14	45.3250	48.3250	37.6250	6020
15	45.3500	48.3500	37.6500	6024
16	45.3750	48.3750	37.6750	6028
17	45.4000	48.4000	37.7000	6032
18	45.4250	48.4250	37.7250	6036
19	45.4500	48.4500	37.7500	6040
20	45.4750	48.4750	37.7750	6044

China Modulation Loop Frequency and Divider

f_{Mod} = 7.7 MHz, P_M = 13,Q_M = 181, M = 1

China Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	110	00	0	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			supra	M = 1	high	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	48.000	45.0000	55.7000	8912
2	48.0250	45.0250	55.7250	8916
3	48.0500	450500	55.7500	8920
4	48.0750	450750	55.7750	8924
5	48.1000	45.1000	55.8000	8928
6	48.1250	45.1250	55.8250	8932
7	48.1500	45.1500	55.8500	8936
8	48.1750	45.1750	55.8750	8940
9	48.2000	45.2000	55.9000	8944
10	48.2250	45.2250	55.9250	8948
11	48.2500	45.2500	55.9500	8952
12	48.2750	45.2750	55.9750	8956
13	48.3000	45.3000	56.0000	8960
14	48.3250	45.3250	56.0250	8964
15	48.3500	45.3500	56.0500	8968
16	48.3750	45.3750	56.0750	8972
17	48.4000	45.4000	56.1000	8976
18	48.4250	45.4250	56.1250	8980
19	48.4500	45.4500	56.1500	8984
20	48.4750	45.4750	56.1750	8988

China Modulation Loop Frequency and Divider

f_{Mod} = 7.7 MHz, P_M = 13,Q_M = 181, M = 1

New Zealand Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	00	01	11	1	01	110	01	1	00	0	1
Value			D1 = 4	D2 = 8	D3 = 2			infra	M = 1	low	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	$f_{LO} = 1/2\ f_{VCO3}$ (MHz)	DV3I[14:0] = N
11	34.2500	40.2500	29.5500	4728
12	34.2750	40.2750	29.5750	4732
13	34.3000	40.3000	29.6000	4736
14	34.3250	40.3250	29.6250	4740
15	34.3500	40.3500	29.6500	4744
16	34.3750	40.3750	29.6750	4748
17	34.4000	40.4000	29.7000	4752
18	34.4250	40.4250	29.7250	4756
19	34.4500	40.4500	29.7500	4760
20	34.4750	40.4750	29.7750	4764

New Zealand Modulation Loop Frequency and Divider

f_{Mod} = 4.7 MHz/4, P_M = 8,Q_M = 96, M = 1

New Zealand Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	00	01	11	1	01	101	01	0	00	0	1
Value	max	min	D1 = 4	D2 = 8	D3 = 2			supra	M = 1	low	low gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 6.25 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
11	40.2500	34.2500	44.9500	7192
12	40.2750	34.2750	44.9750	7196
13	40.3000	34.3000	45.0000	7200
14	40.3250	34.3250	45.0250	7204
15	40.3500	34.3500	45.0500	7208
16	40.3750	34.3750	45.0750	7212
17	40.4000	34.4000	45.1000	7216
18	40.4250	34.4250	45.1250	7220
19	40.4500	34.4500	45.1500	7224
20	40.4750	34.4750	45.1750	7228

New Zealand Modulation Loop Frequency and Divider

f_{Mod} = 4.7 MHz/4, P_M = 8,Q_M = 96, M = 1

Korea Base

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	100	00	1	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			infra	M = 1	high	high gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 5 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	f_{LO} = 1/2 f_{VCO3} (MHz)	DV3I[14:0] = N
1	46.6100	49.6700	38.9700	7794
2	46.6300	49.8450	39.1450	7829
3	46.6700	49.8600	39.1600	7832
4	46.7100	49.7700	39.0700	7814
5	46.7300	49.8750	39.1750	7835
6	46.7700	49.8300	39.1300	7826
7	46.8300	49.8900	39.1900	7838
8	46.8700	49.9300	39.2300	7846
9	46.9300	49.9900	39.2900	7858
10	46.9700	49.9700	39.2700	7854
11	46.5100	49.6950	39.9950	7799
12	46.5300	49.7100	39.0100	7802
13	46.5500	49.7250	39.0250	7805
14	46.5700	49.7400	39.0400	7808
15	46.5900	49.7550	39.0550	7811

Korea Hand

Country Setting

Name	RA1[1:0]	RA2[1:0]	D1[1:0]	D20	D3[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	DR1I[1:0]	FRMT	GDEM
Setting	10	00	01	1	00	100	00	0	00	1	1
Value		max	D1 = 8	D2 = 8	D3 = 1			supra	M = 1	high	high gain

Channel Frequencies and 1st LO Divider, f_{Ref3} = 5 kHz

Channel Number	TX Channel Frequency (MHz)	RX Channel Frequency (MHz)	$f_{LO} = 1/2\ f_{VCO3}$ (MHz)	DV3I[14:0] = N
1	49.6700	46.6100	57.3100	11462
2	49.8450	46.6300	57.3300	11466
3	49.8600	46.6700	57.3700	11474
4	49.7700	46.7100	57.4100	11482
5	49.8750	46.7300	57.4300	11486
6	49.8300	46.7700	57.4700	11494
7	49.8900	46.8300	57.5300	11506
8	49.9300	46.8700	57.5700	11514
9	49.9900	46.9300	57.6300	11526
10	49.9700	46.9700	57.6700	11534
11	49.6950	46.5100	57.2100	11442
12	49.7100	46.5300	57.2300	11446
13	49.7250	46.5500	57.2500	11450
14	49.7400	46.5700	57.2700	11454
15	49.7550	46.5900	57.2900	11458

Korea Modulation Loop Frequencies and Dividers

N Channel	P_M	Q_M	f_{Mod} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700
11	13	107	7.515
12	13	109	7.520
13	13	111	7.525
14	13	113	7.530
15	13	115	7.535

Crystal Specifications

Drive level < 0.01 µW

Parameters	Symbol	Min.	Typ.	Max.	Unit
Load resonance frequency with 14 pF load capacitance			11.15		MHz
Load capacitance			14		pF
Frequency tolerance		–30		+30	ppm
Shunt capacitance				3.1	pF
Motional capacitance		9.2			fF (1)
Series resistance				20	Ω

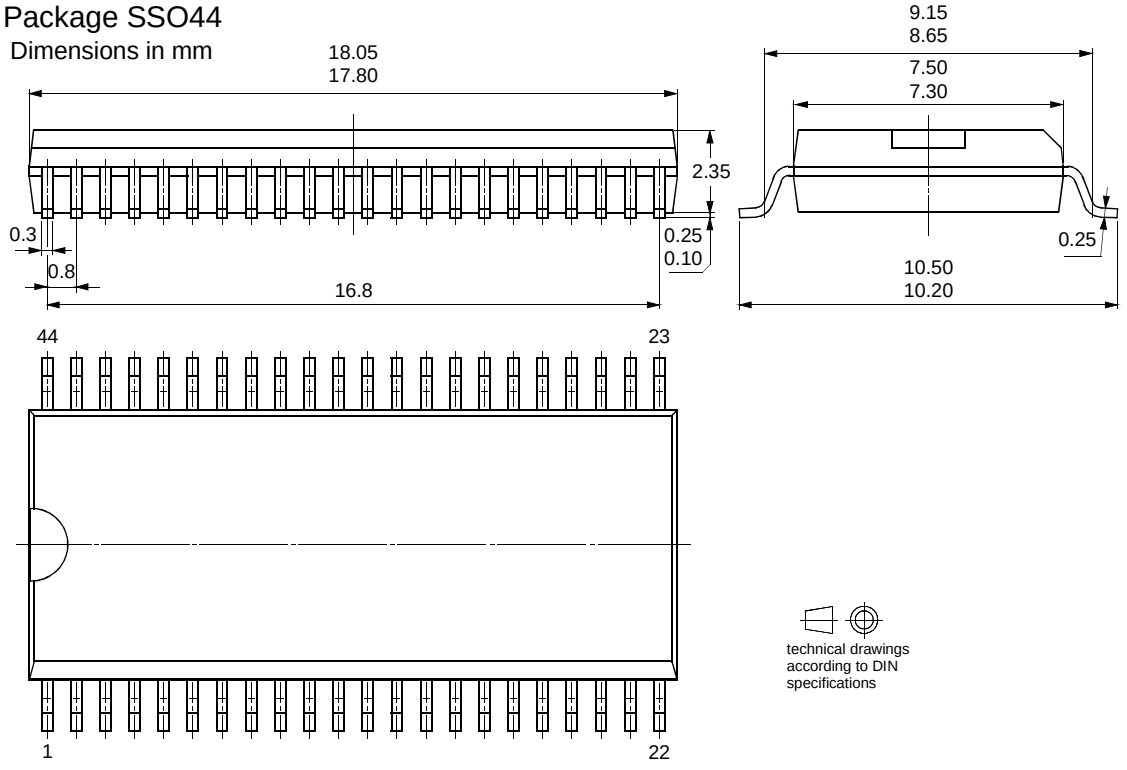
Note: (1) Necessary to stay within adjustment range of oscillator FAOS (0:2) = 0 ... 5

Ordering Information

Extended Type Number	Package	Remarks
U3600BM-NFN	SSO44	Tube
U3600BM-NFNG3	SSO44	Taped and reeled

Package Information

Package SSO44
Dimensions in mm



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