

## Features

- Pixel Size: 11  $\mu\text{m}$  x 13  $\mu\text{m}$  (13  $\mu\text{m}$  Pitch)
- High Data Output Rate: 20 MHz
- High Responsivity and Resolution Over a Wide Spectral Range: from Blue (400 nm) up to Near Infrared (1,100 nm)
- Low Dark Signal and Improved Uniformity
- Low Temporal Noise and High Dynamic Range: Over 6000/1
- Ease and Flexibility of Operation:
  - Only Two External Basic Drive Clocks
  - Choice of Internal or External Sampling and Reset
- 28-lead DIL Package
- Available with Standard Window or Antireflective Window in the Bandwidth 450 to 750 nm

## Pin Identification

Pin Number	Symbol	Designation
2	$V_{\text{OSA}}$	Video Output Signal A (Odd Channel)
3	$\Phi_{\text{ECHA}}$	A Sample-and-hold Gate Input Channel
4	$S\Phi_{\text{ECHA}}$	A Internal Sampling Clock Output Channel
5	$\Phi_{\text{RA}}$	A External Reset Clock Input Channel
9	$V_{\text{DD}}$	Output Amplifier Drain And Internal Logic Supply
10	TP3	Test Point 3
11	TP2	Test Point 2
12	VT	Register and Photosensitive Zone DC Bias
13	TP1	Test Point 1
14, 15, 28	$V_{\text{SS}}$	Substrate Bias (Ground)
16	$V_{\text{INH}}$	Internal Sampling Clock Inhibiting Input (Dc Bias)
18	$\Phi_{\text{P}}$	Transfer Clock
19	$\Phi_{\text{T}}$	Register Transport Clock
20	$V_{\text{GS}}$	Output Gate DC Bias
21	$\Phi_{\text{RB}}$	B External Reset Clock Output Channel
24	$S\Phi_{\text{ECHB}}$	B Internal Sampling Clock Output Channel
25	$\Phi_{\text{ECHB}}$	B Sample-and-hold Gate Input Channel
26	$V_{\text{OSB}}$	Video Output Signal B (Even Channel)
27	$V_{\text{DR}}$	Reset DC Bias
1, 6, 7, 8, 17, 22, 23	DNC	Do not Connect

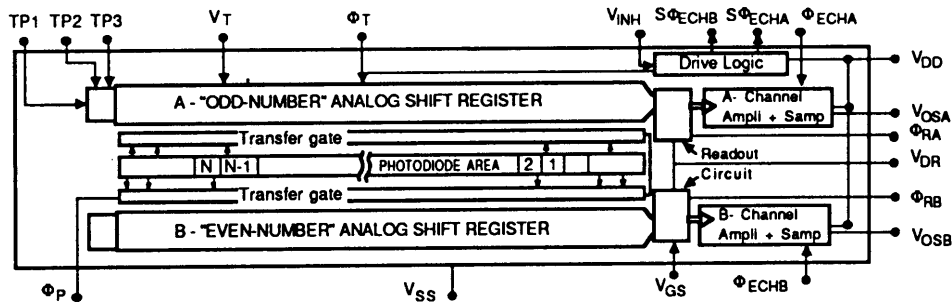
DNC	1	28	VSS
VOSA	2	27	VDR
$\Phi_{\text{ECHA}}$	3	26	VOSB
$S\Phi_{\text{ECHA}}$	4	25	$\Phi_{\text{ECHB}}$
$\Phi_{\text{RA}}$	5	24	$S\Phi_{\text{ECHB}}$
DNC	6	23	DNC
DNC	7	22	DNC
DNC	8	21	$\Phi_{\text{RB}}$
VDD	9	20	VGS
TP3	10	19	$\Phi_{\text{T}}$
TP2	11	18	$\Phi_{\text{P}}$
VT	12	17	DNC
TP1	13	16	VINH
VSS	14	15	VSS



## Linear CCD Image Sensor (2048 Pixels)

TH7841A





## Absolute Maximum Ratings\*

Storage Temperature .....	-55°C to +150°C
Operating Temperature .....	0°C to +70°C
Thermal Cycling .....	15°C/mn
Maximum Voltages:	
• Pins: 3, 5, 9, 10, 11, 13, 16, 19, 20, 21, 25, 27 .....	
-0.3V to +18V	
• Pins: 12, 18 .....	
-0.3V to +16V	
• Pins: 14, 15, 28 .....	
0V	

\*NOTICE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## Operating Range

Operating range defines the temperature limits between which the functionality is guaranteed: 0°C to 70°C.

## Operating Precautions

Shorting the video output to  $V_{SS}$  to  $V_{DD}$ , even temporarily, can permanently damage the output amplifier.

## Operating Conditions (T = 25°C)

**Table 1.** DC Characteristics

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Output Amplifier Drain Supply	V <sub>DD</sub>	14	15	16	V	
Reset DC Bias	V <sub>DR</sub>	12	13	14.5	V	(1)
Output Gate DC Bias	V <sub>GS</sub>	5.5	6	6.5	V	
Photosensitive Zone and Register DC Bias	V <sub>T</sub>	6	6.5	7	V	(2)
Substrate Bias	V <sub>SS</sub>	0.0	0.0			
Test Point 1	TP1		V <sub>DD</sub>		V	(3)
Test Points 2 and 3	TP2, TP3		V <sub>SS</sub>		V	(3)

- Notes:
1. It is recommended to maintain V<sub>DR</sub> at V<sub>DD</sub> - 2V.
  2. V<sub>T</sub> nominal = 
$$\frac{(V\Phi_T)_{high} + (V\Phi_T)_{low}}{2} \pm 5\%$$
  3. No use for operation – For testing purpose only.

## Basic Internal Configuration

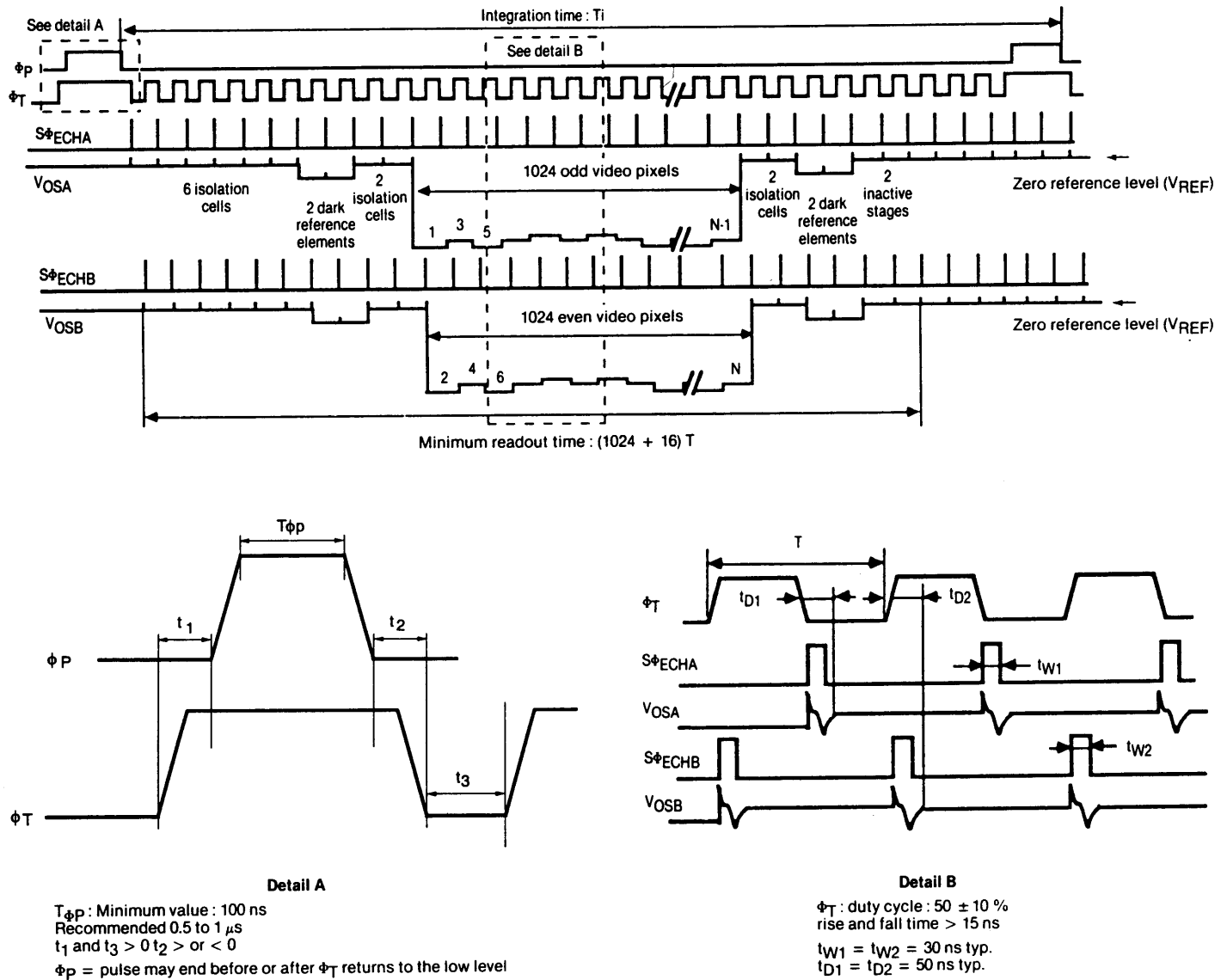
SΦ <sub>ECHA</sub> and Φ <sub>RA</sub>	internal to TH7841A
SΦ <sub>ECHB</sub> and Φ <sub>RB</sub>	

**Table 2.** Selection of Nominal Mode

Option	Implementation	Note
Internal Sampling	V <sub>INH</sub> (16) Connected to V <sub>SS</sub> SΦ <sub>ECHA</sub> (4) and Φ <sub>ECHA</sub> (3) Strapped SΦ <sub>ECHB</sub> (24) and Φ <sub>ECHB</sub> (25) Strapped	(1)
Internal Reset	Φ <sub>RA</sub> (5) and Φ <sub>RB</sub> (21) Connected to VDD	

- Note:
1. Make the straps as short as possible to avoid any parasitic coupling to these connections. The load capacitance introduced by the strap should not exceed 5 pF.

**Figure 1.** Timing Diagram — Clocks and Video Output Timing Diagram in Internal Sampling Mode



**Table 3.** Drive Clock Characteristics (see Figure 1)

Parameter	Symbol	Logic	Values			Unit	Note
			Min	Typ	Max		
Transfer Clock	$\Phi_P \Phi_T$	High	12	13	14	V	(1)
Register Transport Clock		Low	0.0	0.4	0.6		
Register Transport Clock Capacitance	$C\Phi_T$			800	1200	pF	
Transfer Clock Capacitance	$C\Phi_P$			200	300	pF	

Note: 1. Transients under 0.0V in the clock pulses will lead to charge injection, causing a localized increase in the dark signal if such spurious negative transients are present, they can be suppressed by inserting a serial resistor of appropriate value (typically 20 to 100 $\Omega$ ) in the corresponding driver output.

**Table 4.** Static and Dynamic Electrical Characteristics

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
DC Output Level	$V_{REF}$	8	10	12	V	
Output Impedance	$Z_S$		500		$\Omega$	
Register Single-stage Transfer Efficiency	CTE	99.992	99.998		%	$V_{OS} = 1V^{(1)}$
Max. Data Output Frequency	$F_S$ max.	12	20		MHz	<sup>(2)</sup>
Input Current on Pins: 3, 5, 10, 11, 12, 13, 18, 19, 20, 21, 25	$I_e$			2	$\mu A$	$V_e = 15V$ All other pins: 0V
Peak Current Sink on $\Phi_T$ Clock	$(I\Phi_T)_P$		500		mA	$t_{rise} = 15\text{ ns}$
Peak Current Sink on $\Phi_P$ Clock	$(I\Phi_P)_P$		125		mA	$t_{rise} = 15\text{ ns}$
Output Amplifier Drain Supply Current	$I_{DD}$		17		mA	$V_{INH} = 0V$ $V_{DD} = 15V$
Static Power Dissipation	$P_D$		255	300	mW	$V_{INH} = 0V$ $V_{DD} = 15V$

Notes: 1.  $V_{OS}$  = average video output voltage. Measurement excludes first and last pixels.  
2.  $F_S = 2F\Phi_T$ . The minimum clock frequency is limited by the increase in dark signal.

## Electro-optical Performance

General measurement conditions:  $T_C = 25^\circ C$ ;  $T_i = 1\text{ ms}$ ;  $F\Phi_T = 2.5\text{ MHz}$ .

Light source: tungsten filament lamp (2854 K) + BG 38 filter (2 mm thick) + F/3.5 aperture. The filter limits the spectrum to 700 nm; in these conditions,  $1\text{ }\mu J/cm^2$  corresponds to 3.5 lux.s.

Typical operating conditions; internal clock mode (see Table 2).

First and last pixels, as well as reference elements, are excluded from the specification.

Measurements taken on each output in succession.

**Table 5.** Electro-optical Performance

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Saturation Output Voltage	$V_{SAT}$	1.3	1.8	2.2	V	(1)(2)
Saturation Exposure	$E_{SAT}$		0.33		$\mu\text{J}/\text{cm}^2$	
Responsivity	R	2.5	2.9		$\text{V}/\mu\text{J}/\text{cm}^2$	
Responsivity Unbalance	$\Delta R/R$		2	8	%	(3)
Photo-response No-uniformity Peak-to-peak	PRNU		$\pm 5$	$\pm 10$	% $V_{OS}$	$V_{OS} = 50 \text{ mV to } 1\text{V}$
Contrast Transfer Function at FN (38 l p/mm)	CTF		70		%	$V_{OS} = 0.75\text{V}$
Temporal Noise in Darkness			160		$\mu\text{Vrms}$	(4)
Dynamic Range (Relative to rms Noise)	DR	3000	6000			
Average Dark Signal	$V_{DS}$		0.08	0.5	mV	(1)
Dark Signal Non-uniformity	DSNU		0.15	0.5	mV	

Notes: 1. Value measured with respect to zero reference level (see Figure 1).

2. Conversion factor is typically  $1.1 \mu\text{V}/\text{e}^-$ .

3.  $\Delta R/R$  is defined as

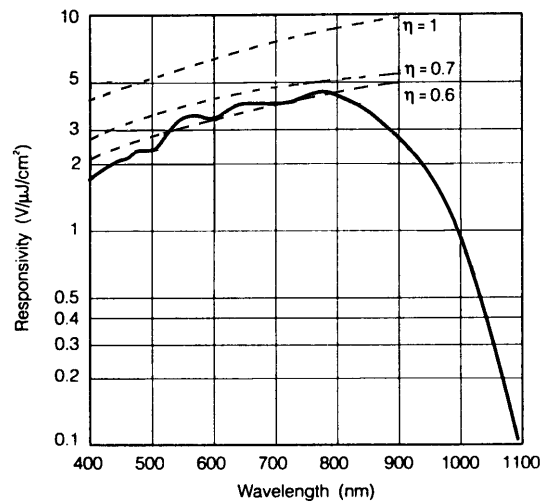
$$\frac{200|RA - RB|}{RA + RB}$$

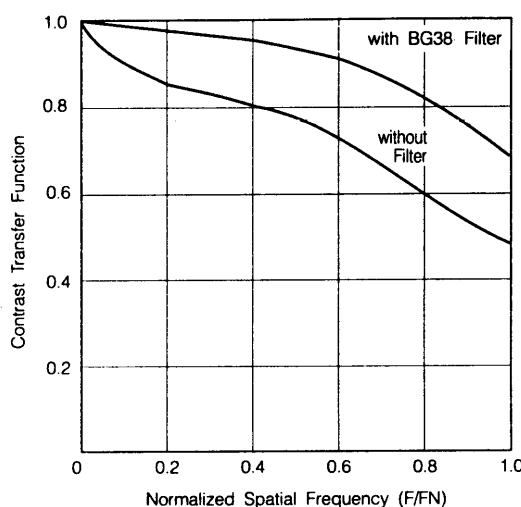
where RA is responsivity of video output A

RB is responsivity of video output B

4. Measured in Correlated Double Sampling (C.D.S.) mode.

**Figure 2.** Typical Spectral Response



**Figure 3. CTF Typical Curves (2854 K Source)**

## Electro-optical Performance Without Infrared Cut-off Filtering

The TH7841A special semiconductor process exploits the silicon's high near infrared sensitivity while maintaining good imaging performance in terms of response uniformity and resolution. Typical changes in performance with and without IR filtering are summarized below.

	With IR Cut-off Filter	No IR Cut-off Filter
Average Video Signal Due To a Given Scene Illumination	$V_{OS}$	$V_{OS} \times 4$
PRNU (Single Defects Excluded)	$\pm 5\%$	$\pm 5\%$
CTF at Nyquist Frequency	70%	50%

## Complementary Operating Modes

The TH7841A may be used in several configurations in regards to video output sampling and charge sensing reset.

### 1. Sampling options

Inhibition of internal sampling pulses allows two possibilities:

- no sampling: video output delivered in unsampled form,
- sampling by external clocks: external sampling pulses directly applied to  $\Phi_{ECHA}$ ,  $\Phi_{ECHB}$  inputs.

If internal sampling clocks  $S\Phi_{ECHA}$  and  $S\Phi_{ECHB}$  are not used, it is recommended to unpower the corresponding clock drivers, as this will greatly reduce on-chip power consumption.

### 2. External reset position

The position and period of the charge reset clocks may be optimized by using external clocks on  $\Phi_{RA}$  and  $\Phi_{RB}$  inputs. This is especially interesting to optimize the video outputs for Correlated Double Sampling (in order to reduce noise and improve S/N Ratio).

Control signals to be applied in the different configurations are shown in Table 6.

**Table 6.** Selection of Operating Modes

Option	Implementation	Note
No Sampling	$\Phi_{ECHA}$ (3) and $\Phi_{ECHB}$ (25) Connected to VDD $S\Phi_{ECHA}$ (4) and $S\Phi_{ECHB}$ (24) Unconnected $V_{INH}$ (16) Connected to $V_{DD}$	(1)
Sampling By External Clocks	Sampling Clocks Connected to $\Phi_{ECHA}$ - $\Phi_{ECHB}$ $S\Phi_{ECHA}$ and $S\Phi_{ECHB}$ Unconnected $V_{INH}$ (16) Connected to $V_{DD}$	See Figure 4 for sampling clock timing <sup>(1)</sup>
Reset Control By External Clocks	Ext. $\Phi_{RA}$ on $\Phi_{RA}$ (5) Input Ext. $\Phi_{RB}$ on $\Phi_{RB}$ (21) Input	See Figure 4 for reset clock timing

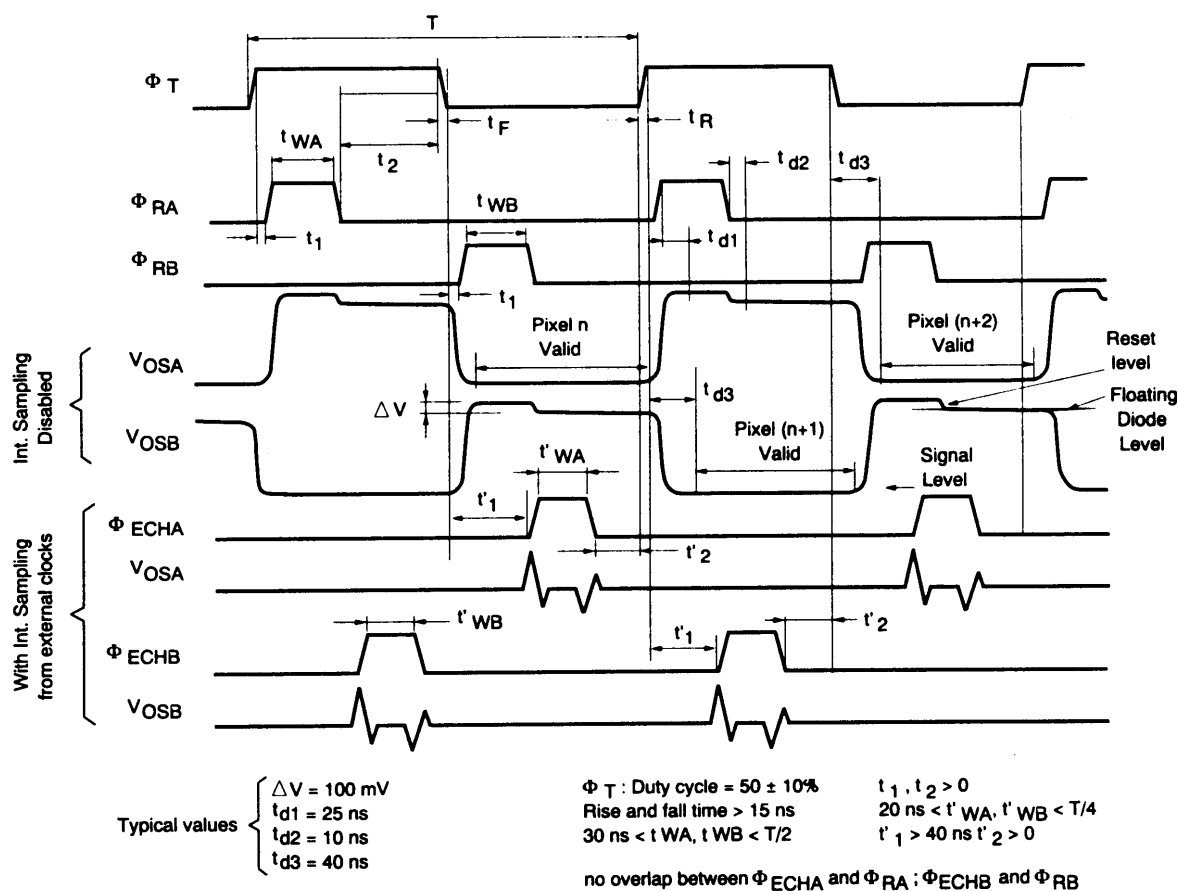
Note: 1. Drain supply current  $I_{DD}$  decreases from 10 mA to 8 mA typically when internal sampling clock is disabled ( $V_{INH} = V_{DD} = 15V$ ).

**Table 7.** External  $\Phi_{RA}$ ,  $\Phi_{RB}$ ,  $\Phi_{ECHA}$ ,  $\Phi_{ECHB}$  Clocks Characteristics

Parameter	Symbol	Logic	Values			Unit
			Min	Typ	Max	
External Reset Clock Sampling Clock	$\Phi_{RA}$ , $\Phi_{RB}$ , $\Phi_{ECHA}$ , $\Phi_{ECHB}$	High	12	13	14	V
		Low	0.0	0.4	0.6	V
Reset And Sampling Clock Capacitance	$C\Phi_{RA}$ $C\Phi_{RB}$ $C\Phi_{ECHA}$ $C\Phi_{ECHB}$			10	15	pF

Insertion of a serial resistor (typically 100 $\Omega$ ) at the driver output avoids spurious negative transients.



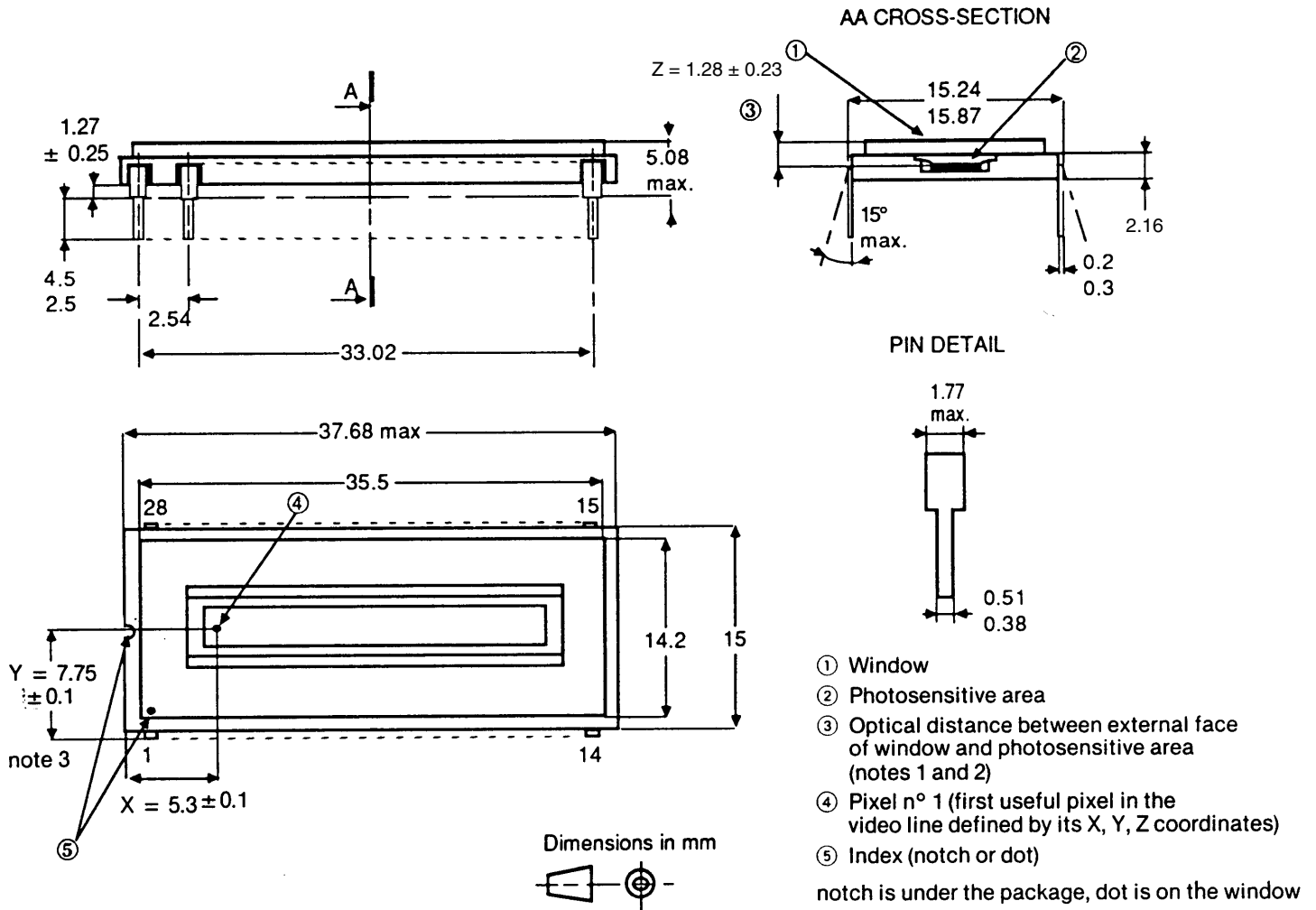
**Figure 4.** Timing Diagram — Clocks and Video Output Timing Diagram With and Without On-chip Sampling

**Table 8.** Performance Improvement with External  $\Phi_{RA}$ ,  $\Phi_{RB}$  Configuration<sup>(1)(2)</sup>

Parameter	Symbol	Values	Unit
		(Typ)	
Saturation Output Voltage	$V_{SAT}$	2.0	V
Responsivity	R	5.0	V/ $\mu\text{J}/\text{cm}^2$
Dynamic Range	DR	8,000	

Notes: 1. Electro-optical performances obtained with complementary modes are not guaranteed for standard products.  
 2. The Conversion factor is typically  $1.8 \mu\text{V}/e^-$ .

## Packaging Information

TH 7841A with standard window.



## Ordering Code

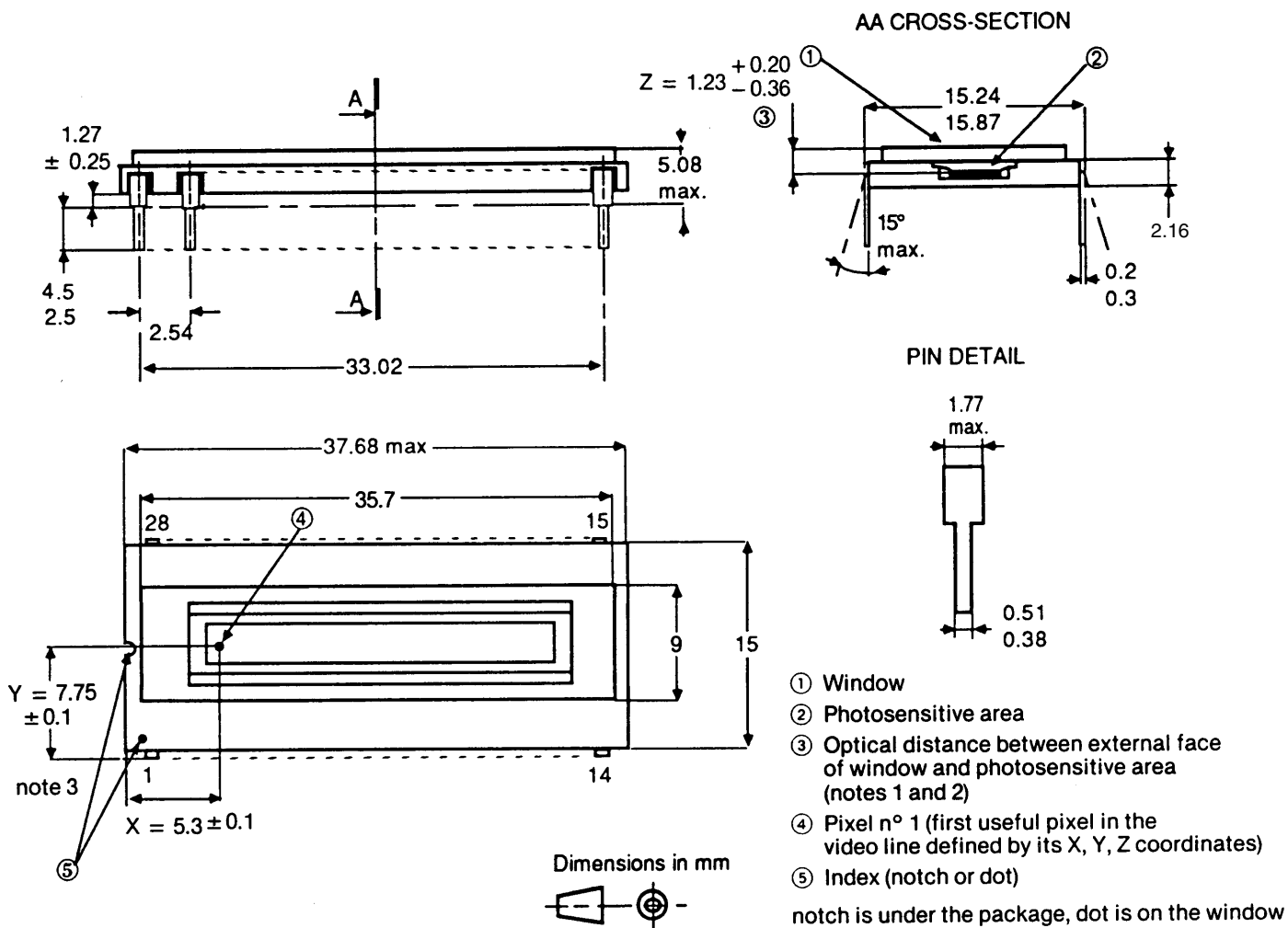
The ordering code is: TH7841 ACC

## TH7841A With Antireflective Window

Improvements in the bandwidth 450-750 nm:

- 5% increase in responsivity (typical value: 3.0 V/μJ/cm<sup>2</sup>).
- limitation of the parasitic reflections.

## Package Drawing



## Ordering Code

The ordering code is: TH7841 ACC-R



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