



Features

- Low 2.7 V supply-voltage
- Single sideband upconverters
- 100 dB control range
- Low current consumption
- Individual block power down capability
- On-chip IF PLL
- 3-wire bus programming
- Full ESD protection

Benefits

- Extended battery-operating time
- Few external components
- VCO control without voltage doubler
- One device for dual band cellular/PCS and dual mode CDMA/AMPS operation
- Only single IF-filter for all 3 modes
- Very small MLF32 package
- Simple 4-bit programming
- Excellent linearity
- Low current consumption
- Very high output power

Electrostatic sensitive device.
Observe precautions for handling.



Description

T0345 is a monolithic integrated circuit, realised using Atmel Wireless & Microcontrollers advanced silicon germanium bipolar SiGe technology. Its RF performance meets the requirements for products designed to IS-95/98 standards. It incorporates the complete transmitter chain for dual-band triple-mode cellular phones supporting CDMA (IS95) in cellular and PCS bands as well as AMPS. The device integrates an I/Q modulator, variable gain amplifier (VGA), two single side-band up-conversion mixer with fully integrated LO phase shifters, a voltage-controlled oscillator (VCO). Furthermore it includes a complete PLL with dividers, phase-frequency detector (PFD) and a charge pump. T0345 provides programmable output power in cellular and PCS band. The IC is available in a small leadless micro lead frame outline 32-pin (MLF32) package.

Ordering Information

Extended Type Number	Package	Remarks
T0345	MLF32	



Dual Band CDMA / AMPS Transmitter

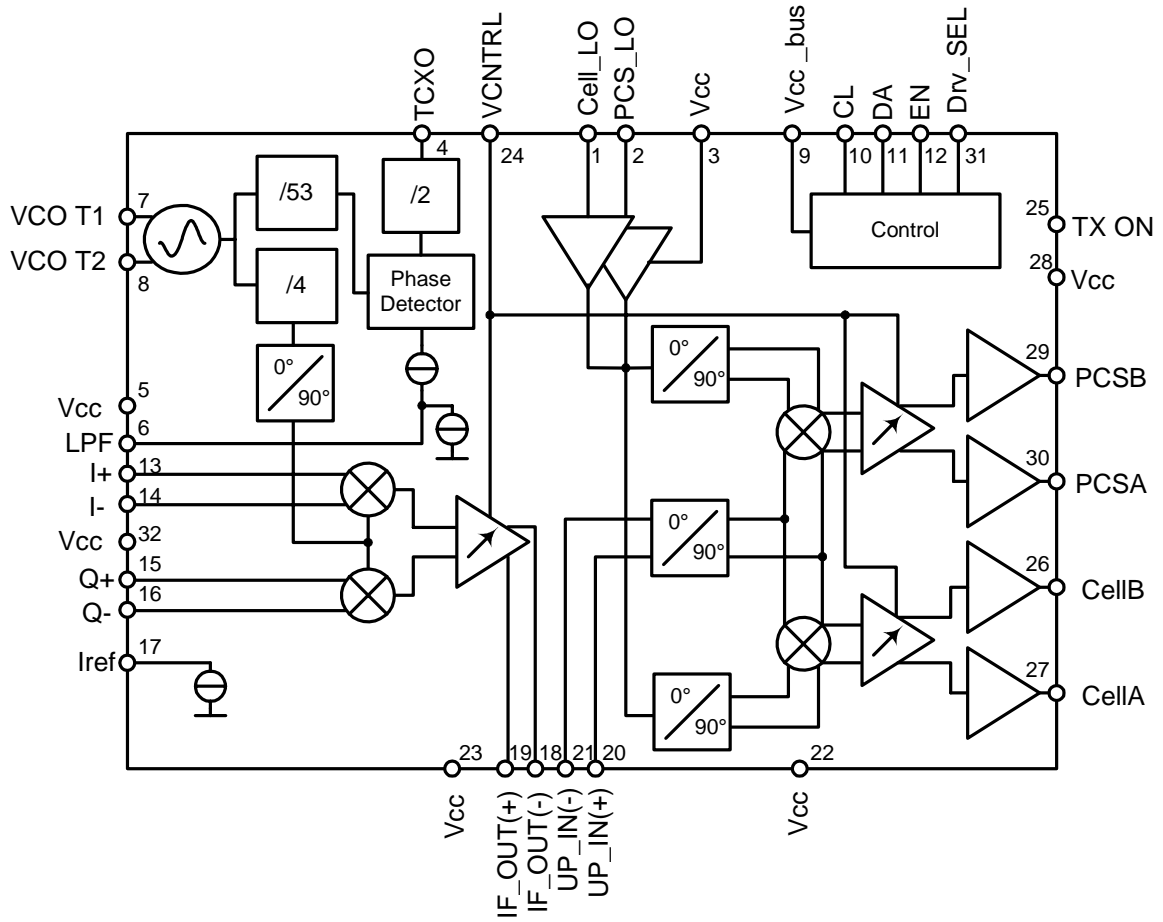
T0345

Rev. A3, 21-Nov-01



Block Diagram

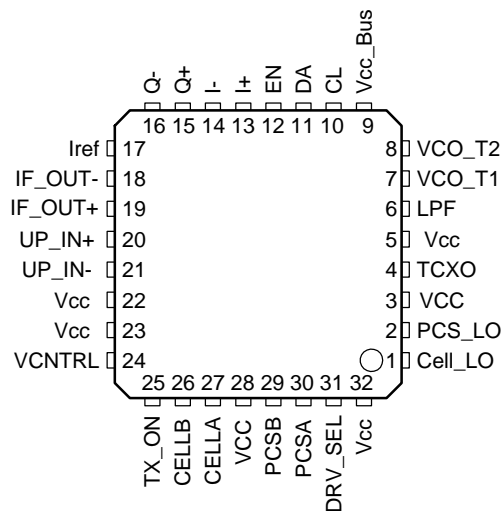
Figure 1.



Pin Description

Pin	Symbol	Function
1	Cell_LO	Local oscillator cellular 900 MHz input
2	PCS_LO	Local oscillator PCS 1800 MHz input
3	VCC	Supply voltage
4	TCXO	TCXO input
5	VCC	Supply voltage
6	LPF	Charge pump loop filter
7	VCO_T1	Voltage controlled oscillator external tank circuit
8	VCO_T2	Voltage controlled oscillator external tank circuit
9	VCC_bus	Supply voltage for serial bus interface
10	CL	3-wire bus, clock input
11	DA	3-wire bus, data input
12	EN	3-wire bus, enable strobe input
13	I+	I+ data differential signal input
14	I-	I- data differential signal input
15	Q+	Q+ data differential signal input
16	Q-	Q- data differential signal input
17	Iref	Constant current sink
18	IF_OUT(-)	Output to IF filter
19	IF_OUT(+)	Output to IF filter
20	UP_IN(+)	Input from IF filter
21	UP_IN(-)	Input from IF filter
22	VCC	Supply RF mixer supply voltage
23	VCC	Supply RF VGA supply voltage
24	VCNTRL	Gain control analog voltage input
25	TX ON	Transmitter ON (= high), power up logic control signal
26	CELLB	Cell band driver amplifier B output, open collector
27	CELLA	Cell band driver amplifier A output, open collector
28	VCC	Supply voltage
29	PCSB	PCS band driver amplifier B output, open collector
30	PCSA	PCS band driver amplifier A output, open collector
31	DRV_SEL	Driver select logic control input
32	Vcc	Supply voltage

Figure 2. Pinning



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltages V _{cc}	V _{CC}	4.0	V
Voltage at any input	V _{Vi}	$-0.5 \leq V_{Vi} \leq V_{VCC} + 0.5$	V
Current at any input/output pin	I _{I#} , I _{O#}	40mA	mA
Case temperature	T _C	-30 to +85	°C
Storage temperature	T _{stg}	-40 to +150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction-ambient MLF32	R _{thJA}	t.b.d.	K/W

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	V _{cc}	2.7 to 3.3	V
Case temperature	T _C	-30 to +85	°C

Electrical Characteristics: DC Supply

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified. Atmel Wireless & Microcontrollers' test board.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	Supply								
1.1	Supply voltages		3, 5, 22, 23, 28, 32	V_{CC}	2.7		3.3	VDC	D
1.2	Cell band mode current consumption (Driver A or Driver B activated)	High power (Pwr_up = 1, Bit1 = 0, Bit2 = 0, AB_SEL = high or low, Pout = 7.7 dBm) Low power (Pwr_up = 1, Bit1 = 0, Bit2 = 0, AB_SEL = high or low, Pout = -90 dBm)				103 90		mA mA	C
1.3	PCS band mode current consumption (Driver A or Driver B activated)	High power (Pwr_up = 1, Bit1 = 1, Bit2 = 0, AB_SEL = high or low, Pout = 8.2 dBm) Low power (Pwr_up = 1, Bit1 = 1, Bit2 = 1, AB_SEL = high or low, Pout = -90 dBm)				103 90		mA mA	C
1.4	Cell band mode current consumption (Driver A and Driver B activated)	High power (Pwr_up = 1, Bit1 = 0, Bit2 = 1, Pout = 10.7 dBm) Low power (Pwr_up = 1, Bit1 = 0, Bit2 = 1, Pout = -87 dBm)				120 90		mA mA	C
1.5	PCS band mode current consumption (Driver A and Driver B activated)	High power (Pwr_up = 1, Bit1 = 1, Bit2 = 1, Pout = 11 dBm) Low power (Pwr_up = 1, Bit1 = 1, Bit2 = 1, Pout = -87 dBm)				120 90		mA mA	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics: DC Supply

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified. Atmel Wireless & Microcontrollers' test board.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.6	Standby mode current consumption (PLL circuitry, partial IQ modulator circuitry, and serial bus interface activated)	Pwr_Up = low, Bit3 = 1				12		mA	C
1.7	Serial bus current consumption (serial bus interface activated)	Vcc_bus = High (powered on)				0.7		mA	C
1.8	Powered off	Pwr_up = low, Bit3 = 0, Vcc_bus = low (powered off)				<10		µA	C

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics: Output

Test conditions: $V_{CC} = 3.00$ VDC, Atmel Wireless & Microcontrollers' test board, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2	Cell Band RF Output (CELLA, Pin 27 and CELLB, Pin 26)								
2.1	Cell band RF output frequency range				824		849	MHz	D
2.2	Cell band RF output power	High power (Pout = 7.7 dBm)				7.7		dBm	A
2.3	Cell band RF output adjacent channel power	High power power (Pout = 7.7 dBm)				-54		dBc	A
2.4	Cell band RF output receive band noise	High power power (Pout = 7.7 dBm)				-130		dBm/Hz	C
3	PCS Band RF Output (PCSA, Pin 30 and PCSB, Pin 29)								
3.1	PCS band RF output frequency range				1750		1910	MHz	D
3.2	PCS band RF output power	High power (Pout = 8.2 dBm)				8.2		dBm	A
3.3	PCS band RF output adjacent channel power	High power (Pout = 8.2 dBm)				-54		dBc	A
3.4	PCS band RF output receive band noise	High power (Pout = 8.2 dBm)				-132		dBm/Hz	C

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics: Output

Test conditions: $V_{CC} = 3.00$ VDC, Atmel Wireless & Microcontrollers' test board, $T_c = 25^\circ\text{C}$ unless otherwise specified.

Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4	IF Section Outputs (IF_OUT(+), Pin 19 and IF_OUT(-), Pin 18)								
4.1	IF section frequency range					130.38		MHz	D
4.2	IF section output power					-13		dBm	C
4.3	IF section adjacent channel power	400 Ω differential load				-63		dBc	C
4.4	IF section carrier suppression	I/Q input: Differential Sin and Cos signals with 200 mV amplitude (400 mVpp) and 100 kHz frequency from a low ohmic source (< 1 k Ω)				-35		dBc	C
4.5	IF section Sideband Suppression	I/Q input: Differential Sin and Cos signals with 200 mV amplitude (400 mVpp) and 100 kHz frequency from a low ohmic source (< 1 k Ω)				-50		dBc	C
4.6	IF Section spurious	I/Q input: Differential Sin and Cos signals with 200 mV amplitude (400 mVpp) and 100 kHz frequency from low ohmic source (< 1 k Ω)				-60		dBc	C
4.7	IF Section Modulator Noise	@ 5 MHz off carrier				142		dBm/Hz	C
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics: Up-Converter

Test conditions: $V_{CC} = 3.00$ VDC, Atmel Wireless & Microcontrollers' test board, $T_c = 25^\circ\text{C}$ unless otherwise specified.

Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	Cellular Band Up-Converter								
5.1	Cellular up-converter output frequency				824		849	MHz	D
5.2	Cellular up-converter IF input power at UP_IN(+) and UP_IN(-)	$f_{IF} = 130.38$ MHz				-16		dBm	C
5.3	Cellular up-converter mixer LO input power at Cell_LO	$f_{LO} = 954$ MHz to 979 MHz			-10	-3		dBm	C
5.4	Cellular up-converter LO-leakage at Cell_A or Cell_B	$P_{LO} = -3$ dBm				-25	-20	dBm	C
5.5	Cellular up-converter image rejection at Cell_A or Cell_B	$P_{RF_OUT} = +7.7$ dBm				-35	-30	dBc	C
6	PCS Band Up-Converter								
6.1	PCS up-converter output frequency				1750		1910	MHz	D
6.2	PCS up-converter IF input power at UP_IN(+) and UP_IN(-)	$f_{IF} = 130.38$ MHz				-16		dBm	C
6.3	PCS up-converter mixer LO input power at PCS_LO	$f_{LO} = 1620$ MHz to 1780 MHz			-10	-3		dBm	C
6.4	PCS up-converter LO-leakage at PCSA or PCSB	$P_{LO} = -3$ dBm				-25	-20	dBm	C
6.5	PCS up-converter image rejection at PCSA or PCSB	$P_{RF_OUT} = +8.2$ dBm				-35	-30	dBc	C
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics: Analog/RF/IF Input

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified.
Atmel Wireless & Microcontrollers' test board

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	TCXO Input (TCXO, Pin 4)								
7.1	TCXO frequency range					19.68		MHz	D
7.2	TCXO input voltage range				100	250	600	mVp	C
7.3	Cell LO input (CELL_LO, Pin 1)								
7.4	Cell LO frequency range				954		979	MHz	D
7.5	Cell LO input power range	50 Ω Source			-10	-3		dBm	C
7.6	Cell LO input impedance ($\text{Re}\{Z_{\text{CELL_LO}}\}$)	Cell LO input freq. ($f_{\text{LOC}} = 966$ MHz, $\text{Pwr_Up} = 0$ or 1)				43		Ω	C
8	PCS LO Input (PCS_LO, Pin 2)								
8.1	PCS LO frequency range (f_{LOP})				1620		1780	MHz	D
8.2	PCS LO input power range (P_{LOP})	50 Ω Source			-10	-3		dBm	C
8.3	PCS LO input impedance ($\text{Re}\{Z_{\text{PCS_LO}}\}$)	PCS LO input freq. ($f_{\text{LOP}} = 1750$ MHz, $\text{Pwr_Up} = 0$ or 1)				43		Ω	C
9	Up-Converter Input (UP_IN(+) Pin 21, UP_IN(-) Pin 20)								
9.1	Up-converter frequency range (f_{VGA})	400 Ω Source				130.38		MHz	D
9.2	Up-converter power	400 Ω Source				-16		dBm	C
9.3	Up-converter input impedance					2000		Ω	D
10	Control Voltage Input (V_{CNTRL}, Pin 24)								
10.1	Control voltage input voltage range				0		2.5	VDC	D
10.2	Control voltage input impedance					3000		Ω	C
11	I/Q Modulator Base-Band Inputs (I+, I-, Q+, Q-, Pins 13, 14, 15, and 16)								
11.1	DC voltage	Referred to GND			1.35	$V_{\text{CC}}/2$	$V_{\text{CC}}/2 + 0.1$	VDC	D
11.2	Frequency range				0		2MHz	MHz	D
11.3	AC voltage	Referred to GND				130		mVpp	C
11.4	AC voltage	Differential				260		mVpp	C
12	I/Q Modulator Local Oscillator Input (VCO_Tank1, Pin 7 and VCO_Tank2, Pin 8)								
12.1	Resonator frequency					520		MHz	D
12.2	Resonator Q	Unloaded			40			None	D

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics: Logical Input

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified.
Atmel Wireless & Microcontrollers' test board

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13	Logic input electrical characteristics Applicable to PWR_UP (Pin 25), and AB_SEL (Pin 31)								
13.1	Logical high voltage level				$V_{CC} - 0.3$	3	V_{CC}	VDC	D
13.2	Logical low voltage level				0	0	0.3	VDC	D
13.3	Logical low or high current consumption					50		μA	D
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Logical Input Function Selection Table

Logical Input	Logical Low	Description
PWR_UP	High	High output power (Cellular +7dBm, PCS +8dBm)
PWR_UP	Low	Low output power (Cellular -90dBm, PCS -90dBm)
DRV_SEL	High	Transmittpath on
DRV_SEL	Low	Transmittpath off (PLL with Bit 3 active)

Note: 1. A complete truth table is shown below in "Mode Programming Truth Table"

Mode Programming Truth Table ¹⁾

Mode		3-Wire Bus Bit Inputs				Logical Inputs	
		Bit 4	Bit 3	Bit 2	Bit 1	PWR_UP	AB_SEL
PLL Off	PLL circuitry and partial IQ modulator circuitry deactivated	X	0	X	X	X	X
PLL On	PLL circuitry and partial IQ modulator circuitry activated	X	1	X	X	X	X
Transmitter On	Complete IQ modulator circuitry, RF up-converters, and IF VGA activated	X	X	X	X	High	X
Transmitter Off	Complete IQ modulator circuitry, RF up-converters, and IF VGA deactivated	X	X	X	X	Low	X
Cell Mode	Driver A (Cell Band DA A activated)	X	X	0	0	High	Low
	Driver B (Cell Band DA B activated)	X	X	0	0	High	High
	Driver A and B (Cell Band DA A and B activated)	X	X	1	0	High	X
PCS Mode	Driver A (PCS Band DA A activated)	X	X	0	1	High	Low
	Driver B (Cell Band DA B activated)	X	X	0	1	High	High
	Driver A and B (Cell Band DA A and B activated)	X	X	1	1	High	X

Note: 1. The symbol X ("do not care") means a logic input does not affect an operating mode.

Electrical Characteristics: 3-Wire Bus Signal Time

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Min./Max. limits are at $+25^\circ\text{C}$ case temperature unless otherwise specified. Atmel Wireless & Microcontrollers' test board

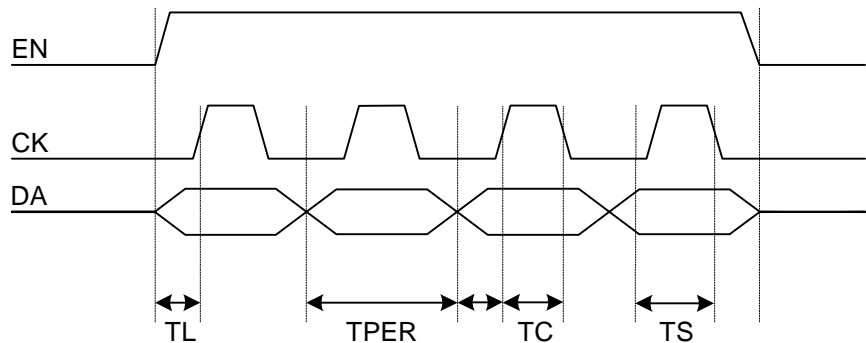
No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
14	3-wire bus, applicable to CL (Pin 10), DA (Pin 25), and EN (Pin 31)								
14.1	Clock period (TPER)					100		ns	D
14.2	Rise time (TR)					10		ns	D
14.3	Fall time (TF)					10		ns	D
14.4	Set time data to clock (TS)					35		ns	D
14.5	Hold time data to clock (TH)					35		ns	D
14.6	Clock pulse width (TC)					50		ns	D
14.7	Set time enable to clock (TL)					40		ns	D
14.8	Set time data to neg. going clock edge (TSC)					10		ns	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

3-Wire Bus Timing Diagram

Enable 'high' selects the T0345. Data are clocked into the shift register with the falling edge of the CK signal.

Figure 3.



Measurement Results

Test conditions: $V_{CC} = 3.00$ VDC, $T_c = 25^\circ\text{C}$ unless otherwise specified. Cell band freq. = 836 MHz, PCS band freq. = 1880 MHz

Figure 4.

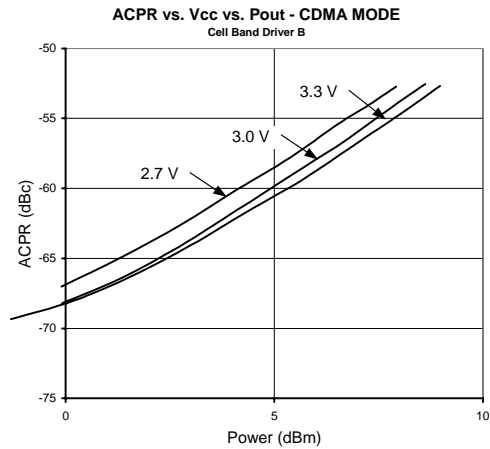


Figure 5.

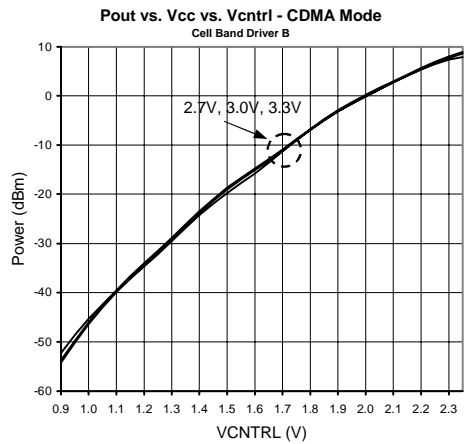


Figure 6.

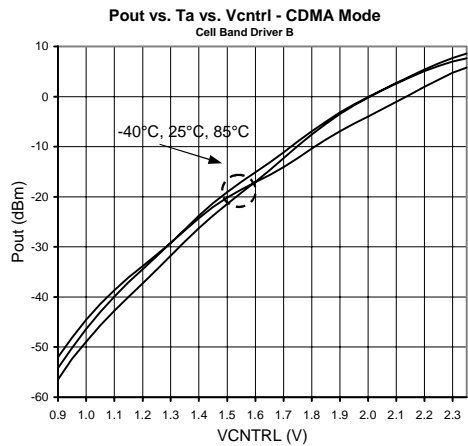


Figure 7.

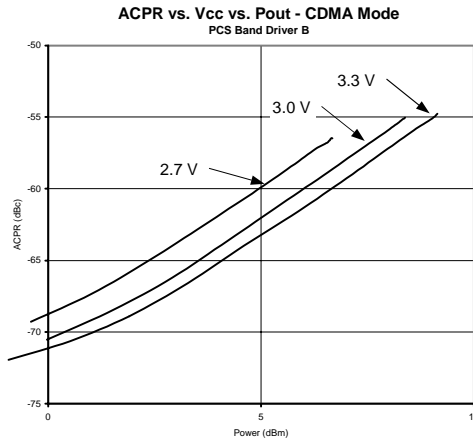


Figure 8.

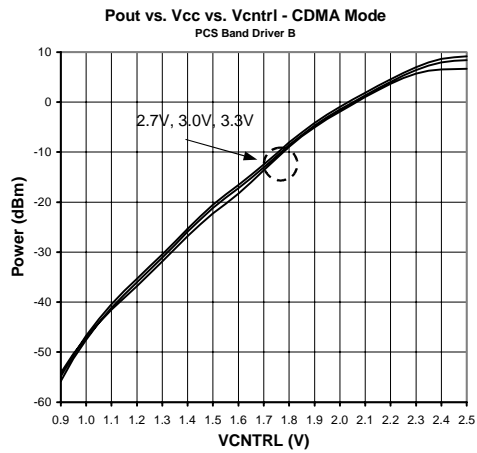
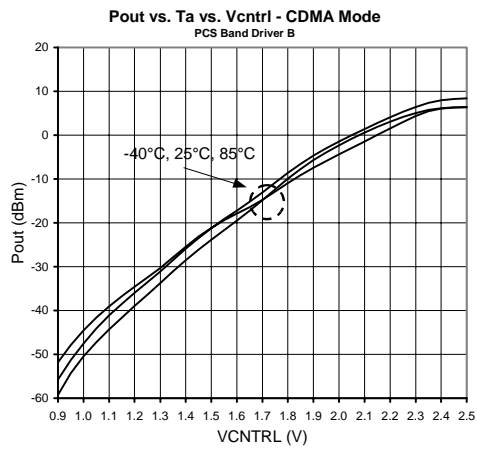
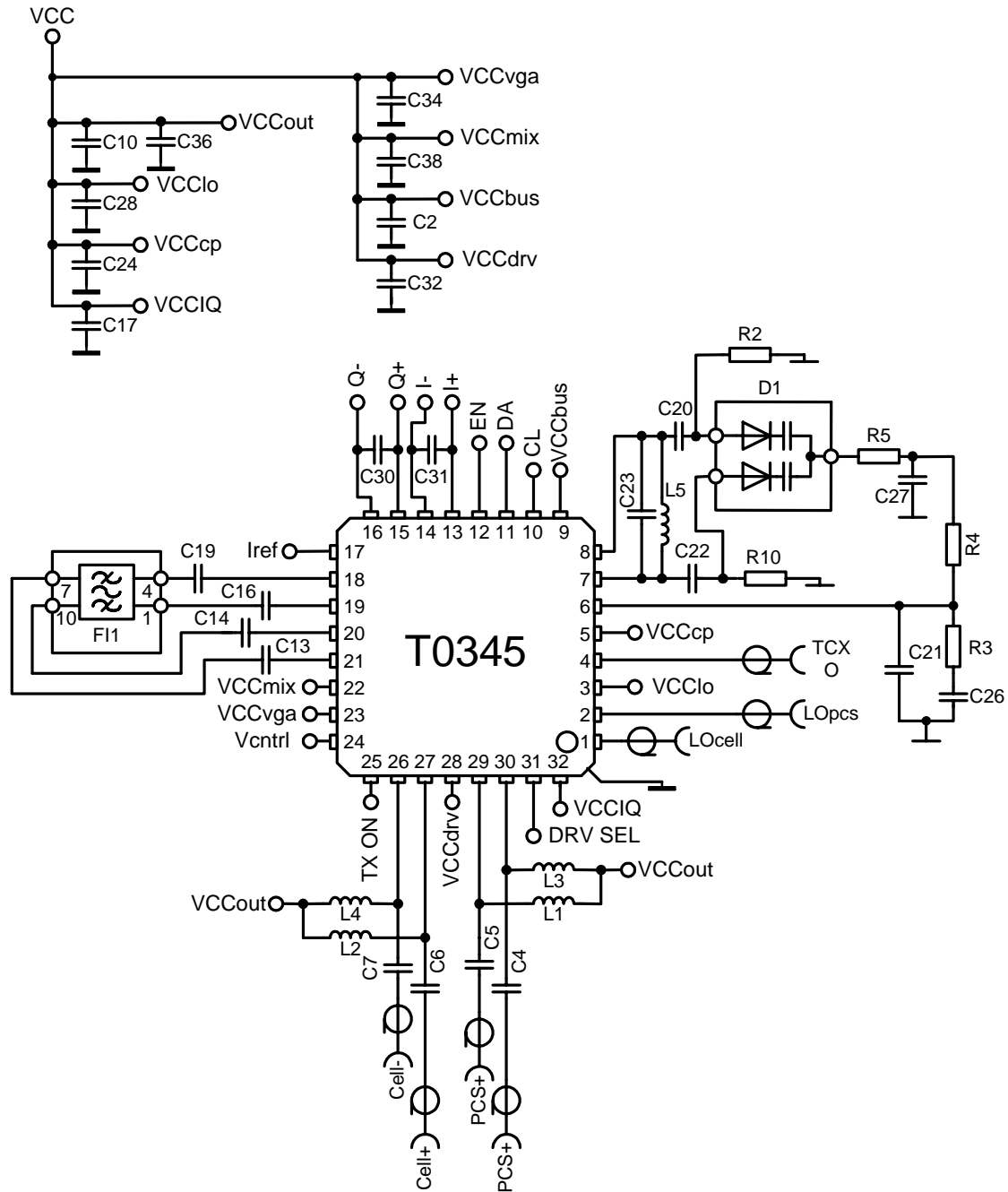


Figure 9.



Demo Board Schematics

Figure 10. Application circuit



Remark: The lines which connects both LOs, the TCXO and the output lines need to be designed with 50 Ohm impedance !

Bill of Materials of Demo Board

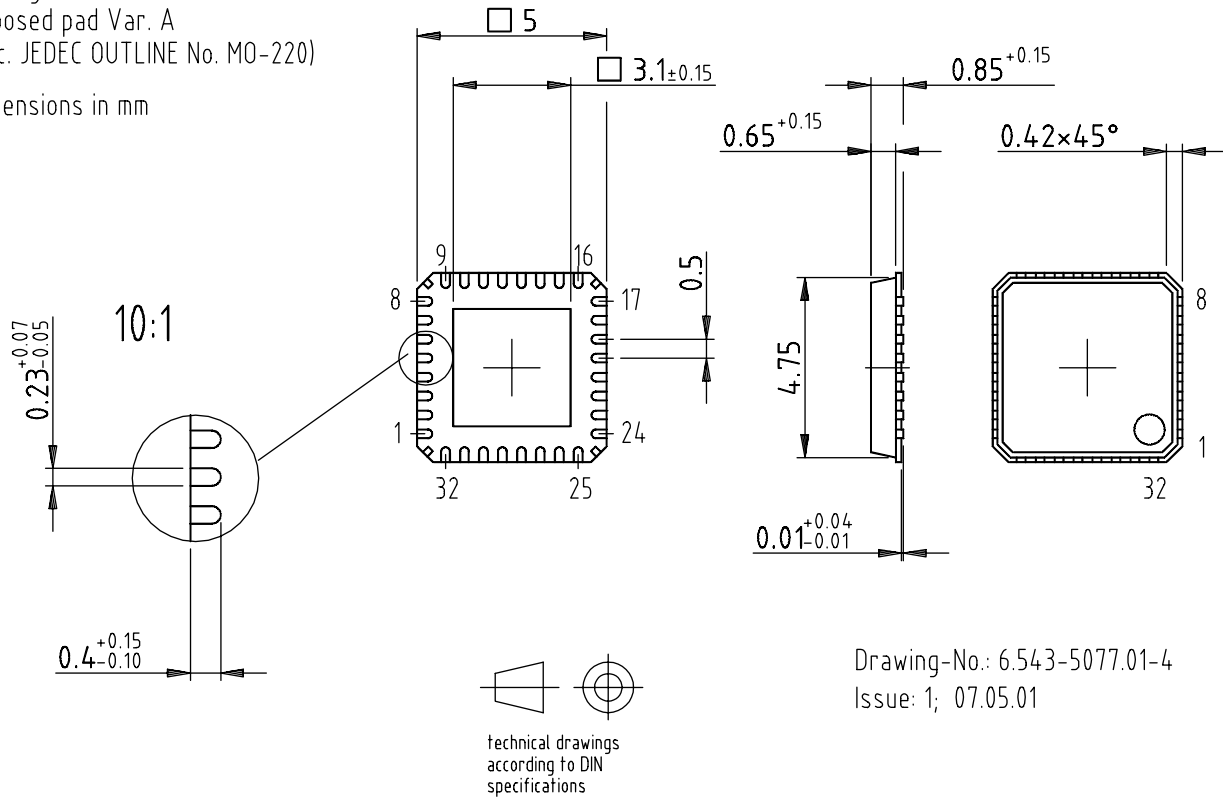
Component	Reference	Part Number	Value	Size / Package
Transmitter IC	IC3	T0345 (ATMEL)		MLF32-55
ZF-Filter	F11	LFSH30N/hc (Murata)	130.38MHz	LFSH30
Varactor-Diode	D1	BBY53-05/06 (Infineon)		SOT-23
Inductor	L5	0805CS-220_X_B (Coilcraft)	18n	0805
Inductor	L1, L3		4n7	0402 ⁽¹⁾
Inductor	L2, L4		15n	0402 ⁽¹⁾
Capacitor	C4, C5		22p	0402 ⁽¹⁾
Capacitor	C10, C17, C28, C38		100n	0402 ⁽¹⁾
Capacitor	C30, C31		68p	0402 ⁽¹⁾
Capacitor	C13, C14, C16, C19		10n	0402 ⁽¹⁾
Capacitor	C20, C22		8p2	0402 ⁽¹⁾
Capacitor	C21		82p	0402 ⁽¹⁾
Capacitor	C27		3p9	0402 ⁽¹⁾
Capacitor	C2, C6, C7, C24, C32, C34		100p	0402 ⁽¹⁾
Capacitor	C26		1n8	0402 ⁽¹⁾
Capacitor	C23		1n2	0402 ⁽¹⁾
Resistor	R5		1k	0402 ⁽¹⁾
Resistor	R3		6k8	0402 ⁽¹⁾
Resistor	R2, R10		2k7	0402 ⁽¹⁾
Resistor	R4		12k	0402 ⁽¹⁾

Note: 1. other size also possible

Package Information

Figure 11.

Package: HP-VFQFP-N32
 Exposed pad Var. A
 (acc. JEDEC OUTLINE No. MO-220)
 Dimensions in mm



Drawing-No.: 6.543-5077.01-4
 Issue: 1; 07.05.01

Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.



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