Features

- **Low-voltage and Standard-voltage Operation, VCC = 2.7V–5.5V**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K), or 2048 x 8 (16K)**
- **Two-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz Compatibility**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes Allowed**
- **Self-timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: One Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >3000V**

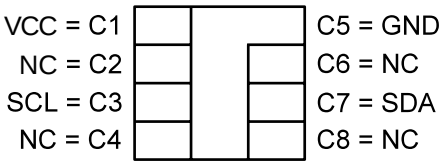
Description

The AT24C01A/02SC/04SC/08SC/16SC provide 1024/2048/4096/8192/16384 bits of serial, electrically-erasable, and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The devices are optimized for use in smart card applications where low-power and low-voltage operation may be essential. The devices are available in several standard ISO 7816 smart card modules (see *Ordering Information,* pages 12–13). All devices are functionally equivalent to Atmel serial EEPROM products offered in standard IC packages (PDIP, SOIC, TSSOP, MAP), with the exception of the slave address and write protect functions, which are not required for smart card applications.

Table 1. Pin Configuration

Pad Name	Description	ISO Module Contact
VCC	Power Supply Voltage	C1
GND	Ground	C5
SCL	Serial Clock Input	C3
SDA	Serial Data Input/Output	C7
NC	No Connect	C2, C4, C6, C8

Figure 1. Card Module Contact



Two-wire Serial EEPROM Smart Card Modules

1K (128 x 8)
2K (256 x 8)
4K (512 x 8)
8K (1024 x 8)
16K (2048 x 8)

AT24C01ASC
AT24C02SC
AT24C04SC
AT24C08SC
AT24C16SC

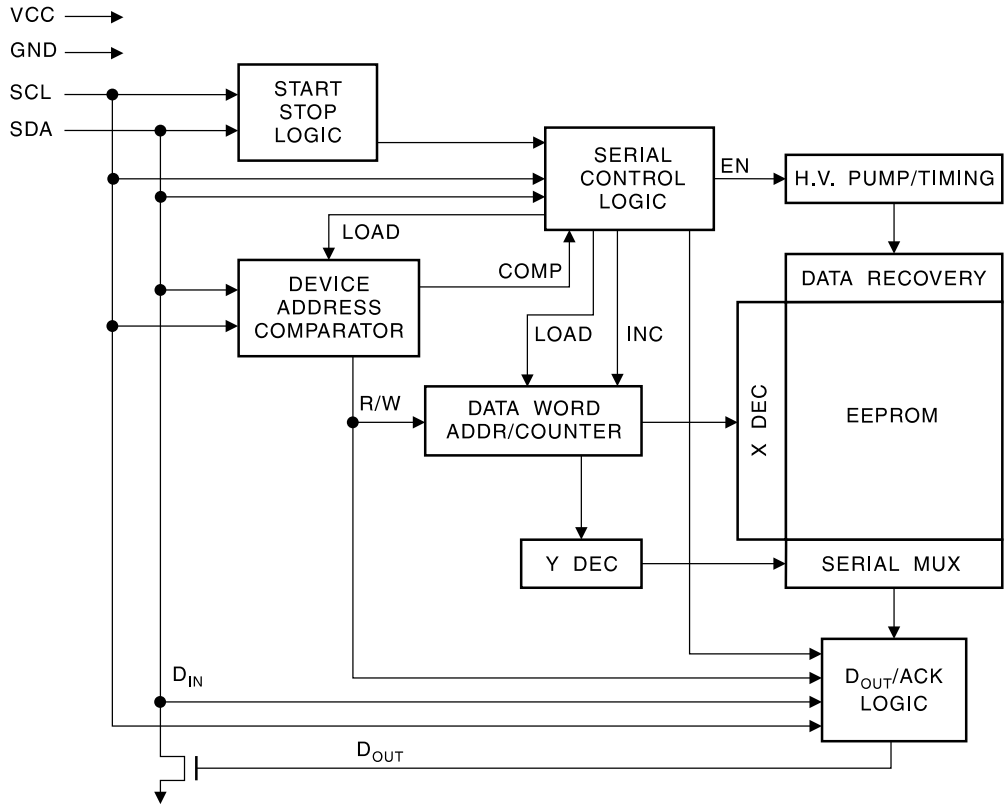
1610B–SEEPR–04/04

Absolute Maximum Ratings

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Memory Organization

AT24C01ASC, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02SC, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04SC, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08SC, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address random word addressing.

AT24C16SC, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address random word addressing.

Pin Capacitance

Table 2. Pin Capacitance[1]
Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +2.7V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Table 3. DC Characteristics[1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.7		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or GND		1.6	4.0	µA
I_{SB2}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or GND		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND		0.05	3.0	µA
V_{IL}	Input Low Level[2]		–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[2]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V

Notes: 1. Applicable over recommended operating range from: T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted)
2. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Table 4. AC Characteristics[1]

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.2		µs
t_{HIGH}	Clock Pulse Width High	0.6		µs
t_I	Noise Suppression Time[2]		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start[1]	1.2		µs

Table 4. AC Characteristics[1] (Continued)

Symbol	Parameter	Min	Max	Units
$t_{HD.STA}$	Start Hold Time	0.6		µs
$t_{SU.STA}$	Start Setup Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Setup Time	100		ns
t_R	Inputs Rise Time[2]		0.3	µs
t_F	Inputs Fall Time[2]		300	ns
$t_{SU.STO}$	Stop Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance[1]	5.0V, 25°C, Byte Mode	1M		Write Cycles

Note: 1. Applicable over recommended operating range from T_A = 0°C to +70°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

2. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK AND DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL-low time periods (see Figure 3 on page 5). Data changes during SCL-high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command (see Figure 4 on page 6).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see Figure 4 on page 6).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. Each word requires the receiver to acknowledge that it has received a valid command or data byte. During the transmission of commands from the host to the EEPROM, the EEPROM will send a zero to the host to acknowledge that it has received a valid command byte. This occurs on the ninth clock cycle of the command byte. During read operations, the host will send a zero to the EEPROM to acknowledge that it has received a valid data byte and that it requests the next sequential data byte to be transmitted during the subsequent eight clock cycles. This occurs on the ninth clock cycle of the data byte. If the host does not transmit this acknowledge bit, the EEPROM will disable the read operation and return to standby mode.

STANDBY MODE: The AT24C01ASC/02SC/04SC/08SC/16SC feature a low-power standby mode that is enabled upon power-up and after the receipt of the stop bit and the completion of any internal operations.

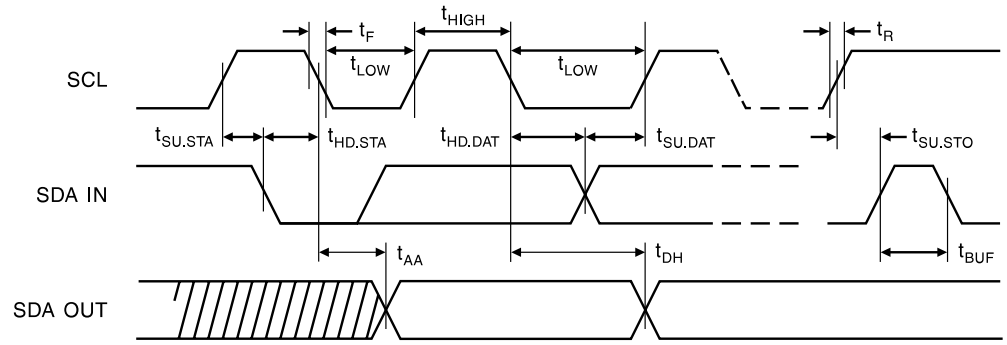
MEMORY RESET: After an interruption in protocol, power loss, or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

Timing Diagrams

Bus Timing

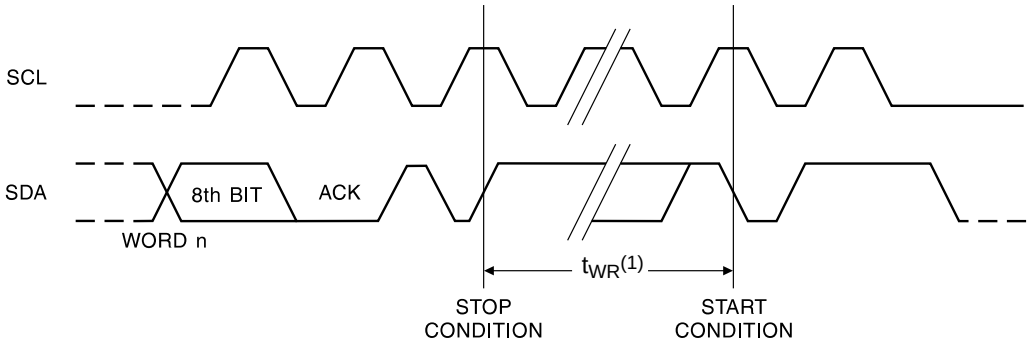
Figure 1. Bus Timing



Note: SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

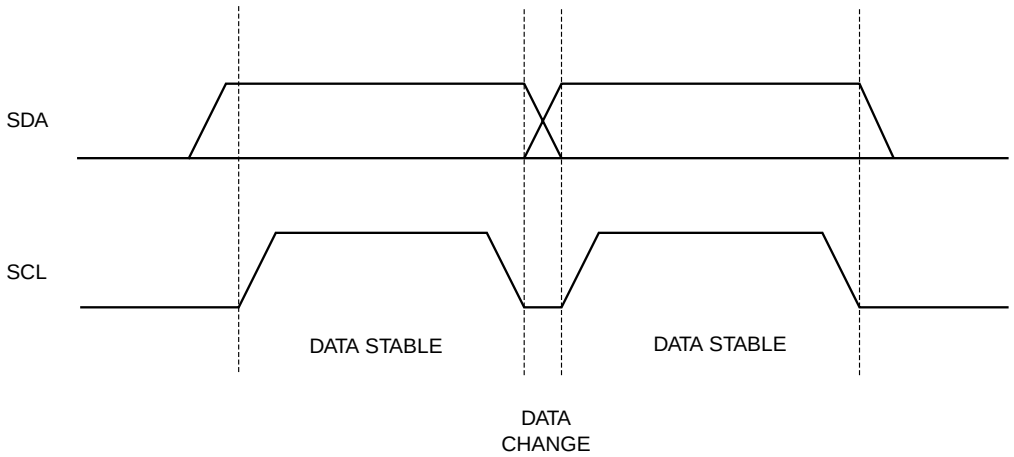
Figure 2. Write Cycle Timing



Notes: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.
2. SCL: Serial Clock, SDA: Serial Data I/O

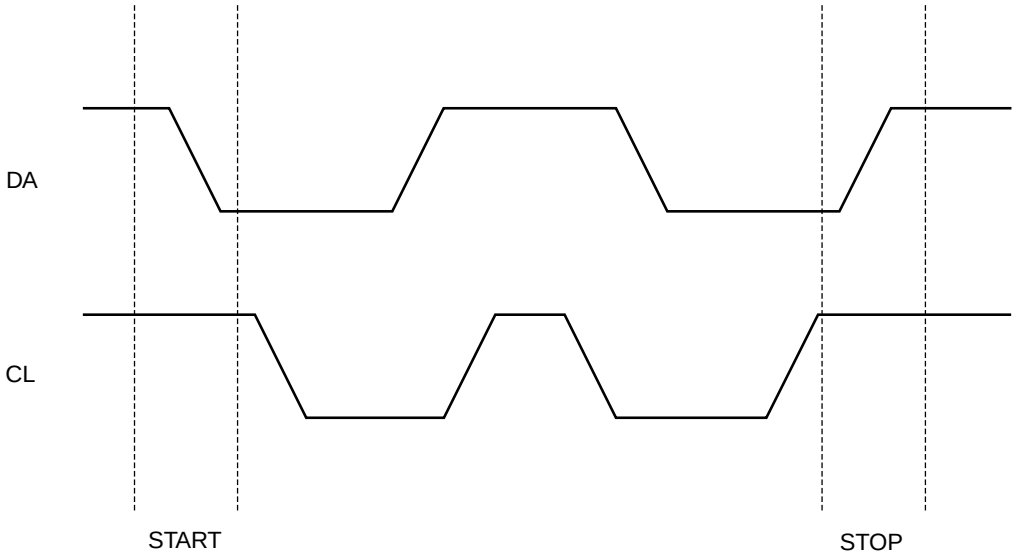
Data Validity

Figure 3. Data Validity



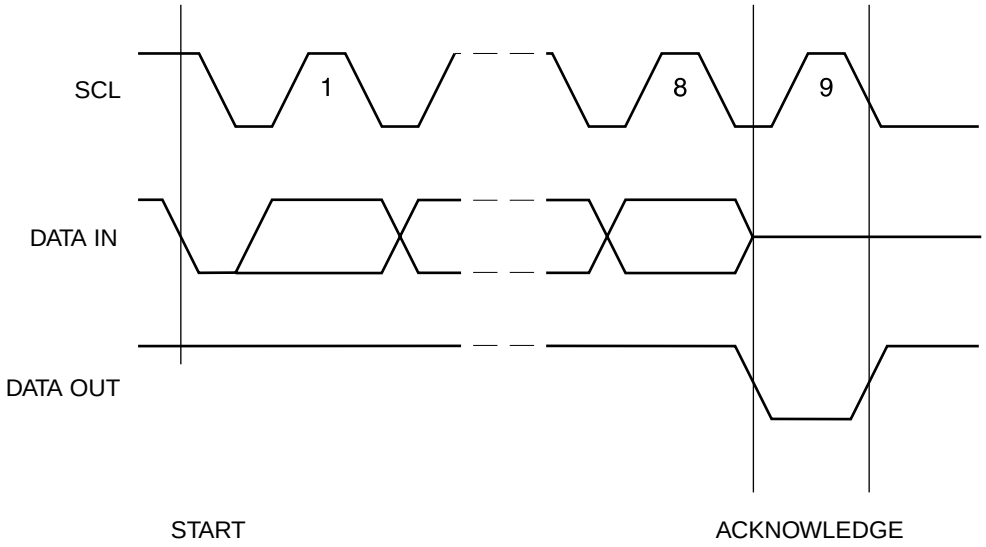
Start and Stop Definition

Figure 4. Start and Stop Definition



Output Acknowledge

Figure 5. Output Acknowledge



Device Addressing

The 1K, 2K, 4K, 8K, and 16K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 6 on page 7).

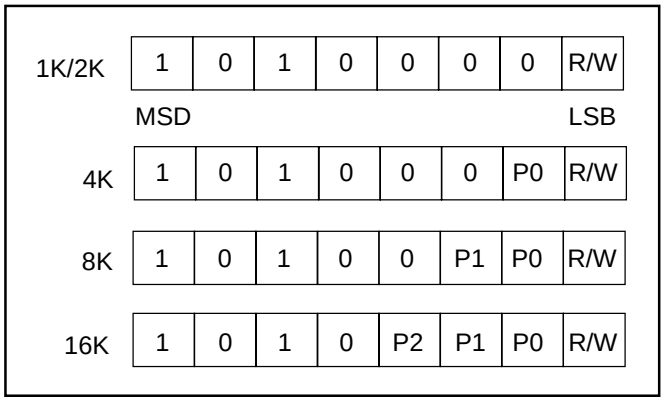
The device address word consists of a mandatory “1”, “0”, “1”, “0” sequence for the first four most significant bits as shown. This is common to all the serial EEPROM devices.

The next three bits of the device address word are the most significant data word address bits for the AT24C16SC (16K), which requires a total of 11 address bits. The AT24C08SC (8K) requires only 10 total word address bits. The most significant two bits are included in the device address word. The unused bit of the device address word should be set to “0”. The AT24C04SC (4K) requires only nine total data word address bits. The most significant bit is included in the device address word. The two unused bits of the device address word should be set to “0”. The AT24C02SC (2K) and AT24C01ASC (1K) do not require any address bits in the device address word. The three unused bits of the device address word should be set to “0”.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0” (ACK). If a successful compare is not made, the chip will return to a standby state (NO ACK).

Figure 6. Device Address

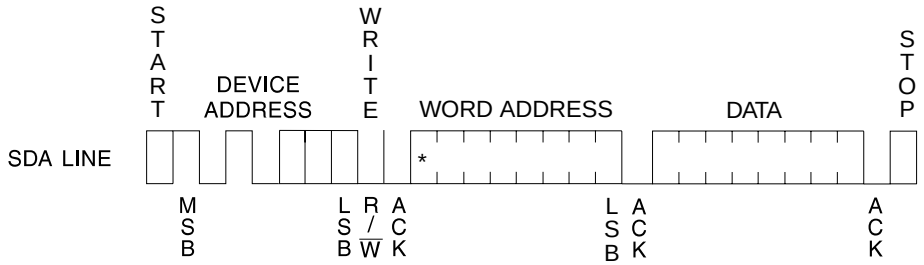


Note: P0, P1, P2 = Data word address bits

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” (ACK) and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0” (ACK) and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 7).

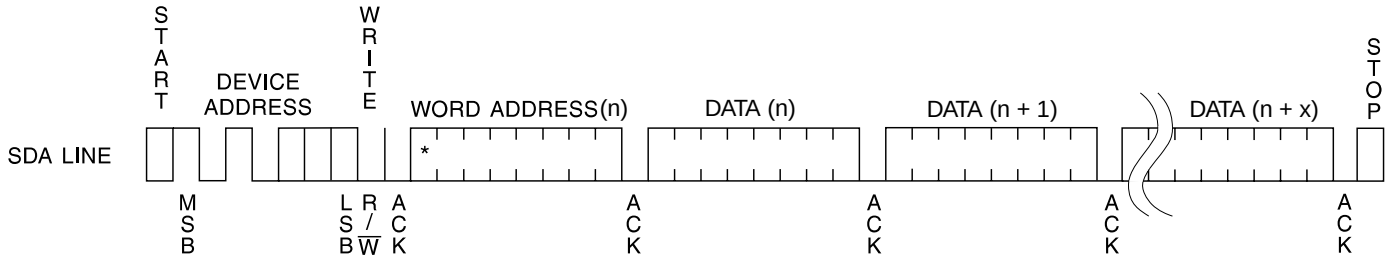
Figure 7. Byte Write



PAGE WRITE: The 1K/2K EEPROM is capable of an 8-byte page write, and the 4K, 8K, and 16K devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 7 (1K/2K) or 15 (4K, 8K, 16K) more data words. The EEPROM will respond with a “0” (ACK) after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 8).

Figure 8. Page Write



Note: * = DON’T CARE bit for 1K

The data word address lower three (1K/2K) or four (4K, 8K, 16K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (1K/2K) or 16 (4K, 8K, 16K) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed

will the EEPROM respond with a “0” (ACK), allowing the read or write sequence to continue.

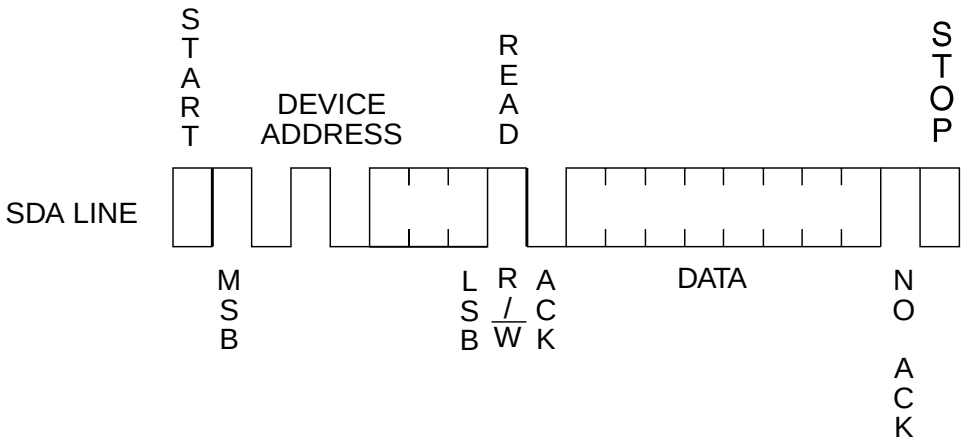
Read Operations

Read operations are initiated the same way as write operations, with the exception that the read/write select bit in the device address word is set to “1”. There are three read operations: current address read, random address read, and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “rollover” during read is from the last byte of the last memory page to the first byte of the first page. The address “rollover” during write is from the last byte of the current page to the first byte of the same page.

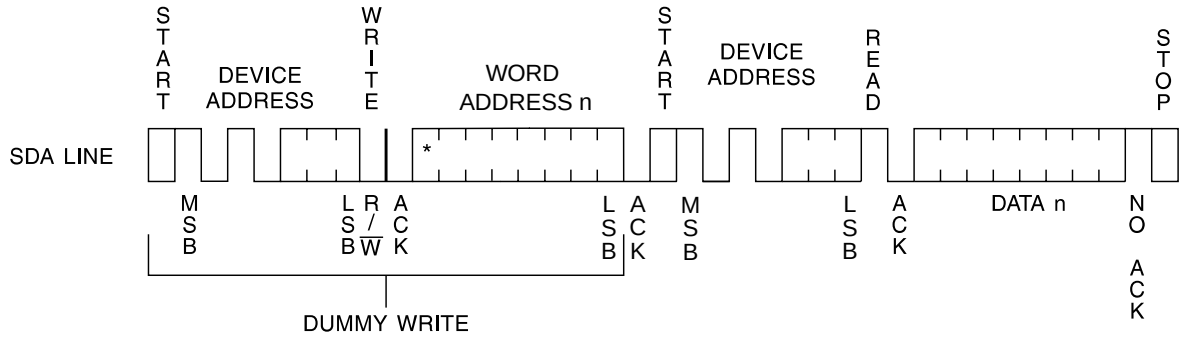
Once the device address with the read/write select bit set to “1” is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input “0” but does generate a following stop condition (refer to Figure 9)

Figure 9. Current Address Read.



RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” (NO ACK) but does generate a following stop condition (refer to Figure 10).

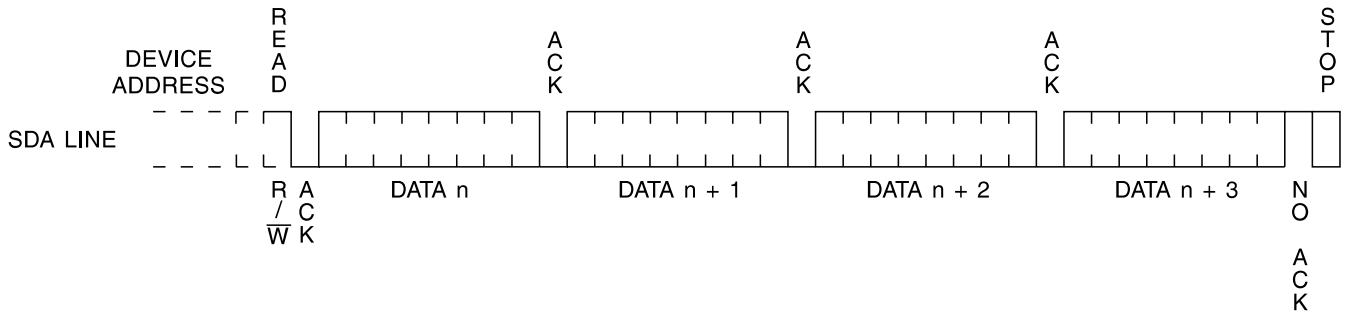
Figure 10. Random Read



Note: * = DON’T CARE bit for 1K)

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “rollover” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a “0” (NO ACK) but does generate a following stop condition (refer to Figure 11).

Figure 11. Sequential Read



AT24C01ASC Ordering Information

Ordering Code	Package	Voltage Range	Operation Range
AT24C01ASC-09ET	M2 – E Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C01ASC-09GT	M3 – G Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C01ASC-09HT	M3 – H Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C01ASC-09PT	M2 – P Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C01ASC-10WI	7 mil Wafer	2.7V–5.5V	Industrial (–40°C–85°C)

AT24C02SC Ordering Information

Ordering Code	Package	Voltage Range	Operation Range
AT24C02SC-09ET	M2 – E Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C02SC-09PT	M2 – PModule	2.7V–5.5V	Commercial (0°C–70°C)
AT24C02SC-10WI	7 mil Wafer	2.7V–5.5V	Industrial (–40°C–85°C)

AT24C04SC Ordering Information

Ordering Code	Package	Voltage Range	Operation Range
AT24C04SC-09ET	M2 – E Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C04SC-09PT	M2 – PModule	2.7V–5.5V	Commercial (0°C–70°C)
AT24C04SC-10WI	7 mil Wafer	2.7V–5.5V	Industrial (–40°C–85°C)

AT24C08SC Ordering Information

Ordering Code	Package	Voltage Range	Operation Range
AT24C08SC-09ET	M2 – E Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C08SC-09PT	M2 – PModule	2.7V–5.5V	Commercial (0°C–70°C)
AT24C08SC-10WI	7 mil Wafer	2.7V–5.5V	Industrial (–40°C–85°C)

AT24C16SC Ordering Information

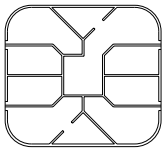
Ordering Code	Package	Voltage Range	Operation Range
AT24C16SC-09ET	M2 – E Module	2.7V–5.5V	Commercial (0°C–70°C)
AT24C16SC-09PT	M2 – PModule	2.7V–5.5V	Commercial (0°C–70°C)
AT24C16SC-10WI	7 mil Wafer	2.7V–5.5V	Industrial (–40°C–85°C)

Package Type[1]	Description
M2 – P Module	M2 ISO 7816 Smart Card Module with Atmel Logo
M2 – E Module	M2 ISO 7816 Smart Card Module
M3 – G Module	M3 ISO 7816 Smart Card Module
M3 – H Module	M3 ISO 7816 Smart Card Module with Atmel Logo

Note: 1. Formal drawings may be obtained from an Atmel sales office.

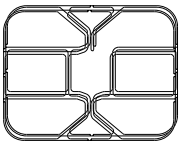
Smart Card Modules

Ordering Code: 09ET-00



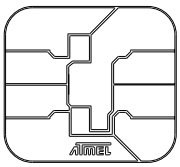
Module Size: **M2-00**
Dimension*: 12.6 x 11.4 [mm]
Glob Top: Clear, Round: ∅ 8.0 [mm] max
Thickness: 0.58 [mm] max
Pitch: 14.25 [mm]

Ordering Code: 09GT-00



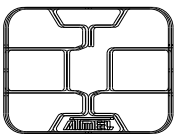
Module Size: **M3**
Dimension*: 10.6 x 8.0 [mm]
Glob Top: Clear, Round: ∅ 6.9 [mm] max
Thickness: 0.58 [mm] max
Pitch: 9.5 [mm]

Ordering Code: 09PT-00



Module Size: **M2**
Dimension*: 12.6 x 11.4 [mm]
Glob Top: Square: 8.8 x 8.8 [mm]
Thickness: 0.58 [mm]
Pitch: 14.25 [mm]

Ordering Code: 09HT-00



Module Size: **M3**
Dimension*: 10.6 x 8.0 [mm]
Glob Top: Clear, Round: ∅6.9 [mm]
Thickness: 0.58 [mm] max
Pitch: 9.5 [mm]

*Note: The module dimensions listed refer to the dimensions of the exposed metal contact area. The actual dimensions of the module after excise or punching from the carrier tape are generally 0.4 mm greater in both directions (i.e., a punched M2 module will yield 13.0 x 11.8 mm).

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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e-mail
literature@atmel.com

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http://www.atmel.com

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