Features

- **Atmel Advanced System Bus (ASB) Arbitration**
- **Customized Options**
  - **Number of Masters (2 to 7)**
  - **Priority of Masters**
  - **Possibility of Inserting Master Hand-over Cycle for Each Master**
- **Atmel AMBA™ Master Compliant**
- **Fully Scan Testable up to 96% Fault Coverage**

32-bit Embedded Core Peripheral

Arbiter

Description

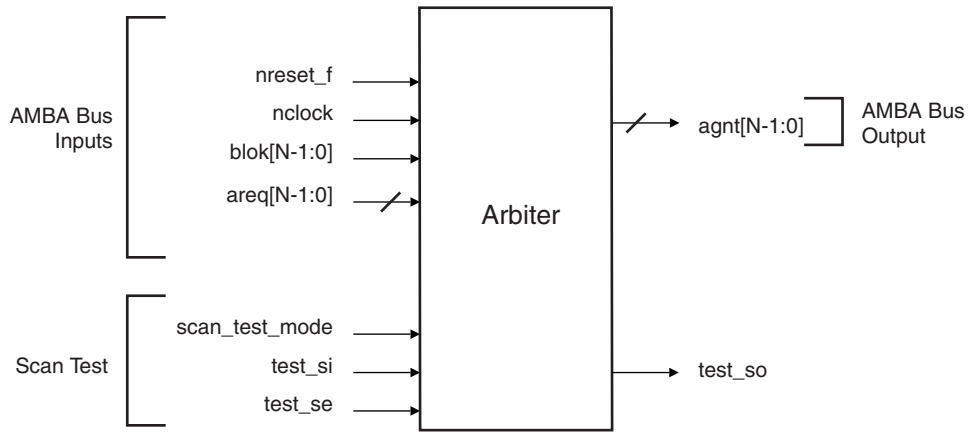
The Advanced System Bus (ASB), part of the Advanced Microcontroller Bus Architecture (AMBA), supports the connection of multiple processors. Therefore, it requires an arbiter to ensure that only one bus master has write access to the ASB at any particular point in time. Each bus master can request the bus; the Arbiter decides which master has the highest priority and issues a grant accordingly. A hand-over cycle is inserted if required.

Each master is connected to the Arbiter via two signals:

- A request signal areq: output from the master, input to the arbiter
- A grant signal agnt: input to the master, output from the arbiter

For further information on the AMBA structure, Master Signals Manager and Read Data Manager, refer to the ARM7TDMI™ System Architecture datasheet, Literature Number 1353.

Figure 1. Arbiter Symbol



Scan Test Configuration

The coverage is maximum if all non-scan inputs can be controlled and all non-scan outputs can be observed. In order to achieve this, the ATPG vectors must be generated on the entire circuit (top level) which includes the Arbiter or all Arbiter I/Os must have a top-level access and ATPG vectors must be applied to these pins.

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Table 1. Pin Description

Name	Type	Source/Destination	Description
AMBA Bus Inputs			
nreset_f	Input	From Reset Controller	System reset for parts synchronized on the falling edge of the ASB clock (nclock). Active low.
nclock	Input		ASB system clock.
blok[N(1)-1:0]	Input	From Masters	Locked transfers. Active high.
areq[N(1)-1:0]	Input	From Masters	Bus request. Each master has a corresponding areq signal. Active high.
agnt[N(1)-1:0]	Output	To Masters	Bus grant. Each master has a corresponding agnt signal. Active high.
Scan Test			
scan_test_mode	Input		For scan test only. This input must be set to 1 only during scan test. Must be set to 0 in normal operating mode.
test_se	Input		Test scan shift enabled when tied to 1.
test_si(2)	Input		Test scan input (input of the scan chain).
test_so(2)	Output		Test scan output (output of the scan chain).

Notes: 1. N = Number of masters
2. The scan chain uses the clock nclock.

Operating in an AMBA System

Figure 2. AMBA Data Buses

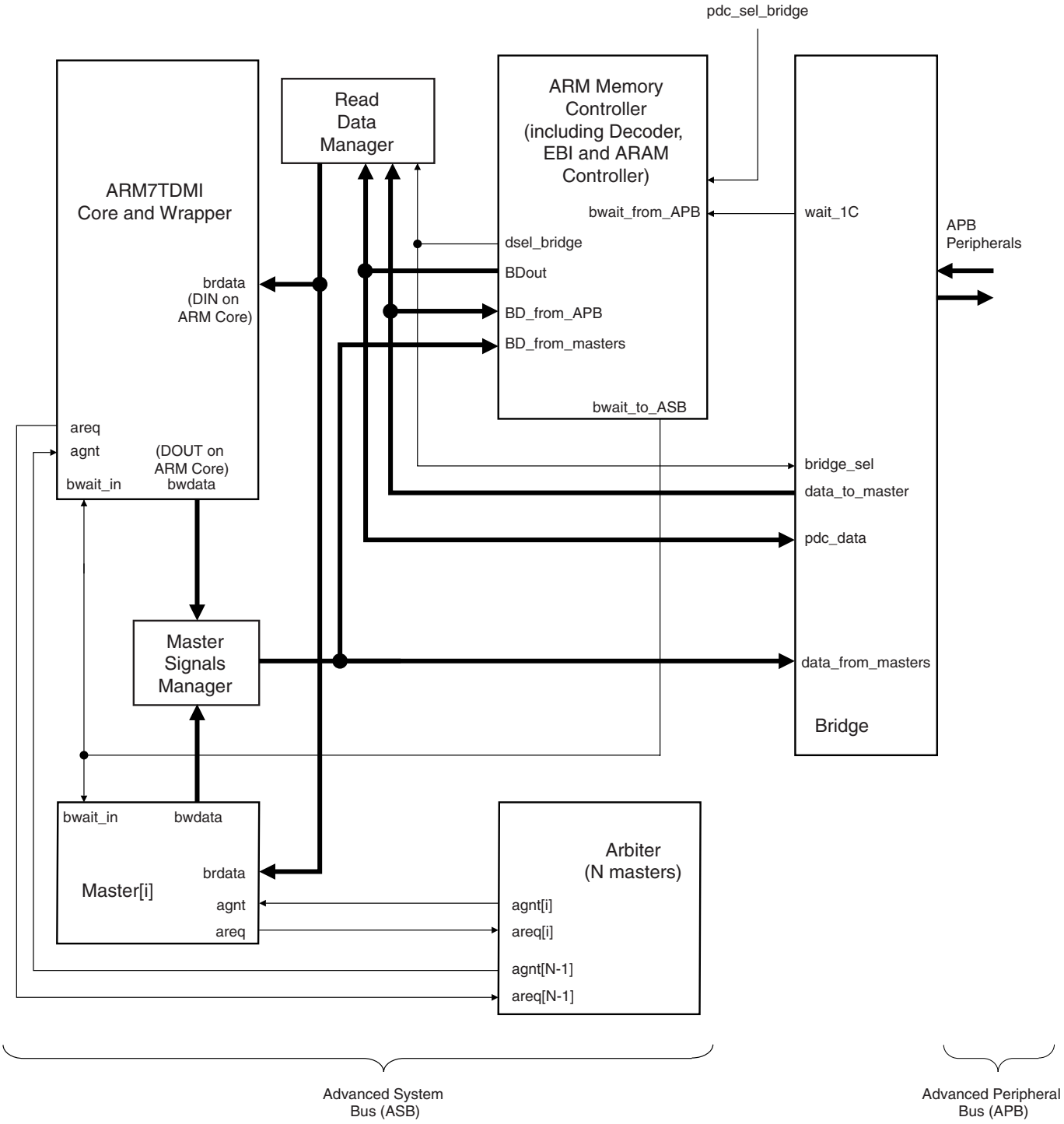
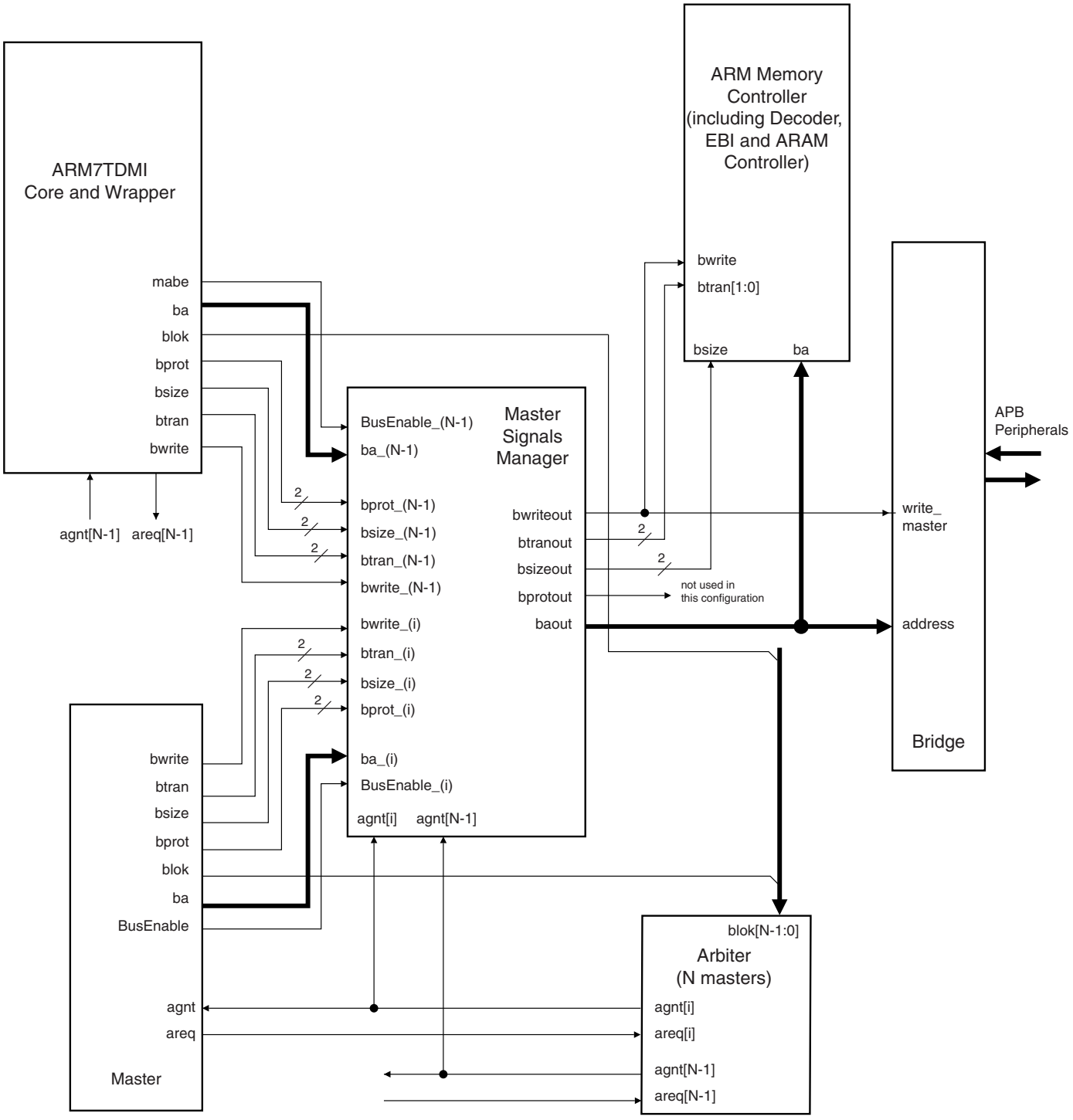


Figure 3. Master Control Signals



Functional Description

The configuration described below is an example in which the arbiter manages six masters. The waveforms which follow use the same configuration.

The arbitration scheme of this implementation is a simple priority encoded scheme where the highest priority master requesting the ASB is granted.

Note: The priority order is defined differently during reset.

Priority

In operational mode (reset inactive), the priority order is defined Table 2 from the highest priority to the lowest priority. If no request is present, the default master is granted and is in charge of driving BTRAN to a valid value.

Table 2. Priority Level

Priority Level	Connection	Example of Master
1	areq[0] and agnt[0]	Default master
2	areq[1] and agnt[1]	Debug
3	areq[2] and agnt[2]	DMA
4	areq[3] and agnt[3]	PDC
5	areq[4] and agnt[4]	Coprocessor core
6	areq[5] and agnt[5]	ARM® Core

Note: During reset (active low), only the default master can be granted control of the bus. Therefore, whatever the value of areq, agnt[5:0] is 000001.

Table 3. Arbitration Examples

Request	Granted Response
areq[5:0] = UUUUU1	agnt [5:0] = 000001
areq[5:0] = UUUU10	agnt [5:0] = 000010
areq[5:0] = UUU100	agnt [5:0] = 000100
areq[5:0] = UU1000	agnt [5:0] = 001000
areq[5:0] = U10000	agnt [5:0] = 010000
areq[5:0] = 100000	agnt [5:0] = 100000
areq[5:0] = 000000	agnt [5:0] = 000001
Therefore:	
areq[5:0] = 000101	agnt [5:0] = 000001
areq[5:0] = 011101	agnt [5:0] = 000001
areq[5:0] = 111110	agnt [5:0] = 000010

Note: U takes the place of 0 or 1.

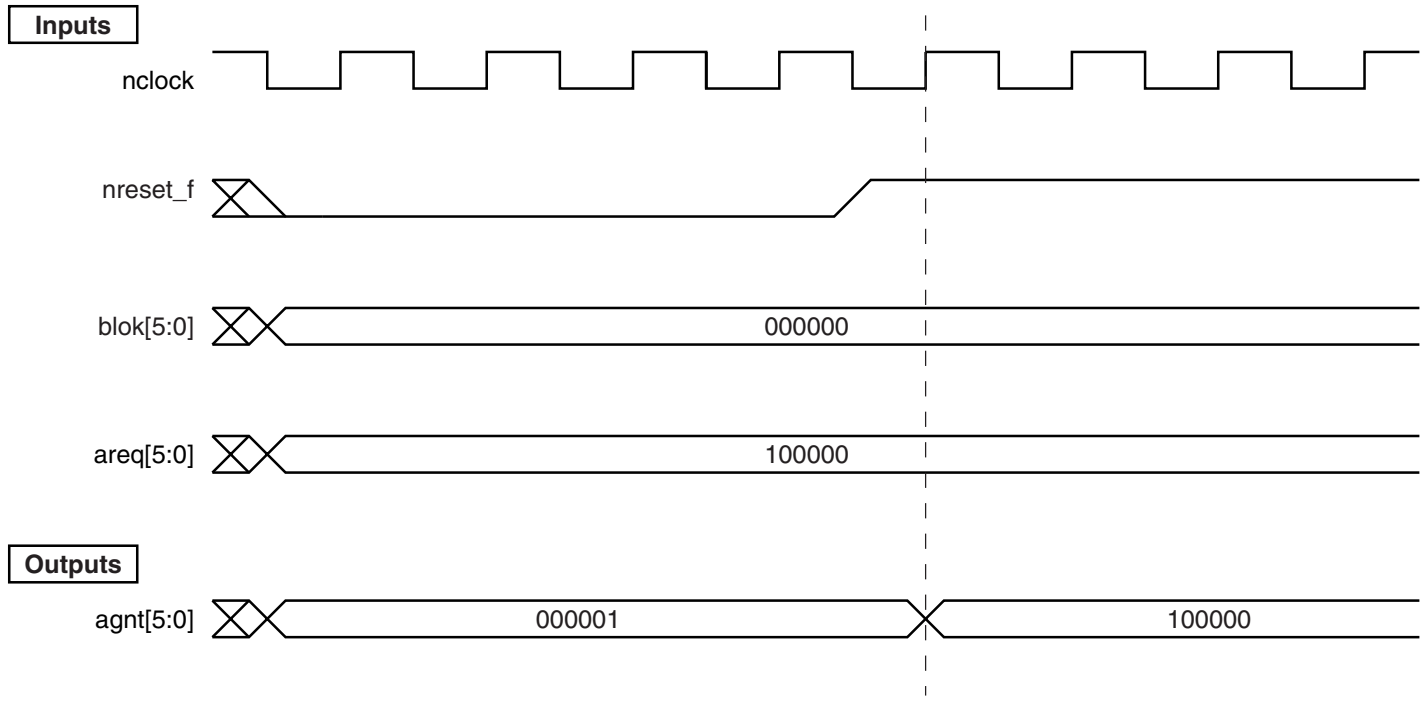
Timing Diagrams

The timing diagrams take into account the priority order described in Table 2.

During System Reset and at the End of System Reset

The master which has the lowest priority is always requesting the bus (typically the ARM core).

Figure 4.



During system reset, Master[0](default master) is granted the bus. agnt is negative-edge triggered.

Figure 5. Master [5] and Master [3] Requesting the Bus, Master [3] Granted After the End of Reset

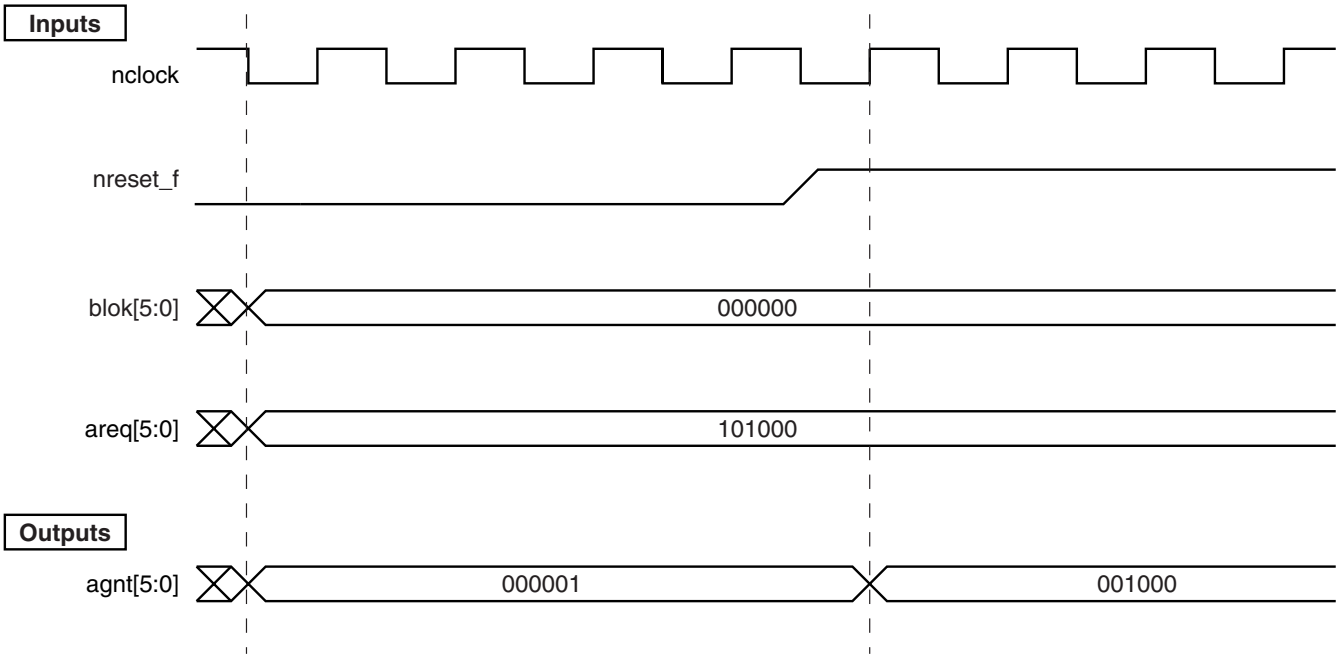
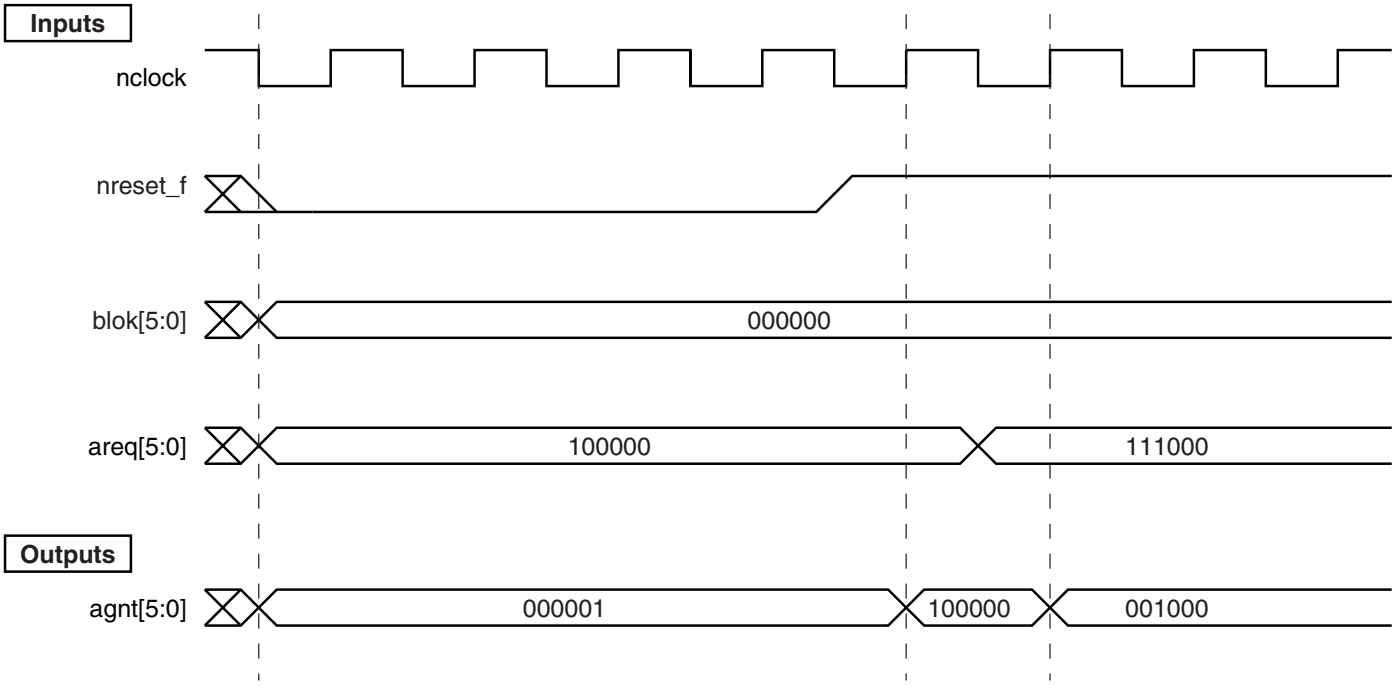


Figure 6. Master Change [5] to [3]



Normal Operating Mode

Figure 7. Master Change Between the Masters [5] and [4]: [5], [4], [5], [4], [5], [4]

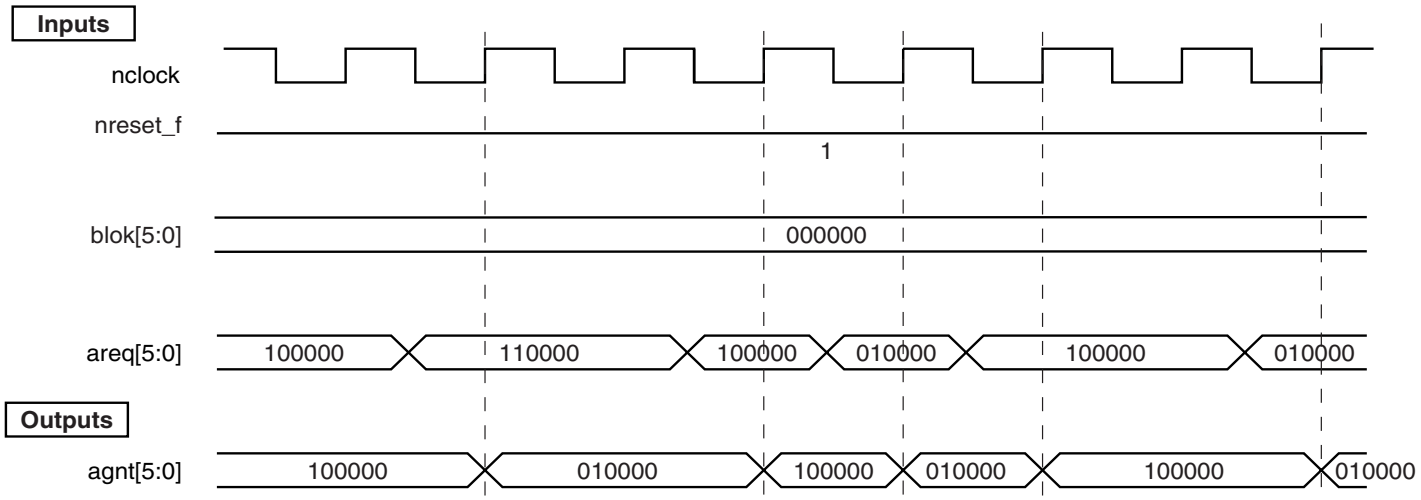


Figure 8. Master Change Between the Masters [5] and [3]: [5], [3], [5], [3], [5], [3]

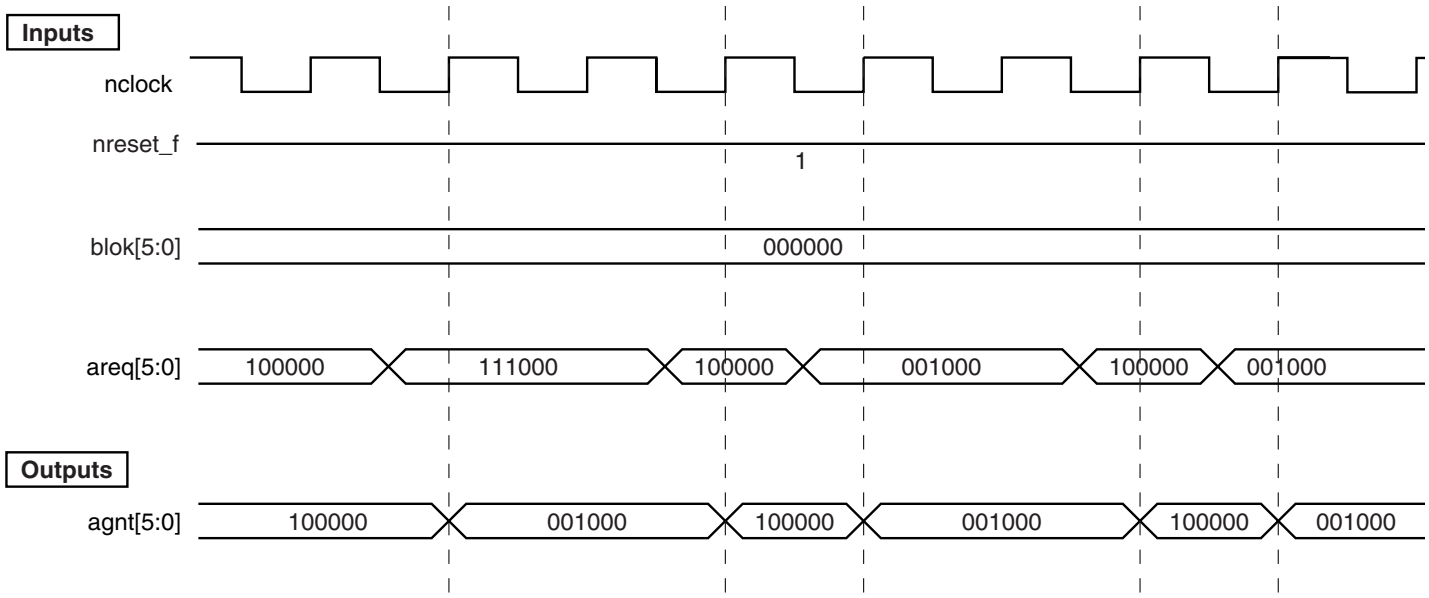


Figure 9. Master Change Between the Masters [4] and [2]: [4], [2], [4], [2], [4], [2]

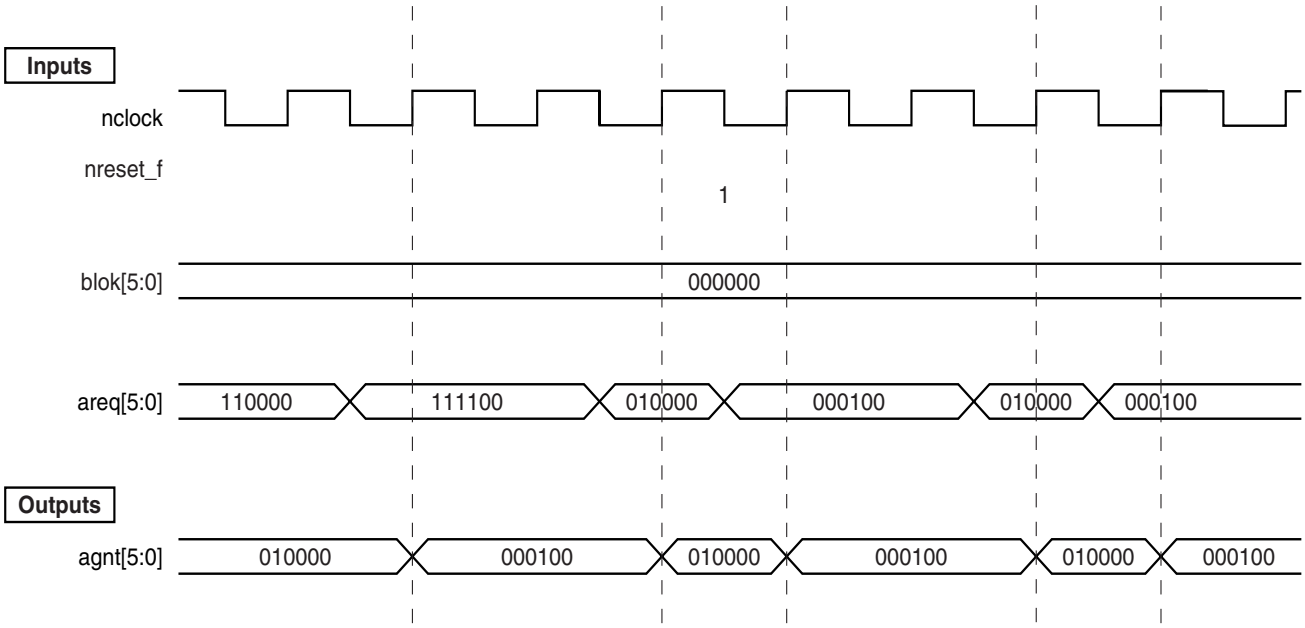


Figure 10. Master Change Between the Masters [3] and [2]: [3], [2], [3], [2], [3]

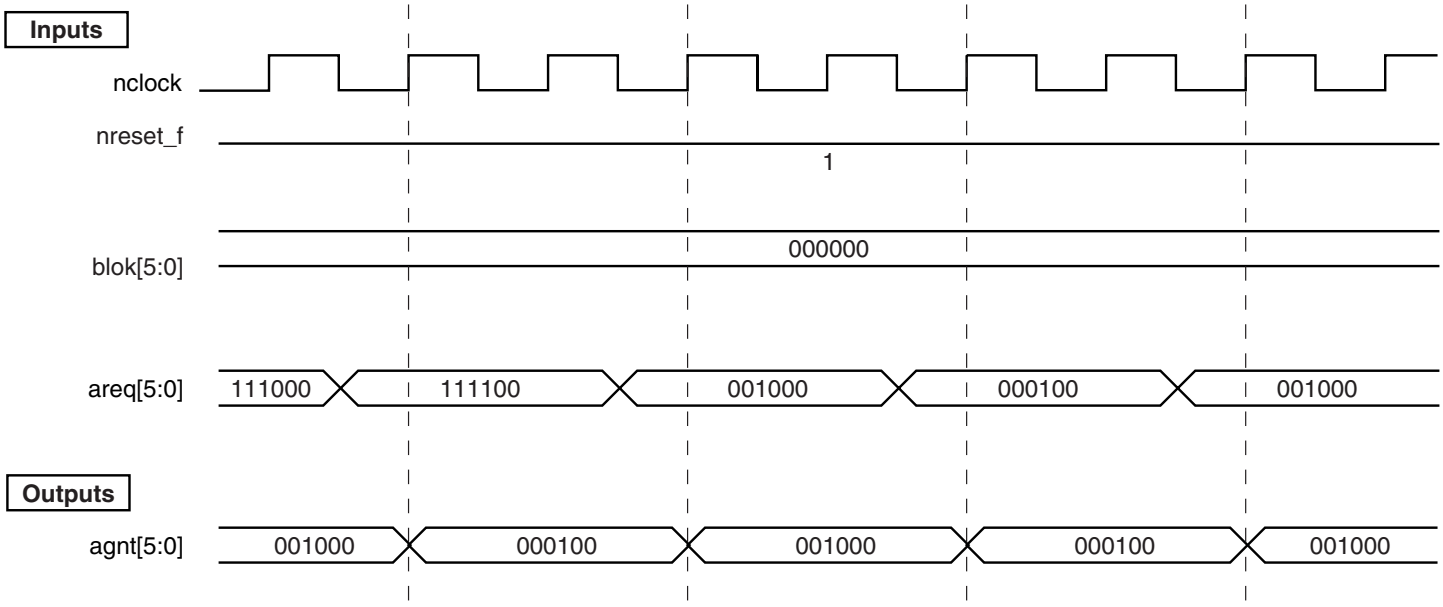


Figure 11. Master Changes with All Masters

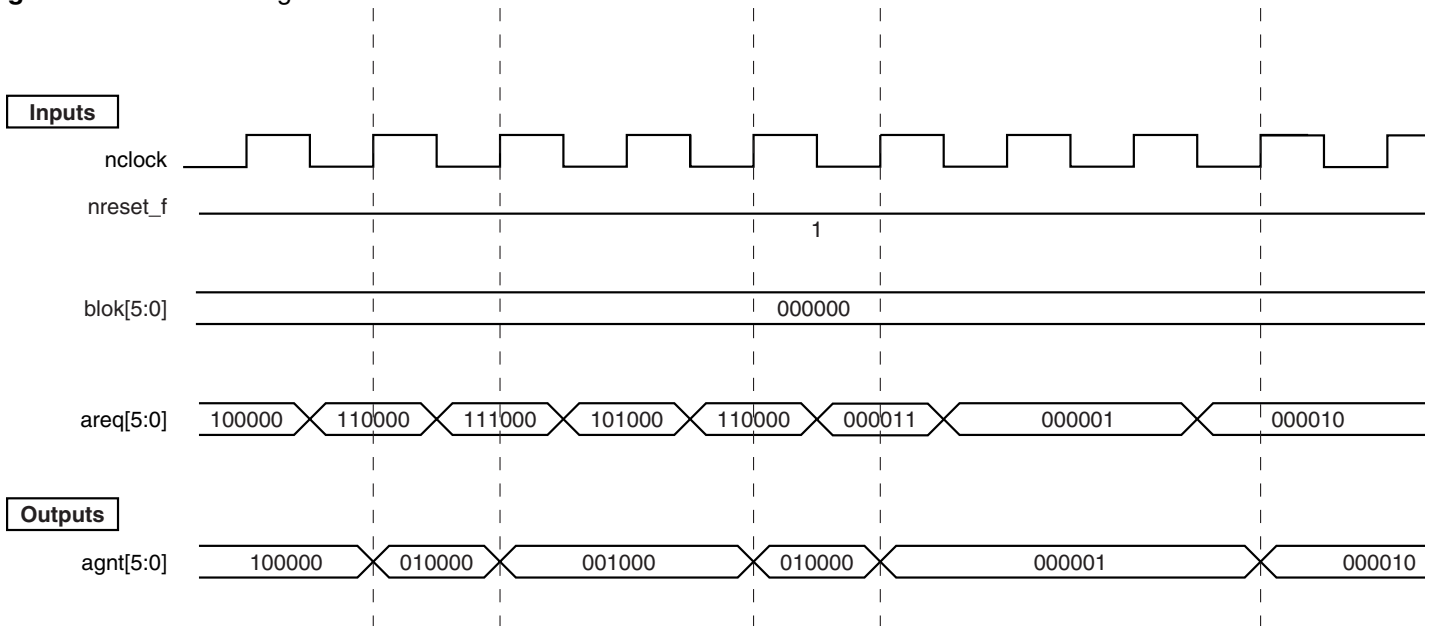
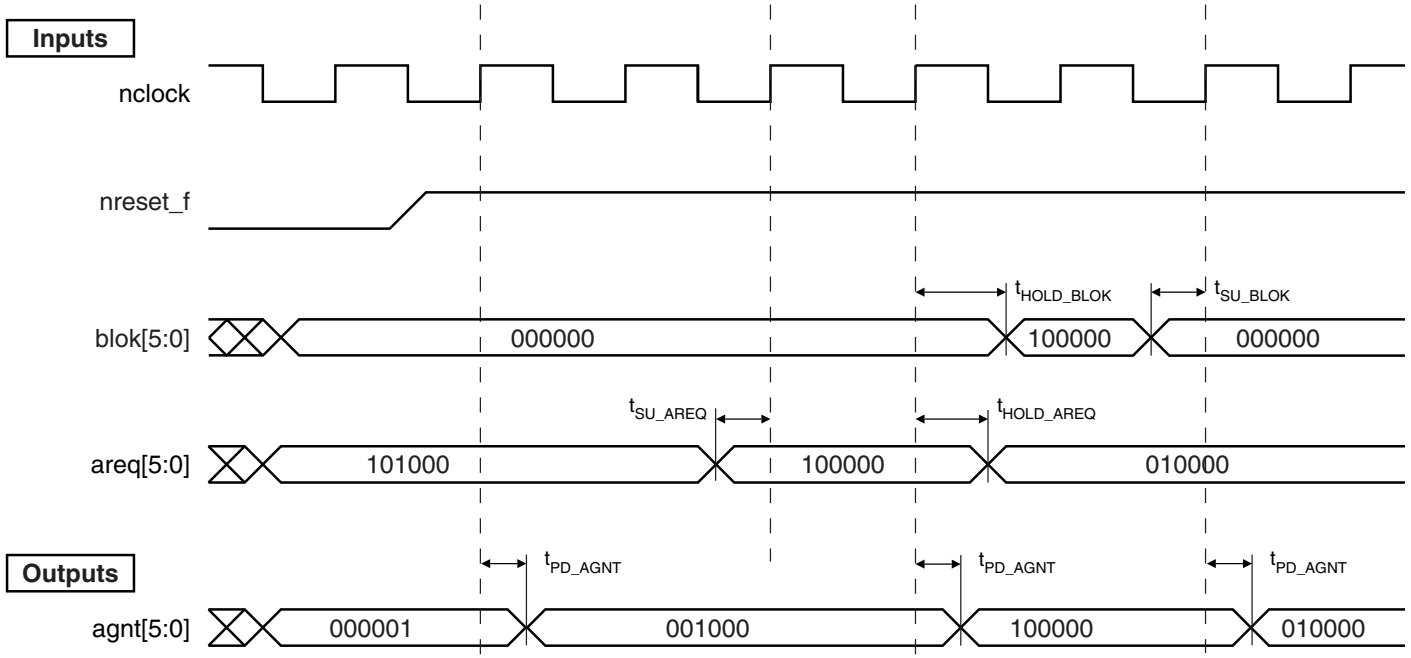


Figure 12. Timing Data



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