

*Preliminary Information*

# **AMD Athlon™**

## **Processor Model 4 Data Sheet**

**AMD** 



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## ***Preliminary Information***

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## Revision History

Date	Rev	Description
November 2001	K	<p>This revision of the <i>AMD Athlon™ Processor Model 4 Data Sheet</i> covers changes since September 2001 that include the following:</p> <ul style="list-style-type: none"> <li>■ In Chapter 5, revised Table 1, “Thermal Design Power,” on page 19</li> <li>■ In Chapter 7, revised Table 8, “VCC_CORE Voltage and Current,” on page 27</li> <li>■ In Chapter 11, revised Figure 14, “PGA OPN Example for the AMD Athlon™ Processor Model 4,” on page 71</li> </ul>
September 2001	J	<p>This revision of the 1400 MHz AMD Athlon™ Processor Model 4 covers changes since June 2001 that include the following:</p> <p>In Chapter 9, added Table 16, “Dimensions for the AMD Athlon™ Processor Model 4 CPGA Package,” on page 40, and revised Figure 11, “AMD Athlon™ Processor Model 4 CPGA Package,” on page 41.</p>
June 2001	I	<p>This revision is for the 1400 MHz AMD Athlon™ Processor Model 4 and covers changes since March 2001 that include the following:</p> <ul style="list-style-type: none"> <li>■ In Chapter 4, included APIC information in “Halt State” on page 10 and “Stop Grant States” on page 10</li> <li>■ In Chapter 5, updated Table 1, “Thermal Design Power,” on page 19</li> <li>■ In Chapter 7, updated Table 8, “VCC_CORE Voltage and Current,” on page 27</li> <li>■ In Chapter 10, revised description of “FERR Pin” on page 61 and in Table 18 on page 52</li> </ul>
March 2001	H	<p>This revision is for the 1333 MHz speed grade and covers changes since October 2000.</p> <ul style="list-style-type: none"> <li>■ In Chapter 1, revised description on the AMD Athlon™ system bus.</li> <li>■ In Chapter 4, revised Figure 3, “AMD Athlon™ Processor Model 4 Power Management States,” on page 9</li> <li>■ In Chapter 5, updated Table 1, “Thermal Design Power,” on page 20</li> <li>■ In Chapter 7, updated IoL specification to 12 mA in Table 14, “APIC Pins AC and DC Characteristics,” on page 34. Updated Table 8, “VCC_CORE Voltage and Current,” on page 27, revised Table 10, “SYSCLK and SYSCLK# AC Characteristics,” on page 29, and revised Note 1 in Table 11, “AMD Athlon™ System Bus DC Characteristics,” on page 30.</li> <li>■ In Chapter 8, revised description of “Serial Initialization Packet (SIP) Protocol” on page 38</li> <li>■ In Chapter 10, revised Table 16, “Pin Name Abbreviations,” on page 48, added description of “APIC Pins, PICCLK, PICD[1:0]#” on page 62, and revised description of “AMD Pin” on page 62</li> </ul>
October 2000	G	<p>Added information about the 133 MHz front side bus (FSB) as follows:</p> <ul style="list-style-type: none"> <li>■ “AMD Athlon™ Processor Model 4 Microarchitecture Summary” on page 2</li> <li>■ Table 1, “Thermal Design Power,” on page 19</li> <li>■ Table 8, “VCC_CORE Voltage and Current,” on page 27</li> <li>■ Table 10, “SYSCLK and SYSCLK# AC Characteristics,” on page 29</li> <li>■ Chapter 11, “Ordering Information” on page 71</li> </ul>

Date	Rev	Description
October 2000	F	Revised VID[4:0] information in Table 3 on page 24 and “VID[4:0] Pins” on page 65
October 2000	E	<p>Added Information about the 1.2 GHz AMD Athlon™ Processor Model 4 as follows:</p> <ul style="list-style-type: none"> <li>■ Chapter 1, “Overview” on page 3</li> <li>■ Table 1, “Thermal Design Power,” on page 21</li> <li>■ Table 6, “Operating Ranges,” on page 25</li> <li>■ Table 8, “VCC_CORE Voltage and Current,” on page 27</li> <li>■ Revised OPN to include the new 1200 MHz speed grade in Chapter 10, “Ordering Information” on page 71</li> <li>■ Revised Maximum and Typical Thermal Power numbers in Table 1, “Thermal Design Power,” on page 19.</li> <li>■ Added note to Table 6 for new Die temperature.</li> <li>■ Revised table note 2 as “The Sleep Voltage is used for the S1 sleep state and as the Power-up voltage before PWROK and PWRGD are asserted.” Table 6, “Operating Ranges,” on page 25.</li> <li>■ Updated “Motherboard PGA Design Guide, order# 90009” with new document name of “Socket A Motherboard Design Guide, order# 24363” throughout book.</li> <li>■ Added SAI#[0] pin in location AJ29 to Figure 15, “AMD Athlon™ Processor Model 4 Pin Diagram—Topside View,” on page 46.</li> </ul> <p>Added the AMD Pin (AH6) to Table 16, “Pin Name Abbreviations,” on page 47, Table 17, “Socket A Pin Cross-Reference by Pin Location,” on page 55 Revised all no connect (NC) pins on the pin grid array (PGA) as follows:</p> <ul style="list-style-type: none"> <li>● Figure 15, “AMD Athlon™ Processor Model 4 Pin Diagram—Topside View,” on page 46.</li> <li>● Table 15, “Pin Name Abbreviations,” on page 47.</li> <li>● Table 16, “Socket A Pin Cross-Reference by Pin Location,” on page 55.</li> </ul> <ul style="list-style-type: none"> <li>■ Revised KLCKOUT/KCLKOUT# verbiage in Chapter , “K7CLKOUT and K7CLKOUT# Pins” on page 65.</li> </ul>
August 2000	D	<p>Added information about the 1.1-GHz AMD Athlon™ Processor Model 4 as follows:</p> <ul style="list-style-type: none"> <li>■ Chapter 1, “Overview” on page 3</li> <li>■ Table 1, “Thermal Design Power,” on page 21</li> <li>■ Table 6, “Operating Ranges,” on page 25</li> <li>■ Table 8, “VCC_CORE Voltage and Current,” on page 27</li> <li>■ Revised and reorganized the AC and DC characteristics for SYSCLK and SYSCLK#. See Table 10, “SYSCLK and SYSCLK# AC Characteristics,” on page 28, and Table 9, “SYSCLK and SYSCLK# DC Characteristics,” on page 27.</li> </ul>

Date	Rev	Description
August 2000	C	<p>Added Table 1, "Thermal Design Power," on page 21 to Chapter 5, "Thermal Design".</p> <p>Revised Chapter 6, "Electrical Data" on page 23 as follows:</p> <ul style="list-style-type: none"> <li>■ Added JTAG, APIC, Test, Miscellaneous rows to Table 2, "AMD Athlon™ Processor Model 4 Interface Signal Groupings," on page 23. Reorganized signals into their correct categories.</li> <li>■ Added "Conventions" on page 23.</li> <li>■ Revised information in Table 3, "VID[4:0] DC Characteristics," on page 24.</li> <li>■ Revised information in Table 4, "FID[3:0] DC Characteristics," on page 24.</li> <li>■ Added and revised information in Table 6, "SYSCLK/SYSCLK# AC and DC Characteristics," on page 23.</li> <li>■ Revised <math>I_{VCCA}</math> information in Table 5, "VCCA AC and DC Characteristics," on page 25.</li> <li>■ Revised maximum values in Table 7, "Absolute Ratings," on page 26.</li> <li>■ Revised and reorganized information in Table 8, "VCC_CORE Voltage and Current," on page 27. For thermal information, see Table 1, "Thermal Design Power," on page 21.</li> <li>■ Changed VCC_CORE to 1.75V for all speed grades.</li> </ul> <p>Made the following changes in Chapter 7:</p> <ul style="list-style-type: none"> <li>■ Changed PLL power source signal name from VDDA to VCCA.</li> <li>■ Revised Figure 10, "Signal Relationship Requirements during Power-Up Sequence" on page 36.</li> <li>■ Revised the timing requirements in Step 4 on page 37.</li> <li>■ Revised and reorganized Table 11, "SYSCLK and SYSCLK# AC and DC Characteristics," on page 27.</li> <li>■ Added <math>V_{CROSS}</math> symbol to this table.</li> </ul>

Date	Rev	Description
August 2000	C	<p>Revised all figures and information in Chapter 8, "Mechanical Data" on page 41.</p> <p>Revised Chapter 9, "Pin Descriptions" on page 45 as follows:</p> <ul style="list-style-type: none"> <li>■ Changed FERR# to FERR in Figure 15, "AMD Athlon™ Processor Model 4 Pin Diagram—Topside View" on page 46. See "FERR Pin" on page 63 for more information.</li> <li>■ Revised definition of the Reference column in Table 17, "Socket A Pin Cross-Reference by Pin Location," on page 55 in "Pin List" on page 53.</li> <li>■ In Table 17, "Socket A Pin Cross-Reference by Pin Location," on page 55, revised information for the following pin locations: <ul style="list-style-type: none"> <li>● N1 (PICCLK), N3 (PIC[0]#), N5 (PIC[1]#), AC7 (VCC_Z), AE33 (SADDIN[5]#), AE35 (SDATAOUTCLK[0]#), AE37 (SDATA[9]#), AG1 (FERR), AJ21 (CLKFWRST), AJ23 (VCCA), AN13 (PLLMON1), AN15 (PLLBYPASSCLK), AN21 (K7CLKOUT#), AN29 (SADINN[12]#), AN31 (SADINN[14]#), AN33 (SDATAINVAL#), AN35 (SADINN[13]#), AN37 (SADINN[9]#)</li> </ul> </li> <li>■ Revised information in "K7CLKOUT and K7CLKOUT# Pins" on page 65.</li> <li>■ Removed all specific resistor values in "Detailed Pin Descriptions" on page 62. For specific implementation information, see the <i>Motherboard PGA Design Guide</i>, order# 90009.</li> </ul> <p>Revised Chapter 10, "Ordering Information" on page 71.</p>
June 2000	B	Initial public release.

# 1 Overview

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**The AMD Athlon™ processor model 4 powers the next generation in computing platforms, delivering compelling performance for cutting-edge applications and an unprecedented computing experience.**

The AMD Athlon processor model 4 with performance-enhancing cache memory is a member of the AMD Athlon family of processors that are designed to meet the computation-intensive requirements of cutting-edge software applications running on high-performance desktop systems, workstations, and servers.

Delivered in a CPGA package and achieving frequencies of 1.4 GHz (1400 MHz), the AMD Athlon processor model 4 delivers the integer, floating-point and 3D multimedia performance needed for highly demanding applications running on x86 system platforms. For cutting-edge software applications, including digital content creation, digital photo editing, digital video, image compression, video encoding for streaming over the internet, soft DVD, commercial 3D modeling, workstation-class computer-aided design (CAD), commercial desktop publishing, and speech recognition, the AMD Athlon processor model 4 delivers compelling performance. It also offers the scalability and reliability that IT managers and business users require for enterprise computing.

The AMD Athlon processor model 4 features the seventh-generation microarchitecture with an integrated L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core of the AMD Athlon processor model 4 includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, a 256-Kbyte on-chip L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering outstanding performance on numerically complex applications.

The AMD Athlon processor model 4 microarchitecture incorporates enhanced 3DNow!™ technology, a high-performance cache architecture, and both a 200-MHz, 1.6-Gigabyte per second system bus, and a 266 MHz, 2.1-Gigabyte per second system bus. The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-based transfers, and low-voltage signaling, to provide an extremely powerful, scalable bus for an x86 processor.

The AMD Athlon processor model 4 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™ and 3DNow! instructions. Using a data format and single-instruction multiple-data (SIMD) operations based on the MMX instruction model, the AMD Athlon processor model 4 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The enhanced 3DNow! technology implemented in the AMD Athlon processor model 4 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for digital signal processing (DSP)/communications applications.

## 1.1 AMD Athlon™ Processor Model 4 Microarchitecture Summary

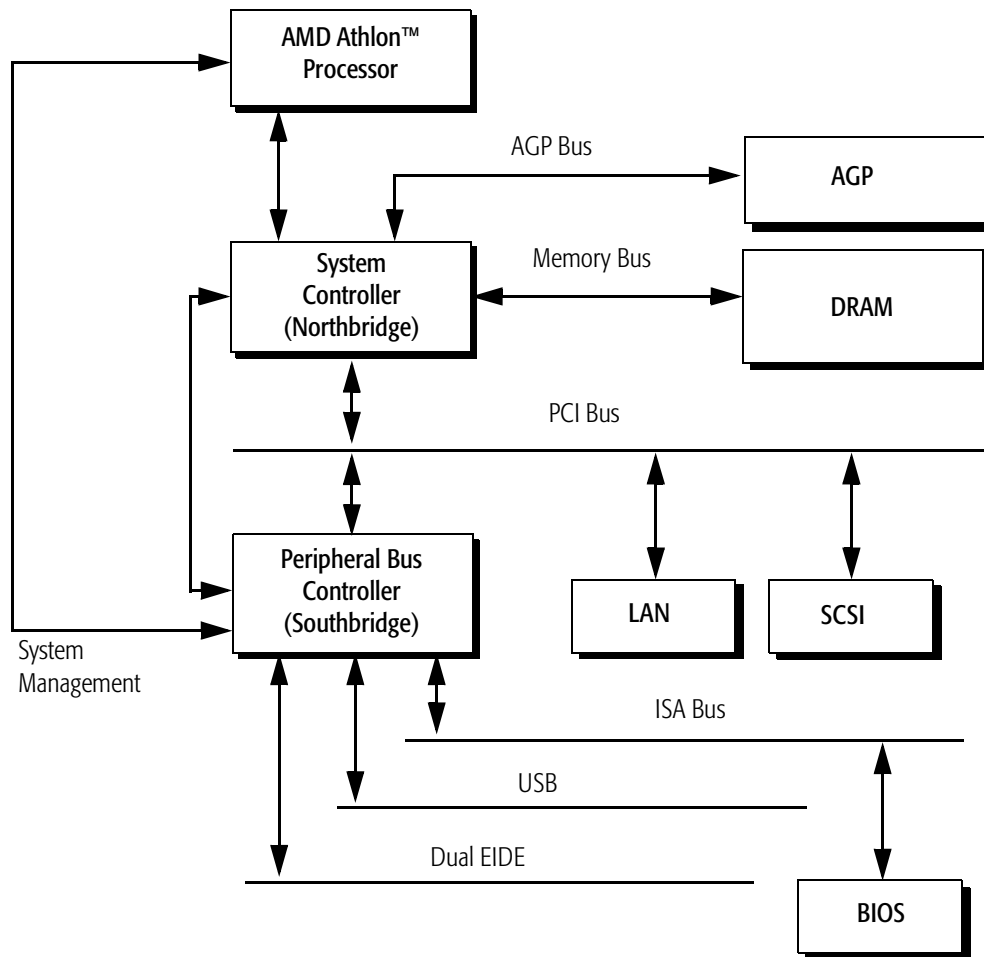
The following features summarize the AMD Athlon processor model 4 microarchitecture:

- An advanced, superpipelined, superscalar x86 processor microarchitecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Three out-of-order, superscalar, fully pipelined floating-point execution units, which execute all x87 (floating-point), MMX and 3DNow! instructions
- Three out-of-order, superscalar, pipelined integer units
- Three out-of-order, superscalar, pipelined address calculation units
- A 72-entry instruction control unit
- Advanced dynamic branch prediction
- Enhanced 3DNow! technology with new instructions to enable improved integer math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications



- 200-MHz and 266 MHz AMD Athlon system bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- High-performance cache architecture featuring an integrated 128-Kbyte L1 cache and a 16-way, on-chip 256-Kbyte L2 cache for a total of 384-Kbytes of on-chip cache

The AMD Athlon processor model 4 delivers excellent system performance in a cost-effective, industry-standard form factor. The AMD Athlon processor model 4 is compatible with motherboards based on AMD's Socket A. Figure 1 on page 3 shows a typical AMD Athlon processor model 4 system block diagram.



**Figure 1. Typical AMD Athlon™ Processor Model 4 System Block Diagram**



## 2 Interface Signals

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### 2.1 Overview

The AMD Athlon™ system bus architecture is designed to deliver unprecedented data movement bandwidth for next-generation x86 platforms, as well as the high performance required by enterprise-class application software. The system bus architecture consists of three high-speed channels (a unidirectional processor request channel, a unidirectional probe channel, and a 72-bit bidirectional data channel), source-synchronous clocking, and a packet-based protocol. In addition, the system bus supports several control, clock, and legacy signals. The interface signals use an impedance controlled push-pull low-voltage swing signaling technology contained within the Socket A socket. For more information, see “AMD Athlon™ System Bus Signals” on page 6, Chapter 10, “Pin Descriptions” on page 43, and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

### 2.2 Signaling Technology

The AMD Athlon system bus uses a low-voltage, swing signaling technology, which has been enhanced to provide larger noise margins, reduced ringing, and variable voltage levels. The signals are push-pull and impedance compensated. The signal inputs use differential receivers, which require a reference voltage ( $V_{REF}$ ). The reference signal is used by the receivers to determine if a signal is asserted or deasserted by the source. Termination resistors are not needed because the driver is impedance matched to the motherboard and a high impedance reflection is used at the receiver to bring the signal past the input threshold.

For more information about pins and signals, see Chapter 10, “Pin Descriptions” on page 43.

## 2.3 Push-Pull (PP) Drivers

The Socket A AMD Athlon processor model 4 supports Push-Pull (PP) drivers. The system logic configures the AMD Athlon processor model 4 with the configuration parameter called SysPushPull (1=PP). The impedance of the PP drivers is set to match the impedance of the motherboard by two external resistors connected to the ZN and ZP pins. See “ZN, VCC\_Z, ZP, and VSS\_Z Pins” on page 66 for more information.

## 2.4 AMD Athlon™ System Bus Signals

The AMD Athlon system bus is a clock-forwarded, point-to-point interface with the following three point-to-point channels:

- A 13-bit unidirectional output address/command channel
- A 13-bit unidirectional input address/command channel
- A 72-bit bidirectional data channel

For more information, see Chapter 7, “Electrical Data” on page 23 and the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

### 3 Logic Symbol Diagram

Figure 2 is the logic symbol diagram of the processor. This diagram shows the logical grouping of the input and output signals.

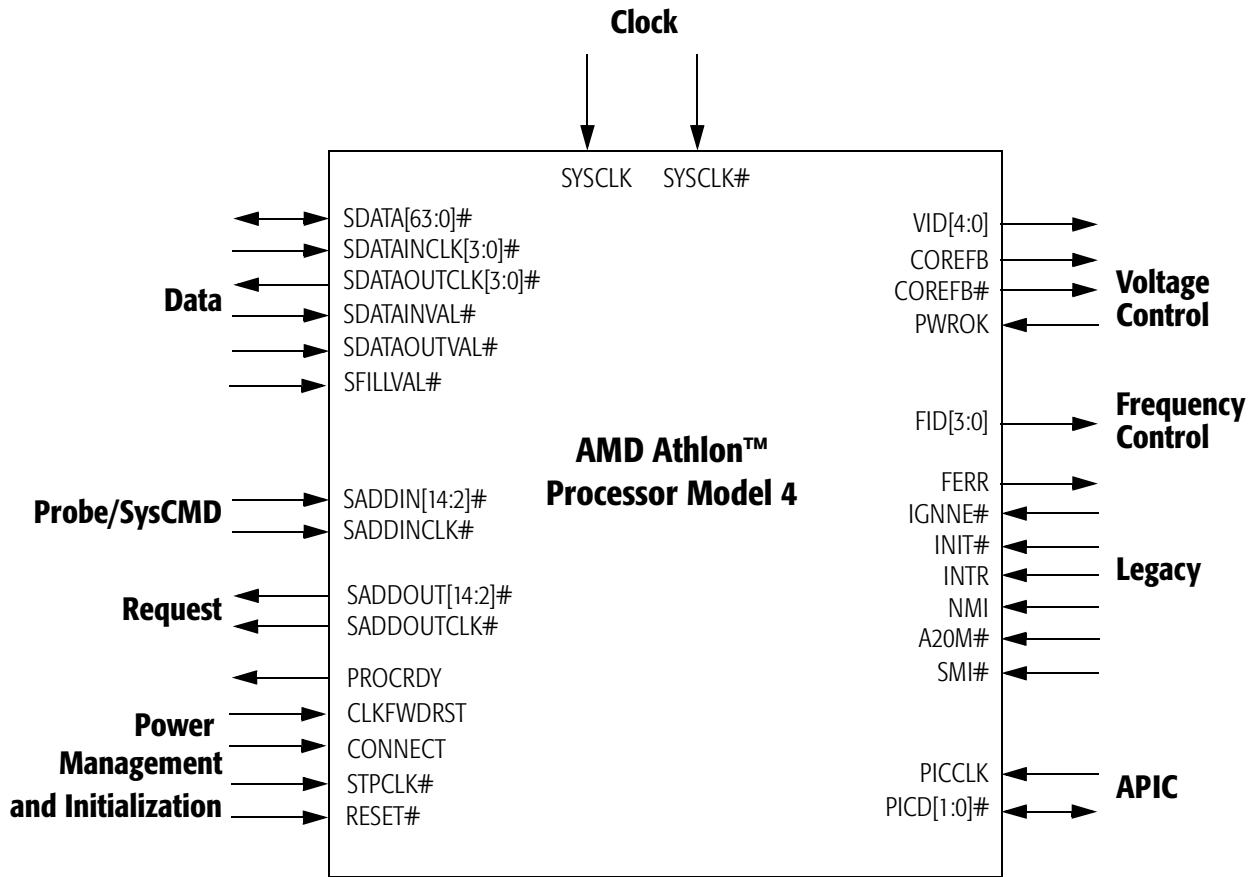


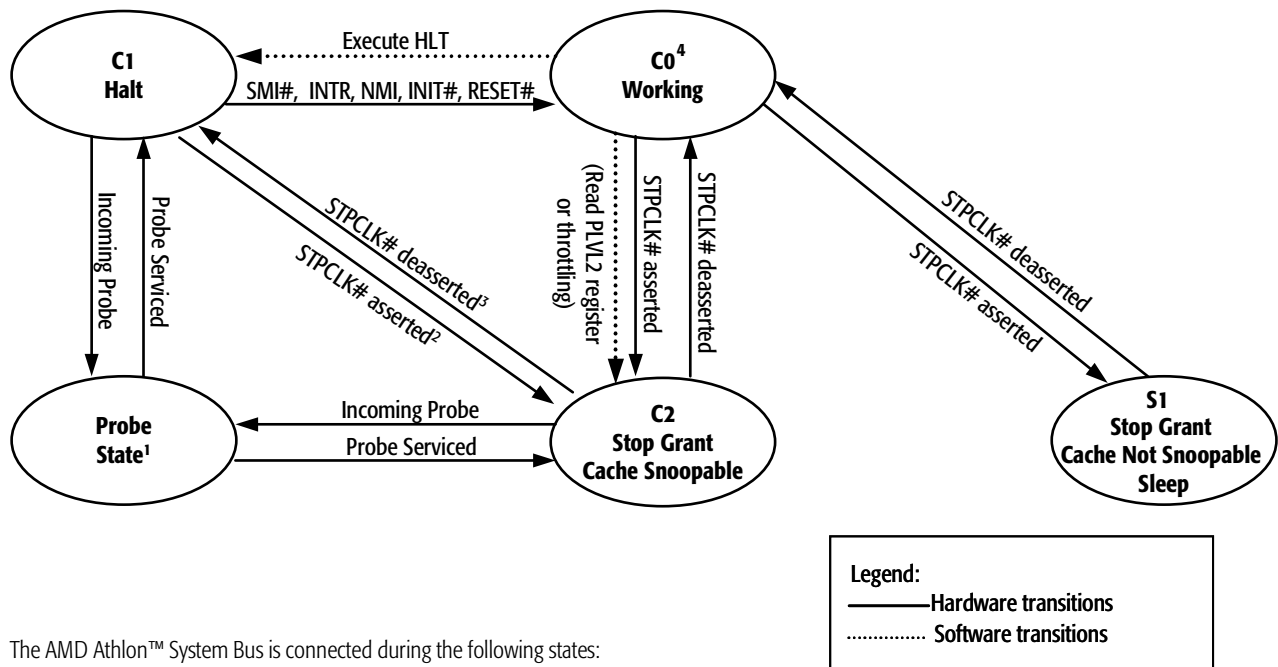
Figure 2. Logic Symbol Diagram



## 4 Power Management

### 4.1 Power Management States

The AMD Athlon™ processor model 4 supports low-power Halt and Stop Grant states. These states are used by Advanced Configuration and Power Interface (ACPI) enabled operating systems for processor power management. Figure 3 shows the power management states of the AMD Athlon processor model 4. The figure includes the ACPI “Cx” naming convention for these states.



The AMD Athlon™ System Bus is connected during the following states:

- 1) The Probe state
- 2) During transitions from the Halt state to the Stop Grant state
- 3) During transitions from Stop Grant state to the Halt state
- 4) The C0 Working state

Figure 3. AMD Athlon™ Processor Model 4 Power Management States

The following paragraphs describe each of the power management states.

*Note: In all power management states, the system must not disable the system clock (SYSCLK/SYSCLK#) to the processor.*

**Working State**

The Working state refers to the state in which the processor is executing instructions.

**Halt State**

When the AMD Athlon processor model 4 executes the HLT instruction, the processor issues a Halt special cycle to the system bus. The Phase-Lock Loop (PLL) continues to run, enabling the processor to monitor bus activity and provide a quick resume from the Halt state. The processor enters a lower power state if the system logic (Northbridge) disconnects the AMD Athlon system bus in response to the Halt special cycle.

The Halt state is exited when the processor detects the assertion of INIT#, RESET#, SMI#, or an interrupt via the INTR or NMI pins, or via a local APIC interrupt message.

**Stop Grant States**

The AMD Athlon processor model 4 enters the Stop Grant state upon recognition of assertion of STPCLK# input. There are two mechanisms for asserting STPCLK#—hardware and software. The Southbridge can force STPCLK# assertion for throttling to protect the processor from exceeding its maximum case temperature. This task is accomplished by asserting the THERM# input to the Southbridge. Throttling asserts STPCLK# for a percentage of a predefined throttling period: STPCLK# is repetitively asserted and deasserted until the THERM# pin is deasserted.

Software can force the processor into the Stop Grant state by accessing ACPI-defined registers typically located in the Southbridge. Software places the processor in C2 by reading the PLVL\_2 register in the Southbridge. In C2, probes are allowed, as shown in Figure 3 on page 9.

If an ACPI Thermal Zone is defined for the processor, the OS can initiate throttling with STPCLK# using the ACPI defined P\_CNT register in the Southbridge. The processor enters the Probe state to service cache snoops initiated by the Northbridge during Stop Grant for C2 or throttling.



The Stop Grant state is also entered for the S1 system sleep state based on a write to the SLP\_TYP field in the ACPI-defined power management 1 control register. During the S1 sleep state, system software ensures no bus master or probe activity occurs.

After recognizing the assertion of STPCLK#, the AMD Athlon processor model 4 completes all pending and in-progress bus cycles and acknowledges the STPCLK# assertion by issuing a Stop Grant special bus cycle to the AMD Athlon system bus. After the Northbridge disconnects the AMD Athlon system bus in response to the Stop Grant special bus cycle, the processor enters a low-power state dictated by the CLK\_Ctl register. During the Stop Grant states, the processor latches INIT#, INTR, NMI, and SMI#, or a local APIC interrupt message if they are asserted.

The Stop Grant state is exited upon the deassertion of STPCLK# or the assertion of RESET#. When STPCLK# is deasserted, the processor initiates a connection of the AMD Athlon system bus if it is disconnected. After the processor enters the Working state, any pending interrupts are recognized and serviced and the processor resumes execution at the instruction boundary where STPCLK# was initially recognized.

If RESET# is sampled asserted during the Stop Grant state, the processor returns to the Working state and the reset process begins.

### **Probe State**

The Probe state is entered when the Northbridge initiates an AMD Athlon system bus connect as required to probe the processor. If the processor has been disconnected from the system bus, the Northbridge must initiate a system bus connection before it probes the processor to snoop the caches of the processor. The processor responds to a probe cycle in the Probe state in the same way it does during the Working state.

When the probe has been serviced, the processor returns to the same state as when it entered the Probe state (Halt or Stop Grant state). Once in the Halt or Stop Grant state, a low-power state is only achieved if the Northbridge initiates a disconnection from the system bus.

## 4.2 Connect and Disconnect Protocol

Significant power savings of the AMD Athlon processor model 4 only occurs if the processor is disconnected from the system bus by the Northbridge while in the Halt or Stop Grant state. The Northbridge can optionally initiate a bus disconnect upon the receipt of a Halt or Stop Grant special cycle. The option of disconnecting is controlled by an enable bit in the Northbridge. If the Northbridge requires the processor to service a probe after the system bus has been disconnected, it must first initiate a system bus connect.

### Connect Protocol

In addition to the legacy STPCLK# signal and the Halt and Stop Grant special cycles, the AMD Athlon system bus connect protocol includes the CONNECT, PROCRDY, and CLKFWDRST signals and a *Connect* special cycle.

AMD Athlon system bus disconnects are initiated by the Northbridge in response to the receipt of a Halt or Stop Grant special cycle. Reconnect is initiated by the processor in response to an interrupt for Halt, STPCLK# deassertion, or by the Northbridge to service a probe.

The Northbridge contains BIOS programmable registers to enable the system bus disconnect in response to Halt and Stop Grant special cycles. When the Northbridge receives the Halt or Stop Grant special cycle from the processor and, if there are no outstanding probes or data movements, the Northbridge deasserts CONNECT a minimum of eight SYSCLK periods after the last command sent to the processor. The processor detects the deassertion of CONNECT on a rising edge of SYSCLK, and deasserts PROCRDY to the Northbridge. In return, the Northbridge asserts CLKFWDRST in anticipation of reestablishing a connection at some later point.

**Note:** *The Northbridge must disconnect the processor from the AMD Athlon system bus before issuing the Stop Grant special cycle to the PCI bus, or passing the Stop Grant special cycle to the Southbridge for systems that connect to the Southbridge with HyperTransport™ technology.*

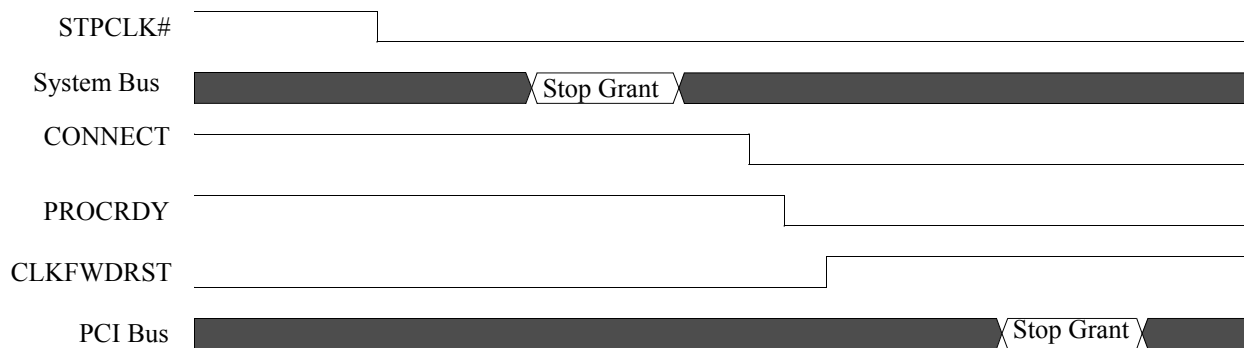
*This note applies to current chipset implementation: alternate chipset implementations that do not require this are possible.*

**Note:** In response to Halt special cycles, the Northbridge passes the Halt special cycle to the PCI bus or Southbridge immediately.

The processor can receive an interrupt after it sends a Halt special cycle, or STPCLK# deassertion after it sends a Stop Grant special cycle to the Northbridge but before the disconnect actually occurs. In this case, the processor sends the Connect special cycle to the Northbridge, rather than continuing with the disconnect sequence. In response to the Connect special cycle, the Northbridge cancels the disconnect request.

The system is required to assert the CONNECT signal before returning the C-bit for the connect special cycle (assuming CONNECT has been deasserted). For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for the definition of the C-bit and the Connect special cycle.

Figure 4 shows the sequence of events from a Northbridge perspective, which leads to disconnecting the processor from the AMD Athlon system bus and placing the processor in the Stop Grant state.



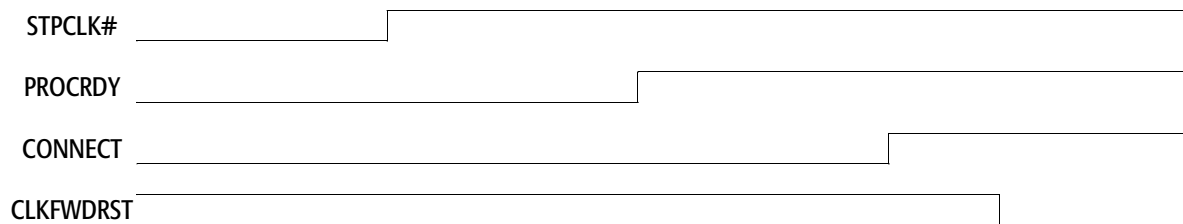
**Figure 4. Example of an AMD Athlon™ System Bus Disconnect Sequence**

The following sequence of events describes how the processor is placed in the Stop Grant state when bus disconnect is enabled within the Northbridge:

1. The Southbridge asserts STPCLK# to place the processor in the Stop Grant state.
2. When the processor recognizes STPCLK# asserted, the processor enters the Stop Grant State, then issues a Stop Grant special cycle on the AMD Athlon system bus.

3. When the Stop Grant special cycle is received by the Northbridge and no probe traffic is pending, the Northbridge deasserts CONNECT, initiating a bus disconnect to the processor.
4. The processor responds to the Northbridge by deasserting PROCRDY, acknowledging the bus disconnect request.
5. The Northbridge asserts CLKFWDRST to complete the bus disconnect sequence.
6. After the processor is disconnected from the bus, the Northbridge passes the Stop Grant special cycle to the Southbridge.

Figure 5 shows the signal sequence of events that take the processor out of the Stop Grant state, reconnect the processor to the AMD Athlon system bus, and put the processor into the Working state.



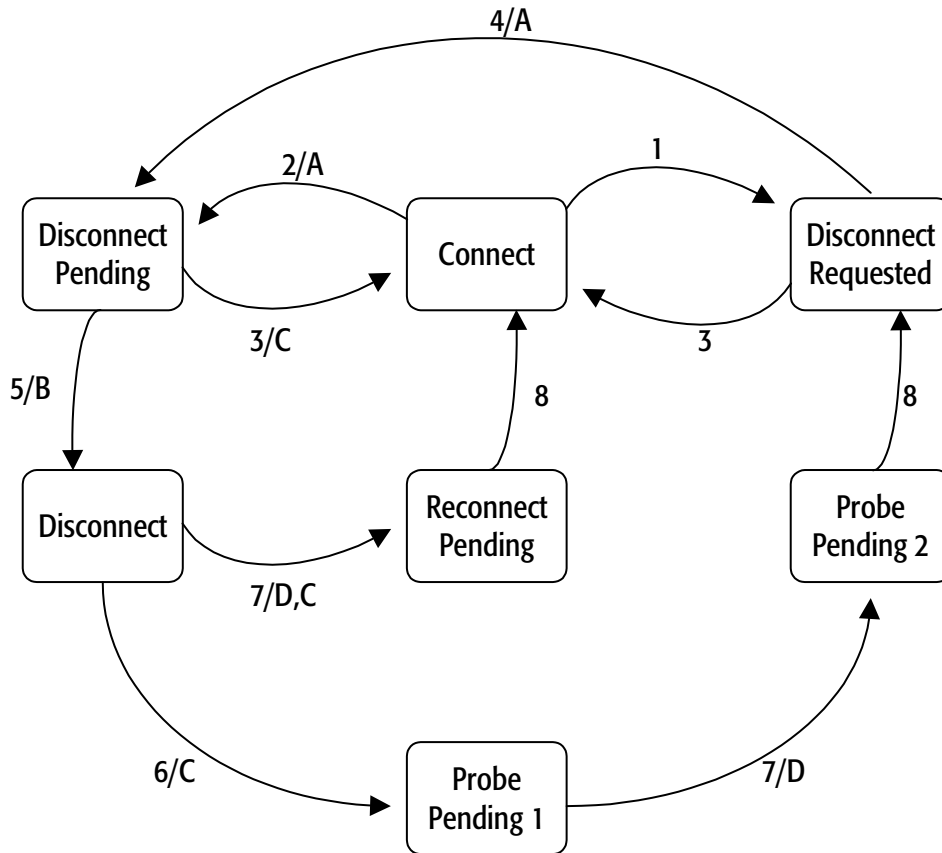
**Figure 5. Exiting Stop Grant State/Bus Reconnect Sequence**

The following sequence of events removes the processor from the Stop Grant state and reconnects it to the AMD Athlon system bus:

1. The Southbridge deasserts STPCLK# in response to a resume event.
2. When the processor recognizes STPCLK# deassertion, it asserts PROCRDY, notifying the Northbridge to reconnect to the bus.
3. The Northbridge asserts CONNECT.
4. The Northbridge finally deasserts CLKFWDRST, which synchronizes the forwarded clocks between the processor and the Northbridge.

**Connect State Diagram**

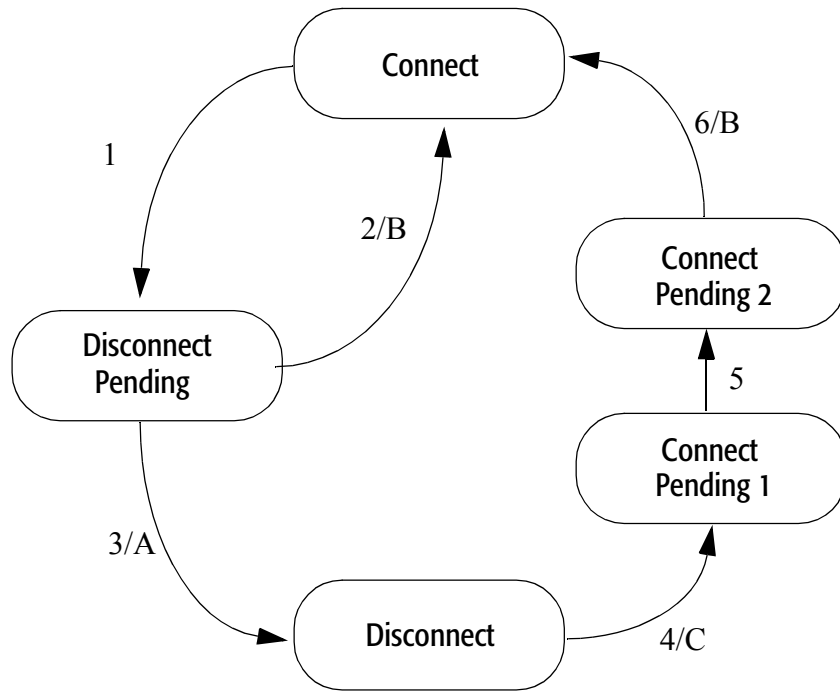
Figure 6 below and Figure 7 on page 16 describe the Northbridge and processor connect state diagrams, respectively.



Condition	
1	A disconnect is requested and probes are still pending
2	A disconnect is requested and no probes are pending
3	A CONNECT special cycle from the processor
4	No probes are pending
5	PROCRDY is deasserted
6	A probe needs service
7	PROCRDY is asserted
8	Three SYSCLK periods after CLKFWRST is deasserted. <i>Although reconnected to the system interface, the Northbridge must not issue any non-NOP SysDC commands for a minimum of four SYSCLK periods after deasserting CLKFWRST.</i>

Action	
A	Deassert CONNECT eight SYSCLK periods after last SysDC sent
B	Assert CLKFWRST
C	Assert CONNECT
D	Deassert CLKFWRST

**Figure 6. Northbridge Connect State Diagram**



	Condition
1	CONNECT is deasserted by the Northbridge (for a previously sent Halt or Stop Grant special cycle).
2	Processor receives a wake-up event and must cancel the disconnect request.
3	Deassert PROCRDY and slow down internal clocks.
4	Processor wake-up event or CONNECT asserted by Northbridge.
5	CLKFWRST is deasserted by the Northbridge.
6	Forward clocks start three SYCLK periods after CLKFWRST is deasserted.

	Action
A	CLKFWRST is asserted by the Northbridge.
B	Issue a CONNECT special cycle.*
C	Return internal clocks to full speed and assert PROCRDY
<p>* The Connect special cycle is only issued after a processor wake-up event (interrupt or STPCLK# deassertion) occurs. If the AMD Athlon system bus is connected so the Northbridge can probe the processor a Connect special cycle is not issued at that time (it is only issued after a subsequent processor wake-up event).</p>	

Figure 7. Processor Connect State Diagram

### 4.3 Clock Control

The processor implements a Clock Control (CLK\_Ctl) MSR (address C001\_001Bh) that determines the internal clock divisor when the AMD Athlon system bus is disconnected.

Refer to the *AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656, for more details on the CLK\_Ctl register.





## 5 Thermal Design

For information about thermal design for the AMD Athlon™ processor model 4, including layout and airflow considerations, see the *AMD Thermal, Mechanical, and Chassis Cooling Design Guide*, order# 23794, and the cooling guidelines on [www.amd.com](http://www.amd.com).

Table 1 shows the thermal design power. The thermal design power represents the maximum sustained power dissipated while executing publicly available software or instruction sequences under normal system operation at nominal VCC\_CORE. Thermal solutions must monitor the processor temperature to prevent the processor from exceeding its maximum die temperature.

**Table 1. Thermal Design Power**

Frequency (MHz)	Nominal Voltage	Maximum Thermal Power	Typical Thermal Power	Max Die Temperature
900	1.75 V	51.0 W	45.8 W	90°C
950		53.1 W	47.6 W	
1000		55.1 W	49.5 W	
1100		60.3 W	54.1 W	
1133		62.1 W	55.7 W	
1200		65.7 W	58.9 W	95°C
1266		66.9 W	60.1 W	
1300		68.3 W	61.3 W	
1333		69.8 W	62.6 W	
1400		72.1 W	64.7 W	



## 6 CPUID Support

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AMD Athlon™ processor model 4 version and feature set recognition can be performed through the use of the CPUID instruction that provides complete information about the processor—vendor, type, name, etc., and its capabilities. Software can make use of this information to accurately tune the system for maximum performance and benefit to users.

For information on the use of the CPUID instruction, see the *AMD Processor Recognition Application Note*, order# 20734.



## 7 Electrical Data

### 7.1 Conventions

The conventions used in this chapter are as follows:

- Current specified as being sourced by the processor is *negative*.
- Current specified as being sunk by the processor is *positive*.

### 7.2 Interface Signal Groupings

The electrical data in this chapter is presented separately for each signal group. Table 2 defines each group and the signals contained in each group.

**Table 2. Interface Signal Groupings**

Signal Group	Signals	Notes
Power	VID[4:0], VCC_CORE, VCCA, COREFB, COREFB#	See “Voltage Identification (VID[4:0])” on page 24, “VID[4:0] Pins” on page 65, and “VCCA AC and DC Characteristics” on page 25.
Frequency	FID[3:0]	See “Frequency Identification (FID[3:0])” on page 24 and “FID[3:0] Pins” on page 61.
System Clocks	SYSCLK, SYSCLK# (Tied to CLKIN/CLKIN# and RSTCLK/RSTCLK#), PLLBYPASSCLK#, PLLBYPASSCLK	See “SYSCLK and SYSCLK# DC Characteristics” on page 28.
AMD Athlon™ System Bus	SADDIN[14:2]#, SADDOUT[14:2]#, SADDINCLK#, SADDOUTCLK#, SFILLVAL#, SDATAINVAL#, SDATAOUTVAL#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAOUTCLK[3:0]#, CLKFWRST, PROCRDY, CONNECT	See “AMD Athlon™ System Bus AC and DC Characteristics” on page 30.
Southbridge	RESET#, INTR, NMI, SMI#, INIT#, A20M#, FERR, IGNNE#, STPCLK#, FLUSH#	See “General AC and DC Characteristics” on page 32.
JTAG	TMS, TCK, TRST#, TDI, TDO	See “General AC and DC Characteristics” on page 32.
APIC	PICD[1:0]#, PICCLK	See “APIC Pins AC and DC Characteristics” on page 34 and “APIC Pins, PICCLK, PICD[1:0]#” on page 60

**Table 2. Interface Signal Groupings (continued)**

Signal Group	Signals	Notes
Test	PLLTEST#, PLLMON1, PLLMON2, SCANCLK1, SCANCLK2, SCANSHIFTEN, SCANINTEVAL, ANALOG	See "General AC and DC Characteristics" on page 32.
Miscellaneous	DBREQ#, DBRDY, PWROK, PLLBYPASS#	See "General AC and DC Characteristics" on page 32.

### 7.3 Voltage Identification (VID[4:0])

Table 3 shows the VID[4:0] DC characteristics. For more information, see "VID[4:0] Pins" on page 65.

**Table 3. VID[4:0] DC Characteristics**

Parameter	Description	Min	Max
I <sub>OL</sub>	Output Current Low	16 mA	
V <sub>OH</sub>	Output High Voltage		2.625 V *
<b>Note:</b> * The VID pins must not be pulled above this voltage by an external pullup resistor.			

### 7.4 Frequency Identification (FID[3:0])

Table 4 shows the FID[3:0] DC characteristics. For more information, see "FID[3:0] Pins" on page 61.

**Table 4. FID[3:0] DC Characteristics**

Parameter	Description	Min	Max
I <sub>OL</sub>	Output Current Low	16 mA	
V <sub>OH</sub>	Output High Voltage		2.625 V *
<b>Note:</b> * The FID pins must not be pulled above this voltage by an external pullup resistor.			

## 7.5 VCCA AC and DC Characteristics

Table 5 shows the AC and DC characteristics for VCCA. For more information, see “VCCA Pin” on page 65.

**Table 5. VCCA AC and DC Characteristics**

Symbol	Parameter	Min	Nominal	Max	Units	Notes
$V_{VCCA}$	VCCA Pin Voltage	2.25	2.5	2.75	V	1
$I_{VCCA}$	VCCA Pin Current	0		50	mA/GHz	2

**Notes:**

1. Minimum and maximum voltages are absolute. No transients below minimum nor above maximum voltages are permitted.
2. Measured at 2.5 V.

## 7.6 Decoupling

See the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363, or contact your local AMD office for information about the decoupling required on the motherboard for use with the AMD Athlon™ processor model 4.

## 7.7 Operating Ranges

The AMD Athlon processor model 4 is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 6.

**Table 6. Operating Ranges**

Parameter	Description	Min	Nominal	Max	Notes	
VCC_CORE	Processor core supply	900-1400 MHz	1.65 V	1.75 V	1.85 V	1
VCC_CORE_SLEEP	Processor core supply in Sleep state		1.2 V	1.3 V	1.4 V	2
T <sub>DIE</sub>	Temperature of processor die			95°C		3

**Notes:**

1. For normal operating conditions (nominal VCC\_CORE is 1.75 V).
2. Sleep Voltage can be used for the S1 sleep state. For more information see the AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide, order# 21656.
3. Die temperature is 90°C for frequencies of 1100 MHz and lower.

## 7.8 Absolute Ratings

The AMD Athlon processor model 4 should not be subjected to conditions exceeding the absolute ratings listed in Table 7, as such conditions can adversely affect long-term reliability or result in functional damage.

**Table 7. Absolute Ratings**

Parameter	Description	Min	Max
VCC_CORE	AMD Athlon™ Processor Model 4 core supply	-0.5 V	VCC_CORE Max + 0.5 V
VCCA	AMD Athlon Processor Model 4 PLL Supply	-0.5 V	VCCA Max + 0.5 V
V <sub>PIN</sub>	Voltage on any signal pin	-0.5 V	VCC_CORE Max + 0.5 V
T <sub>STORAGE</sub>	Storage temperature of processor	-40°C	100°C



## 7.9 VCC\_CORE Voltage and Current

Table 8 shows the power and current of the processor during normal and reduced power states.

**Table 8. VCC\_CORE Voltage and Current**

Frequency (MHz)	Nominal Voltage	Maximum Voltage	Stop Grant (Maximum) <sup>1</sup>	Maximum I <sub>CC</sub> (Power Supply Current) <sup>2</sup>	Die Temperature
900	1.75 V	1.85 V	5 W	29.2 A	90°C
950				30.3 A	
1000				31.5 A	
1100				34.5 A	
1133				35.5 A	
1200				37.5 A	95°C
1266				38.3 A	
1300				39.0 A	
1333				39.9 A	
1400				41.2 A	

**Notes:**

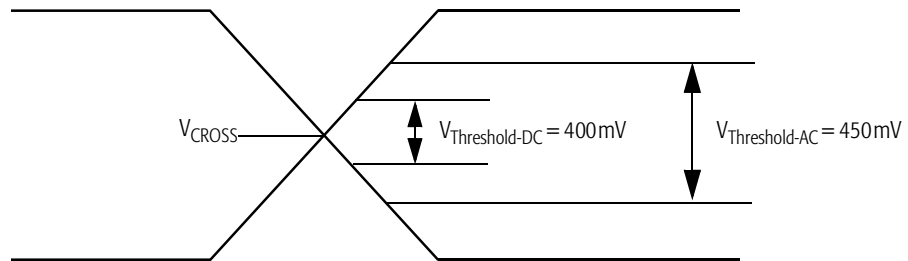
1. Measured at 1.3 V for Sleep state operating conditions. The BIOS must program the CLK\_Ctrl MSR to fff0\_d22fh for the AMD Athlon™ Processor Model 4.
2. Measured at Nominal voltage of 1.75 V.

## 7.10 SYSCLK and SYSCLK# AC and DC Characteristics

Table 9 shows the DC characteristics of the SYSCLK and SYSCLK# differential clocks. The SYSCLK signal represents CLKIN and RSTCLK tied together while the SYSCLK# signal represents CLKIN# and RSTCLK# tied together. Figure 8 shows the waveforms of the SYSCLK and SYSCLK# signals.

**Table 9. SYSCLK and SYSCLK# DC Characteristics**

Symbol	Description	Min	Max	Units
$V_{\text{Threshold-DC}}$	Crossing before transition is detected (DC)	400		mV
$V_{\text{Threshold-AC}}$	Crossing before transition is detected (AC)	450		mV
$I_{\text{LEAK\_P}}$	Leakage current through P-channel pullup to VCC_CORE	-1		mA
$I_{\text{LEAK\_N}}$	Leakage current through N-channel pulldown to VSS (Ground)		1	mA
$V_{\text{CROSS}}$	Differential signal crossover		$V_{\text{CC\_CORE}}/2$ +/- 100	mV
$C_{\text{PIN}}$	Capacitance	4	12	pF



**Figure 8. SYSCLK and SYSCLK# Differential Clock Signals**

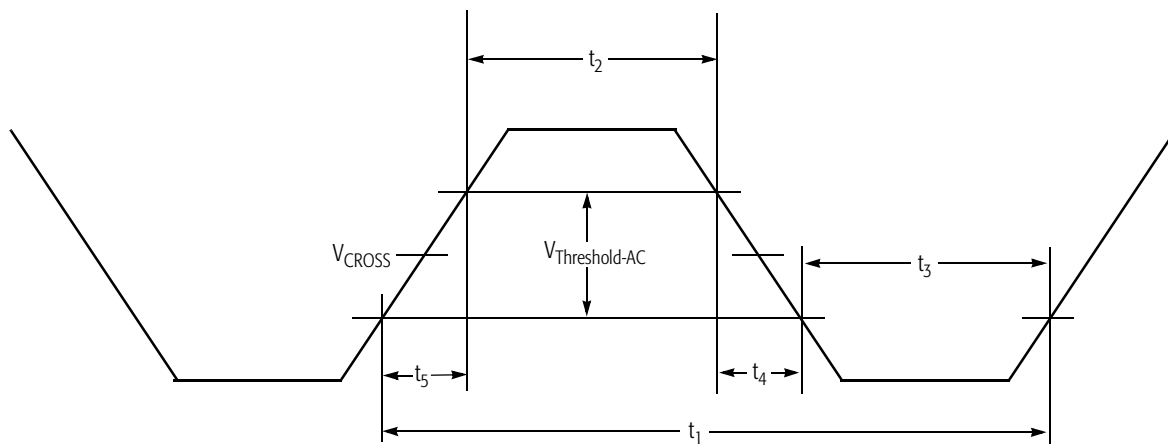
Table 10 shows the SYSCLK/SYSCLK# differential clock AC characteristics of the AMD Athlon processor model 4. Figure 9 shows a sample waveform.

**Table 10. SYSCLK and SYSCLK# AC Characteristics**

Symbol	Parameter Description	Min @		Max @		Units	Notes
	Clock Frequency	100	133	100	133	MHz	
	Duty Cycle	30%	30%	70%	70%		
$t_1$	Period	10	7.5			ns	1, 2
$t_2$	High Time	1.8	1.05			ns	
$t_3$	Low Time	1.8	1.05			ns	
$t_4$	Fall Time			2	2	ns	
$t_5$	Rise Time			2	2	ns	
	Period Stability			$\pm 300$	$\pm 300$	ps	

**Notes:**

1. Circuitry driving the SYSCLK and SYSCLK# inputs must exhibit a suitably low closed-loop jitter bandwidth to allow the PLL to track the jitter. The -20 dB attenuation point, as measured into a 10 or 20-pF load must be less than 500 kHz.
2. Circuitry driving the SYSCLK and SYSCLK# inputs can purposely alter the SYSCLK and SYSCLK# period (spread spectrum clock generators). In no cases can the SYSCLK and SYSCLK# period violate the minimum specification above. SYSCLK and SYSCLK# inputs can vary from 100% of the specified period to 99% of the specified period at a maximum rate of 100 kHz.



**Figure 9. SYSCLK Waveform**

## 7.11 AMD Athlon™ System Bus AC and DC Characteristics

Table 11 shows the DC characteristics of the AMD Athlon system bus used by the AMD Athlon processor model 4.

**Table 11. AMD Athlon™ System Bus DC Characteristics**

Symbol	Parameter	Condition	Min	Max	Units	Notes
$V_{REF}$	DC Input Reference Voltage		$(0.5 * VCC\_CORE) - 50$	$(0.5 * VCC\_CORE) + 50$	mV	1
$I_{VREF\_LEAK\_P}$	$V_{REF}$ Tristate Leakage Pullup	$V_{IN} = V_{REF}$ Nominal	-100		$\mu A$	
$I_{VREF\_LEAK\_N}$	$V_{REF}$ Tristate Leakage Pulldown	$V_{IN} = V_{REF}$ Nominal		+100	$\mu A$	
$V_{IH}$	Input High Voltage		$V_{REF} + 200$	$VCC\_CORE + 500$	mV	
$V_{IL}$	Input Low Voltage		-500	$V_{REF} - 200$	mV	
$V_{OH}$	Output High Voltage	$I_{OUT} = -200 \mu A$	$0.85 * VCC\_CORE$	$VCC\_CORE + 500$	mV	2
$V_{OL}$	Output Low Voltage	$I_{OUT} = 1 \text{ mA}$	-500	400	mV	2
$I_{LEAK\_P}$	Tristate Leakage Pullup	$V_{IN} = VSS$ (Ground)	-1		mA	
$I_{LEAK\_N}$	Tristate Leakage Pulldown	$V_{IN} = VCC\_CORE$ Nominal		+1	mA	
$C_{IN}$	Input Pin Capacitance		4	12	pF	3

**Notes:**

- $V_{REF}$  is nominally set to 50% of  $VCC\_CORE$  with actual values that are specific to motherboard design implementation.  $V_{REF}$  must be created with a sufficiently accurate DC source and a sufficiently quiet AC response to adhere to the  $\pm 50$  mV specification listed above.
- Specified at  $T_{DIE}$  given in Table 6, and  $VCC\_CORE$  in Table 8.
- The following processor inputs have twice the listed capacitance because they connect to two input pads— $SYSCLK$ , and  $SYSCLK\#$ .  $SYSCLK$  connects to  $CLKIN/RSTCLK$ .  $SYSCLK\#$  connects to  $CLKIN\#/RSTCLK\#$ . For more information, see Table 17 on page 46.

The AC characteristics of the AMD Athlon system bus are shown in Table 12. The parameters are grouped based on the source or destination of the signals involved.

**Table 12. AMD Athlon™ System Bus AC Characteristics**

Group	Symbol	Parameter	Min	Max	Units	Notes
All Signals	$T_{RISE}$	Output Rise Slew Rate	1	3	V/ns	1
	$T_{FALL}$	Output Fall Slew Rate	1	3	V/ns	1
Forward Clocks	$T_{SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge		385	ps	2
	$T_{SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge		770	ps	2
	$T_{SU}$	Input Data Setup Time	300		ps	3
	$T_{HD}$	Input Data Hold Time	300		ps	3
	$C_{IN}$	Capacitance on input Clocks	4	12	pF	
	$C_{OUT}$	Capacitance on output Clocks	4	12	pF	
Sync	$T_{VAL}$	RSTCLK to Output Valid	250	2000	ps	4, 5
	$T_{SU}$	Setup to RSTCLK	500		ps	4, 6
	$T_{HD}$	Hold from RSTCLK	1000		ps	4, 6

**Notes:**

1. Rise and fall time ranges are guidelines over which the I/O has been characterized.
2.  $T_{SKEW-SAMEEDGE}$  is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.  
 $T_{SKEW-DIFFEDGE}$  is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
3. Input SU and HD times are with respect to the appropriate Clock Forward Group input clock.
4. The synchronous signals include PROCRDY, CONNECT, and CLKFWRDST.
5.  $T_{VAL}$  is RSTCLK rising edge to output valid for PROCRDY. Test Load is 25 pF.
6.  $T_{SU}$  is setup of CONNECT/CLKFWRDST to rising edge of RSTCLK.  $T_{HD}$  is hold of CONNECT/CLKFWRDST from rising edge of RSTCLK.

## 7.12 General AC and DC Characteristics

Table 13 shows the AMD Athlon processor model 4 AC and DC characteristics of the Southbridge, JTAG, test, and miscellaneous pins.

**Table 13. General AC and DC Characteristics**

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V <sub>IH</sub>	Input High Voltage		(VCC_CORE/2) + 200mV	VCC_CORE + 300mV	V	1,2
V <sub>IL</sub>	Input Low Voltage		-300	350	mV	1,2
V <sub>OH</sub>	Output High Voltage		VCC_CORE - 400	VCC_CORE + 300	mV	
V <sub>OL</sub>	Output Low Voltage		-300	400	mV	
I <sub>LEAK_P</sub>	Tristate Leakage Pullup	V <sub>IN</sub> = VSS (Ground)	-1		mA	
I <sub>LEAK_N</sub>	Tristate Leakage Pulldown	V <sub>IN</sub> = VCC_CORE Nominal		600	μA	
I <sub>OH</sub>	Output High Current			-16	mA	3
I <sub>OL</sub>	Output Low Current		16		mA	3
T <sub>SU</sub>	Sync Input Setup Time		2.0		ns	4, 5
T <sub>HD</sub>	Sync Input Hold Time		0.0		ps	4, 5
T <sub>DELAY</sub>	Output Delay with respect to RSTCLK		0.0	6.1	ns	5
T <sub>BIT</sub>	Input Time to Acquire		20.0		ns	7,8
T <sub>RPT</sub>	Input Time to Reacquire		40.0		ns	9–13

**Notes:**

1. Characterized across DC supply voltage range.
2. Values specified at nominal VCC\_CORE. Scale parameters between VCC\_CORE Min and VCC\_CORE Max.
3. I<sub>OL</sub> and I<sub>OH</sub> are measured at V<sub>OL</sub> max and V<sub>OH</sub> min, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to ensure capture.
8. This value assumes RSTCLK period is 10ns ==> T<sub>BIT</sub> = 2\*FRST.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.

**Table 13. General AC and DC Characteristics (continued)**

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
T <sub>RISE</sub>	Signal Rise Time		1.0	3.0	V/ns	6
T <sub>FALL</sub>	Signal Fall Time		1.0	3.0	V/ns	6
C <sub>PIN</sub>	Pin Capacitance		4	12	pF	

**Notes:**

1. Characterized across DC supply voltage range.
2. Values specified at nominal VCC\_CORE. Scale parameters between VCC\_CORE Min and VCC\_CORE Max.
3. I<sub>OL</sub> and I<sub>OH</sub> are measured at V<sub>OL</sub> max and V<sub>OH</sub> min, respectively.
4. Synchronous inputs/outputs are specified with respect to RSTCLK and RSTCK# at the pins.
5. These are aggregate numbers.
6. Edge rates indicate the range over which inputs were characterized.
7. In asynchronous operation, the signal must persist for this time to ensure capture.
8. This value assumes RSTCLK period is 10ns ==> TBIT = 2\*FRST.
9. The approximate value for standard case in normal mode operation.
10. This value is dependent on RSTCLK frequency, divisors, LowPower mode, and core frequency.
11. Reassertions of the signal within this time are not guaranteed to be seen by the core.
12. This value assumes that the skew between RSTCLK and K7CLKOUT is much less than one phase.
13. This value assumes RSTCLK and K7CLKOUT are running at the same frequency, though the processor is capable of other configurations.

## 7.13 APIC Pins AC and DC Characteristics

Table 14 shows the AMD Athlon processor model 4 AC and DC characteristics of the APIC pins.

**Table 14. APIC Pins AC and DC Characteristics**

Symbol	Parameter Description	Condition	Min	Max	Units	Notes
V <sub>IH</sub>	Input High Voltage		1.7	2.625	V	1, 3
V <sub>IL</sub>	Input Low Voltage		-300	700	mV	1, 2
V <sub>OH</sub>	Output High Voltage			2.625	V	3
V <sub>OL</sub>	Output Low Voltage		-300	400	mV	
I <sub>LEAK_P</sub>	Tristate Leakage Pullup	V <sub>IN</sub> = VSS (Ground)	-1		mA	
I <sub>LEAK_N</sub>	Tristate Leakage Pulldown	V <sub>IN</sub> = 2.5 V		1	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> Max	12		mA	
T <sub>RISE</sub>	Signal Rise Time		1.0	3.0	V/ns	4
T <sub>FALL</sub>	Signal Fall Time		1.0	3.0	V/ns	4
C <sub>PIN</sub>	Pin Capacitance		4	12	pF	
<b>Notes:</b> <ol style="list-style-type: none"> <li>1. Characterized across DC supply voltage range.</li> <li>2. Values specified at nominal VDD (1.5 V). Scale parameters with VDD.</li> <li>3. 2.625 V = 2.5 V + 5% maximum</li> <li>4. Edge rates indicate the range over which inputs were characterized.</li> </ol>						



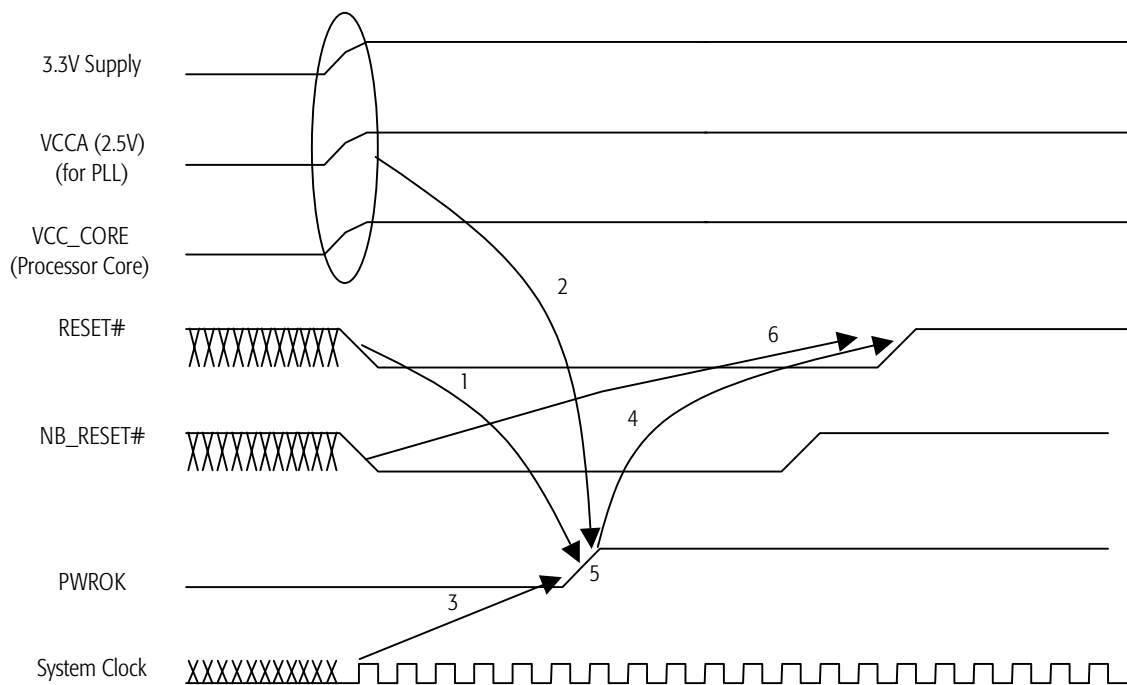
## 8 Signal and Power-Up Requirements

This chapter describes the AMD Athlon™ processor model 4 power-up requirements during system power-up and warm resets.

### 8.1 Power-Up Requirements

#### Signal Sequence and Timing Description

Figure 10 shows the relationship between key signals in the system during a power-up sequence. This figure details the requirements of the processor.



**Figure 10. Signal Relationship Requirements During Power-Up Sequence**

- Notes:**
1. Figure 10 represents several signals generically by using names not necessarily consistent with any pin lists or schematics.
  2. Requirements 1-6 in Figure 10 are described in “Power-Up Timing Requirements” on page 36.

**Power-Up Timing Requirements.** The following signal timing requirements correspond to numbers 1-6 in Figure 10 on page 35.

1. RESET# must be asserted before PWROK is asserted.

The AMD Athlon processor model 4 does not set the correct clock multiplier if PWROK is asserted prior to a RESET# assertion. It is recommended that RESET# be asserted at least **10 ns** prior to the assertion of PWROK.

In practice, Southbridges assert RESET# milliseconds before PWROK is deasserted.

2. All motherboard voltage planes must be within specification before PWROK is asserted.

PWROK is an output of the voltage regulation circuit on the motherboard. PWROK indicates that VCC\_CORE and all other voltage planes in the system are within specification.

The motherboard is required to delay PWROK assertion for a minimum of three milliseconds from the 3.3 V supply being within specification. This ensures that the system clock (SYSCLK/SYSCLK#) is operating within specification when PWROK is asserted.

The processor core voltage, VCC\_CORE, must be within specification as dictated by the VID[4:0] pins driven by the processor before PWROK is asserted. Before PWROK assertion, the AMD Athlon processor is clocked by a ring oscillator.

The AMD Athlon processor PLL is powered by VCCA. The processor PLL does not lock if VCCA is not high enough for the processor logic to switch for some period before PWROK is asserted. VCCA must be within spec at least five microseconds before PWROK is asserted.

In practice VCCA, VCC\_CORE, and all other voltage planes must be within specification for several milliseconds before PWROK is asserted.

After PWROK is asserted, the processor PLL locks to its operational frequency.

3. The system clock (SYSCLK/SYSCLK#) must be running within specification before PWROK is asserted.

When PWROK is asserted, the processor switches from driving the internal processor clock grid from the ring oscillator to driving from the PLL. The reference system clock should be valid at this time. The system clocks are guaranteed to be running after 3.3 V has been within specification for three milliseconds.

4. PWROK assertion to deassertion of RESET#.

The duration of RESET# assertion during cold boots is intended to satisfy the time it takes for the PLL to lock with a less than 1-ns phase error. The processor PLL begins to run after PWROK is asserted and the internal clock grid is switched from the ring oscillator to the PLL. The PLL lock time may take from hundreds of nanoseconds to tens of microseconds. It is recommended that the minimum time between PWROK assertion to the deassertion of RESET# be at least **1.0 ms**. AMD Southbridges enforce a delay of 1.5 to 2.0 milliseconds between PWRGD (Southbridge version of PWROK) assertion and NB\_RESET# deassertion.

5. PWROK must be monotonic.

The processor should not switch between the ring oscillator and the PLL after the initial assertion of PWROK.

6. NB\_RESET# must be asserted (causing CONNECT to also assert) before RESET# is deasserted. In practice all Southbridges enforce this requirement.

If NB\_RESET# does not assert until after RESET# has deasserted, the processor misinterprets the CONNECT assertion (due to NB\_RESET# being asserted) as the beginning of the SIP transfer (See “Serial Initialization Packet (SIP) Protocol” on page 38). There must be sufficient overlap in the resets to ensure that CONNECT is sampled asserted by the processor before RESET# is deasserted.

### **Clock Multiplier Selection (FID[3:0])**

When RESET# is deasserted, the chipset samples the FID[3:0] frequency ID from the processor in a chipset-specific manner. For more information, see “FID[3:0] Pins” on page 61.

The chipset uses this FID information and other information sampled at the deassertion of RESET# to determine the correct Serial Initialization Packet (SIP) to send to the processor for configuration of the AMD system bus for the clock multiplier processor frequency indicated by the FID[3:0] code. The SIP is

sent to the processor using the SIP protocol. This protocol uses the PROCRDY, CONNECT, and CLKFWRST signals, which are synchronous to SYSCLK.

**Serial Initialization Packet (SIP) Protocol** Refer to *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902 for details of the SIP protocol.

## 8.2 Processor Warm Reset Requirements

### The AMD Athlon™ Processor Model 4 and Northbridge Reset Pins

RESET cannot be asserted to the processor without also being asserted to the Northbridge. RESET# to the Northbridge is the same in as PCI RESET#. The minimum assertion for PCI RESET# is one millisecond. AMD Southbridges enforce a minimum assertion of RESET# to the processor, Northbridge, or PCI of 1.5 to 2.0 milliseconds.

## 9 Mechanical Data

### 9.1 Introduction

The AMD Athlon™ processor model 4 connects to the motherboard through a PGA socket named Socket A and utilizes the Ceramic Pin Grid Array (CPGA) package type described in “AMD Athlon™ Processor Model 4 CPGA Package Dimensions” on page 40. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

### 9.2 Die Loading

The processor die on the CPGA package is exposed at the top of the package. This is done to facilitate heat transfer from the die to an approved heat sink. It is critical that the mechanical loading of the heat sink does not exceed the limits shown in Table 15. Tool-assisted zero-insertion force sockets should be designed such that no load is placed on the ceramic substrate of the package. Any heat sink design should avoid loads on corners and edges of die. The CPGA package has compliant pads that serve to bring surfaces in planar contact.

**Table 15. CPGA Mechanical Loading**

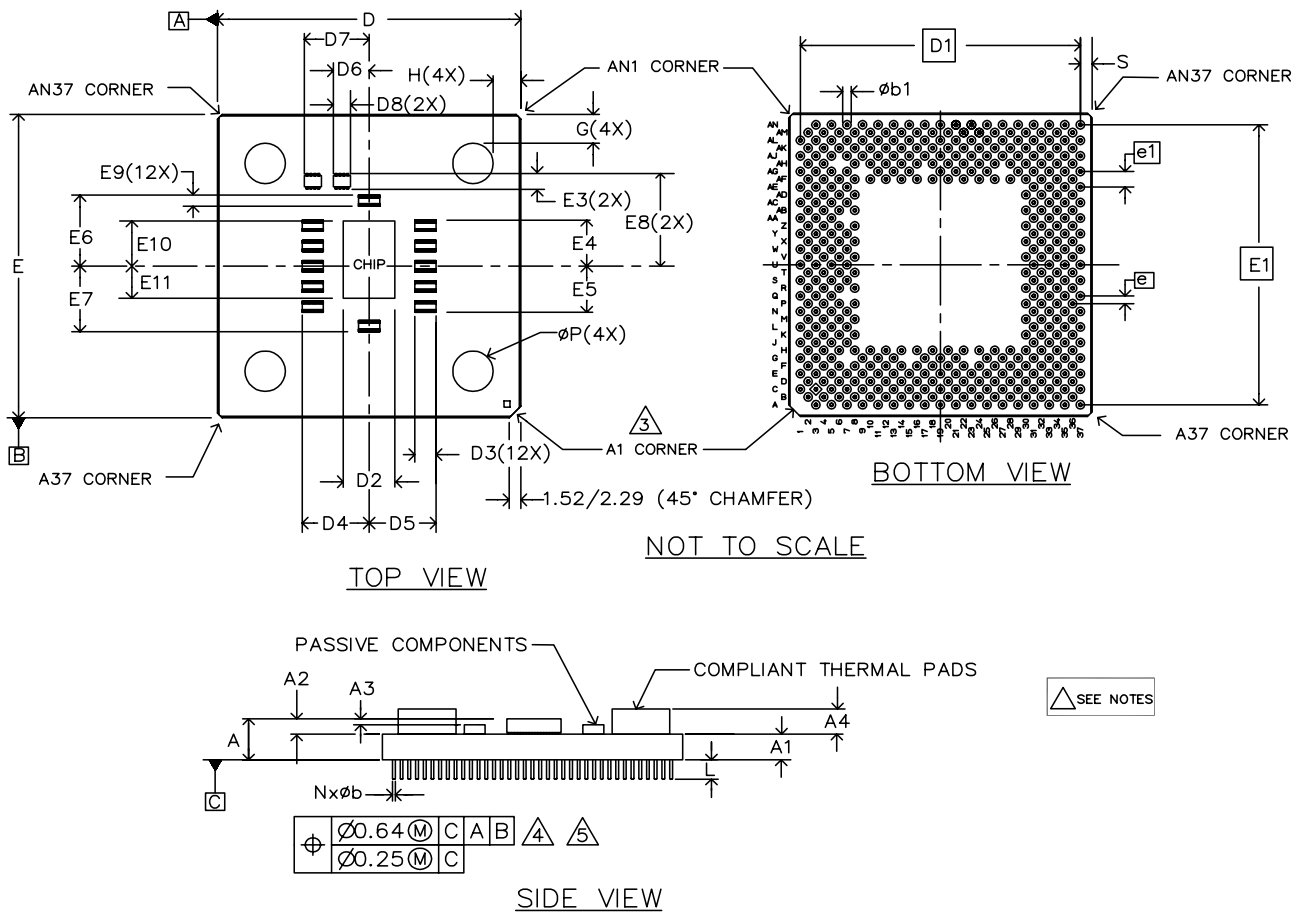
Location	Dynamic (MAX)	Static (MAX)	Units	Note
Die Surface	100	30	lbf	2
Die Edge	10	10	lbf	3
<b>Notes:</b>				
1. Load specified for coplanar contact to die surface.				
2. Load defined for a surface at no more than a two degree angle of inclination to die surface.				

### 9.3 AMD Athlon™ Processor Model 4 CPGA Package Dimensions

Figure 11 on page 41 shows a diagram and notes for the AMD Athlon processor model 4 CPGA package. Table 16 provides the dimensions in millimeters assigned to the letters and symbols shown in the Figure 11 diagram.

**Table 16. Dimensions for the AMD Athlon™ Processor Model 4 CPGA Package**

Letter or Symbol	Minimum Dimension*	Maximum Dimension*	Letter or Symbol	Minimum Dimension*	Maximum Dimension*
D/E	49.27	49.78	E11	5.79 REF	
D1/E1	45.72 BSC		G/H	–	4.50
D2	9.10 REF		A	2.24 REF	
D3	3.30	3.60	A1	1.27	1.53
D4	10.64	11.19	A2	0.80	0.88
D5	10.64	11.19	A3	0.116	–
D6	5.78	6.33	A4	–	1.90
D7	10.52	11.07	φP	–	6.60
D8	3.05	3.35	φb	0.43	0.50
E3	2.35	2.65	φb1	–	1.63
E4	7.25	7.80	S	1.435	2.375
E5	7.25	7.80	L	3.05	3.31
E6	14.15	14.42	M	37	
E7	10.41	10.96	N	453	
E8	14.84	15.39	e	1.27 BSC	
E9	1.66	1.96	e1	2.54 BSC	
E10	7.31 REF				
<b>Note:</b>					
* Dimensions are given in millimeters.					



GENERAL NOTES:

1. All dimensions are specified in millimeter (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner has a chamfer, and is marked with a square on top of the package to identify the pin A1 corner for handling and orientation purposes.
4. Pin tips should have radius.
5. Symbol "M" determines pin matrix size and "N" is number of pins.
6. For staggered pin configuration, pins on the same row are on a 2.54 mm grid. Adjacent rows offset by 1.27 mm.

Figure 11. AMD Athlon™ Processor Model 4 CPGA Package





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## 10 Pin Descriptions

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### 10.1 Pin Diagram and Pin Name Abbreviations

Figure 12 on page 44 shows the staggered Ceramic Pin Grid Array (CPGA) for the AMD Athlon™ processor model 4. Because some of the pin names are too long to fit in the grid, they are abbreviated. Figure 13 on page 45 shows the bottomside view of the array. Table 17 on page 46 lists all the pins in alphabetical order by pin name, along with the abbreviation where necessary.





Table 17. Pin Name Abbreviations

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	A20M#	AE1		NC	A19
	AMD	AH6		NC	A31
ANLOG	ANALOG	AJ13		NC	C13
CLKFR	CLKFWDRESET	AJ21		NC	E25
	CLKIN	AN17		NC	E33
	CLKIN#	AL17		NC	F8
CNNCT	CONNECT	AL23		NC	F30
	COREFB	AG11		NC	G11
	COREFB#	AG13		NC	G13
CPR#	CPU_PRESENCE#	AK6		NC	G19
	DBRDY	AA1		NC	G21
	DBREQ#	AA3		NC	G27
	FERR	AG1		NC	G29
	FID[0]	W1		NC	G31
	FID[1]	W3		NC	H6
	FID[2]	Y1		NC	H8
	FID[3]	Y3		NC	H10
	FLUSH#	AL3		NC	H28
	IGNNE#	AJ1		NC	H30
	INIT#	AJ3		NC	H32
	INTR	AL1		NC	J5
K7CO	K7CLKOUT	AL21		NC	J31
K7CO#	K7CLKOUT#	AN21		NC	K8
	KEY	G7		NC	K30
	KEY	G9		NC	L31
	KEY	G15		NC	L35
	KEY	G17		NC	N31
	KEY	G23		NC	Q31
	KEY	G25		NC	S7
	KEY	N7		NC	S31
	KEY	Q7		NC	U7
	KEY	Y7		NC	U31
	KEY	AA7		NC	U37
	KEY	AG7		NC	W7
	KEY	AG9		NC	W31
	KEY	AG15		NC	Y5
	KEY	AG17		NC	Y31
	KEY	AG27		NC	Y33
	KEY	AG29		NC	AA31

Table 17. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	NC	AC31	PICD#0	PICD[0]#	N3
	NC	AD8	PICD#1	PICD[1]#	N5
	NC	AD30	PLBYP#	PLLBYPASS#	AJ25
	NC	AE31	PLBYC	PLLBYPASSCLK	AN15
	NC	AF6	PLBYC#	PLLBYPASSCLK#	AL15
	NC	AF8	PLMN1	PLLMON1	AN13
	NC	AF10	PLMN2	PLLMON2	AL13
	NC	AF28	PLTST#	PLLTST#	AC3
	NC	AF30	PRCRDY	PROCREADY	AN23
	NC	AF32		PWROK	AE3
	NC	AG5		RESET#	AG3
	NC	AG19	RCLK	RSTCLK	AN19
	NC	AG21	RCLK#	RSTCLK#	AL19
	NC	AG23	SAI#0	SADDIN[0]#	AJ29
	NC	AG25	SAI#1	SADDIN[1]#	AL29
	NC	AG31	SAI#2	SADDIN[2]#	AG33
	NC	AH8	SAI#3	SADDIN[3]#	AJ37
	NC	AH30	SAI#4	SADDIN[4]#	AL35
	NC	AJ7	SAI#5	SADDIN[5]#	AE33
	NC	AJ9	SAI#6	SADDIN[6]#	AJ35
	NC	AJ11	SAI#7	SADDIN[7]#	AG37
	NC	AJ15	SAI#8	SADDIN[8]#	AL33
	NC	AJ17	SAI#9	SADDIN[9]#	AN37
	NC	AJ19	SAI#10	SADDIN[10]#	AL37
	NC	AJ27	SAI#11	SADDIN[11]#	AG35
	NC	AK8	SAI#12	SADDIN[12]#	AN29
	NC	AL7	SAI#13	SADDIN[13]#	AN35
	NC	AL9	SAI#14	SADDIN[14]#	AN31
	NC	AL11	SAIC#	SADDINCLK#	AJ33
	NC	AL25	SAO#0	SADDOUT[0]#	J1
	NC	AL27	SAO#1	SADDOUT[1]#	J3
	NC	AM8	SAO#2	SADDOUT[2]#	C7
	NC	AN7	SAO#3	SADDOUT[3]#	A7
	NC	AN9	SAO#4	SADDOUT[4]#	E5
	NC	AN11	SAO#5	SADDOUT[5]#	A5
	NC	AN25	SAO#6	SADDOUT[6]#	E7
	NC	AN27	SAO#7	SADDOUT[7]#	C1
	NMI	AN3	SAO#8	SADDOUT[8]#	C5
	PICCLK	N1	SAO#9	SADDOUT[9]#	C3

Table 17. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SAO#10	SADDOUT[10]#	G1	SD#29	SDATA[29]#	J37
SAO#11	SADDOUT[11]#	E1	SD#30	SDATA[30]#	A37
SAO#12	SADDOUT[12]#	A3	SD#31	SDATA[31]#	E35
SAO#13	SADDOUT[13]#	G5	SD#32	SDATA[32]#	E31
SAO#14	SADDOUT[14]#	G3	SD#33	SDATA[33]#	E29
SAOC#	SADDOUTCLK#	E3	SD#34	SDATA[34]#	A27
SCNCK1	SCANCLK1	S1	SD#35	SDATA[35]#	A25
SCNCK2	SCANCLK2	S5	SD#36	SDATA[36]#	E21
SCNINV	SCANINTEVAL	S3	SD#37	SDATA[37]#	C23
SCNSN	SCANSHIFTEN	Q5	SD#38	SDATA[38]#	C27
SD#0	SDATA[0]#	AA35	SD#39	SDATA[39]#	A23
SD#1	SDATA[1]#	W37	SD#40	SDATA[40]#	A35
SD#2	SDATA[2]#	W35	SD#41	SDATA[41]#	C35
SD#3	SDATA[3]#	Y35	SD#42	SDATA[42]#	C33
SD#4	SDATA[4]#	U35	SD#43	SDATA[43]#	C31
SD#5	SDATA[5]#	U33	SD#44	SDATA[44]#	A29
SD#6	SDATA[6]#	S37	SD#45	SDATA[45]#	C29
SD#7	SDATA[7]#	S33	SD#46	SDATA[46]#	E23
SD#8	SDATA[8]#	AA33	SD#47	SDATA[47]#	C25
SD#9	SDATA[9]#	AE37	SD#48	SDATA[48]#	E17
SD#10	SDATA[10]#	AC33	SD#49	SDATA[49]#	E13
SD#11	SDATA[11]#	AC37	SD#50	SDATA[50]#	E11
SD#12	SDATA[12]#	Y37	SD#51	SDATA[51]#	C15
SD#13	SDATA[13]#	AA37	SD#52	SDATA[52]#	E9
SD#14	SDATA[14]#	AC35	SD#53	SDATA[53]#	A13
SD#15	SDATA[15]#	S35	SD#54	SDATA[54]#	C9
SD#16	SDATA[16]#	Q37	SD#55	SDATA[55]#	A9
SD#17	SDATA[17]#	Q35	SD#56	SDATA[56]#	C21
SD#18	SDATA[18]#	N37	SD#57	SDATA[57]#	A21
SD#19	SDATA[19]#	J33	SD#58	SDATA[58]#	E19
SD#20	SDATA[20]#	G33	SD#59	SDATA[59]#	C19
SD#21	SDATA[21]#	G37	SD#60	SDATA[60]#	C17
SD#22	SDATA[22]#	E37	SD#61	SDATA[61]#	A11
SD#23	SDATA[23]#	G35	SD#62	SDATA[62]#	A17
SD#24	SDATA[24]#	Q33	SD#63	SDATA[63]#	A15
SD#25	SDATA[25]#	N33	SDIC#0	SDATAINCLK[0]#	W33
SD#26	SDATA[26]#	L33	SDIC#1	SDATAINCLK[1]#	J35
SD#27	SDATA[27]#	N35	SDIC#2	SDATAINCLK[2]#	E27
SD#28	SDATA[28]#	L37	SDIC#3	SDATAINCLK[3]#	E15

**Table 17. Pin Name Abbreviations (continued)**

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
SDINV#	SDATAINVALID#	AN33	VCC	VCC_CORE	F34
SDOC#0	SDATAOUTCLK[0]#	AE35	VCC	VCC_CORE	F36
SDOC#1	SDATAOUTCLK[1]#	C37	VCC	VCC_CORE	H2
SDOC#2	SDATAOUTCLK[2]#	A33	VCC	VCC_CORE	H4
SDOC#3	SDATAOUTCLK[3]#	C11	VCC	VCC_CORE	H12
SDOV#	SDATAOUTVALID#	AL31	VCC	VCC_CORE	H16
SFILLV#	SFILLVALID#	AJ31	VCC	VCC_CORE	H20
	SMI#	AN5	VCC	VCC_CORE	H24
STPC#	STPCLK#	AC1	VCC	VCC_CORE	K32
SVRFM	SYSVREFMODE	AA5	VCC	VCC_CORE	K34
	TCK	Q1	VCC	VCC_CORE	K36
	TDI	U1	VCC	VCC_CORE	M2
	TDO	U5	VCC	VCC_CORE	M4
	TMS	Q3	VCC	VCC_CORE	M6
	TRST#	U3	VCC	VCC_CORE	M8
VCC	VCC_CORE	B4	VCC	VCC_CORE	P30
VCC	VCC_CORE	B8	VCC	VCC_CORE	P32
VCC	VCC_CORE	B12	VCC	VCC_CORE	P34
VCC	VCC_CORE	B16	VCC	VCC_CORE	P36
VCC	VCC_CORE	B20	VCC	VCC_CORE	R2
VCC	VCC_CORE	B24	VCC	VCC_CORE	R4
VCC	VCC_CORE	B28	VCC	VCC_CORE	R6
VCC	VCC_CORE	B32	VCC	VCC_CORE	R8
VCC	VCC_CORE	B36	VCC	VCC_CORE	T30
VCC	VCC_CORE	D2	VCC	VCC_CORE	T32
VCC	VCC_CORE	D4	VCC	VCC_CORE	T34
VCC	VCC_CORE	D8	VCC	VCC_CORE	T36
VCC	VCC_CORE	D12	VCC	VCC_CORE	V2
VCC	VCC_CORE	D16	VCC	VCC_CORE	V4
VCC	VCC_CORE	D20	VCC	VCC_CORE	V6
VCC	VCC_CORE	D24	VCC	VCC_CORE	V8
VCC	VCC_CORE	D28	VCC	VCC_CORE	X30
VCC	VCC_CORE	D32	VCC	VCC_CORE	X32
VCC	VCC_CORE	F12	VCC	VCC_CORE	X34
VCC	VCC_CORE	F16	VCC	VCC_CORE	X36
VCC	VCC_CORE	F20	VCC	VCC_CORE	Z2
VCC	VCC_CORE	F24	VCC	VCC_CORE	Z4
VCC	VCC_CORE	F28	VCC	VCC_CORE	Z6
VCC	VCC_CORE	F32	VCC	VCC_CORE	Z8

Table 17. Pin Name Abbreviations (continued)

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
VCC	VCC_CORE	AB30	VCC	VCC_CORE	AM34
VCC	VCC_CORE	AB32		VCCA	AJ23
VCC	VCC_CORE	AB34		VCC_Z	AC7
VCC	VCC_CORE	AB36		VID[0]	L1
VCC	VCC_CORE	AD2		VID[1]	L3
VCC	VCC_CORE	AD4		VID[2]	L5
VCC	VCC_CORE	AD6		VID[3]	L7
VCC	VCC_CORE	AF14		VID[4]	J7
VCC	VCC_CORE	AF18	VREF_S	VREF_SYS	W5
VCC	VCC_CORE	AF22		VSS	B2
VCC	VCC_CORE	AF26		VSS	B6
VCC	VCC_CORE	AF34		VSS	B10
VCC	VCC_CORE	AF36		VSS	B14
VCC	VCC_CORE	AH2		VSS	B18
VCC	VCC_CORE	AH4		VSS	B22
VCC	VCC_CORE	AH10		VSS	B26
VCC	VCC_CORE	AH14		VSS	B30
VCC	VCC_CORE	AH18		VSS	B34
VCC	VCC_CORE	AH22		VSS	D6
VCC	VCC_CORE	AH26		VSS	D10
VCC	VCC_CORE	AK10		VSS	D14
VCC	VCC_CORE	AK14		VSS	D18
VCC	VCC_CORE	AK18		VSS	D22
VCC	VCC_CORE	AK22		VSS	D26
VCC	VCC_CORE	AK26		VSS	D30
VCC	VCC_CORE	AK30		VSS	D34
VCC	VCC_CORE	AK34		VSS	D36
VCC	VCC_CORE	AK36		VSS	F2
VCC	VCC_CORE	AJ5		VSS	F4
VCC	VCC_CORE	AL5		VSS	F6
VCC	VCC_CORE	AM2		VSS	F10
VCC	VCC_CORE	AM10		VSS	F14
VCC	VCC_CORE	AM14		VSS	F18
VCC	VCC_CORE	AM18		VSS	F22
VCC	VCC_CORE	AM22		VSS	F26
VCC	VCC_CORE	AM26		VSS	H14
VCC	VCC_CORE	AM22		VSS	H18
VCC	VCC_CORE	AM26		VSS	H22
VCC	VCC_CORE	AM30		VSS	H26



**Table 17. Pin Name Abbreviations (continued)**

Abbreviation	Full Name	Pin	Abbreviation	Full Name	Pin
	VSS	H34		VSS	AD36
	VSS	H36		VSS	AF2
	VSS	K2		VSS	AF4
	VSS	K4		VSS	AF12
	VSS	K6		VSS	AF16
	VSS	M30		VSS	AH12
	VSS	M32		VSS	AH16
	VSS	M34		VSS	AH20
	VSS	M36		VSS	AH24
	VSS	P2		VSS	AH28
	VSS	P4		VSS	AH32
	VSS	P6		VSS	AH34
	VSS	P8		VSS	AH36
	VSS	R30		VSS	AK2
	VSS	R32		VSS	AK4
	VSS	R34		VSS	AK12
	VSS	R36		VSS	AK16
	VSS	T2		VSS	AK20
	VSS	T4		VSS	AK24
	VSS	T6		VSS	AK28
	VSS	T8		VSS	AK32
	VSS	V30		VSS	AM4
	VSS	V32		VSS	AM6
	VSS	V34		VSS	AM12
	VSS	V36		VSS	AM16
	VSS	X2		VSS	AM20
	VSS	X4		VSS	AM24
	VSS	X6		VSS	AM28
	VSS	X8		VSS	AM32
	VSS	Z30		VSS	AM36
	VSS	Z32		VSS_Z	AE7
	VSS	Z34		ZN	AC5
	VSS	Z36		ZP	AE5
	VSS	AB2			
	VSS	AB8			
	VSS	AB4			
	VSS	AB6			
	VSS	AD32			
	VSS	AD34			

## 10.2 Pin List

Table 18 cross-references Socket A pin location to signal name.

The “L” (Level) column shows the electrical specification for this pin. “P” indicates a push-pull mode driven by a single source. “O” indicates open-drain mode that allows devices to share the pin.

*Note: The Socket A AMD Duron Processor supports push-pull drivers. For more information, see “Push-Pull (PP) Drivers” on page 6.*

The “P” (Port) column indicates if this signal is an input (I), output (O), or bidirectional (B) signal. The “R” (Reference) column indicates if this signal should be referenced to VSS (G) or VCC\_CORE (P) planes for the purpose of signal routing with respect to the current return paths.

**Table 18. Cross-Reference by Pin Location**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
A1	No Pin	page 63	-	-	-	B2	VSS		-	-	-
A3	SADDOUT[12]#		P	O	G	B4	VCC_CORE		-	-	-
A5	SADDOUT[5]#		P	O	G	B6	VSS		-	-	-
A7	SADDOUT[3]#		P	O	G	B8	VCC_CORE		-	-	-
A9	SDATA[55]#		P	B	P	B10	VSS		-	-	-
A11	SDATA[61]#		P	B	P	B12	VCC_CORE		-	-	-
A13	SDATA[53]#		P	B	G	B14	VSS		-	-	-
A15	SDATA[63]#		P	B	G	B16	VCC_CORE		-	-	-
A17	SDATA[62]#		P	B	G	B18	VSS		-	-	-
A19	NC Pin	page 63	-	-	-	B20	VCC_CORE		-	-	-
A21	SDATA[57]#		P	B	G	B22	VSS		-	-	-
A23	SDATA[39]#		P	B	G	B24	VCC_CORE		-	-	-
A25	SDATA[35]#		P	B	P	B26	VSS		-	-	-
A27	SDATA[34]#		P	B	P	B28	VCC_CORE		-	-	-
A29	SDATA[44]#		P	B	G	B30	VSS		-	-	-
A31	NC Pin	page 63	-	-	-	B32	VCC_CORE		-	-	-
A33	SDATAOUTCLK[2]#		P	O	P	B34	VSS		-	-	-
A35	SDATA[40]#		P	B	G	B36	VCC_CORE		-	-	-
A37	SDATA[30]#		P	B	P	C1	SADDOUT[7]#		P	O	G

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
C3	SADDOUT[9]#		P	O	G	D34	VSS		-	-	-
C5	SADDOUT[8]#		P	O	G	D36	VSS		-	-	-
C7	SADDOUT[2]#		P	O	G	E1	SADDOUT[11]#		P	O	P
C9	SDATA[54]#		P	B	P	E3	SADDOUTCLK#		P	O	G
C11	SDATAOUTCLK[3]#		P	O	G	E5	SADDOUT[4]#		P	O	P
C13	NC Pin	page 63	-	-	-	E7	SADDOUT[6]#		P	O	G
C15	SDATA[51]#		P	B	P	E9	SDATA[52]#		P	B	P
C17	SDATA[60]#		P	B	G	E11	SDATA[50]#		P	B	P
C19	SDATA[59]#		P	B	G	E13	SDATA[49]#		P	B	G
C21	SDATA[56]#		P	B	G	E15	SDATAINCLK[3]#		P	I	G
C23	SDATA[37]#		P	B	P	E17	SDATA[48]#		P	B	P
C25	SDATA[47]#		P	B	G	E19	SDATA[58]#		P	B	G
C27	SDATA[38]#		P	B	G	E21	SDATA[36]#		P	B	P
C29	SDATA[45]#		P	B	G	E23	SDATA[46]#		P	B	P
C31	SDATA[43]#		P	B	G	E25	NC Pin	page 63	-	-	-
C33	SDATA[42]#		P	B	G	E27	SDATAINCLK[2]#		P	I	G
C35	SDATA[41]#		P	B	G	E29	SDATA[33]#		P	B	P
C37	SDATAOUTCLK[1]#		P	O	G	E31	SDATA[32]#		P	B	P
D2	VCC_CORE		-	-	-	E33	NC Pin	page 63	-	-	-
D4	VCC_CORE		-	-	-	E35	SDATA[31]#		P	B	P
D6	VSS		-	-	-	E37	SDATA[22]#		P	B	G
D8	VCC_CORE		-	-	-	F2	VSS		-	-	-
D10	VSS		-	-	-	F4	VSS		-	-	-
D12	VCC_CORE		-	-	-	F6	VSS		-	-	-
D14	VSS		-	-	-	F8	NC Pin	page 63	-	-	-
D16	VCC_CORE		-	-	-	F10	VSS		-	-	-
D18	VSS		-	-	-	F12	VCC_CORE		-	-	-
D20	VCC_CORE		-	-	-	F14	VSS		-	-	-
D22	VSS		-	-	-	F16	VCC_CORE		-	-	-
D24	VCC_CORE		-	-	-	F18	VSS		-	-	-
D26	VSS		-	-	-	F20	VCC_CORE		-	-	-
D28	VCC_CORE		-	-	-	F22	VSS		-	-	-
D30	VSS		-	-	-	F24	VCC_CORE		-	-	-
D32	VCC_CORE		-	-	-	F26	VSS		-	-	-

**Table 18. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
F28	VCC_CORE		-	-	-	H22	VSS		-	-	-
F30	NC Pin	page 63	-	-	-	H24	VCC_CORE		-	-	-
F32	VCC_CORE		-	-	-	H26	VSS		-	-	-
F34	VCC_CORE		-	-	-	H28	NC Pin	page 63	-	-	-
F36	VCC_CORE		-	-	-	H30	NC Pin	page 63	-	-	-
G1	SADDOUT[10]#		P	O	P	H32	NC Pin	page 63	-	-	-
G3	SADDOUT[14]#		P	O	G	H34	VSS		-	-	-
G5	SADDOUT[13]#		P	O	G	H36	VSS		-	-	-
G7	Key Pin	page 63	-	-	-	J1	SADDOUT[0]#	page 64	P	O	-
G9	Key Pin	page 63	-	-	-	J3	SADDOUT[1]#	page 64	P	O	-
G11	NC Pin	page 63	-	-	-	J5	NC Pin	page 63	-	-	-
G13	NC Pin	page 63	-	-	-	J7	VID[4]	page 65	O	O	-
G15	Key Pin	page 63	-	-	-	J31	NC Pin	page 63	-	-	-
G17	Key Pin	page 63	-	-	-	J33	SDATA[19]#		P	B	G
G19	NC Pin	page 63	-	-	-	J35	SDATAINCLK[1]#		P	I	P
G21	NC Pin	page 63	-	-	-	J37	SDATA[29]#		P	B	P
G23	Key Pin	page 63	-	-	-	K2	VSS		-	-	-
G25	Key Pin	page 63	-	-	-	K4	VSS		-	-	-
G27	NC Pin	page 63	-	-	-	K6	VSS		-	-	-
G29	NC Pin	page 63	-	-	-	K8	NC Pin	page 63	-	-	-
G31	NC Pin	page 63	-	-	-	K30	NC Pin	page 63	-	-	-
G33	SDATA[20]#		P	B	G	K32	VCC_CORE		-	-	-
G35	SDATA[23]#		P	B	G	K34	VCC_CORE		-	-	-
G37	SDATA[21]#		P	B	G	K36	VCC_CORE		-	-	-
H2	VCC_CORE		-	-	-	L1	VID[0]	page 65	O	O	-
H4	VCC_CORE		-	-	-	L3	VID[1]	page 65	O	O	-
H6	NC Pin	page 63	-	-	-	L5	VID[2]	page 65	O	O	-
H8	NC Pin	page 63	-	-	-	L7	VID[3]	page 65	O	O	-
H10	NC Pin	page 63	-	-	-	L31	NC Pin	page 63	-	-	-
H12	VCC_CORE		-	-	-	L33	SDATA[26]#		P	B	P
H14	VSS		-	-	-	L35	NC Pin	page 63	-	-	-
H16	VCC_CORE		-	-	-	L37	SDATA[28]#		P	B	P
H18	VSS		-	-	-	M2	VCC_CORE		-	-	-
H20	VCC_CORE		-	-	-	M4	VCC_CORE		-	-	-

**Table 18. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
M6	VCC_CORE		-	-	-	R30	VSS		-	-	-
M8	VCC_CORE		-	-	-	R32	VSS		-	-	-
M30	VSS		-	-	-	R34	VSS		-	-	-
M32	VSS		-	-	-	R36	VSS		-	-	-
M34	VSS		-	-	-	S1	SCANCLK1	page 64	P	I	-
M36	VSS		-	-	-	S3	SCANINTEVAL	page 64	P	I	-
N1	PICCLK	page 60	O	I	-	S5	SCANCLK2	page 64	P	I	-
N3	PICD#[0]	page 60	O	B	-	S7	NC Pin	page 63	-	-	-
N5	PICD#[1]	page 60	O	B	-	S31	NC Pin	page 63	-	-	-
N7	Key Pin	page 63	-	-	-	S33	SDATA[7]#		P	B	G
N31	NC Pin	page 63	-	-	-	S35	SDATA[15]#		P	B	P
N33	SDATA[25]#		P	B	P	S37	SDATA[6]#		P	B	G
N35	SDATA[27]#		P	B	P	T2	VSS		-	-	-
N37	SDATA[18]#		P	B	G	T4	VSS		-	-	-
P2	VSS		-	-	-	T6	VSS		-	-	-
P4	VSS		-	-	-	T8	VSS		-	-	-
P6	VSS		-	-	-	T30	VCC_CORE		-	-	-
P8	VSS		-	-	-	T32	VCC_CORE		-	-	-
P30	VCC_CORE		-	-	-	T34	VCC_CORE		-	-	-
P32	VCC_CORE		-	-	-	T36	VCC_CORE		-	-	-
P34	VCC_CORE		-	-	-	U1	TDI	page 63	P	I	-
P36	VCC_CORE		-	-	-	U3	TRST#	page 63	P	I	-
Q1	TCK	page 63	P	I	-	U5	TDO	page 63	P	O	-
Q3	TMS	page 63	P	I	-	U7	NC Pin	page 63	-	-	-
Q5	SCANSHIFTEN	page 64	P	I	-	U31	NC Pin	page 63	-	-	-
Q7	Key Pin	page 63	-	-	-	U33	SDATA[5]#		P	B	G
Q31	NC Pin	page 63	-	-	-	U35	SDATA[4]#		P	B	G
Q33	SDATA[24]#		P	B	P	U37	NC Pin	page 63	-	-	-
Q35	SDATA[17]#		P	B	G	V2	VCC_CORE		-	-	-
Q37	SDATA[16]#		P	B	G	V4	VCC_CORE		-	-	-
R2	VCC_CORE		-	-	-	V6	VCC_CORE		-	-	-
R4	VCC_CORE		-	-	-	V8	VCC_CORE		-	-	-
R6	VCC_CORE		-	-	-	V30	VSS		-	-	-
R8	VCC_CORE		-	-	-	V32	VSS		-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
V34	VSS		-	-	-	AA1	DBRDY	page 61	P	O	-
V36	VSS		-	-	-	AA3	DBREQ#	page 61	P	I	-
W1	FID[0]	page 62	O	-	-	AA5	SYSVREFMODE	page 64	P	I	-
W3	FID[1]	page 62	O	-	-	AA7	Key Pin	page 63	-	-	-
W5	VREFSYS	page 66	P	-	-	AA31	NC Pin	page 63	-	-	-
W7	NC Pin	page 63	-	-	-	AA33	SDATA[8]#		P	B	P
W31	NC Pin	page 63	-	-	-	AA35	SDATA[0]#		P	B	G
W33	SDATAINCLK[0]#		P	I	G	AA37	SDATA[13]#		P	B	G
W35	SDATA[2]#		P	B	G	AB2	VSS		-	-	-
W37	SDATA[1]#		P	B	P	AB4	VSS		-	-	-
X2	VSS		-	-	-	AB6	VSS		-	-	-
X4	VSS		-	-	-	AB8	VSS		-	-	-
X6	VSS		-	-	-	AB30	VCC_CORE		-	-	-
X8	VSS		-	-	-	AB32	VCC_CORE		-	-	-
X30	VCC_CORE		-	-	-	AB34	VCC_CORE		-	-	-
X32	VCC_CORE		-	-	-	AB36	VCC_CORE		-	-	-
X34	VCC_CORE		-	-	-	AC1	STPCLK#	page 64	P	I	-
X36	VCC_CORE		-	-	-	AC3	PLLTEST#	page 64	P	I	-
Y1	FID[2]	page 62	O	-	-	AC5	ZN	page 66	P	-	-
Y3	FID[3]	page 62	O	-	-	AC7	VCC_Z	page 66	-	-	-
Y5	NC Pin	page 63	-	-	-	AC31	NC Pin	page 63	-	-	-
Y7	Key Pin	page 63	-	-	-	AC33	SDATA[10]#		P	B	P
Y31	NC Pin	page 63	-	-	-	AC35	SDATA[14]#		P	B	G
Y33	NC Pin	page 63	-	-	-	AC37	SDATA[11]#		P	B	G
Y35	SDATA[3]#		P	B	G	AD2	VCC_CORE		-	-	-
Y37	SDATA[12]#		P	B	P	AD4	VCC_CORE		-	-	-
Z2	VCC_CORE		-	-	-	AD6	VCC_CORE		-	-	-
Z4	VCC_CORE		-	-	-	AD8	NC Pin	page 63	-	-	-
Z6	VCC_CORE		-	-	-	AD30	NC Pin	page 63	-	-	-
Z8	VCC_CORE		-	-	-	AD32	VSS		-	-	-
Z30	VSS		-	-	-	AD34	VSS		-	-	-
Z32	VSS		-	-	-	AD36	VSS		-	-	-
Z34	VSS		-	-	-	AE1	A20M#		P	I	-
Z36	VSS		-	-	-	AE3	PWROK		P	I	-

**Table 18. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AE5	ZP	page 66	P	-	-	AG21	NC Pin	page 63	-	-	-
AE7	VSS_Z	page 66	-	-	-	AG23	NC Pin	page 63	-	-	-
AE31	NC Pin	page 63	-	-	-	AG25	NC Pin	page 63	-	-	-
AE33	SADDIN[5]#		P	I	G	AG27	Key Pin	page 63	-	-	-
AE35	SDATAOUTCLK[0]#		P	O	P	AG29	Key Pin	page 63	-	-	-
AE37	SDATA[9]#		P	B	G	AG31	NC Pin	page 63	-	-	-
AF2	VSS		-	-	-	AG33	SADDIN[2]#		P	I	G
AF4	VSS		-	-	-	AG35	SADDIN[11]#		P	I	G
AF6	NC Pin	page 63	-	-	-	AG37	SADDIN[7]#		P	I	P
AF8	NC Pin	page 63	-	-	-	AH2	VCC_CORE		-	-	-
AF10	NC Pin	page 63	-	-	-	AH4	VCC_CORE		-	-	-
AF12	VSS		-	-	-	AH6	AMD Pin	page 60	-	-	-
AF14	VCC_CORE		-	-	-	AH8	NC Pin	page 63	-	-	-
AF16	VSS		-	-	-	AH10	VCC_CORE		-	-	-
AF18	VCC_CORE		-	-	-	AH12	VSS		-	-	-
AF20	VSS		-	-	-	AH14	VCC_CORE		-	-	-
AF22	VCC_CORE		-	-	-	AH16	VSS		-	-	-
AF24	VSS		-	-	-	AH18	VCC_CORE		-	-	-
AF26	VCC_CORE		-	-	-	AH20	VSS		-	-	-
AF28	NC Pin	page 63	-	-	-	AH22	VCC_CORE		-	-	-
AF30	NC Pin	page 63	-	-	-	AH24	VSS		-	-	-
AF32	NC Pin	page 63	-	-	-	AH26	VCC_CORE		-	-	-
AF34	VCC_CORE		-	-	-	AH28	VSS		-	-	-
AF36	VCC_CORE		-	-	-	AH30	NC Pin	page 63	-	-	-
AG1	FERR	page 61	P	O	-	AH32	VSS		-	-	-
AG3	RESET#		-	I	-	AH34	VSS		-	-	-
AG5	NC Pin	page 63	-	-	-	AH36	VSS		-	-	-
AG7	Key Pin	page 63	-	-	-	AJ1	IGNNE#	page 63	P	I	-
AG9	Key Pin	page 63	-	-	-	AJ3	INIT#	page 63	P	I	-
AG11	COREFB	page 61	-	-	-	AJ5	VCC_CORE		-	-	-
AG13	COREFB#	page 61	-	-	-	AJ7	NC Pin	page 63	-	-	-
AG15	Key Pin	page 63	-	-	-	AJ9	NC Pin	page 63	-	-	-
AG17	Key Pin	page 63	-	-	-	AJ11	NC Pin	page 63	-	-	-
AG19	NC Pin	page 63	-	-	-	AJ13	Analog	page 60	-	-	-

Table 18. Cross-Reference by Pin Location (continued)

Pin	Name	Description	L	P	R	Pin	Name	Description	L	P	R
AJ15	NC Pin	page 63	-	-	-	AL9	NC Pin	page 63	-	-	-
AJ17	NC Pin	page 63	-	-	-	AL11	NC Pin	page 63	-	-	-
AJ19	NC Pin	page 63	-	-	-	AL13	PLLMON2	page 64	O	O	-
AJ21	CLKFWDRST	page 60	P	I	P	AL15	PLLBYPASSCLK#	page 64	P	I	-
AJ23	VCCA	page 65	-	-	-	AL17	CLKIN#	page 60	P	I	P
AJ25	PLLBYPASS#	page 64	P	I	-	AL19	RSTCLK#	page 60	P	I	P
AJ27	NC Pin	page 63	-	-	-	AL21	K7CLKOUT	page 63	P	O	-
AJ29	SADDIN[0]#	page 64	P	I	-	AL23	CONNECT	page 60	P	I	P
AJ31	SFILLVALID#		P	I	G	AL25	NC Pin	page 63	-	-	-
AJ33	SADDINCLK#		P	I	G	AL27	NC Pin	page 63	-	-	-
AJ35	SADDIN[6]#		P	I	P	AL29	SADDIN[1]#	page 64	P	I	-
AJ37	SADDIN[3]#		P	I	G	AL31	SDATAOUTVALID#		P	O	P
AK2	VSS		-	-	-	AL33	SADDIN[8]#		P	I	P
AK4	VSS		-	-	-	AL35	SADDIN[4]#		P	I	G
AK6	CPU_PRESENCE#	page 61	-	-	-	AL37	SADDIN[10]#		P	I	G
AK8	NC Pin	page 63	-	-	-	AM2	VCC_CORE		-	-	-
AK10	VCC_CORE		-	-	-	AM4	VSS		-	-	-
AK12	VSS		-	-	-	AM6	VSS		-	-	-
AK14	VCC_CORE		-	-	-	AM8	NC Pin	page 63	-	-	-
AK16	VSS		-	-	-	AM10	VCC_CORE		-	-	-
AK18	VCC_CORE		-	-	-	AM12	VSS		-	-	-
AK20	VSS		-	-	-	AM14	VCC_CORE		-	-	-
AK22	VCC_CORE		-	-	-	AM16	VSS		-	-	-
AK24	VSS		-	-	-	AM18	VCC_CORE		-	-	-
AK26	VCC_CORE		-	-	-	AM20	VSS		-	-	-
AK28	VSS		-	-	-	AM22	VCC_CORE		-	-	-
AK30	VCC_CORE		-	-	-	AM24	VSS		-	-	-
AK32	VSS		-	-	-	AM26	VCC_CORE		-	-	-
AK34	VCC_CORE		-	-	-	AM28	VSS		-	-	-
AK36	VCC_CORE		-	-	-	AM30	VCC_CORE		-	-	-
AL1	INTR	page 63	P	I	-	AM32	VSS		-	-	-
AL3	FLUSH#	page 63	P	I	-	AM34	VCC_CORE		-	-	-
AL5	VCC_CORE		-	-	-	AM36	VSS		-	-	-
AL7	NC Pin	page 63	-	-	-	AN1	No Pin	page 63	-	-	-



**Table 18. Cross-Reference by Pin Location (continued)**

Pin	Name	Description	L	P	R
AN3	NMI		P	I	-
AN5	SMI#		P	I	-
AN7	NC Pin	page 63	-	-	-
AN9	NC Pin	page 63	-	-	-
AN11	NC Pin	page 63	-	-	-
AN13	PLLMON1	page 64	O	B	-
AN15	PLLBYPASSCLK	page 64	P	I	-
AN17	CLKIN	page 60	P	I	P
AN19	RSTCLK	page 60	P	I	P
AN21	K7CLKOUT#	page 63	P	O	-
AN23	PROCRDY		P	O	P
AN25	NC Pin	page 63	-	-	-
AN27	NC Pin	page 63	-	-	-
AN29	SADDIN[12]#		P	I	G
AN31	SADDIN[14]#		P	I	G
AN33	SDATAINVALID#		P	I	P
AN35	SADDIN[13]#		P	I	G
AN37	SADDIN[9]#		P	I	G

### 10.3 Detailed Pin Descriptions

The information in this section pertains to Table 18 on page 52.

<b>A20M# Pin</b>	A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.
<b>AMD Pin</b>	AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.
<b>AMD Athlon™ System Bus Pins</b>	See the <i>AMD Athlon™ and AMD Duron™ System Bus Specification</i> , order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.
<b>Analog Pin</b>	Treat this pin as a NC.
<b>APIC Pins, PICCLK, PICD[1:0]#</b>	The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. The pin, PICCLK, must be driven with a valid clock input. For more information, see Table 14, “APIC Pins AC and DC Characteristics,” on page 34.
<b>CLKFWRST Pin</b>	CLKFWRST resets clock-forward circuitry for both the system and processor.
<b>CLKIN, RSTCLK (SYSCLK) Pins</b>	Connect CLKIN (AN17) with RSTCLK (AN19) and name it SYSCLK. Connect CLKIN# (AL17) with RSTCLK# (AL19) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor. See “SYSCLK and SYSCLK# Pins” on page 64 for more information.
<b>CONNECT Pin</b>	CONNECT is an input from the system used for power management and clock-forward initialization at reset.

<b>COREFB and COREFB# Pins</b>	COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.
<b>CPU_PRESENCE# Pin</b>	CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# can be used to detect the presence or absence of a processor in the Socket A-style socket.
<b>DBRDY and DBREQ# Pins</b>	DBRDY (AA1) and DBREQ# (AA3) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.
<b>FERR Pin</b>	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the <i>AMD Athlon™ Processor-Based Motherboard Design Guide</i> order# 24363.
<b>FID[3:0] Pins</b>	<p>See “Frequency Identification (FID[3:0])” on page 24 for the AC and DC characteristics for FID[3:0].</p> <p>FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYCLK ratio. Table 19 on page 62 describes the encodings of the clock multipliers on FID[3:0].</p>

**Table 19. FID[3:0] Clock Multiplier Encodings**

FID[3]	FID[2]	FID[1]	FID[0]	Processor Clock to SYSCLK Frequency Ratio
0	0	0	0	11
0	0	0	1	11.5
0	0	1	0	12
0	0	1	1	≥ 12.5*
0	1	0	0	5
0	1	0	1	5.5
0	1	1	0	6
0	1	1	1	6.5
1	0	0	0	7
1	0	0	1	7.5
1	0	1	0	8
1	0	1	1	8.5
1	1	0	0	9
1	1	0	1	9.5
1	1	1	0	10
1	1	1	1	10.5

**Note:**  
\*All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011, which causes the SIP configuration for all ratios of 12.5x or greater to be the same.

The FID[3:0] signals are open drain processor outputs that are pulled High on the motherboard and sampled by the chipset at the deassertion of RESET# to determine the SIP (Serialization Initialization Packet) that gets sent to the processor. See the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order#21902 for more information about the Serialization Initialization Packets and SIP protocol.

The processor FID[3:0] outputs are open drain and 2.5V tolerant. To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor. For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

<b>FLUSH# Pin</b>	FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
<b>IGNNE# Pin</b>	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
<b>INIT# Pin</b>	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0_FFFF_FFF0h.
<b>INTR Pin</b>	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
<b>JTAG Pins</b>	TCK (Q1), TMS (Q3), TDI (U1), TRST# (U3), and TDO (U5) are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE with pullup resistors.
<b>K7CLKOUT and K7CLKOUT# Pins</b>	K7CLKOUT (AL21) and K7CLKOUT# (AN21) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.
<b>Key Pins</b>	These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (no connect) pins. See “NC Pins” on page 63 for more information. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.
<b>NC Pins</b>	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
<b>NMI Pin</b>	NMI is an input from the system that causes a non-maskable interrupt.
<b>PGA Orientation Pins</b>	No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations.

For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

**PLL Bypass and Test Pins**

PLLTEST# (AC3), PLLBYPASS# (AJ25), PLLMON1 (AN13), PLLMON2 (AL13), PLLBYPASSCLK (AN15), and PLLBYPASSCLK# (AL15) are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC\_CORE with pullup resistors.

**PWROK Pin**

The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.

For more information, See “Signal and Power-Up Requirements” on page 35.

**SADDIN[1:0]# and SADDOUT[1:0]# Pins**

The AMD Athlon processor model 4 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ and AMD Duron™ System Bus Specification*, order# 21902.

**Scan Pins**

SCANSHIFTEN (Q5), SCANCLK1 (S1), SCANINTEVAL (S3), and SCANCLK2 (S5) are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.

**SMI# Pin**

SMI# is an input that causes the processor to enter the system management mode.

**STPCLK# Pin**

STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.

**SYSCLK and SYSCLK# Pins**

SYSCLK and SYSCLK# are differential input clock signals provided to the processor’s PLL from a system-clock generator. See “CLKIN, RSTCLK (SYSCLK) Pins” on page 60 for more information.

**SYSVREFMODE Pin**

SYSVREFMODE (AA5) is Low to ensure that the external VREFSYS voltage is the actual voltage used by the input buffers and that no scaling occurs internally between the

VREFSYS voltage and the input threshold. This pin is tied Low with a pulldown resistor.

**VCCA Pin**

VCCA is the processor PLL supply. For information about the VCCA pin, see Table 5, “VCCA AC and DC Characteristics,” on page 25 and the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

**VID[4:0] Pins**

The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC\_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor's package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC\_CORE DC/DC converter.

These voltage ID values are defined Table 20 on page 66.

**Table 20. VID[4:0] Code to Voltage Definition**

VID[4:0]	VCC_CORE (V)	VID[4:0]	VCC_CORE (V)
00000	1.850	10000	1.450
00001	1.825	10001	1.425
00010	1.800	10010	1.400
00011	1.775	10011	1.375
00100	1.750	10100	1.350
00101	1.725	10101	1.325
00110	1.700	10110	1.300
00111	1.675	10111	1.275
01000	1.650	11000	1.250
01001	1.625	11001	1.225
01010	1.600	11010	1.200
01011	1.575	11011	1.175
01100	1.550	11100	1.150
01101	1.525	11101	1.125
01110	1.500	11110	1.100
01111	1.475	11111	No CPU

For more information, see the “Required Circuits” chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

#### VREFSYS Pin

VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC\_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

#### ZN, VCC\_Z, ZP, and VSS\_Z Pins

ZN (AC5), VCC\_Z (AC7), ZP (AE5), and VSS\_Z(AE7) are the push-pull compensation circuit pins. VCC\_Z is tied to VCC\_CORE. VSS\_Z is tied to VSS.

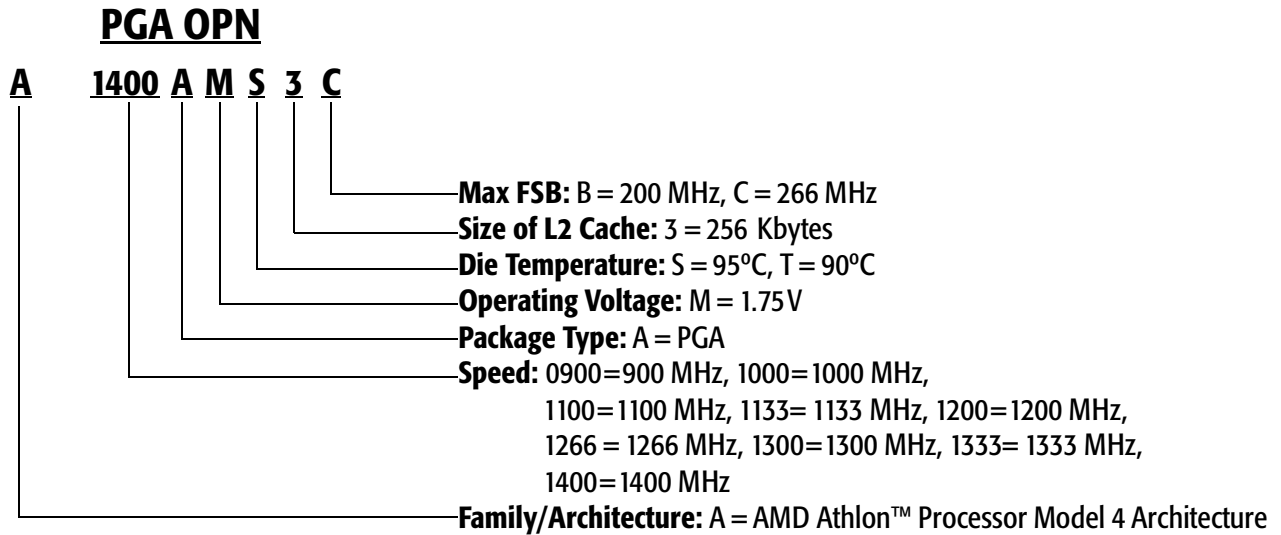
In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC\_CORE with a resistor that has a resistance matching the impedance  $Z_0$  of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance  $Z_0$  of the transmission line.



# 11 Ordering Information

## Standard AMD Athlon™ Processor Model 4 Products

AMD standard products are available in several operating ranges. The ordering part numbers (OPN) are formed by a combination of the elements, as shown in Figure 14.



**Note:** Spaces are added to the number shown above for viewing clarity only.

**Figure 14. PGA OPN Example for the AMD Athlon™ Processor Model 4**



# Appendix A

## Conventions and Abbreviations

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This section contains information about the conventions and abbreviations used in this document.

### Signals and Bits

- **Active-Low Signals**—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- **Signal Ranges**—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- **Reserved Bits and Signals**—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- **Three-State**—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.

- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

## Data Terminology

The following list defines data terminology:

- Quantities
  - ï A *word* is two bytes (16 bits)
  - ï A *doubleword* is four bytes (32 bits)
  - ï A *quadword* is eight bytes (64 bits)
- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - ï Kilo (K, as in 4-Kbyte page)
  - ï Mega (M, as in 4 Mbits/sec)
  - ï Giga (G, as in 4 Gbytes of memory space)See Table 21 on page 75 for more abbreviations.
- Little-Endian Convention—The byte with the address *xx...xx00* is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

## Abbreviations and Acronyms

Table 21 contains the definitions of abbreviations used in this document.

**Table 21. Abbreviations**

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
μ	Micro-
μA	Microampere
μF	Microfarad
μH	Microhenry
μs	Microsecond
μV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
p	pico-
pA	picoampere

**Table 21. Abbreviations (continued)**

Abbreviation	Meaning
pF	picofarad
pH	picoHenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 22 contains the definitions of acronyms used in this document.

**Table 22. Acronyms**

Abbreviation	Meaning
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
FIFO	First In, First Out
GART	Graphics Address Remapping Table
HSTL	High-Speed Transistor Logic
IDE	Integrated Device Electronics
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group

**Table 22. Acronyms (continued)**

<b>Abbreviation</b>	<b>Meaning</b>
LAN	Large Area Network
LRU	Least-Recently Used
LVTTL	Low Voltage Transistor Transistor Logic
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open-Drain
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
RAM	Random Access Memory
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMBus	System Management Bus
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
USB	Universal Serial Bus

**Table 22. Acronyms (continued)**

<b>Abbreviation</b>	<b>Meaning</b>
ZDB	Zero Delay Buffer