2.5 GBIT QUAD MUX WITH FAN OUT BUFFERS S3053

FEATURES

- Supports 2.5 Gbit/sec data rates
- Fully differential for minimum jitter accumulation
- TTL select
- High speed 50Ω source terminated outputs
- 0.84 W typical power dissipation
- 3.3 V power supply
- 52 Pin TQFP/TEP

GENERAL DESCRIPTION

The S3053 is a high performance quad mux with fan out buffers. It is designed to minimize jitter accumulation by providing a high bandwidth fully differential signal path. It can be used to switch OC-48 data signals in Dense Wavelength Division Multiplexer designs and other high speed serial switch designs.

The chip is designed using four 2:1 multiplexers. It can be used to fan out and/or multiplex high speed clock and data signals. The S3053 is compatible with the AMCC OC-48 clock recovery, MUX/DEMUX and Crosspoint Switch products. This allows signal integrity to be maintained throughout the system design.

The primary AC parameter of importance is the deterministic jitter or data eye degradation inserted by the crosspoint. The design minimizes jitter accumulation by using high bandwidth, low skew fully differential circuits. This provides for symmetric rise and fall delays as well as noise rejection.

Figure 1. S3053 Block Diagram

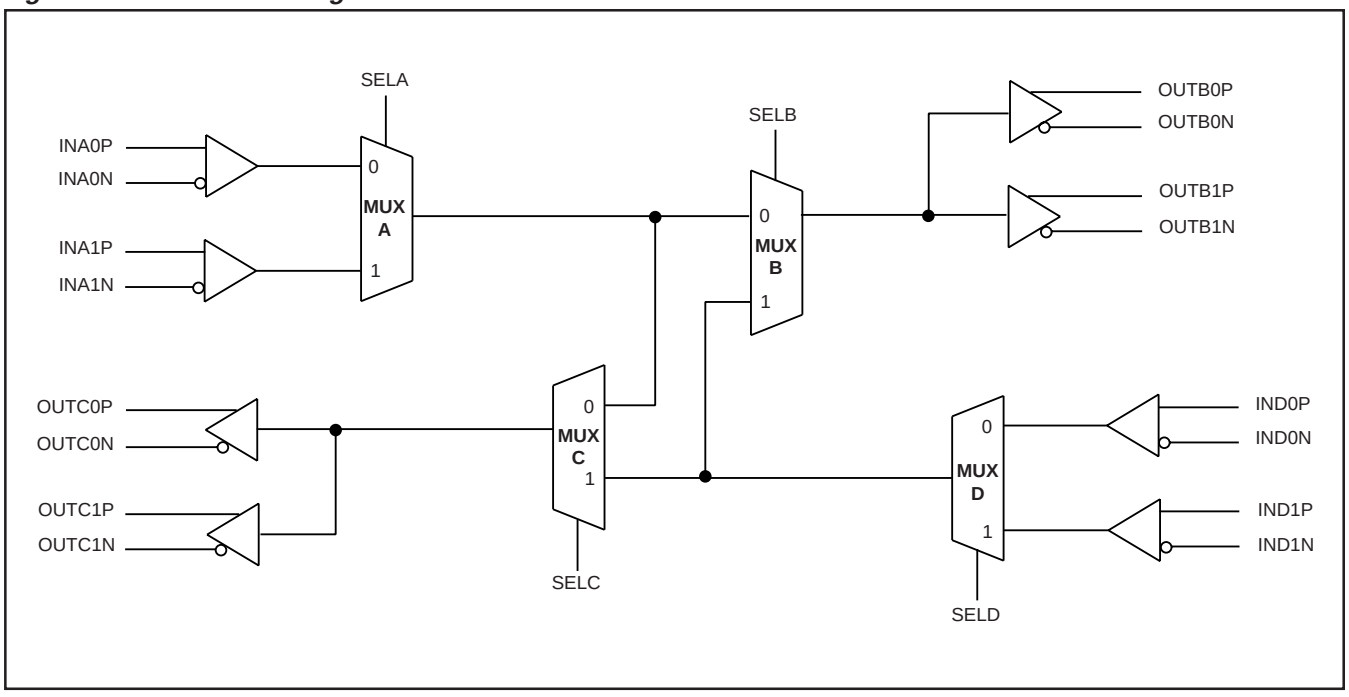


Table 1. Truth Table

SELA	SELB	SELC	SELD	OUTB	OUTC
0	0	0	0	INA0	INA0
0	0	0	1	INA0	INA0
0	0	1	0	INA0	IND0
0	0	1	1	INA0	IND1
0	1	0	0	IND0	INA0
0	1	0	1	IND1	INA0
0	1	1	0	IND0	IND0
0	1	1	1	IND1	IND1
1	0	0	0	INA1	INA1
1	0	0	1	INA1	INA1
1	0	1	0	INA1	IND0
1	0	1	1	INA1	IND1
1	1	0	0	IND0	INA1
1	1	0	1	IND1	INA1
1	1	1	0	IND0	IND0
1	1	1	1	IND1	IND1

Programable Swing Control

An external resistor can be connected across adjacent pins, VSWx to VEEx, where x is B0, B1, C0 and C1. This will result in a decreased Vswing for the specified output and a decrease in chip power dissipation. For example, if a 700 Ohm resistor is used, the Vswing will decrease from its full scale swing of approximately 570mV to 250mV and that specific output will draw approximately 13mA less. All four outputs can be independently set. If no external resistor is used, the output swing will default to its full scale value. See Figure 7.

The 700 Ohm value is only used as an example. The power concious user could use as small a resistor value as the application can handle.

Figure 2. Timing Waveforms

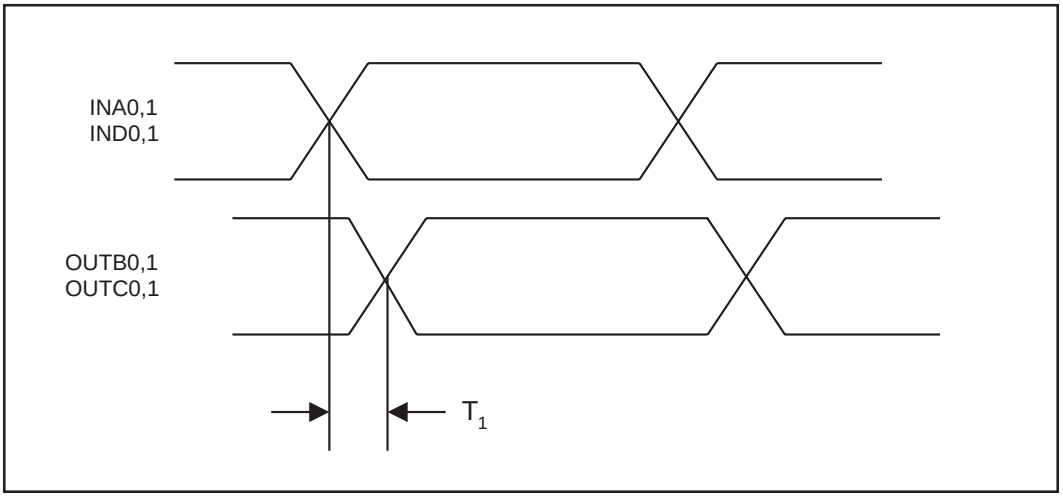


Figure 3. Differential Voltage

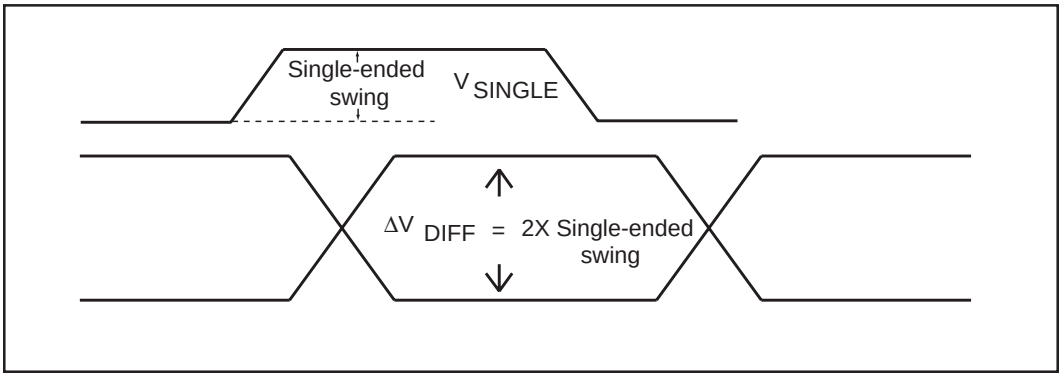


Table 2. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
INA0P INA0N INA1P INA1N	Int. Biased Diff. LVPECL	I	42 41 50 51	Differential inputs to the multiplexer.
IND0P IND0N IND1P IND1N	Int. Biased Diff. LVPECL	I	29 28 37 38	Differential inputs to the multiplexer.
SELA SELD	LVTTL	I	43 36	A Low selects IN0. When High, this signal selects IN1.
OUTB0P OUTB0N OUTB1P OUTB1N	Diff. CML	O	17 18 23 22	Serial output from Mux B.
OUTC0P OUTC0N OUTC1P OUTC1N	Diff. CML	O	4 5 10 9	Serial output from Mux C.
SELB SELC	LVTTL	I	49 30	A Low selects Mux A output. When High, this signal selects the Mux D output.
VCC			6, 8, 19, 20, 21, 32, 34, 45, 46, 47,	Power Supply. 3.3V nominal.
VSWB0 VSWB1 VSWC0 VSWC1	Analog	I	15 25 2 12	Voltage Swing Control pin.
VEE			1, 7, 13, 14, 26, 27, 31, 33, 35, 39, 40, 44, 48, 52,	Ground.
VEEB0 VEEB1 VEEC0 VEEC1	Output GND		16 24 3 11	Ground for B0, B1, C0, C1.

Figure 4. S3053 Pinout Package

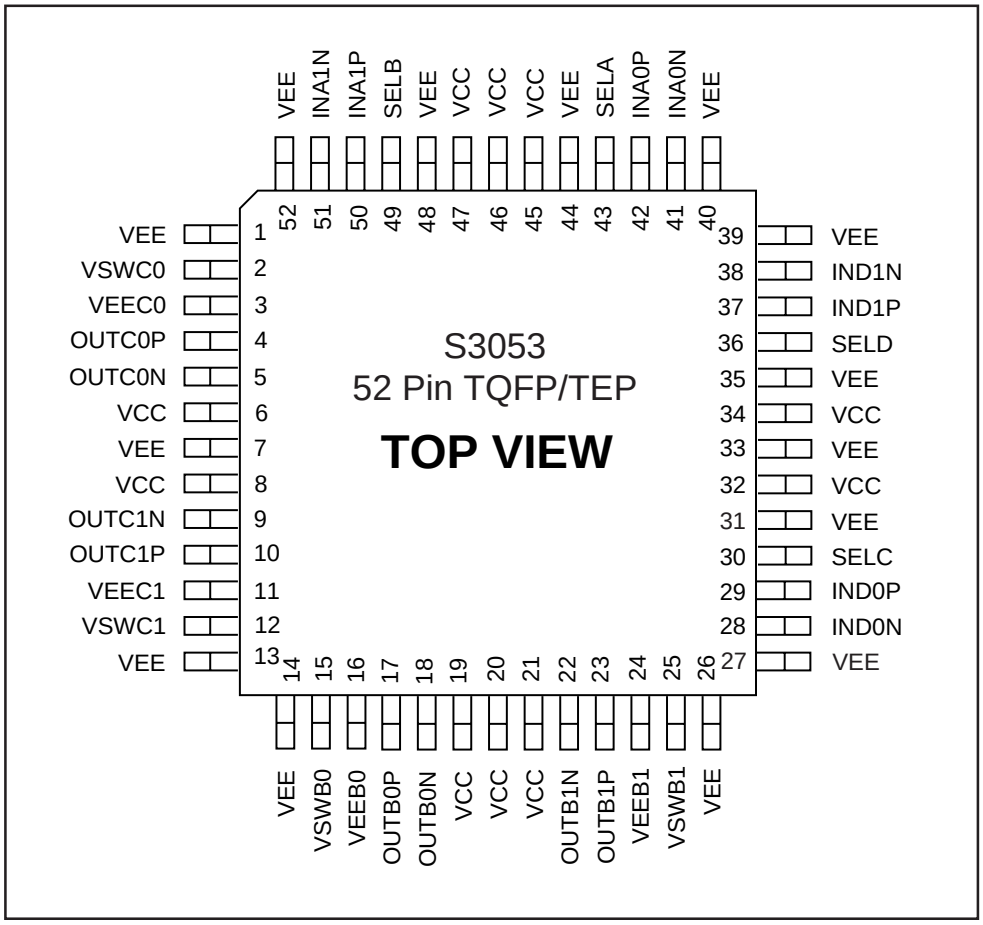
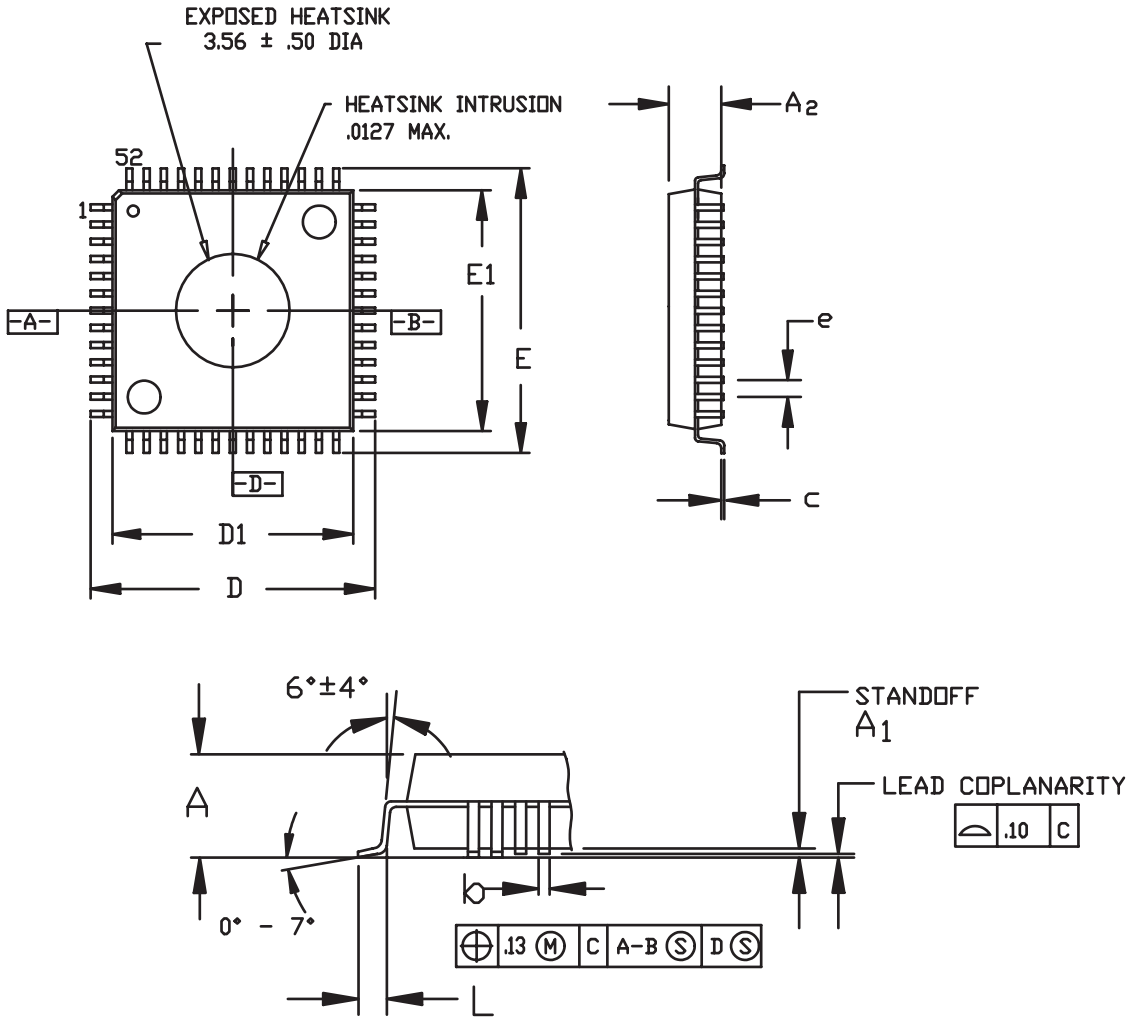


Figure 5. S3053 52 Pin TQFP/TEP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	11.75	9.90	11.75	9.90	0.50	0.65 BSC.	0.25	0.127
NOM			1.40	12.00	10.00	12.00	10.00	0.60		0.30	
MAX	1.60	0.15	1.45	12.25	10.10	12.25	10.10	0.75		0.35	0.17

Table 3. Thermal Management

Device	Power	Θja Still Air	Θjc Still Air
S3053	1.1W	42° C/W	2.2° C/W

Table 4. AC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units	Conditions
T_R	Serial Data rise time. (OUT0, OUT1).			175	ps	20% to 80% tested on a sample basis. (100Ω line-to-line.)
T_F	Serial Data fall time. (OUT0, OUT1).			150	ps	
T1	Flow through propagation delay IN to OUT.			2.0	ns	100Ω load line-to-line.
R_J	Random jitter		2	4	ps	
D_J	Deterministic jitter		20		ps	

Table 5. LVTTL Input DC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{IH(ITL)}$	Input HIGH voltage (SEL-TTL)	2.0		VCC	V	
$V_{IL(ITL)}$	Input LOW voltage (SEL-TTL)	0		0.8	V	
$I_{IH(ITL)}$	Input HIGH current (SEL-TTL)			50	µA	V_{IN} = 2.4V
$I_{IL(ITL)}$	Input LOW current (SEL-TTL)	-500		-50	µA	V_{IN} = 0.5V

Table 6. CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL}	CML Output LOW Voltage	Vcc -1.0		Vcc -0.55	V	100Ω line-to-line.
V_{OH}	CML Output HIGH Voltage	Vcc -0.35		Vcc -0.10	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	CML Serial Output Differential Voltage Swing	900		1460	mV	100Ω line-to-line. See Figure 3. Rext = open.
$\Delta V_{OUTSINGLE}$	CML Serial Output Single-ended Voltage Swing	450		730	mV	100Ω line-to-line. See Figure 3. Rext =ch open.

Table 7. Internally Biased LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Min. Differential Input Voltage Swing	300		1200	mV	See Figure 3.
$\Delta V_{INSINGLE}$	Min. Single-ended Input Voltage Swing	150		600	mV	See Figure 3.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 8. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	-0.5		+4	V
PECL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
TTL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
Case Temperature Under Bias (T_C)	-55		125	C°
Junction Temperature Under Bias	-55		150	C°
Storage Temperature (T_{STG})	-65		150	C°
Static Discharge Voltage		500		V

1. CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 9. Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		85	° C
Junction Temperature Under Bias	-40		+130	° C
Voltage on VCC with respect to GND	3.13	3.3	3.47	V
Voltage on any LVPECL Input Pin	Vcc -2		Vcc	V
ICC Supply Current		260	330	mA

1. AMCC guarantees the functional and parametric operation of the part under “Recommended Operating Conditions” (except where specifically noted in the AC and DC Parametric tables).

Input Structures

Two input structures exist in this part; TTL and High Speed, Differential Inputs. The LVTTL Inputs will interface with any LVTTL outputs. The High Speed, Differential Inputs can be AC Coupled. Therefore, the High Speed, differential Input buffers are biased at Vcc -0.5V. Refer to Figure 6 for High Speed Differential Input termination.

Figure 6. Input Termination

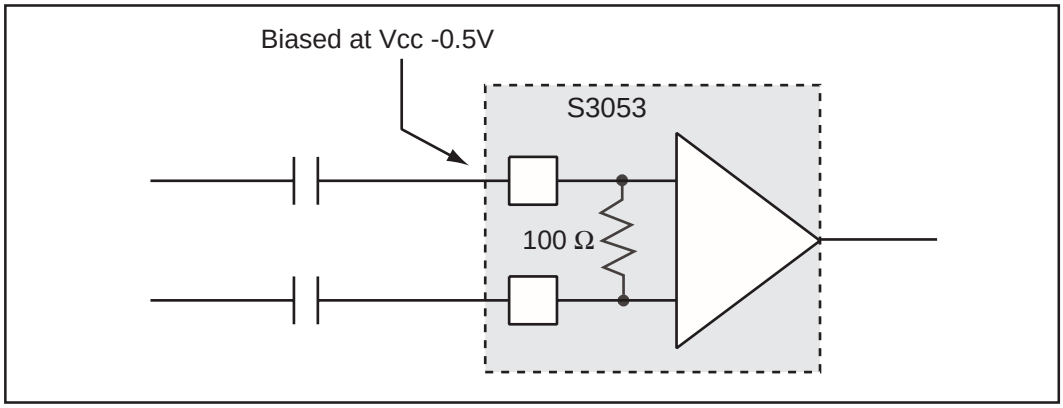
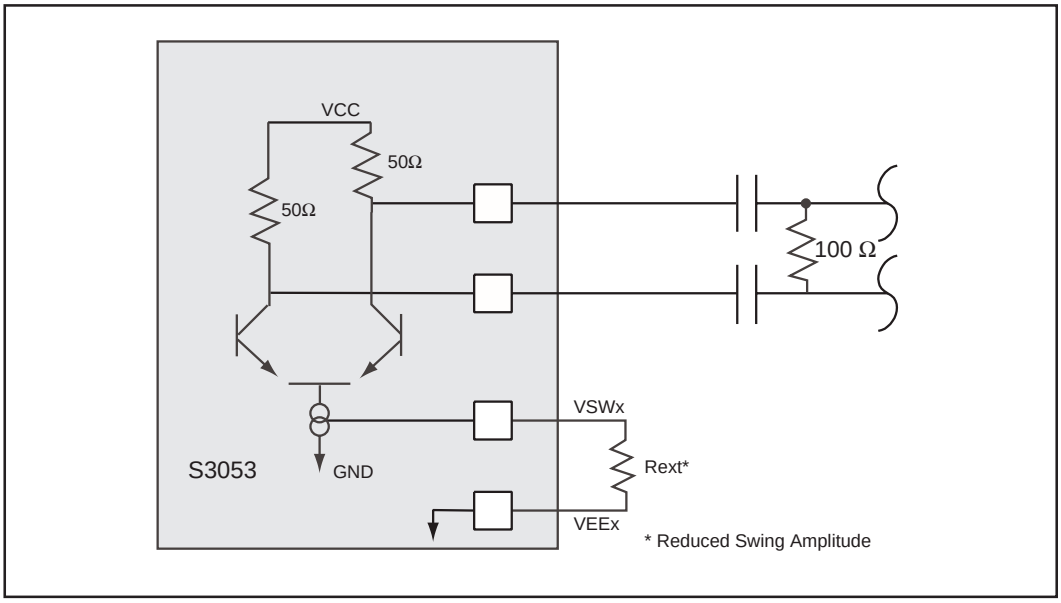
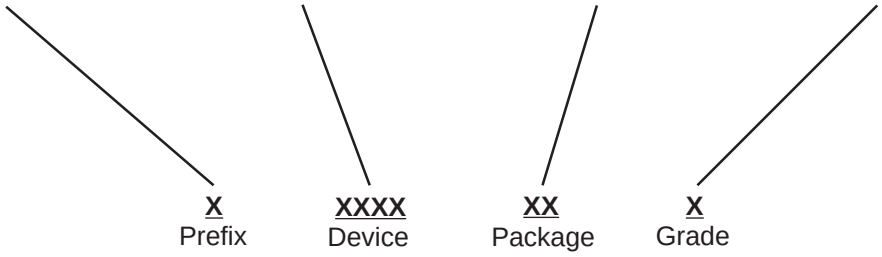


Figure 7. Output Termination



Ordering Information

PREFIX	DEVICE	PACKAGE	GRADE
S- Integrated Circuit	3053	TT – 52 TQFP/TEP	(blank) – Commercial I – Industrial



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