Stratix GX

FPGA Family

March 2003, ver. 1.2 Data Sheet

Introduction

Preliminary Information

The Stratix™ GX family of devices is Altera's second FPGA family to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock data recovery (CDR) technology and embedded SERDES capability at data rates of up to 3.125 gigabits per second (Gbps). These transceivers are grouped in integrated, four-channel blocks, and are designed for low power consumption and small die size. The Stratix GX FPGA technology is built upon the Stratix architecture, and offers a 1.5-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features...

- Transceiver block features
  - High-speed serial transceiver channels with CDR provides 622-megabits per second (Mbps) to 3.125-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 16, or 20 high-speed serial transceiver channels providing up to 62.5 Gbps of serial bandwidth (full-duplex)
  - Support for transceiver-based protocols, including 10 Gigabit Ethernet XAUI, SONET/SDH, 1 Gigabit Ethernet, PCI Express, SMPTE 292M, SFI-5, SPI-5, InfiniBand, Fibre Channel, and Serial RapidIO
  - Programmable differential output voltage (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Selectable on-chip termination resistors (50 Ω, 60 Ω, or 75 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, and 20-bit wide data transfer
  - 1.5-V pseudo current mode logic (PCML) for 622 Mbps to 3.125 Gbps (both AC and DC coupling)
  - Receiver indicator for loss of signal
  - Built-in self test (BIST)
  - Hot insertion/removal protection circuitry
  - Pattern detector and word aligner supports programmable patterns

- 8B/10B encoder/decoder performs 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
- Transceiver synchronizer buffer performs clock domain translation between the transceiver block and the logic array
- Receiver FIFO resynchronizes the received data with the local reference clock
- Rate matcher and channel aligner compliant with XAUI
- Device can bypass these transceiver block features if necessary

- FPGA features
  - 10,570 to 41,250 logic elements (LEs); see Table 1
  - Up to 3,423,744 RAM bits (427,968 bytes) available without reducing logic resources
  - TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 312 MHz
  - Up to 16 global clock networks with up to 22 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 250 MHz), multiply- accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 45 channels with up to 40 channels optimized for 1-Gbps performance
  - Support for source-synchronous bus standards, including 10-Gigabit Ethernet XSBI, Parallel RapidIO, UTOPIA IV, Network Packet Streaming Interface (NPSI), HyperTransport™ technology, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
  - Terminator™ technology provides on-chip termination for differential and single-ended I/O pins with impedance matching
  - Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
  - Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
  - Support for remote configuration updates

Table 1. Stratix GX Device Features

Feature	EP1SGX10C EP1SGX10D	EP1SGX25C EP1SGX25D EP1SGX25F	EP1SGX40D EP1SGX40G
LEs	10,570	25,660	41,250
Transceiver channels	4, 8	4, 8, 16	8, 20
Source-synchronous channels	22	39	45
M512 RAM blocks (32 × 18 bits)	94	224	384
M4K RAM blocks (128 × 36 bits)	60	138	183
M-RAM blocks (4K × 144 bits)	1	2	4
Total RAM bits	920,448	1,944,576	3,423,744
Digital signal processing (DSP) blocks	6	10	14
Embedded multipliers *(1)*	48	80	112
PLLs	4	4	8

Note to Table 1:

(1) This parameter lists the total number of 9 × 9-bit multipliers for each device. For the total number of 18 × 18-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 2. For the total number of 36 × 36-bit multipliers per device, decide the total number of 9 × 9-bit multipliers by 8.

Stratix GX devices are available in space-saving FineLine BGA® and ball-grid array (BGA) packages (see Tables 2 through 3). All Stratix GX devices support vertical migration within the same package (e.g., the designer can migrate between the EP1SGX10C and EP1SGX25C devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. The Quartus® II software can automatically cross reference and place all pins except LVDS pins for migration when given a device migration list. The designer must use the pin-outs for each device to verify the LVDS placement migration. A future version of the Quartus II software will support LVDS pin migration.

Table 2. Stratix GX Package Options & I/O Pin Counts Note (1)		
Device	**672-Pin FineLine BGA**	**1,020-Pin FineLine BGA**
EP1SGX10C	330	
EP1SGX10D	330	
EP1SGX25C	426	
EP1SGX25D	426	542
EP1SGX25F		542
EP1SGX40D		548
EP1SGX40G		548

Note to Table 2:

(1) The number of I/O pins listed for each package includes dedicated clock pins and dedicated fast I/O pins. However, these numbers do not include high-speed or clock reference pins for high-speed I/O standards.

Table 3. Stratix GX FineLine BGA Package Sizes		
Dimension	**672 Pin**	**1,020 Pin**
Pitch (mm)	1.00	1.00
Area (mm^2)	729	1,089
Length × width (mm × mm)	27 × 27	33 × 33

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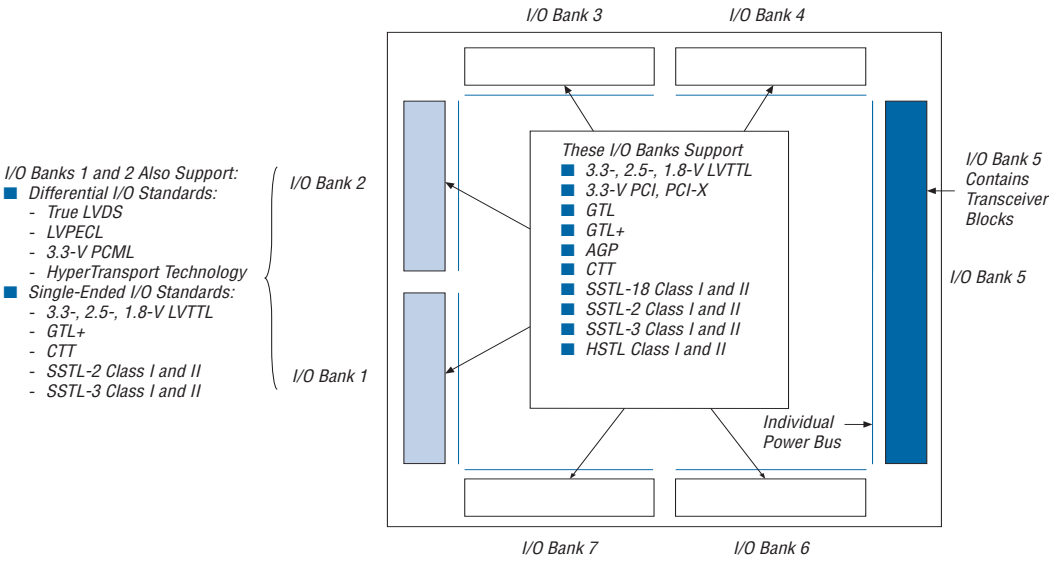
High-Speed I/O Interface Functional Description

The Stratix GX device family supports high-speed serial transceiver blocks with CDR circuitry as well as source-synchronous interfaces. The channels on the right side of the device use an embedded circuit dedicated for receiving and transmitting high-speed serial data streams to and from the system board. These channels are clustered in a four-channel serial transceiver building block and deliver high-speed bidirectional point-to-point data transmissions to provide up to 3.125 Gbps of full-duplex data transmission per channel. The channels on the left side of the device support source-synchronous data transfers at up to 1 Gbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards. Figure 1 shows the Stratix GX I/O blocks. The differential source-synchronous serial interface is described in "Dedicated Source-Synchronous Circuitry" on page 32 and the high-speed serial interface is described in "Transceiver Blocks" on page 8.

Figure 1. Stratix GX I/O Blocks



FPGA Functional Description

Stratix GX devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 LEs in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 312 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 312 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 300 MHz. Several M-RAM blocks are located individually or in pairs within the device's logic array.

DSP blocks can implement up to either eight full-precision 9×9-bit multipliers, four full-precision 18×18-bit multipliers, or one full-precision 36×36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix GX device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM, FCRAM, ZBT, and QDR SRAM devices.

The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 4 lists the resources available in Stratix GX devices.

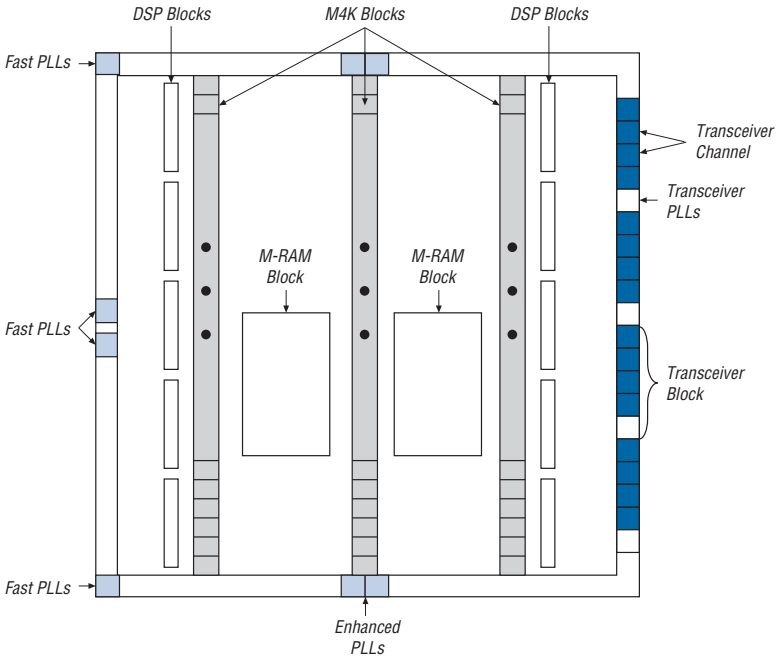
Table 4. Stratix GX Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1SGX10C	4 / 94	2 / 60	1	2 / 6	40	30
EP1SGX10D	4 / 94	2 / 60	1	2 / 6	40	30
EP1SGX25C	6 / 224	3 / 138	2	2 / 10	62	46
EP1SGX25D	6 / 224	3 / 138	2	2 / 10	62	46
EP1SGX25F	6 / 224	3 / 138	2	2 / 10	62	46
EP1SGX40D	8 / 384	3 / 183	4	2 / 14	77	61
EP1SGX40G	8 / 384	3 / 183	4	2 / 14	77	61

Transceiver Blocks

Stratix GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.125-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 12.5 Gbps (3.125 Gbps per channel) of data transition per transceiver block. Figure 2 shows the transceiver blocks within the Stratix GX device.

Figure 2. Placement of Stratix GX Transceiver Blocks



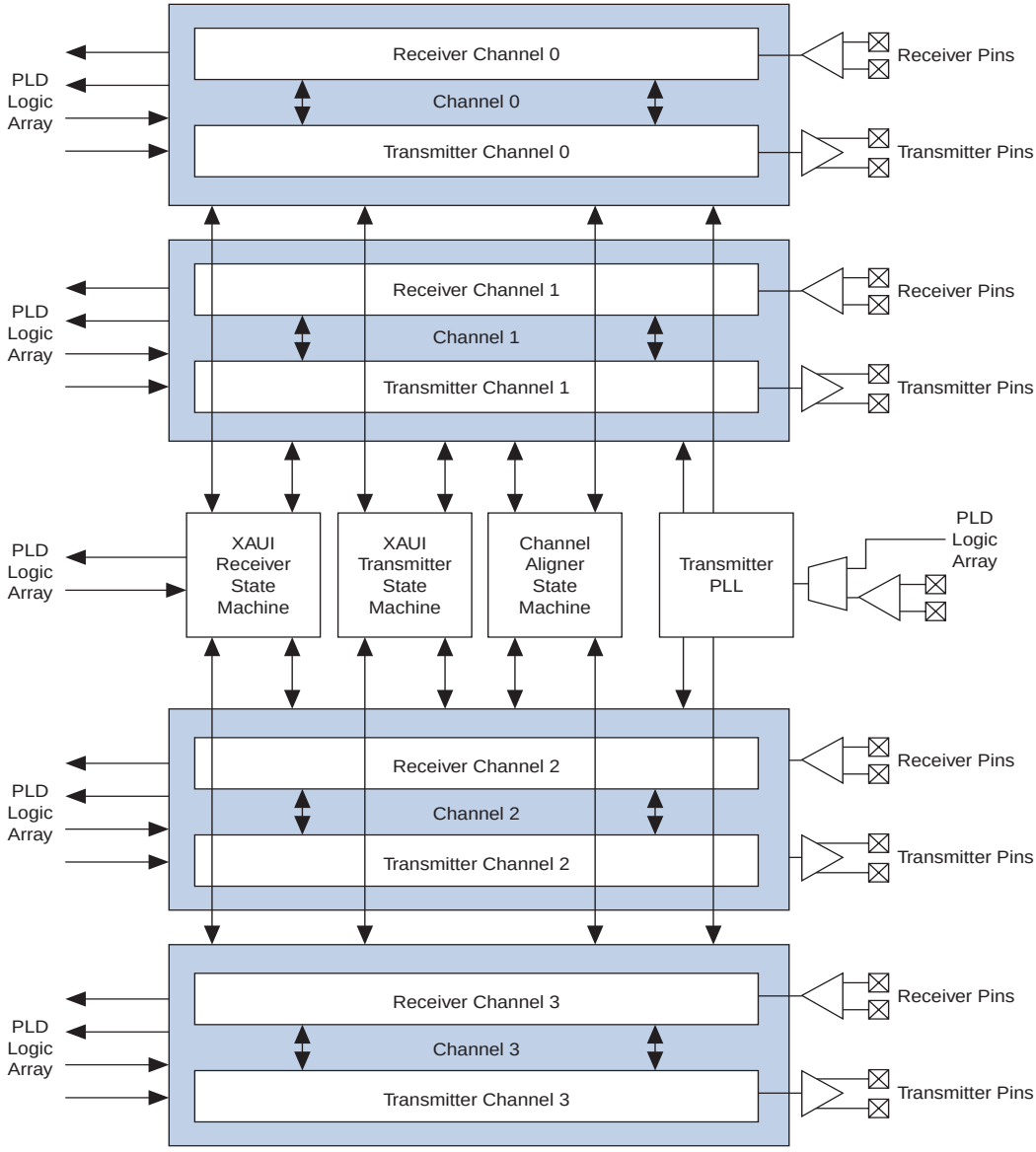
There are up to 20 transceiver channels available on a single Stratix GX device. Table 5 shows the number of transceiver channels available on each Stratix GX device.

Table 5. Stratix GX Transceiver Channels

Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 3 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching and channel alignment for XAUI applications.

Figure 3. Stratix GX Transceiver Block



The Stratix GX transceiver channels implement functionality associated with physical media attachment (PMA) and physical coding sublayer (PCS) protocol layers. The circuitry for programmable pre-emphasis, equalization, clock data recovery (CDR) as well as the serializer/deserializer (SERDES) and I/O buffers themselves address PMA functions. Pattern detection, word alignment, rate matching, channel alignment, 8B/10B encoding/decoding, and synchronization are implemented in circuitry that addresses the requirements of the PCS. The supporting logic within a transceiver block contains the transmitter and receiver PLL, the reset control, the XAUI receiver state machine, the XAUI transmitter state machine, and the XAUI deskew state machine.

Figure 4 shows a block diagram of the transceiver channel.

Figure 4. Transceiver Channel

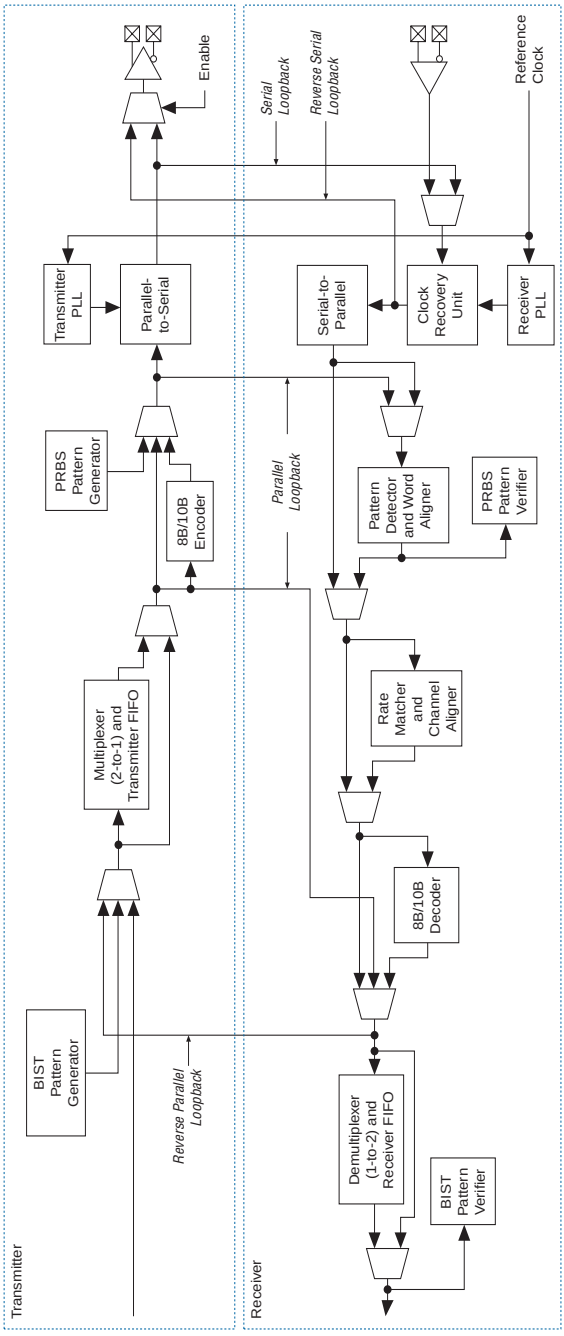


Table 6 describes the transceiver input ports.

Table 6. Stratix GX Input Ports (Part 1 of 2) *Note (1)*

Port Name	Description	Comments
inclk[]	Transmitter PLL and receiver PLL reference input clock.	Input port [NUMBER_OF_QUADS - 1..0] wide. If the transmitter PLL and receiver PLL are used, the inclk[] port is required. If the OPERATION_MODE parameter is set to TX or DUPLEX, the inclk[] port is required.
coreclk[]	Clock from the device's logic array.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. When the OPERATION_MODE is set to TX or DUPLEX, the coreclk port cannot be used.
pll_areset[]	Asynchronous clear for the transmitter and receiver PLLs.	Input port [NUMBER_OF_QUADS - 1..0] wide.
rx_in[]	Receiver channel data input port.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_cruclk[]	CRU reference input clock.	Input port [NUMBER_OF_QUADS - 1..0] wide.
rx_aclr[]	Asynchronous clear for the receiver channels.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The rx_aclr input port must connect to the rxdigitalreset input port of the receiver channel.
rx_bitslip[]	Bit slippage input. Enables bit slippage.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The rx_bitslip input port can be used only when the USE_AUTO_BIT_SLIP parameter is set to OFF.
rx_enacdet[]	Comma detection input. Enables comma detection.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The rx_enacdet input port can be used only when the USE_AUTO_BIT_SLIP parameter is set to OFF.
rx_we[]	Write enable input. Enables write operations from the rate matching FIFO.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_re[]	Read enable input. Enables read operations to the rate matching FIFO.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_slpbk[]	Serial loopback input. Enables serial loopback.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. If the rx_slpbk input port is connected, the OPERATION_MODE is set to DUPLEX and the serialfdbk port of the receiver channel must be connected.
rx_a1a2size[]	Comma detection input for A1A2 or A1A1A2A2 commas.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The rx_a1a2size port can be used only when the PROTOCOL parameter is set to SONET.
rx_equalizerctrl[]	Indicates whether to control the equalizer.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.

Table 6. Stratix GX Input Ports (Part 2 of 2) *Note (1)*

Port Name	Description	Comments
rx_locktorefclk[]	Control signal for the receiver PLL to lock the CRU.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_locktodata[]	Control signal for the receiver PLL to lock the received data.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The rx_locktodata port can overwrite the rx_locktorefclk port.
tx_in[]	Transmitter channel data input port.	Input port [CHANNEL_WIDTH * NUMBER_OF_CHANNELS - 1..0] wide. If the USE_8B_10B_MODE parameter is set to OFF and the USE_DOUBLE_DATA_MODE parameter is set to ON, the DESERIALIZATION_FACTOR parameter value is CHANNEL_WIDTH. If the USE_8B_10B_MODE parameter is set to OFF and the USE_DOUBLE_DATA_MODE parameter is set to OFF, the DESERIALIZATION_FACTOR parameter value is CHANNEL_WIDTH / 2. If the USE_8B_10B_MODE parameter is set to ON, the DESERIALIZATION_FACTOR parameter value is 10.
tx_aclr[]	Asynchronous clear for the transmitter channels.	Input port [NUMBER_OF_CHANNELS - 1..0] wide. The tx_aclr input port must connect to the txdigitalreset input port of the transmitter channel.
tx_ctrlenable[]	Control character enable. Enables 8B/10B encoder to identify control characters.	Input port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If tx_ctrlenable output port is high, the data being sent is a control character and not data.
tx_forcedisparity[]	Disparity enable. Enables 8B/10B encoder to identify disparity.	Input port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If tx_forcedisparity input port is high, positive disparity (more 1s than 0s) is used.
tx_srlpbk[]	Serial loopback input. Enables serial loopback.	Input port [NUMBER_OF_CHANNELS - 1..0] wide.
tx_vodctrl[]		Input port [NUMBER_OF_CHANNELS - 1..0] wide.
tx_preemphasisctrl[]		Input port [NUMBER_OF_CHANNELS - 1..0] wide.
txdigitalreset[]		Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.
rxdigitalreset[]		Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.
rxanalogreset[]		Input port [NUMBER_OF_QUADS * 4 - 1..0] wide.
pllenable[]		Input port [NUMBER_OF_QUADS - 1..0] wide.

Note to Table 6:

(1) For the most up-to-date Stratix GX input port descriptions, see the altgxb megafunction in the Quartus II software.

Table 7 describes the transceiver output ports.

Table 7. Stratix GX Output Ports (Part 1 of 2) *Note (1)*

Port Name	Description	Comments
pll_locked[]	Gives the status of the transmitter PLL and receiver PLL.	Output port [NUMBER_OF_QUADS - 1..0] wide. The pll_locked port is available only when the transceiver PLL is used.
coreclk_out[]	Output clock feed from the clk2 port of the transmitter PLL or receiver PLL.	Output port [NUMBER_OF_QUADS - 1..0] wide. If a transmitter PLL and receiver PLL are used, the coreclk_out output port is used.
rx_channelaligned[]	Channel alignment for the transmitter PLL or receiver PLL.	Output port [NUMBER_OF_QUADS - 1..0] wide. When the PROTOCOL parameter is “XAUI”, the rx_channelaligned port must be connected.
rx_out[]	Deserialized data signal.	Output port [CHANNEL_WIDTH * NUMBER_OF_CHANNELS - 1..0] wide. If the USE_8B_10B_MODE parameter is set to OFF and USE_DOUBLE_DATA_MODE is set to ON, the DESERIALIZATION_FACTOR parameter value is CHANNEL_WIDTH. If the USE_8B_10B_MODE parameter is set to OFF and USE_DOUBLE_DATA_MODE is set to OFF, the DESERIALIZATION_FACTOR parameter value is CHANNEL_WIDTH / 2. If the USE_8B_10B_MODE parameter is set to OFF, the DESERIALIZATION_FACTOR parameter value is 10.
rx_clkout[]	Internal reference clock.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_locked[]	Gives the status of the receiver channel.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_freqlocked[]	Indicates whether receiver channel has locked to the receiver PLL frequency but not to the rx_in port.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_rlv[]	Indicates whether the receiver channel has violated the value specified for the RUN_LENGTH parameter.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_syncstatus[]	Gives the status of the pattern detector and word aligner.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
rx_patterndetect[]	Indicates whether the pattern detector detects a comma.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
rx_ctrldetect[]	Indicates whether the 8B/10B decoder detects a control code.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If the USE_8B_10B_MODE parameter is specified to "OFF", the rx_ctrldetect port is not available.

Table 7. Stratix GX Output Ports (Part 2 of 2) *Note (1)*

Port Name	Description	Comments
rx_errdetect[]	Indicates whether the 8B/10B decoder detects a code error.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide. If the USE_8B_10B_MODE parameter is specified to "OFF", the rx_errdetect port is not available.
rx_disperr[]	Indicates whether the 8B/10B decoder detects a disparity error.	Output port [NUMBER_OF_CHANNELS * DWIDTH_FACTOR - 1..0] wide.
rx_signaldetect[]	Indicates whether there is a legal voltage level on the input buffer.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_fifoempty[]	Indicates when the rate matching FIFO is less than 4 bytes of data.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_fifofull[]	Indicates when the rate matching FIFO is equal to 13 bytes of data.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_fifoalmostempty[]	Indicates when the rate matching FIFO is less than 7 bytes of data.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_fifoalmostfull[]	Indicates when the rate matching FIFO is greater than 9 bytes of data.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_bisterr[]		Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_bistdone[]		Output port [NUMBER_OF_CHANNELS - 1..0] wide.
rx_a1a2sizeout[]		Output port [NUMBER_OF_CHANNELS - 1..0] wide.
tx_out[]	Serialized transmitter channel data signal.	Output port [NUMBER_OF_CHANNELS - 1..0] wide.

Note to Table 7:

(1) For the most up-to-date Stratix GX output port descriptions, see the altgxb megafunction in the Quartus II software.

Table 8 describes the Stratix GX I/O parameters.

Table 8. Stratix GX I/O Parameters (Part 1 of 2) *Note (1)*

Parameter	Comments
OPERATION_MODE	Specifies the operation of the transmitter PLL and receiver PLL. Values are “RX”, “TX”, and “DUPLEX”.
LOOPBACK_MODE	Specifies the operation of the loopback. Values are “NONE”, “SLB”, “PLB”, and “P8LB”.
REVERSE_LOOPBACK_MODE	Specifies the operation of the reverse loopback. Values are “NONE”, “RSLB”, and “RPLB”.
PROTOCOL	Specifies the protocol. Values are “XAUI”, “GIGE”, “RAPIDIO”, “FIBRECHANNEL”, and “CUSTOM”.
NUMBER_OF_CHANNELS	Specifies the number of receiver channels.
NUMBER_OF_QUADS	Specifies the number of transceivers.
CHANNEL_WIDTH	Specifies the width of the receiver channel. Values are 8, 10, 16, and 20.
PLL_INCLOCK_PERIOD	Specifies the period or frequency of the transmitter PLL and receiver PLL. When the PLL_INCLOCK_PERIOD parameter is specified, the CRU_INCLOCK_PERIOD parameter cannot be used.
DATA_RATE	Specifies the rate of data from the transmitter channel.
DATA_RATE_REMAINDER	
USE_8B_10B_MODE	Specifies whether to use the 8B/10B decoder.
USE_DOUBLE_DATA_MODE	Specifies whether to use double data mode. If the USE_DOUBLE_DATA_MODE parameter is specified to ON, the CHANNEL_WIDTH parameter value is 16 or 20. When the CHANNEL_WIDTH parameter value is 8 or 16, the receiver channel is not in double data mode.
DWIDTH_FACTOR	Specifies the width of the double data factor.
DISPARITY_MODE	Specifies whether to use disparity mode.
CRU_INCLOCK_PERIOD	Specifies the period or frequency of the CRU. When the CRU_INCLOCK_PERIOD is specified, the PLL_INCLOCK_PERIOD parameter cannot be used.
RUN_LENGTH	Specifies the maximum run length allowed for the incoming data signal.
RUN_LENGTH_ENABLE	Specifies whether to use the run length detection.
USE_CHANNEL_ALIGN	Specifies whether to use the channel aligner. The USE_CHANNEL_ALIGN parameter can only be used when the PROTOCOL parameter is specified to XAUI.
USE_AUTO_BIT_SLIP	Specifies whether to use auto bit slippage.
USE_RATE_MATCH_FIFO	Specifies whether to use rate matching FIFO.
USE_SYMBOL_ALIGN	Specifies whether to use the word aligner.
ALIGN_PATTERN	Specifies the value used by the comma detector for the USE_SYMBOL_ALIGN parameter. If the USE_SYMBOL_ALIGN parameter is specified to OFF, this value is not used.

Table 8. Stratix GX I/O Parameters (Part 2 of 2) *Note (1)*

Parameter	Comments
ALIGN_PATTERN_LENGTH	Specifies the length of the ALIGN_PATTERN parameter. Values are “7”, “10”, or “16”.
INFINIBAND_INVALID_CODE	Specifies the codes that are illegal for the Infiniband protocol. Values are “0”, “1”, “2”, or “3”.
CLK_OUT_MODE_REFERENCE	Specifies whether to use the clock that operates the post rate matching FIFO buffer of the receiver channel.
USE_FIFO_MODE	Specifies whether to use FIFO mode.
SELF_TEST_MODE	
USE_EQUALIZER_CTRL_SIGNAL	
EQUALIZER_CTRL_SETTING	
SIGNAL_LOSS_THRESHOLD_SELECT	
RX_BANDWIDTH_TYPE	
RX_ENABLE_DC_COUPLING	
FORCE_DISPARITY_MODE	Specifies whether to use force disparity mode.
USE_VOD_CTRL_SIGNAL	
VOD_CTRL_SETTING	
USE_PREEMPHASIS_CTRL_SIGNAL	
PREEMPHASIS_CTRL_SETTING	
RX_USED	
TX_USED	
USE_CONTINUOUS_CALIBRATION_MODE	
RX_PPM_SETTING	

Note to Table 8:

(1) For the most up-to-date Stratix GX I/O parameter descriptions, see the `altgxb` megafunction in the Quartus II software.

Interface Protocols

Each transceiver block is designed to operate at any serial bit rate from 622 Mbps to 3.125 Gbps per channel.

The transceiver circuitry supports the following interface protocols:

- 10 Gigabit Ethernet XAUI
- Serial RapidIO
- 1 Gigabit Ethernet
- InfiniBand
- Fibre Channel
- PCI Express
- SMPTE 292M
- SPI-5
- SFI-5
- Custom applications

Stratix GX devices are ideal for many high-speed communication applications such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications standards support. Table 9 lists the embedded circuitry in the Stratix GX transceiver channel used for some of the Stratix GX interface protocols.

Table 9. Dedicated Circuitry for Stratix GX Device Protocols

Transceiver Elements	Supported Interface Protocols				
	10 Gigabit Ethernet XAUI	1 Gigabit Ethernet	Serial RapidIO	Fibre Channel	InfiniBand
CDR	✓	✓	✓	✓	✓
SERDES	✓	✓	✓	✓	✓
Pattern detector	✓	✓	✓	✓	✓
Word aligner	✓	✓	✓	✓	✓
8B/10B encoder/decoder	✓	✓	✓	✓	✓
Channel aligner	✓				
Rate matcher	✓	✓			
Synchronizer	✓	✓	✓	✓	✓
Word aligner state machine *(1)*	✓	✓			
Transmitter state machine	✓				
Receiver state machine	✓				
Channel aligner state machine	✓				
Rate matcher state machine	✓	✓			

Note to Table 9:

(1) For the InfiniBand and Serial RapidIO interface protocols, the word aligner state machine is implemented in the logic array.

For information on electrical specifications, see "Electrical Specifications" on page 159.

Transmitter

The transmitter consists of the I/O buffer, the multiplexer, and the synchronizer blocks. All four transmitters can operate synchronously to the transmitter reference clock (REFCLK0) or synchronously to the channel 0 transmitter clock (TXCLK0), which serves as the master clock.

Transmitter Synchronizer

The transmitter synchronizer converts the data sent from the logic array to the clock domain of the transmitter channel. The designer must send all data and control signals through this synchronizer. The device logic array must match a multiple of the fast clock generated from the transmitter PLL.

Transmitter Multiplexer

The multiplexer takes a 16- or 20-bit input and converts it to two 8- or 10-bit outputs, respectively. The PLL reference clock clocks the multiplexer if the FIFO buffer is enabled. If the design bypasses the FIFO buffer, the clock from the device logic array clocks the multiplexer. If the design does not double the width of the bus, it bypasses the multiplexer.

Transmitter 8B/10B Encoder

The Stratix GX transmitter contains an embedded 8B/10B encoder to automatically implement this function. This encoding scheme ensures a high transition density, which enables the receiving device to acquire and maintain lock. The 8B/10B encoding scheme also maintains the signal DC balance by keeping the number of 1's and 0's the same, which allows for AC-coupled data transmission. The 8B/10B encoding scheme provides an excellent transition density for clock recovery and improves error checking. The 8B/10B encoder converts 8-bit-wide data to a 10-bit-wide encoded data character. The encoder may be bypassed.

Transmitter PLL

The transmitter PLL provides the following outputs:

- The transmitter high-speed serial clock
- The receiver low-speed reference clock
- The transmitter and receiver low-speed parallel clocks
- A low-speed clock for FPGA operation, which can be further divided by 2

The transmitter PLL has a four-to-one multiplexer to select the reference clock source. The multiplexer outputs one of the following four inputs:

- Global clock
- I/O bus
- Generic routing
- Local reference clock

Table 10 shows reference clock and multiplication settings for common Stratix GX device protocols.

Table 10. Reference Clock & Multiplier Settings for Applicable Standards

CDR Applications	Data Rate (Gbps)	Frequency Multiplication (W)		Reference Clock Frequency (MHz)		Maximum Run Length
		Min	Max	Min	Max	
10 Gigabit Ethernet XAUI	3.125	10	20	156.25	625.00	10
RapidIO	1.0625 to 2.125	4	20	125.00	625.00	10
1 Gigabit Ethernet	1.25	4	10	125.00	312.50	10
InfiniBand	2.5	4	20	125.00	625.00	10
Fibre Channel	2.5	4	8	150.00	300.00	10
Custom applications	0.622 to 3.125	4, 8, 10, 16, 20		62.50	625.00	80

Transmitter Serializer

The serializer can support 8- or 10-bit-wide words. When used with the transmitter multiplexer, the transmitter serializer can support either 8-, 10-, 16-, or 20-bit words within Stratix GX transceiver blocks. The serializer converts incoming parallel data from the 8B/10B encoder or device logic array to serial data. Serialization factors and transmitter serializer information is available in *AN 237: Using High-Speed Transceiver Blocks in Stratix GX Devices*.

Programmable V_{OD} in Transmitter

The designer can program the output buffer V_{OD} to drive either short or long distances through connectors and cable.

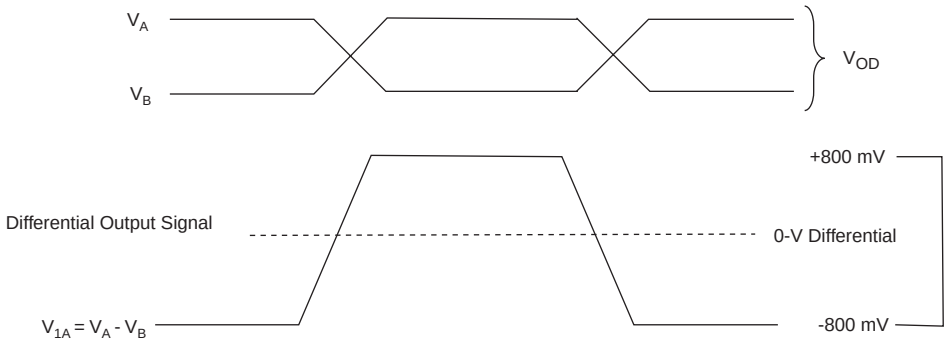
The designer programs V_{OD} between 200 to 800 mV by setting the current level, as shown in Figure 5. See Table 11. The V_{OD} is reduced depending on the transmission medium's attenuation to reduce power dissipation.

Table 11. Programmable V_{OD}

Current Level (mA)	V_{OD}		
	50 Ω (mV)	60 Ω (mV)	70 Ω (mV)
4	200	240	300
8	400	480	600
10	500	600	750
12	600	720	
14	700		
16	800		

Figure 5 shows the V_{OD} signal levels.

Figure 5. VOD Signal Levels



Pre-emphasis

A programmable pre-emphasis circuit boosts the high frequencies in the transmit data signal which may be lost in the transmission media. This maximizes the data eye opening at the far-end receiver. Pre-emphasis is particularly useful when transmitting data over backplanes or low-quality coaxial cables. The designer can use the V_{OD} setting to change the pre-emphasis, as shown in Table 12.

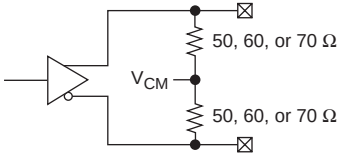
Table 12. Programmable Pre-Emphasis

V_{OD}	Pre-emphasis Setting				
	5%	10%	15%	20%	25%
200	210	220	230	240	250
240	252	264	276	288	300
300	315	330	345	360	375
400	420	440	460	480	500
480	504	528	552	576	600
500	525	550	575	600	625
600	630	660	690	720	750
700	735	770	-	-	-
720	756	792	-	-	-
750	787.5	-	-	-	-
800	-	-	-	-	-

Transmitter Termination

The transmitter's 1.5-V PCML output buffer is terminated on-chip to reduce the number of discrete components required on the board. The designer can set the termination resistor to 50, 60,or 70 Ω (see Figure 6).

Figure 6. Stratix GX 1.5-V PCML Buffer



PRBS Generator & BIST

In addition to the regular functional blocks, each transceiver channel has a built-in pseudo-random bit stream (PRBS) generator and a built-in PRBS verifier for a built-in self test (BIST) function. The designer can use the BIST function to verify that the system is operating properly. Both the PRBS generator and verifier work with an 8- or 10-bit data pattern. The pattern generator can generate a $2^{10} - 1$ or $2^{8} - 1$ PRBS. The designer can use these functions with either local loopback, which does not drive off the device, or line loopback, which does drive off the device.

The BISTEN pin enables the self-test function. The PRBS generator feeds into the 10-bit parallel-to-serial conversion when in BIST mode. The transceiver channel will ignore the data on the incoming data bus. The PRBS data is fed through the transmit circuitry and either sent out to the PCB or looped back to the receiver. The output can be sent to a bit error rate tester (BERT), the receiver of another Stratix GX channel, or looped back to the receive input of the same channel. Since the PRBS is not random but a predetermined sequence of 1's and 0's, a BERT can capture and check the data for errors. The test result is reported on the BISTERR pin.

Receiver

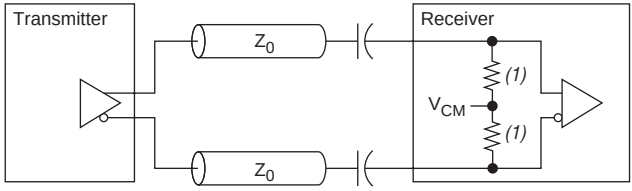
For each channel, the receiver input pins (rxip and rxin) receive serial data. The clock recovery unit locks on to the data stream and generates a recovered clock that is aligned in frequency and phase with the data. The serial data is then clocked into the deserializer. The receiver consists of the I/O buffer CRU, deserializer, pattern detector, word aligner, channel aligner, rate matcher, 8B/10B decoder, and synchronizer.

Receiver Termination

The receiver provides a programmable on-chip termination circuit, eliminating the need for external termination. The receiver includes programmable on-chip termination circuitry for 50- (default), 60-, or 70-Ω impedance.

The transceiver block supports an AC-coupled topology as shown in Figure 7.

Figure 7. Differential 1.5-V PCML Output to Input



Note to Figure 7:
(1) These resistors are either 50, 60, or 70 Ω.

Receiver Equalizer

Protocols minimize the effect of cross talk and other interference between channels. However, it is important to compensate for the protocol inter-symbol interference (ISI) that distorts the signal in order to extend the length of a transmission medium. Each receiver incorporates a programmable equalizer to reduce ISI distortion. This adaptive equalizer automatically compensates for ISI dielectric and skin losses.

Receiver CRU

The CRU is located in the receiver and uses the reference clock and the serial data input at the receiver to generate a high-speed clock based on the transitions inside the data. The high-speed clock is fed to the serial side of the SERDES. The receiver then uses the recovered clock throughout the remaining blocks, and can feed it to the logic array for use in other logic.

The programmable run length violation (RLV) detection circuit monitors the changes in the data used to generate the clock. The RLV detection circuit in the CDR block detects and reports when the data in the bit stream exceeds a preset maximum number of consecutive 1's or 0's. The designer sets this maximum during configuration, and if the data exceeds this maximum, the RLV detection circuit returns an error signal. Table 13 shows the CDR specifications.

Table 13. CDR Specifications

Parameter	Minimum	Maximum
Reference frequency input	62.5 MHz	650 MHz
Serial input data rate	622 Mbps	3.125 Gbps
Run length tolerance	80 UI	-
Frequency offset tolerance (refclk)	– 100 PPM	100 PPM
Bit error rate	-	10^{-12}
Lock time (frequency)	-	10 ms
Lock time (data)	-	0.05 ms

Receiver Deserializer

The deserializer can support 8- or 10-bit wide words. It converts incoming high-speed serial data streams to either 8- or 10-bit-wide parallel data with the recovered clock for synchronization to the logic array.

Receiver Word Alignment

The receiver aligns the bits in the parallel data arriving from the SERDES into a new set of parallel bits. To do this, the receiver includes three blocks for word alignment. These two elements work both in conjunction and independently of each other, as described in this section.

Receiver Pattern Detector

The main function of the word aligner is to synchronize the word clock with the data steam word boundary by detecting and aligning a programmable synchronization pattern. This unique pattern of `1`'s and `0`'s either cannot occur as part of valid data or is a pattern that repeats at defined intervals. Stratix GX devices provide a programmable 16-bit register for detecting patterns. The designer can configure this 16-bit register to detect several pattern lengths: 10-bits, 8-bits, and 7-bits. Patterns associated with 8B/10B-based protocols are often known as commas. Table 14 shows the applications and the associated patterns that Stratix GX devices support. The pattern detector can be bypassed.

Table 14. Application & Pattern Support

Applications	Pattern	Bit Length	Bit Pattern
Fibre Channel, Serial RapidIO, XAUI, InfiniBand, Gigabit Ethernet	/K28.5/ or / K28.1/ or / K28.7 /	7 or 10	b'0011111XXX or b'1100000XXX
A1, A2 Detect	A1 Followed by A2	8	b'11110110 followed by b'00101000
A1A1, A2A2 Detect	A1, followed by A1, followed by A2, followed by A2	8	b'11110110 followed by b'11110110 followed by b'00101001 followed by b'00101001
Custom	Any	16	Any

Data Realigner

The data realigner determines the word boundaries in either an automatic mode or manual mode. In automatic mode (for Gigabit Ethernet or XAUI), the internal logic locates the pattern in the incoming data, determines the word boundary, and may change the word boundary. The output of the word aligner is coordinated using a selection register that is controlled by the XAUI state machine. This state machine uses the pattern detect signal from the pattern detector and a known protocol to update the register that controls the data realignment.

When the data realigner operates in manual mode, the selection register that coordinates the word aligner is updated using the logic array's `realign` port.

Table 15 shows the data realigner modes:

Table 15. Data Realignment Modes

Data Realignment Mode	Effective Mode
Automatic data realignment	Gigabit Ethernet or XAUI
Manual data realignment	Manual data realignment and manual synchronization
Automatic data realignment	Automatic data realignment with synchronization in the logic array

Channel Aligner

The channel aligner consists of a channel alignment symbol detector and a channel aligner FIFO buffer. The system uses a common state machine to synchronize all the channels to the recovered clock. The channel aligner system is active when the transceiver channel is operating in XAUI mode.

Each receiver has its own CDR block. The channel aligner synchronizes the data to the clock edge of the recovered clock of channel 0.

Rate Matcher

The Stratix GX transceiver blocks use rate matchers to adjust for ±100 PPM clock fluctuation. The receiver performs rate matching following the channel alignment. The rate matching circuit contains a basic FIFO buffer which operates in either rate matching mode or generic FIFO buffer mode. The rate matcher is a Gigabit Ethernet- or XAUI-specific protocol for reading and writing from the FIFO buffer while the generic FIFO controls reading and writing with a write-enable or read-enable signal specified from the logic array.

Receiver 8B/10B Decoder

The 8B/10B decoder decodes a 10-bit parallel input stream into 8-bit data. The 8B/10B decoder can receive data encoded by a standard 8B/10B encoder. The 8B/10B decoder also detects invalid code groups and running disparity errors. The designer can modify the invalid code group mechanism to accommodate the different reserved or unsupported code for different protocols. This operation is controlled by `INVALID_CODE [1..0]` pins. Table 16 shows the `INVALID_CODE` pin setting and the invalid codes that the decoder detects. When the decoder detects a disparity error, it generates a disparity error signal synchronized with data. The combination of encoding and decoding allows for the transmission of special characters and allows for error detection. The 8B/10B system can operate in two modes: standard mode or XAUI mode.

Table 16. INVALID_CODE Pin Setting

Pin Setting	Invalid Codes
01	K28.1, K28.3, K28.4, K28.7
10	K28.6

Receiver Demultiplexer & Synchronizer

The byte demultiplexer converts high-speed serial data to either 8- or 10-bit wide parallel data. This synchronized data is sent with the clock to the device logic array. This data can also be deserialized and sent at half the rate but with double the amount of bits in parallel. The synchronizer compensates for the phase disparity between the logic array clock and the recovered clock.

Operation Modes

The following sections describe the general operations of a Stratix GX transceiver block.

Loopback Modes

The Stratix GX device provides several loopback modes for effectively debugging a high-speed system. These loopback modes allow each channel to operate as a full-duplex channel or to loop back within the transceiver block. Loopback occurs when the transmitter feeds data directly to the receiver. Reverse loopback occurs when the receiver feeds data directly to the transmitter.

In serial loopback mode, the channel's transmit differential serial output is looped back to the channel's clock recovery unit. In reverse serial loopback mode, the receiver retransmits the differential data on the receiver input pins via the transmitter pins.

The transceiver channels can also perform parallel loopback by bypassing the SERDES, allowing the design to test the digital circuitry of the transceiver channel. A reverse parallel loopback mode is also available, where the receiver's parallel output feeds into the transmitter's parallel inputs. See Figure 4 for the transceiver channel's loopback circuitry.

Power Down & Reset Capabilities

Each receiver and transmitter in the channel can power down individual blocks that are not used. The device can power down the PLL and channel aligner individually. Additionally, the device can individually reset the receiver and transmitter blocks as well as the FIFO buffer and the PLLs. Reset functions depend on device logic array configuration, test, and functionality.

Source-Synchronous Differential I/O Support

The left side of the Stratix GX devices contains dedicated circuitry for supporting differential standards at speeds up to 1 Gbps when using dynamic phase alignment (DPA). The Stratix GX devices support differential standards at up to 840 Mbps without using DPA. Stratix GX device source-synchronous circuitry supports LVDS, LVPECL, HyperTransport technology, and 3.3-V PCML I/O standards.

EP1SGX25 and EP1SGX10 devices have two dedicated high-speed PLLs and EP1SGX40 devices have four dedicated high-speed PLLs to multiply reference clocks and drive the source-synchronous differential SERDES channels. Table 17 shows the maximum number of channels each Stratix GX device supports.

Table 17. Source-Synchronous Differential I/O Resources in Stratix GX Devices

Device	Number of Fast PLLs	Device Pin Count	Number of Receiver Channels *(1)*	Receiver Channel Speed (Mbps)	Number of Transmitter Channels *(1)*	Transmitter Channel Speed (Mbps)
EP1SGX10C	2	672	22	1,000 *(2)*	22	1,000
EP1SGX10D	2	672	22	1,000 *(2)*	22	1,000
EP1SGX25C	2	672	39	1,000 *(2)*	39	1,000
EP1SGX25D	2	672	39	1,000 *(2)*	39	1,000
		1,020	39	1,000 *(2)*	39	1,000
EP1SGX25F	2	1,020	39	1,000 *(2)*	39	1,000
EP1SGX40D	4	1,020	45	1,000 *(2)*	45	1,000
EP1SGX40G	4	1,020	45	1,000 *(2)*	45	1,000

Notes to Table 17:
(1) This is the number of receiver or transmitter channels on the source-synchronous (left) side of the device.
(2) Receiver channels operate at 1,000 Mbps with DPA. Without DPA, the receiver channels operate at 840 Mbps.

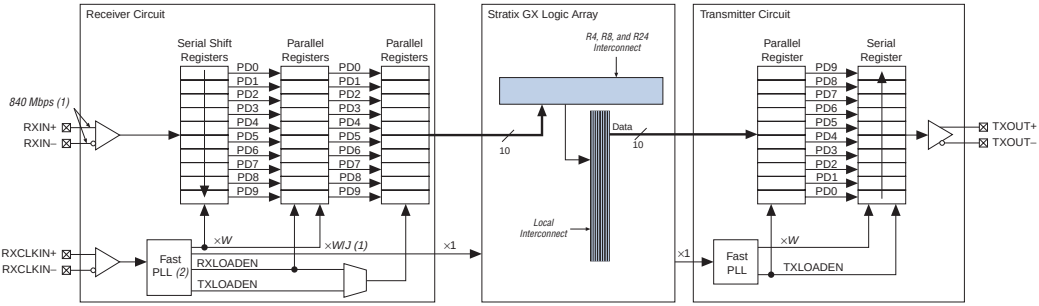
The source-synchronous differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- 10 Gigabit Ethernet XSBI
- RapidIO
- HyperTransport technology
- NPSI
- Utopia IV

Dedicated Source-Synchronous Circuitry

The left side of the Stratix GX device interfaces with LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology signaling at up to 1 Gbps. Stratix GX devices can transmit or receive serial channels along with a low-speed clocks. The receiving device multiplies the clock by a factor of 1, 2, 4, 8, or 10. The serialization/deserialization factor can be any number from 1, 2, 4, 8, or 10 and does not have to equal the clock-multiplication value. A design using the dynamic phase aligner can only have a serialization/deserialization factor of 8 or 10. For a SERDES factor of 1, the Stratix GX device bypasses the SERDES. For a SERDES factor of 2, the DDR input and output is used in the IOE. Figure 8 illustrates the dedicated receiver and transmitter interface.

Figure 8. Source-Synchronous Differential I/O Receiver/Transmitter Interface Example *Note (1)*



Note to Figure 8:

(1) Figure 8 shows the source-synchronous circuitry without the dynamic phase aligner. If a design uses the dynamic phase aligner, the source-synchronous differential I/O receiver and transmitter can input and output at up to 1.0 Gbps.

An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied differential I/O clocks, SERDES block, and/or external pin, and a low-speed clock to drive the logic array.

Each fast PLL can support up to 20 receiver and/or transmitter differential I/O channels in source-synchronous mode (without DPA). Table 18. shows how many receiver and transmitter channels each PLL supports.

Table 18. Number of Receiver & Transmitter Channels per PLL

Device	PLL Number	Receiver & Transmitter Channels	
		With DPA	Without DPA
EP1SGX10	PLL1	0	20
	PLL2	22	20
EP1SGX25	PLL1	19	20
	PLL2	20	20
EP1SGX40	PLL1	22	20
	PLL2	23	20
	PLL7	*(1)*	20
	PLL8	*(1)*	20

Note to Table 18:

(1) The corner PLLs (PLLs 7 and 8) do not support DPA.

Figure 9 shows the fast PLL and channel layout in EP1SGX25 and EP1SGX10 devices. Figure 10 shows the fast PLL and channel layout in the EP1SGX40 devices.

Figure 9. Fast PLL & Channel Layout in EP1SGX25D or EP1SGX10D Devices

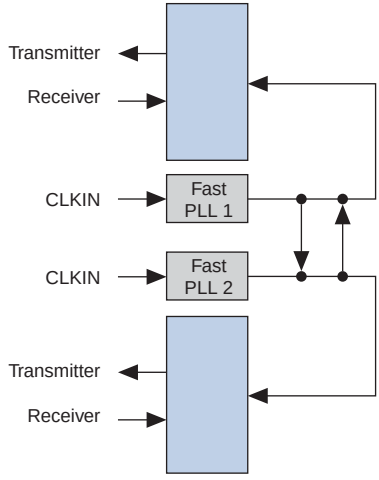
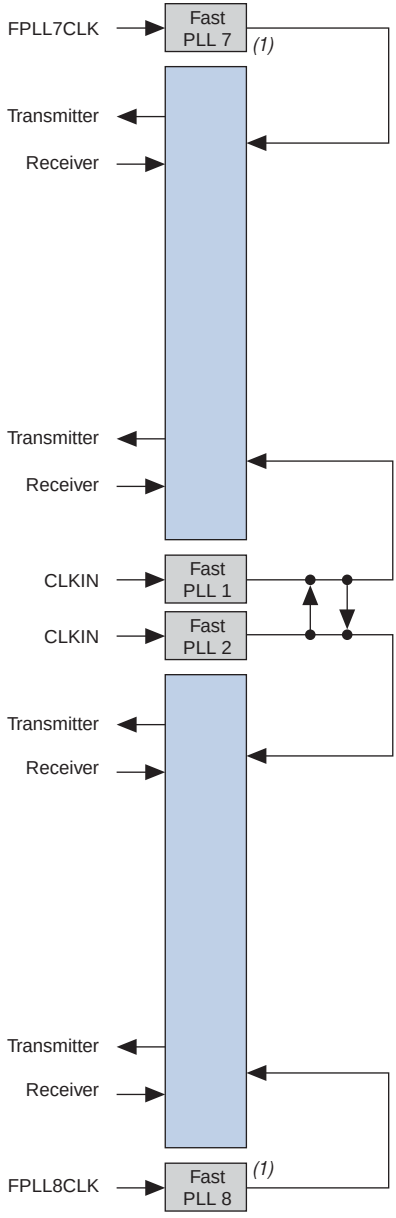


Figure 10. Fast PLL & Channel Layout in EP1SGX40 Devices



Note to Figure 10:
(1) PLLs 7 and 8 do not support any channels when using the dynamic phase aligner.

The transmitter external clock output is transmitted on a data channel. The `txclk` pin for each bank is located in between data transmitter pins. For ×1 clocks (e.g., 622 Mbps, 622 MHz), the high-speed PLL clock bypasses the SERDES to drive the output pins. For half-rate clocks (e.g., 622 Mbps, 311 MHz) or any other even-numbered factor such as 1/4, 1/8, or 1/10, the SERDES automatically generates the clock in the Quartus II software.

The designer can use a SERDES bypass implementation using DDR for systems that require more than four source-synchronous differential I/O clock domains. The dynamic phase aligner does not support SERDES bypass.

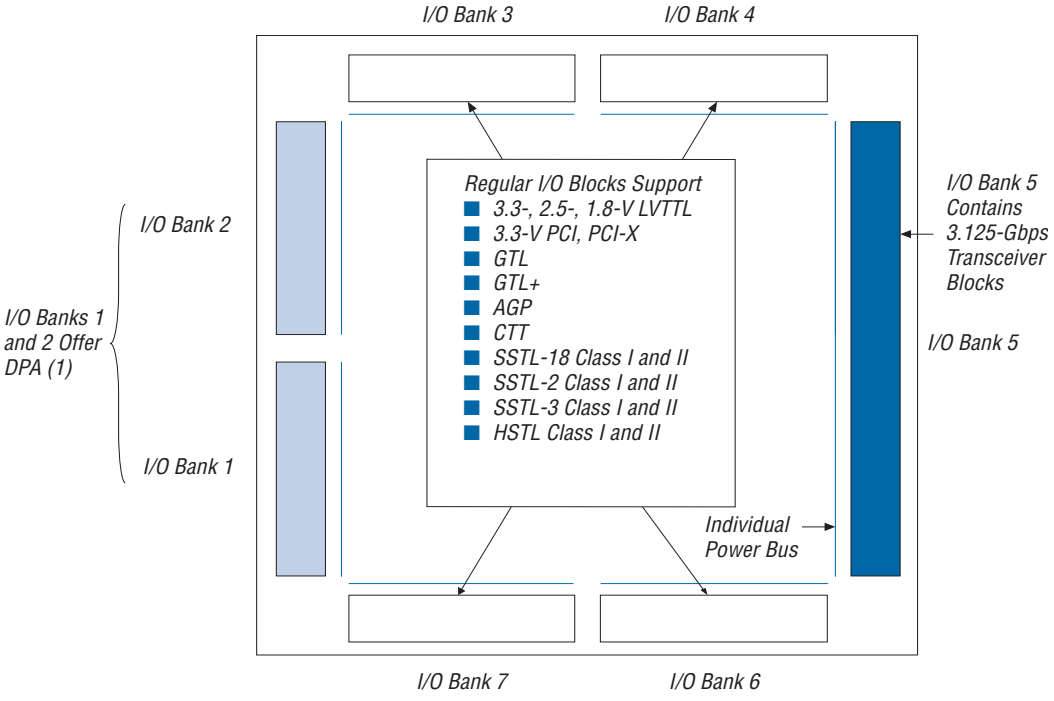
Byte Alignment

The source-synchronous clock rate for high-speed source-synchronous interfaces such as the POS-PHY 4 and XSBI interfaces is not a byte-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source-synchronous clock does not provide a byte or word boundary because the clock is one half the data rate, not one eighth. The Stratix GX device source-synchronous differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving LE resources. An input signal to each fast PLL can stall deserializer parallel data outputs by one bit period. The designer can use an LE-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

DPA

Stratix GX devices incorporate embedded dynamic phase alignment circuitry on their source-synchronous parallel interface in I/O banks 1 and 2 (see Figure 11). The dynamic phase aligner aligns the phase of the incoming clock with the phase of the incoming serial data. This allows the source-synchronous circuitry to capture data correctly regardless of the channel-to-channel skew or channel-to-clock skew.

Figure 11. DPA Support in Stratix GX Devices



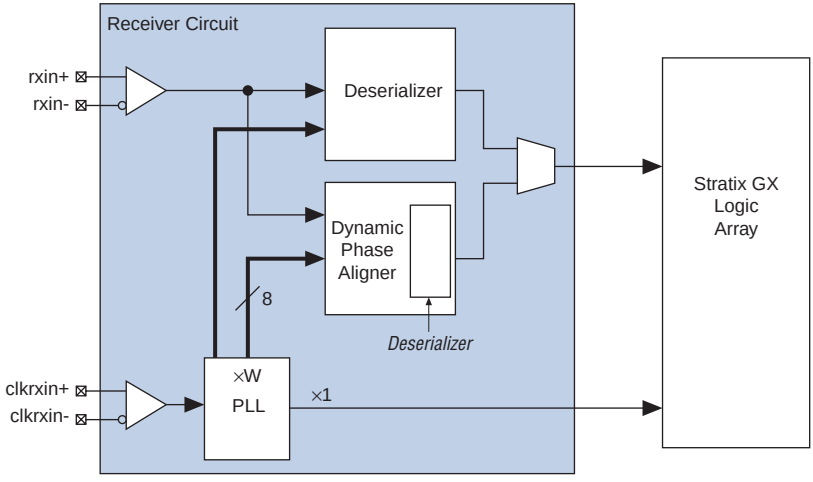
Note to Figure 11:
(1) Only inputs are connected to the differential receiver and clock input pins.

DPA Overview

The dynamic phase aligner operates in conjunction with the dedicated source-synchronous circuitry, and it may be bypassed without affecting the original source-synchronous operations described in "Dedicated Source-Synchronous Circuitry" on page 32. The dynamic phase alignment must have both the source clock and the serial data available during operation. Both the clock and the data must have identical frequency after multiplication factors. The dynamic phase aligner then automatically and continually adjusts for the phase skew between the multiplied clock and the serial data.

The source clock is fed to the fast PLL through the dedicated clock input pins (see "PLLs & Clock Networks" on page 109 for more information). The clock is then multiplied by the multiplication value *W* to match the serial data rate. The fast PLL generates eight phase-shifted versions of the clock. The dynamic phase aligner samples the incoming serial data and uses the clock phase closest to the center of the incoming serial data eye. Figure 12 shows the source-synchronous circuitry and the dynamic phase aligner.

Figure 12. Source-Synchronous Circuitry & the Dynamic Phase Aligner



Note to Figure 12:
(1) Figure 12 does not provide details of the dynamic phase aligner.

DPA Specifications

DPA source-synchronous circuitry supports specifications listed in Table 19

Table 19. Training Patterns for Different Protocols

Protocols	Training Pattern	Number of Repetitions
SPI-4, NPSI	Ten 0's, ten 1's (0000000000111111111)	256
RapidIO	Four 0's, four 1's (00001111) or one 1, two 0's, one 1, four 0's (10010000)	
Other designs	Eight alternating 1's and 0's (10101010 or 01010101)	
SFI-4, XSBI	Not specified	

Differential Protocols

Stratix GX device dynamic phase aligner supports the source-synchronous standards specified below in Table 20.

Table 20. Dynamic Phase Aligner Protocols

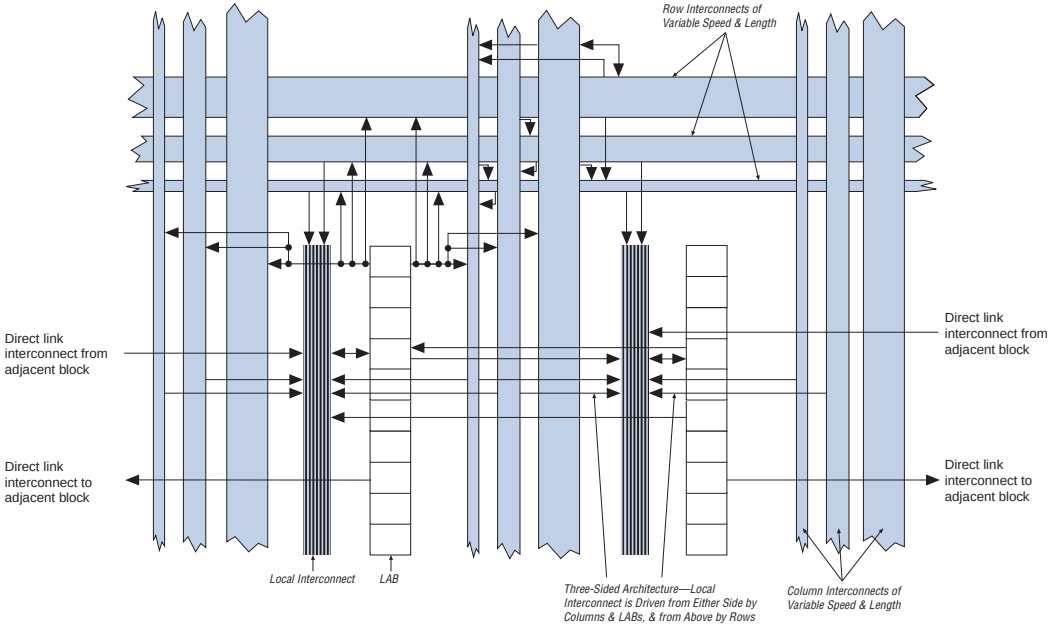
Parameters	SPI-4	SFI-4	XSBI	RapidIO	NPSI
Data lanes	16	16	16	8, 16	16
Control/frame	1	0	0	1	1
Maximum data rate (Mbps)	840	644.53	644.53	1,000	1,000
Number of clocks	1	1	1	1, 2	1
SDR / DDR	DDR	SDR	SDR	DDR	DDR
Maximum clock rate (MHz)	420	622.08	644.53	500	500
I/O standards	LVDS	LVDS	LVDS	LVDS	LVDS
Channel topology	Full duplex / uniplex	Full duplex	Full duplex	Full duplex	Full duplex

For more information on DPA, see *AN 236: Using Source-Synchronous Signaling with DPA in Stratix GX Devices*.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 13 shows the Stratix GX LAB.

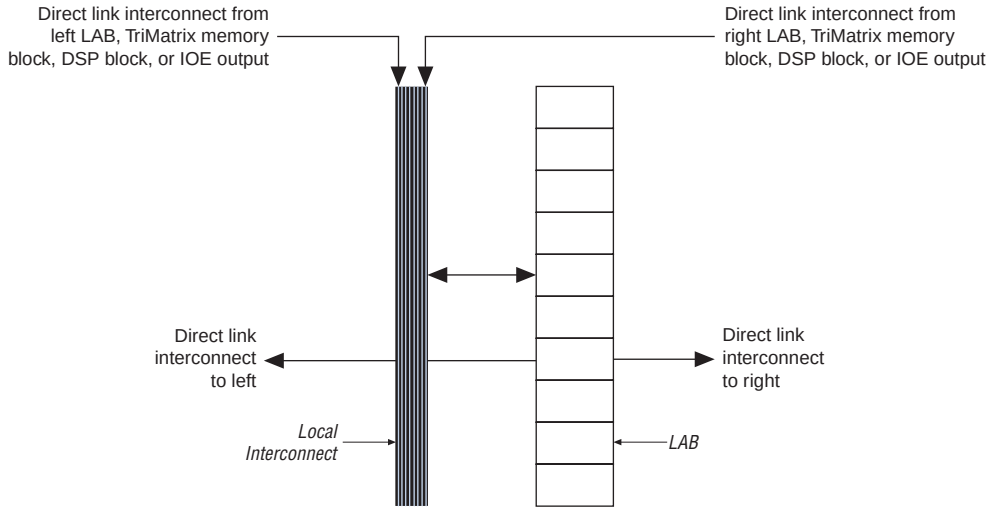
Figure 13. Stratix GX LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 14 shows the direct link connection.

Figure 14. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

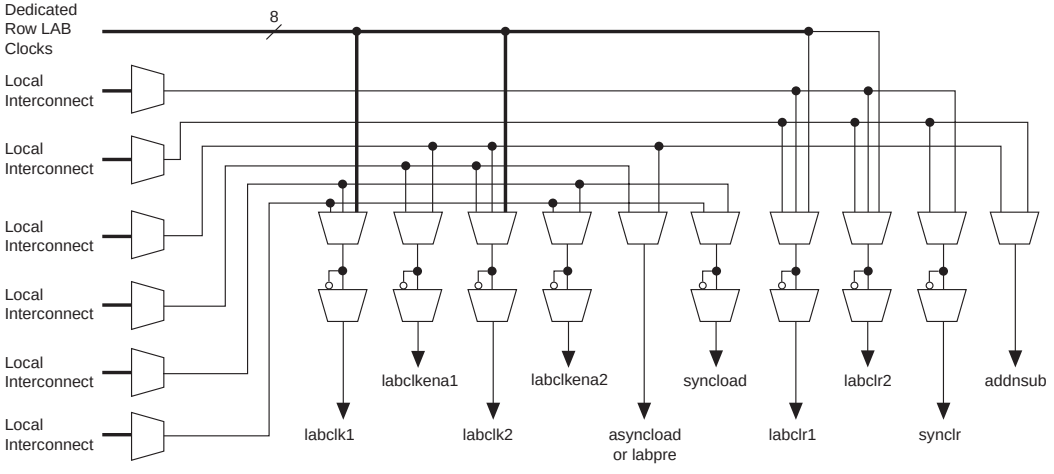
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and additional signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 15 shows the LAB control signal generation circuit.

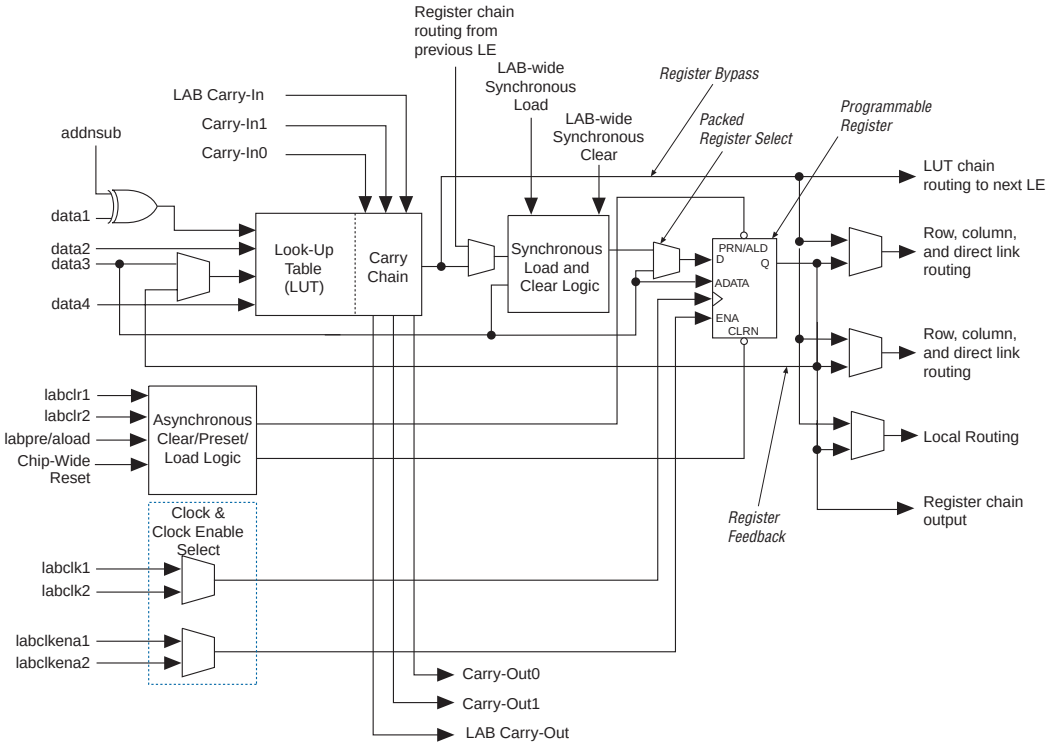
Figure 15. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Stratix GX architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 16.

Figure 16. Stratix GX LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the register is bypassed and the output of the LUT drives directly to the outputs of the LE.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 51 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the A bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Stratix GX LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

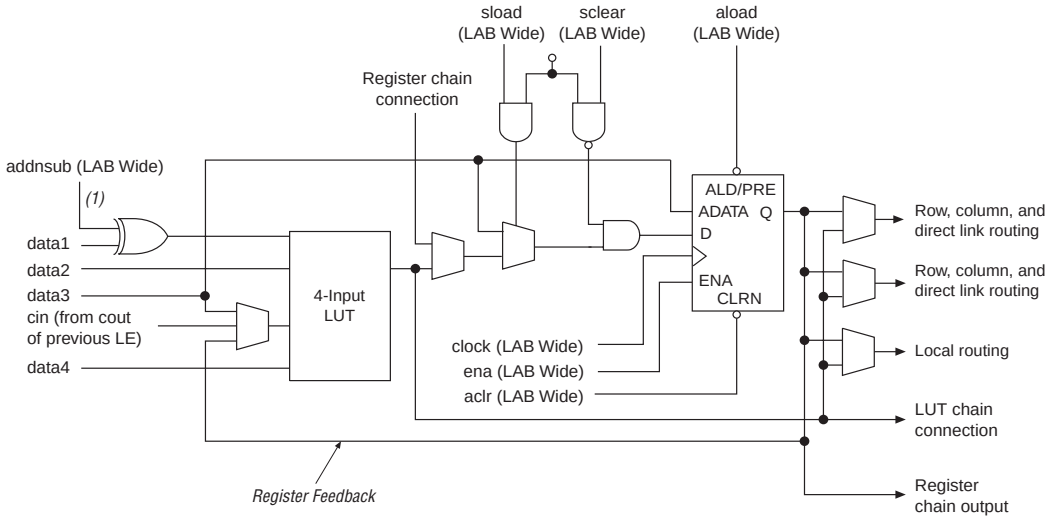
Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 17). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

Figure 17. LE in Normal Mode



Note to Figure 17:

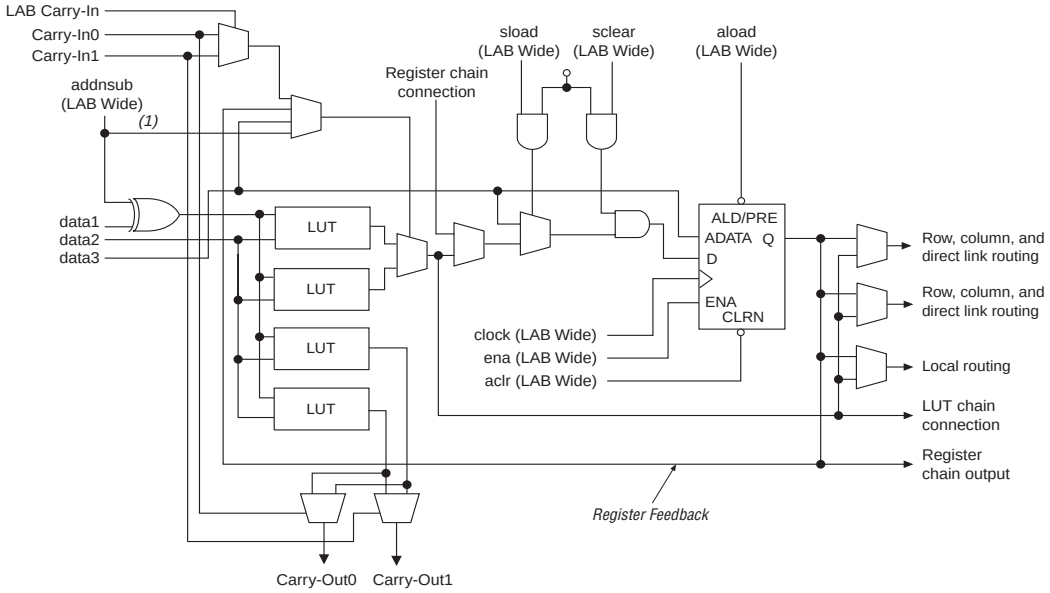
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 18, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums: `data1` + `data2` + `carry-in0` or `data1` + `data2` + `carry-in1`. The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 18. LE in Dynamic Arithmetic Mode



Note to Figure 18:
(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

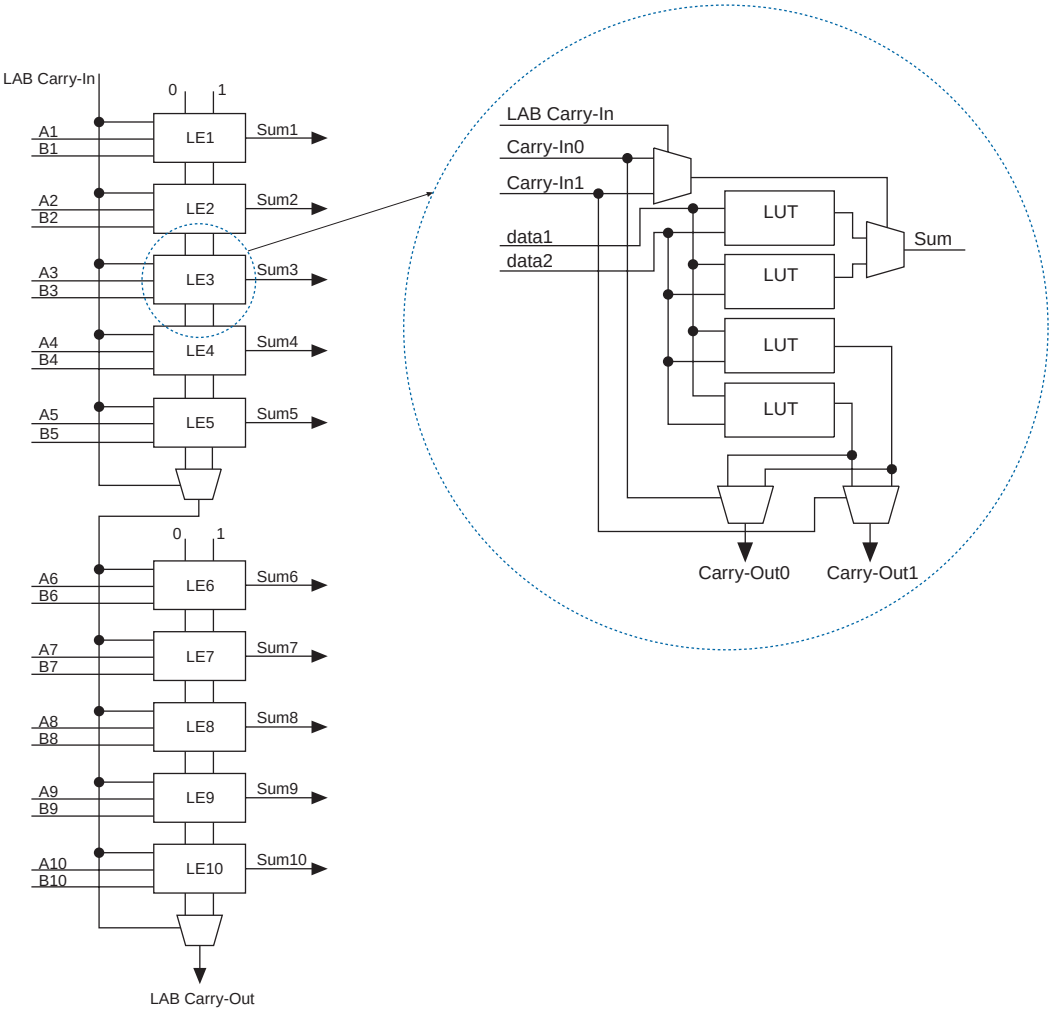
The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix GX architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 19 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or the designer can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

Figure 19. Carry Select Chain



Clear & Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix GX devices support simultaneous preset/asynchronous load, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Stratix GX devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix GX architecture, connections between LEs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

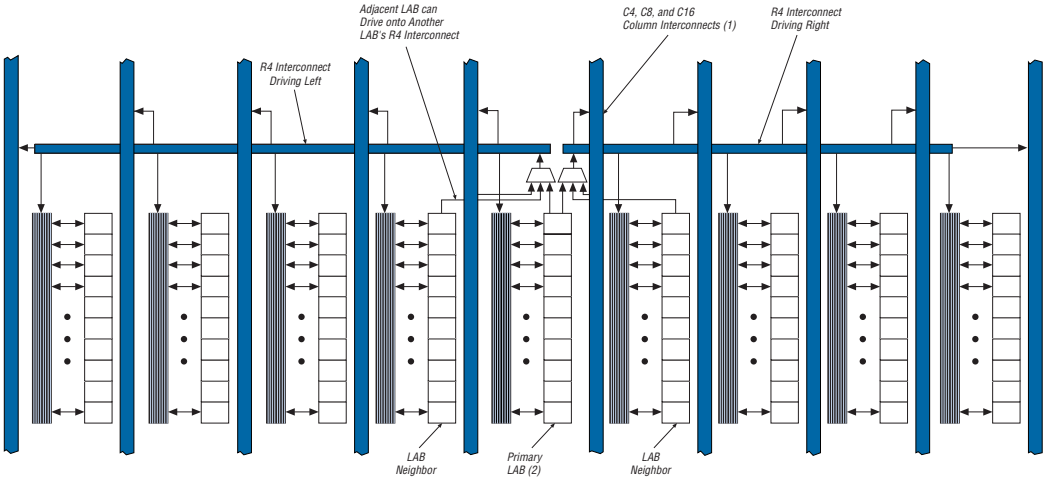
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks.
- R4 interconnects traversing four blocks to the right or left.
- R8 interconnects traversing eight blocks to the right or left.
- R24 row interconnects for high-speed access across the length of the device.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. Only one side of a M-RAM block interfaces with direct link and row interconnects. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 20 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and horizontal IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 20. R4 Interconnect Connections



Notes to Figure 20:
(1) C4 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.

The R8 interconnects span eight LABs, M512 or M4K RAM blocks, or DSP blocks to the right or left from a source LAB. These resources are used for fast row connections in an eight-LAB region. Every LAB has its own set of R8 interconnects to drive either left or right. R8 interconnect connections between LABs in a row are similar to the R4 connections shown in Figure 20, with the exception that they connect to eight LABs to the right or left, not four. Like R4 interconnects, R8 interconnects can drive and be driven by all types of architecture blocks. R8 interconnects can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

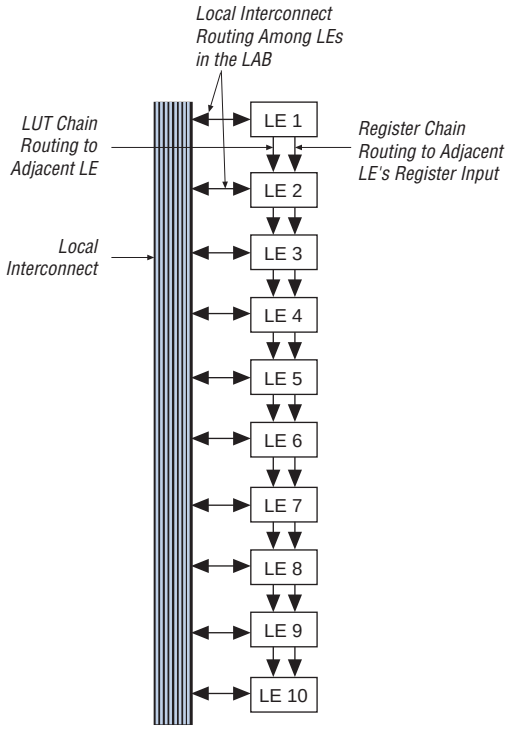
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

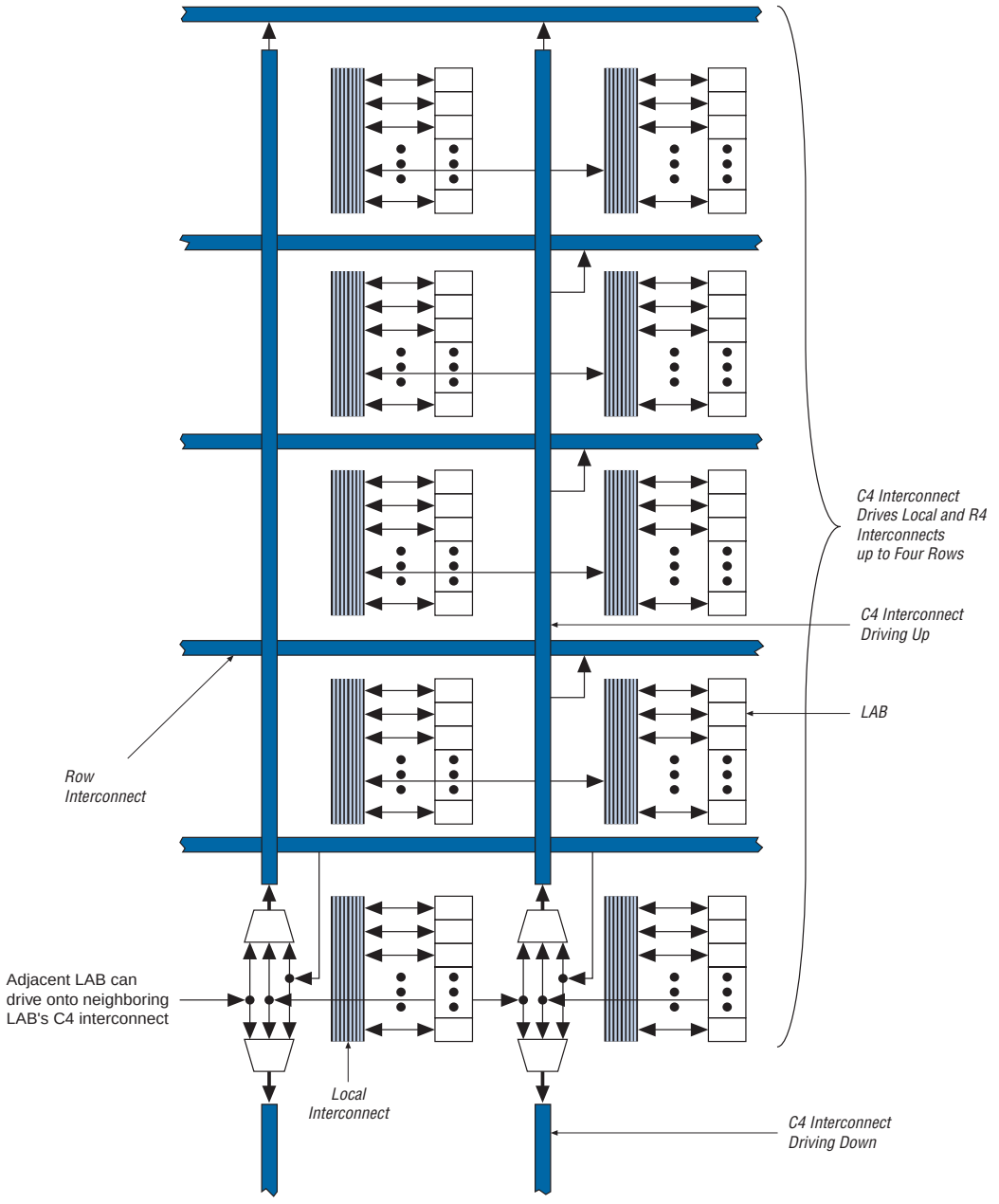
Stratix GX devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 21 shows the LUT chain and register chain interconnects.

Figure 21. LUT Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 22 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and vertical IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 22. C4 Interconnect Connections *Note (1)*



Note to Figure 22:

(1) Each C4 interconnect can drive either up or down four rows.

C8 interconnects span eight LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C8 interconnects to drive either up or down. C8 interconnect connections between the LABs in a column are similar to the C4 connections shown in Figure 22 with the exception that they connect to eight LABs above and below. The C8 interconnects can drive and be driven by all types of architecture blocks similar to C4 interconnects. C8 interconnects can drive each other to extend their range as well as R8 interconnects for column-to-column connections. C8 interconnects are faster than two C4 interconnects.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[7..0]`.

Table 21 shows the Stratix GX device's routing scheme.

Table 21. Stratix GX Device Routing Scheme

Source	Destination																
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R8 Interconnect	R24 Interconnect	C4 Interconnect	C8 Interconnect	C16 Interconnect	LE	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
LUT Chain											✓						
Register Chain											✓						
Local Interconnect											✓	✓	✓	✓	✓	✓	✓
Direct Link Interconnect			✓														
R4 Interconnect			✓		✓		✓	✓		✓							
R8 Interconnect			✓			✓			✓								
R24 Interconnect					✓		✓	✓		✓							
C4 Interconnect			✓		✓			✓									
C8 Interconnect			✓			✓			✓								
C16 Interconnect					✓		✓	✓		✓							
LE			✓	✓	✓	✓		✓	✓								
M512 RAM Block			✓	✓	✓	✓		✓	✓								
M4K RAM Block			✓	✓	✓	✓		✓	✓								
M-RAM Block								✓	✓								
DSP Blocks			✓	✓	✓	✓		✓	✓								
Column IOE				✓				✓	✓	✓							
Row IOE				✓		✓	✓	✓	✓	✓							

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM blocks. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 22 shows the size and features of the different RAM blocks.

Table 22. TriMatrix Memory Features

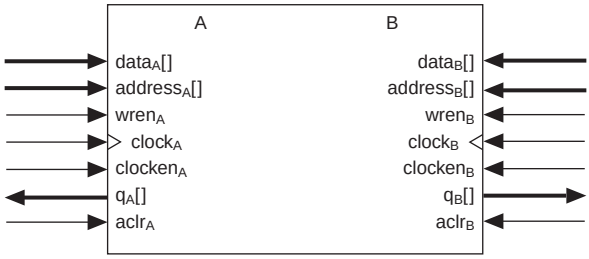
Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	*(1)*	*(1)*	*(1)*
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Byte enable		✓	✓
Parity bits	✓	✓	✓
Shift register	✓	✓	
Mixed clock mode	✓	✓	✓
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Note to Table 22:
(1) See Table 89 for maximum performance information.

Memory Modes

TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K and M-RAM memory blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 23 shows true dual-port memory.

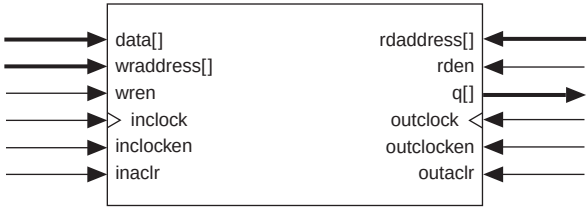
Figure 23. True Dual-Port Memory Configuration



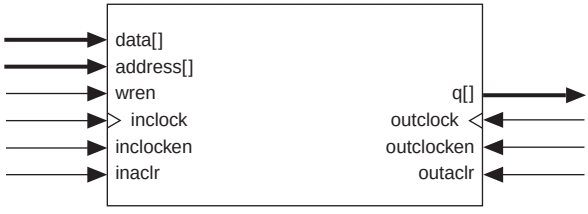
In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write. Single-port memory supports non-simultaneous reads and writes. Figure 24 shows these different RAM memory port configurations for TriMatrix memory.

Figure 24. Simple Dual-Port & Single-Port Memory Configurations

Simple Dual-Port Memory



Single-Port Memory *(1)*



Note to Figure 24:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in ×1 mode at port A and read out in ×16 mode from port B.

TriMatrix memory architecture can implement fully synchronous RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`WREN`) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM `WREN` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `WREN` signal. The output registers can be bypassed. Pseudo-asynchronous reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 × 16-bit RAM blocks can be combined to form a 256 × 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words allowed. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

Parity Bit Support

The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. Designers can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

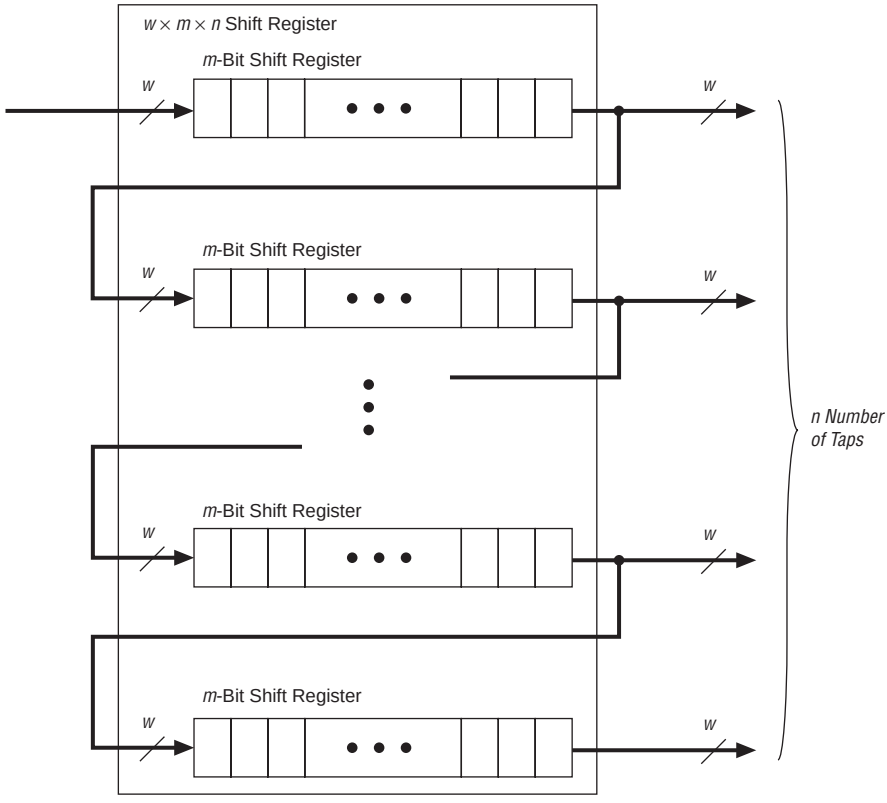
Shift Register Support

The designer can configure embedded memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a $w \times m \times n$ shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a $w \times m \times n$ shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 RAM block and 4,608 bits for the M4K RAM block. The total number of shift register outputs (number of taps $n \times$ width w) must be less than the maximum data width of the RAM block (18 for M512 blocks, 36 for M4K blocks). To create larger shift registers, the memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 25 shows the TriMatrix memory block in the shift register mode.

Figure 25. Shift Register Memory Configuration



Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix GX devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. The designer can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 512 × 1, 256 × 2, 128 × 4, 64 × 8 (64 × 9 bits with parity), and 32 × 16 (32 × 18 bits with parity). Mixed-width configurations are also possible, allowing different read and write widths. Table 23 summarizes the possible M512 RAM block configurations.

Table 23. M512 RAM Block Configurations (Simple Dual-Port RAM)

Read Port	Write Port						
	512 × 1	256 × 2	128 × 4	64 × 8	32 × 16	64 × 9	32 × 18
512 × 1	✓	✓	✓	✓	✓		
256 × 2	✓	✓	✓	✓	✓		
128 × 4	✓	✓	✓		✓		
64 × 8	✓	✓		✓			
32 × 16	✓	✓	✓		✓		
64 × 9						✓	
32 × 18							✓

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 137 for details on dedicated SERDES in Stratix GX devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight labclk signals or local interconnect can drive the inclock, outclock, wren, rden, inclr, and outclr signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the wren and rden signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 26 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix GX devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 27 shows the M512 RAM block to logic array interface.

Figure 26. M512 RAM Block Control Signals

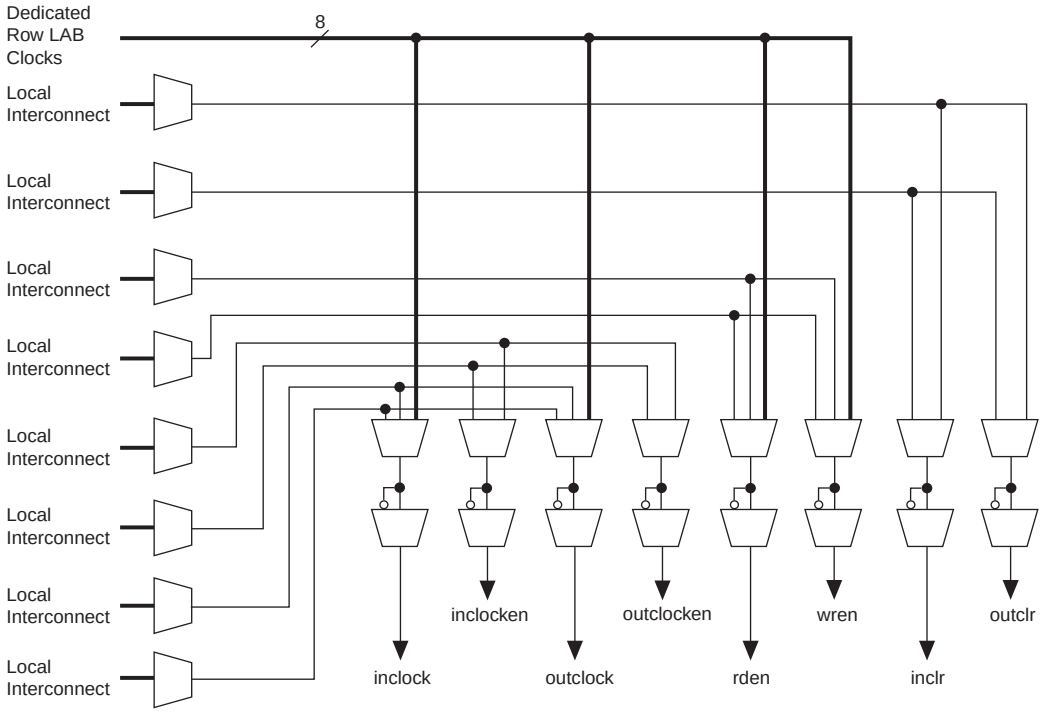
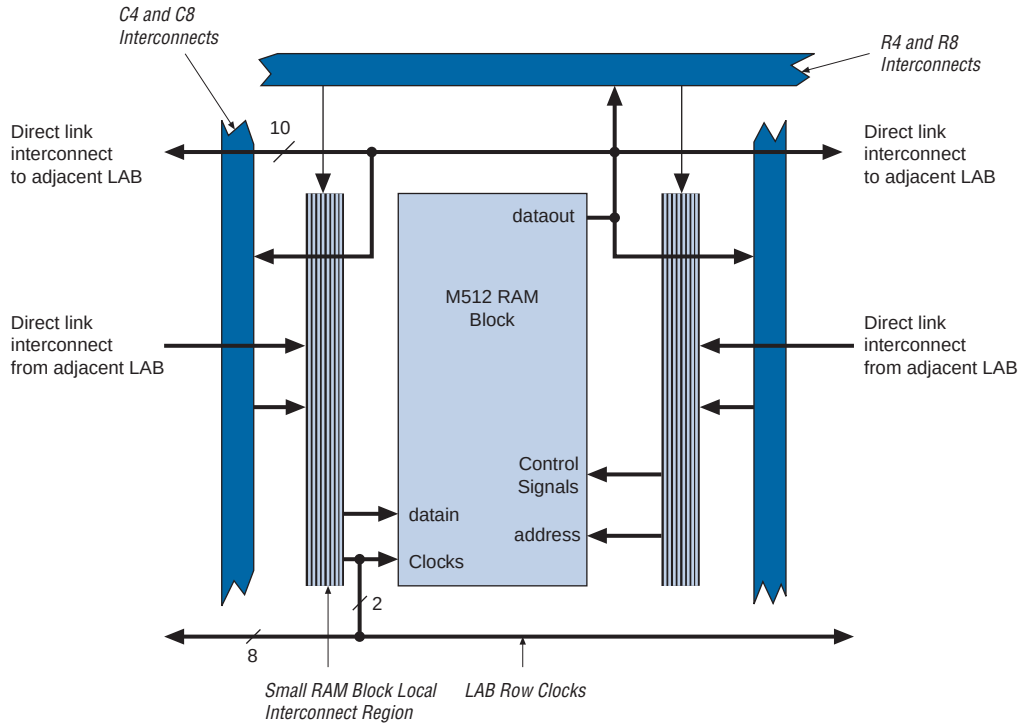


Figure 27. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 4,096 × 1, 2,048 × 2, 1,024 × 4, 512 × 8 (or 512 × 9 bits), 256 × 16 (or 256 × 18 bits), and 128 × 32 (or 128 × 36 bits). The 128 × 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 24 and 25 summarize the possible M4K RAM block configurations.

Table 24. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	128 × 32	512 × 9	256 × 18	128 × 36
4K × 1	✓	✓	✓	✓	✓	✓			
2K × 2	✓	✓	✓	✓	✓	✓			
1K × 4	✓	✓	✓	✓	✓	✓			
512 × 8	✓	✓	✓	✓	✓	✓			
256 × 16	✓	✓	✓	✓	✓	✓			
128 × 32	✓	✓	✓	✓	✓	✓			
512 × 9							✓	✓	✓
256 × 18							✓	✓	✓
128 × 36							✓	✓	✓

Table 25. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K × 1	2K × 2	1K × 4	512 × 8	256 × 16	512 × 9	256 × 18
4K × 1	✓	✓	✓	✓	✓		
2K × 2	✓	✓	✓	✓	✓		
1K × 4	✓	✓	✓	✓	✓		
512 × 8	✓	✓	✓	✓	✓		
256 × 16	✓	✓	✓	✓	✓		
512 × 9						✓	✓
256 × 18						✓	✓

When the M4K RAM block is configured as a shift register block, the designer can create a shift register up to 4,608 bits ($w \times m \times n$).

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 26 summarizes the byte selection.

Table 26. Byte Enable for M4K Blocks *Notes (1), (2)*

byteena[3..0]	datain ×18	datain ×36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 26:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 28.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 29 shows the M4K RAM block to logic array interface.

Figure 28. M4K RAM Block Control Signals

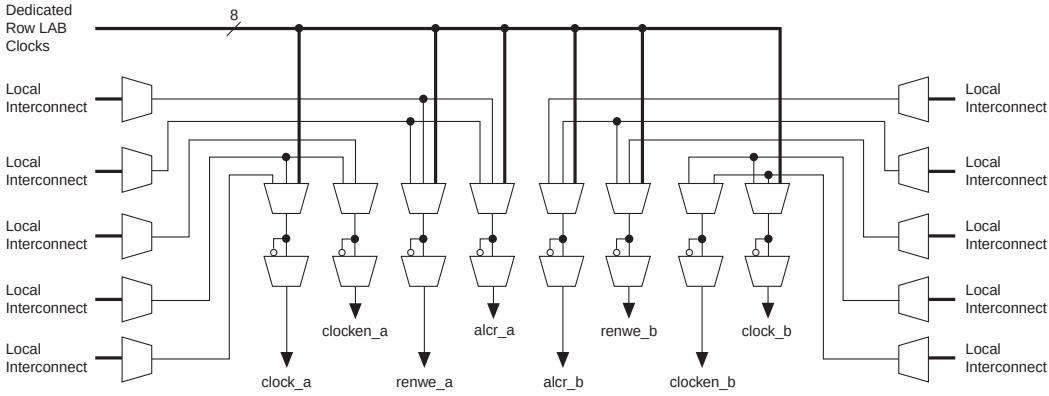
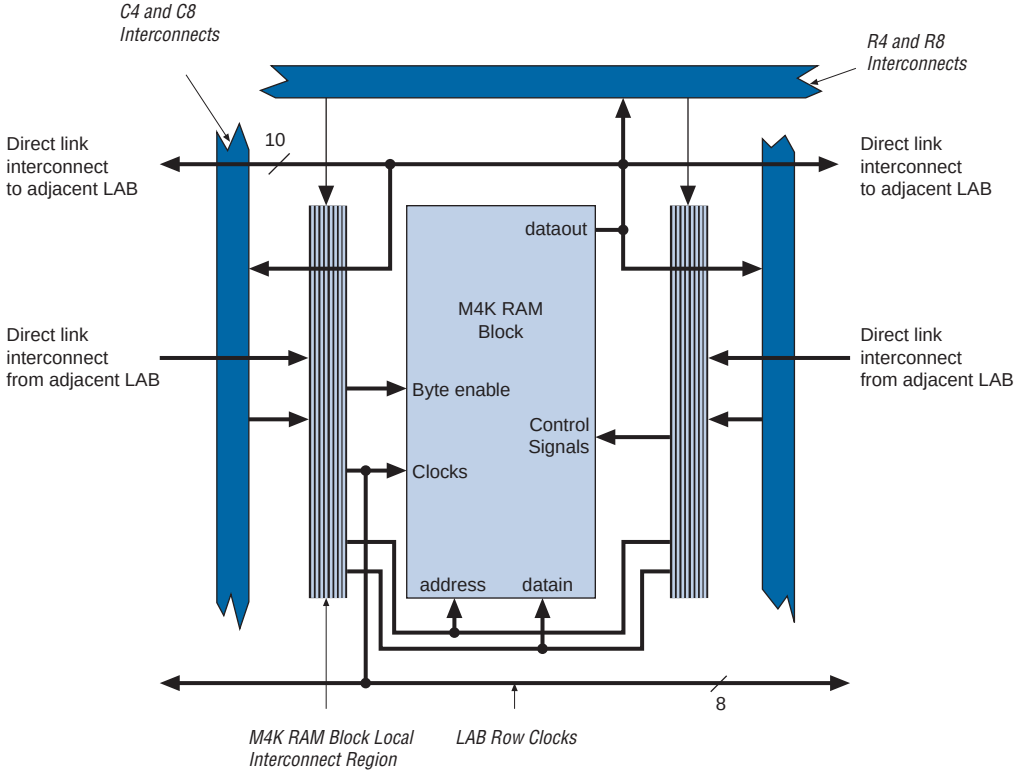


Figure 29. M4K RAM Block LAB Row Interface



M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- Shift register

The designer cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as 64K × 8 (or 64K × 9 bits), 32K × 16 (or 32K × 18 bits), 16K × 32 (or 16K × 36 bits), 8K × 64 (or 8K × 72 bits), and 4K × 128 (or 4K × 144 bits). The 4K × 128 configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. Tables 27 and 28 summarizes the possible M-RAM block configurations:

Table 27. M-RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port				
	64K × 9	32K × 18	16K × 36	8K × 72	4K × 144
64K × 9	✓	✓	✓	✓	
32K × 18	✓	✓	✓	✓	
16K × 36	✓	✓	✓	✓	
8K × 72	✓	✓	✓	✓	
4K × 144					✓

Table 28. M-RAM Block Configurations (True Dual-Port)

Port A	Port B			
	64K × 9	32K × 18	16K × 36	8K × 72
64K × 9	✓	✓	✓	✓
32K × 18	✓	✓	✓	✓
16K × 36	✓	✓	✓	✓
8K × 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the WREN signal, which sets the ports into either read or write modes. There is no separate read enable (RE) signal.

Writing into RAM is controlled by both the WREN and byte enable (byteena) signals for each port. The default value for the byteena signal is high, in which case writing is controlled only by the WREN signal. The byte enables are available for the ×18, ×36, and ×72 modes. In the ×144 simple dual-port mode, the two sets of byteena signals (byteena_a and byteena_b) are combined to form the necessary 16 byte enables. Table 29 and Table 30 summarize the byte selection.

Table 29. Byte Enable for M-RAM Blocks *Notes (1), (2)*

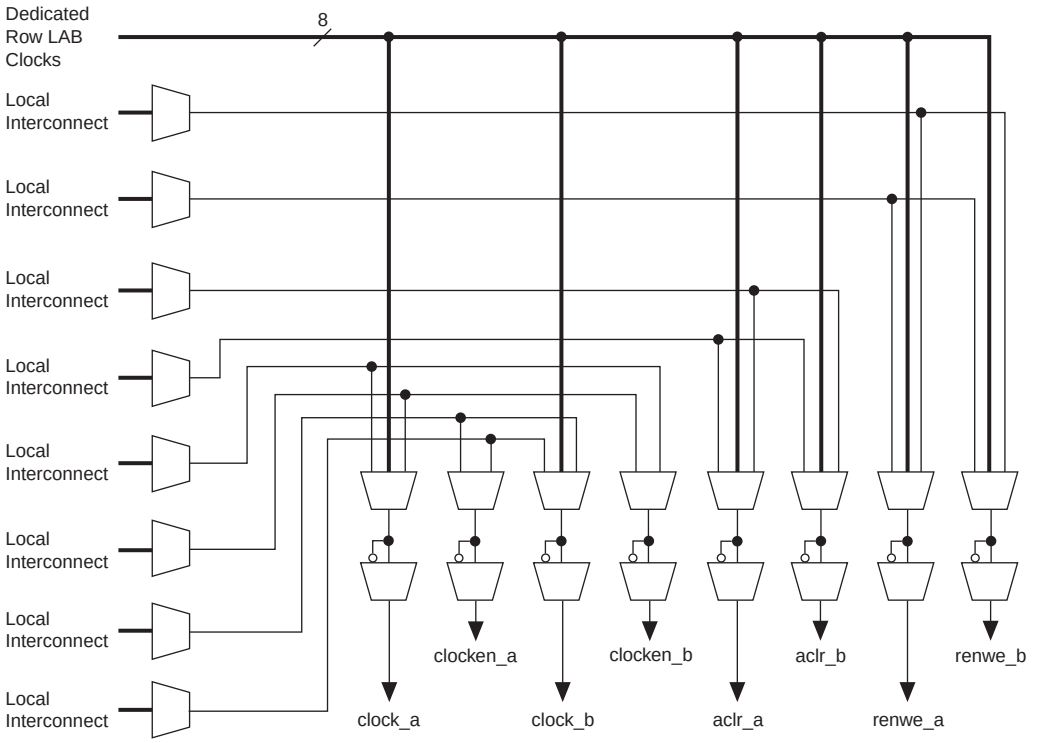
byteena[3..0]	datain ×18	datain ×36	datain ×72
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Table 30. M-RAM Combined Byte Selection for ×144 Mode Notes (1), (2)	
byteena[15..0]	**datain ×144**
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

Notes to Tables 29 and 30:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, ×64, and ×128 modes.

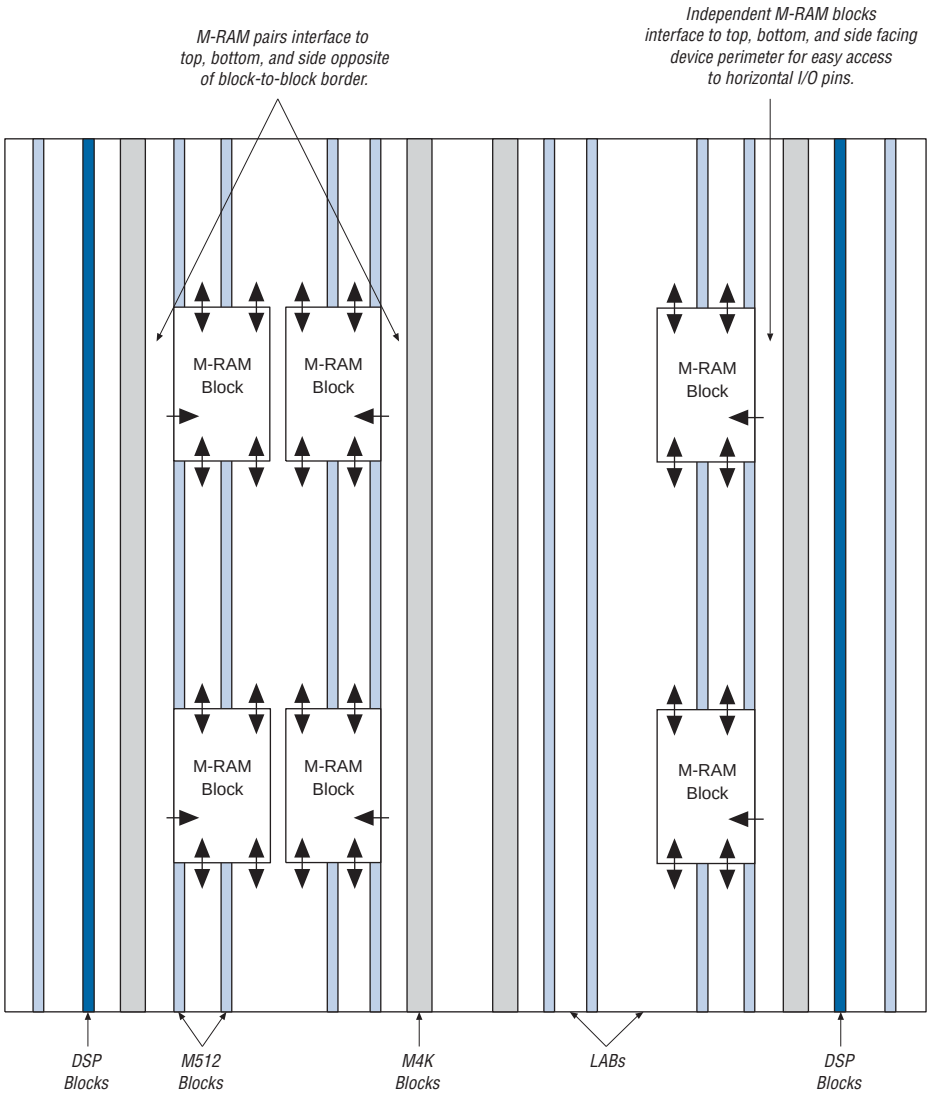
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, clr_b, `clocken_a`, and `clocken_b` signals as shown in Figure 30.

Figure 30. M-RAM Block Control Signals



One of the M-RAM block's horizontal sides drive the address and control signal (clock, renwe, byteena, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 31 shows an example floorplan for the EP1S60 device and the location of the M-RAM interfaces.

Figure 31. EP1SGX40 Device with M-RAM Interface Locations *Note (1)*



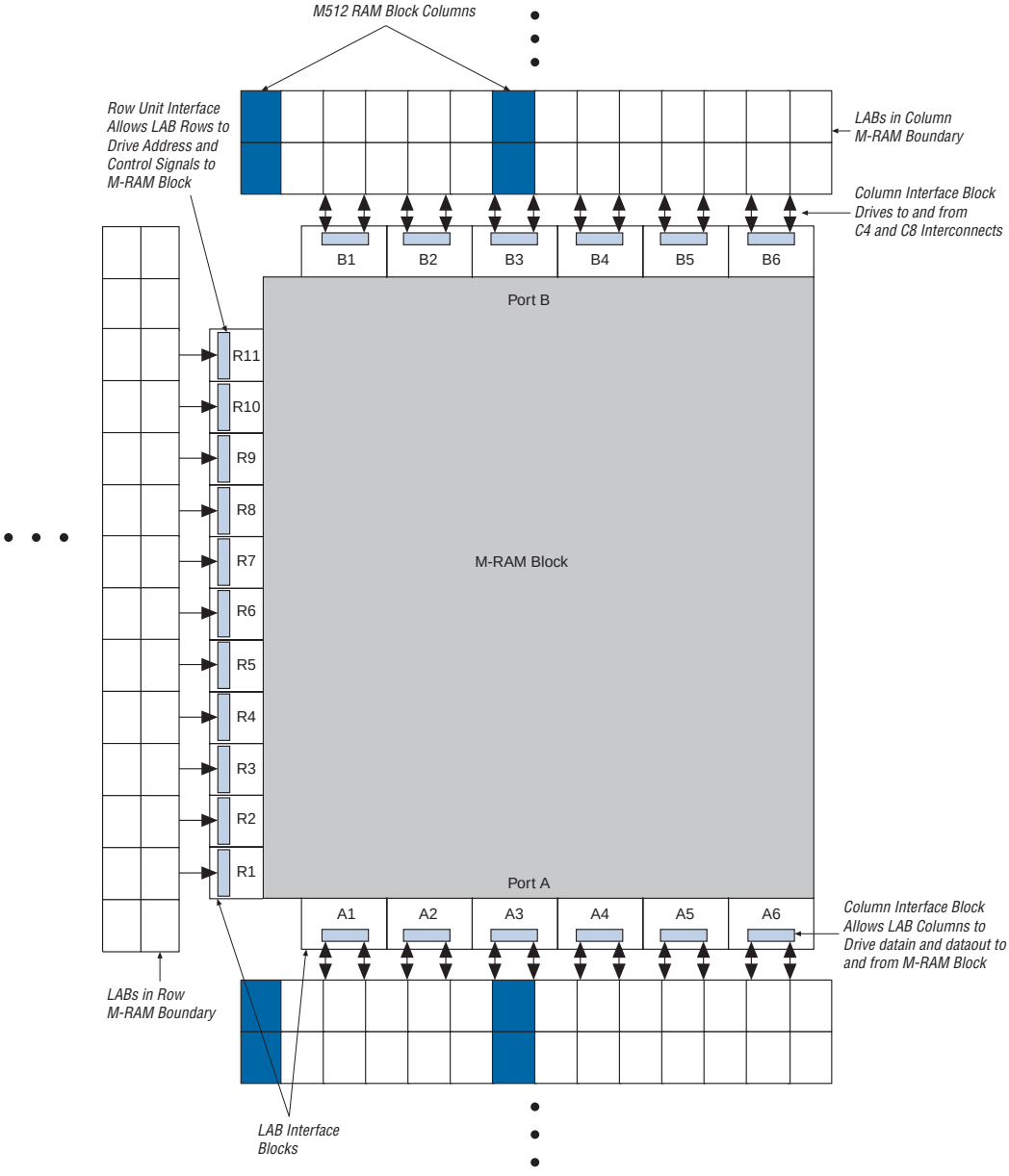
Note to Figure 31:

(1) Device shown is an EP1SGX40 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM Block are possible from the left adjacent LABs for M-RAM blocks facing to the left, and another 10 possible from the right adjacent LABs for M-RAM blocks facing to the right. For column interfacing, every M-RAM column unit connects to the right and left column lines, allowing each M-RAM column unit to communicate directly with three columns of LABs. Figures 32 through 34 show the interface between the M-RAM block and the logic array.

Table 31 shows the input and output data signal connections for the column units (B1 to B6 and A1 to A6). It also shows the address and control signal input connections to the row units (R1 to R11).

Figure 32. Left-Facing M-RAM to Interconnect Interface *Notes (1), (2)*



Notes to Figure 32:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Figure 33. M-RAM Row Unit Interface to Interconnect

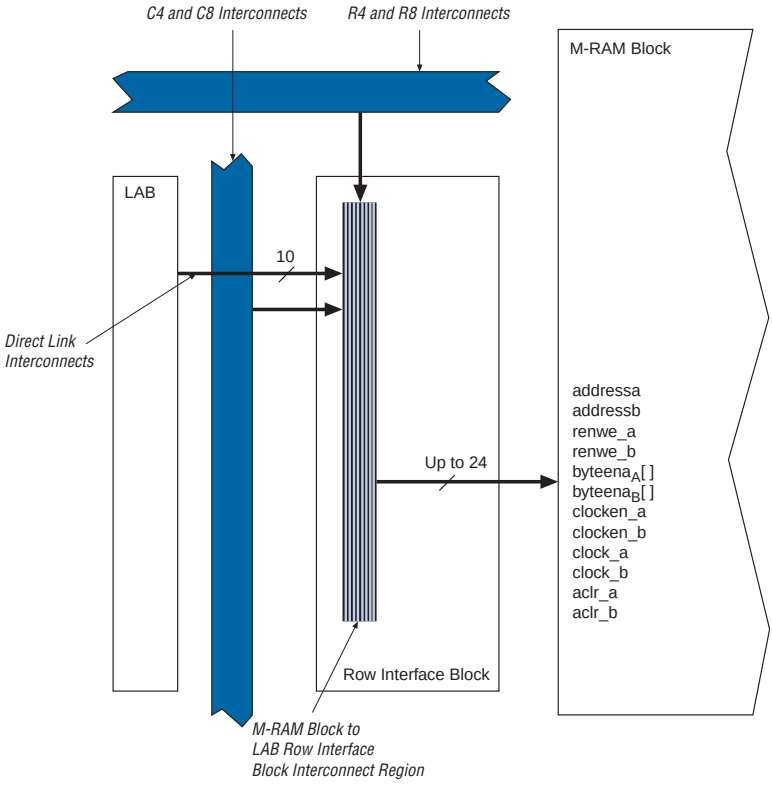


Figure 34. M-RAM Column Unit Interface to Interconnect

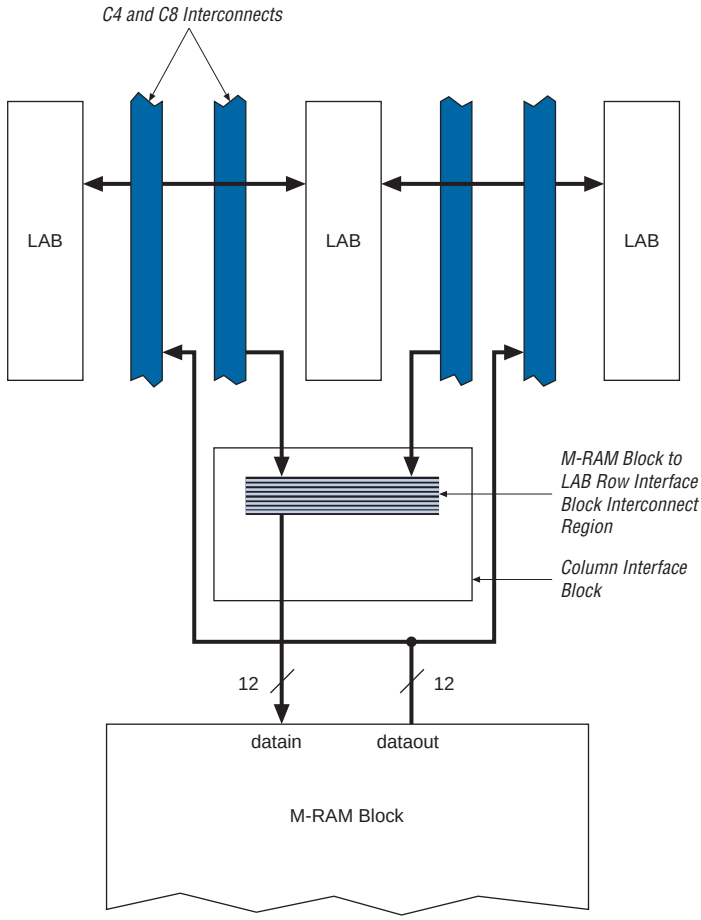


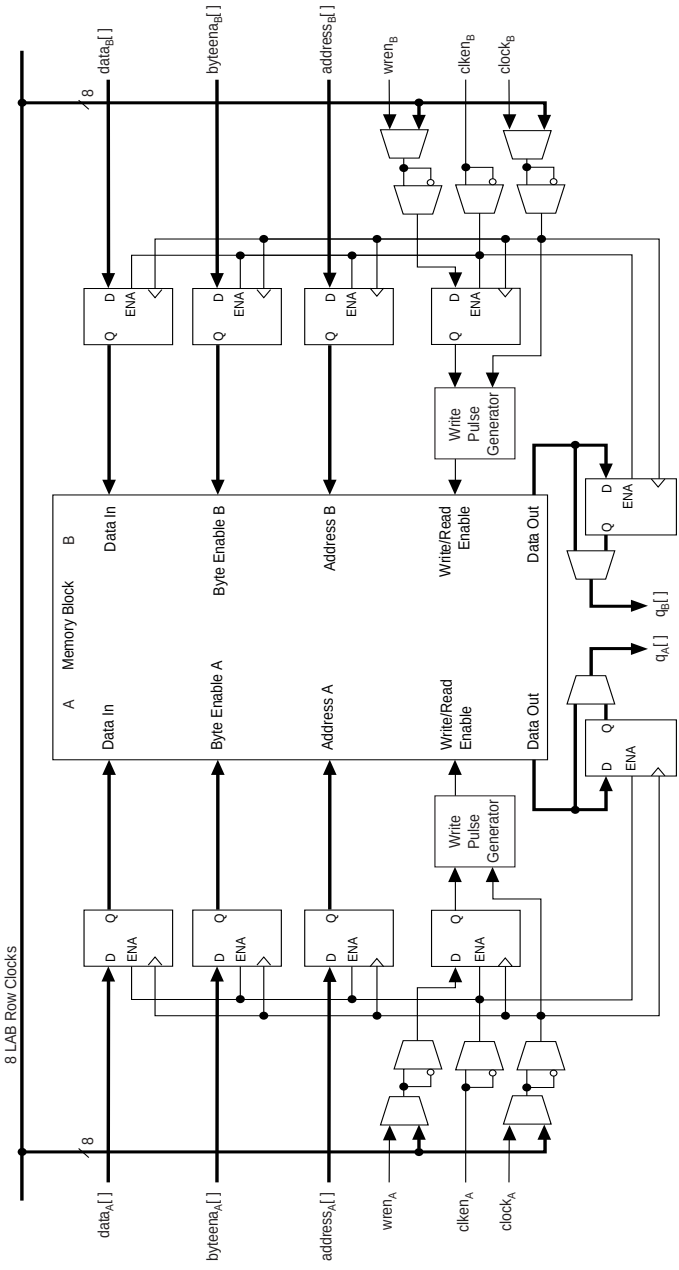
Table 31. M-RAM Row & Column Interface Unit Signals

Unit Interface Block	Input SIgnals	Output Signals
R1	addressa[7..0]	
R2	addressa[15..8]	
R3	byte_enable_a[7..0] renwe_a	
R4	-	
R5	-	
R6	clock_a clocken_a clock_b clocken_b	
R7	-	
R8	-	
R9	byte_enable_b[7..0] renwe_b	
R10	addressb[15..8]	
R11	addressb[7..0]	
B1	datain_b[71..60]	dataout_b[71..60]
B2	datain_b[59..48]	dataout_b[59..48]
B3	datain_b[47..36]	dataout_b[47..36]
B4	datain_b[35..24]	dataout_b[35..24]
B5	datain_b[23..12]	dataout_b[23..12]
B6	datain_b[11..0]	dataout_b[11..0]
A1	datain_a[71..60]	dataout_a[71..60]
A2	datain_a[59..48]	dataout_a[59..48]
A3	datain_a[47..36]	dataout_a[47..36]
A4	datain_a[35..24]	dataout_a[35..24]
A5	datain_a[23..12]	dataout_a[23..12]
A6	datain_a[11..0]	dataout_a[11..0]

Independent Clock Mode

The memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 35 shows a TriMatrix memory block in independent clock mode.

Figure 35. Independent Clock Mode *Note (1)*



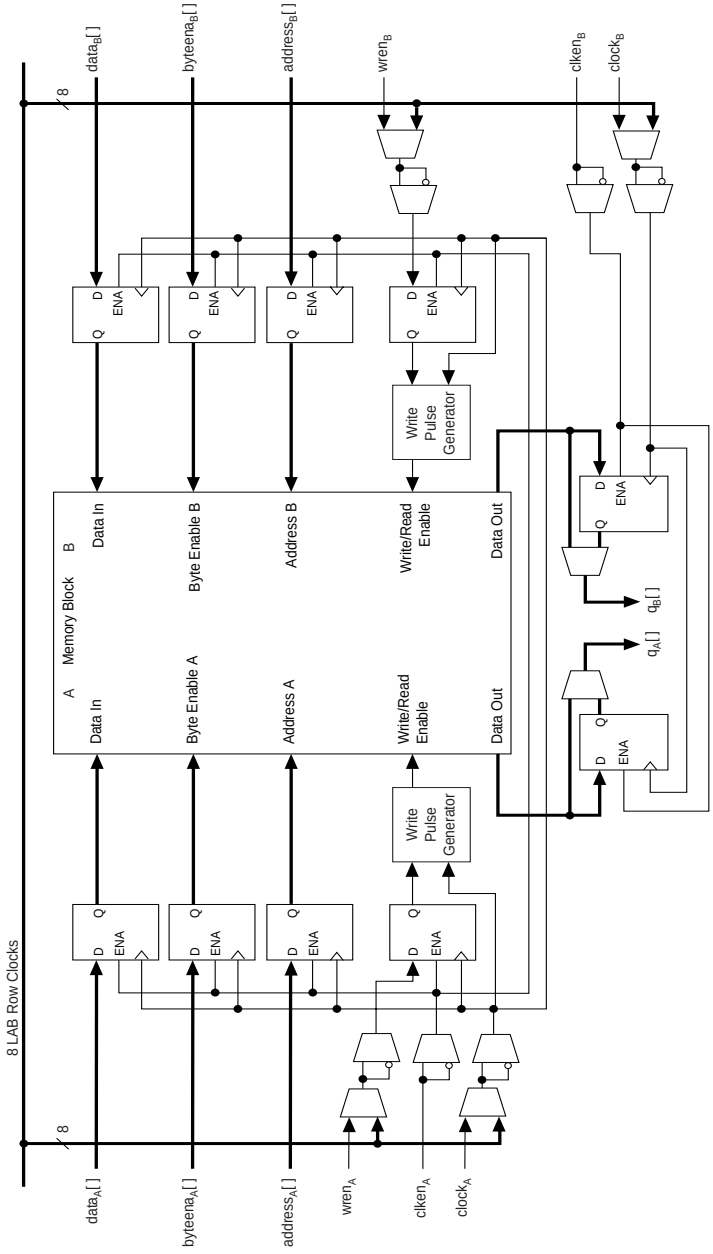
Note to Figure 35:

(1) All registers shown have asynchronous clear ports.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 36 and 37 show the memory block in input/output clock mode.

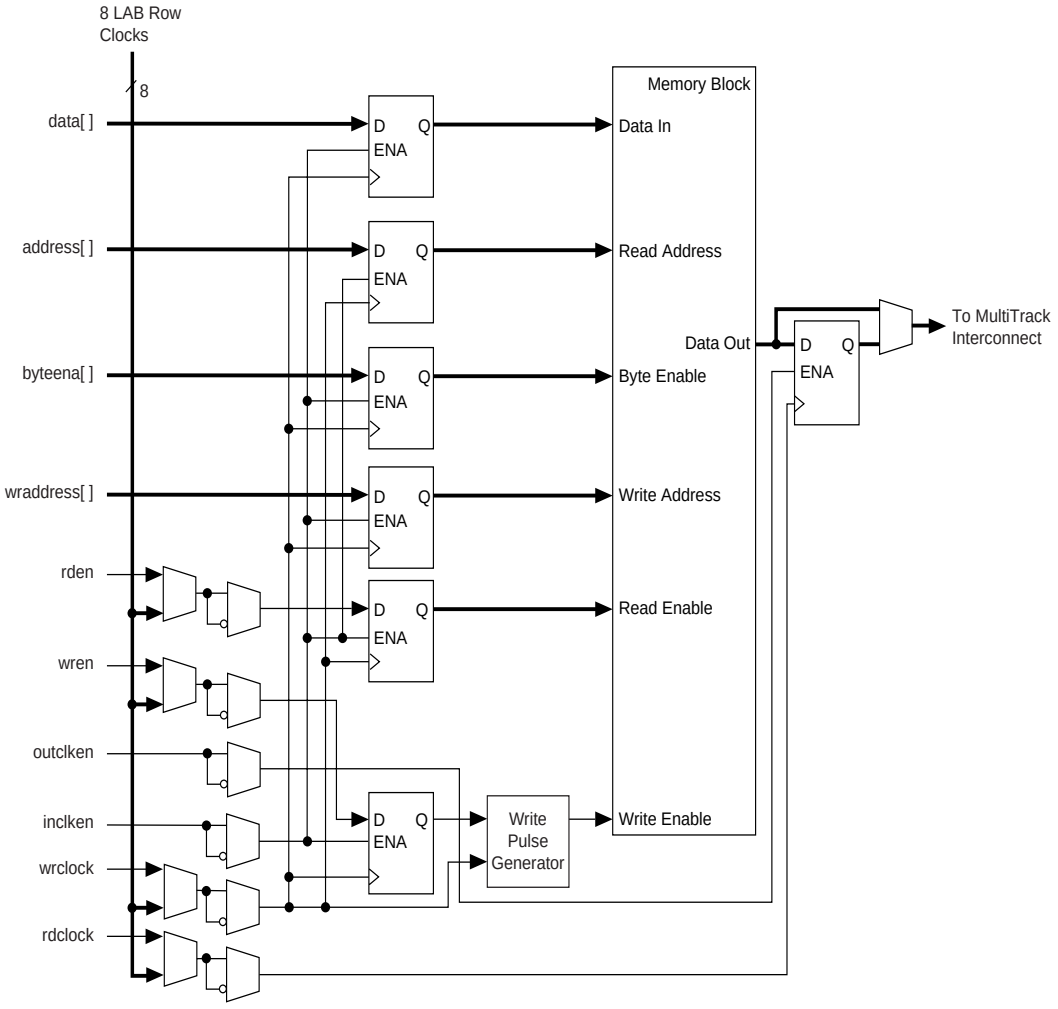
Figure 36. Input/Output Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 36:

(1) All registers shown have asynchronous clear ports.

Figure 37. Input/Output Clock Mode in Simple Dual-Port Mode *Note (1)*



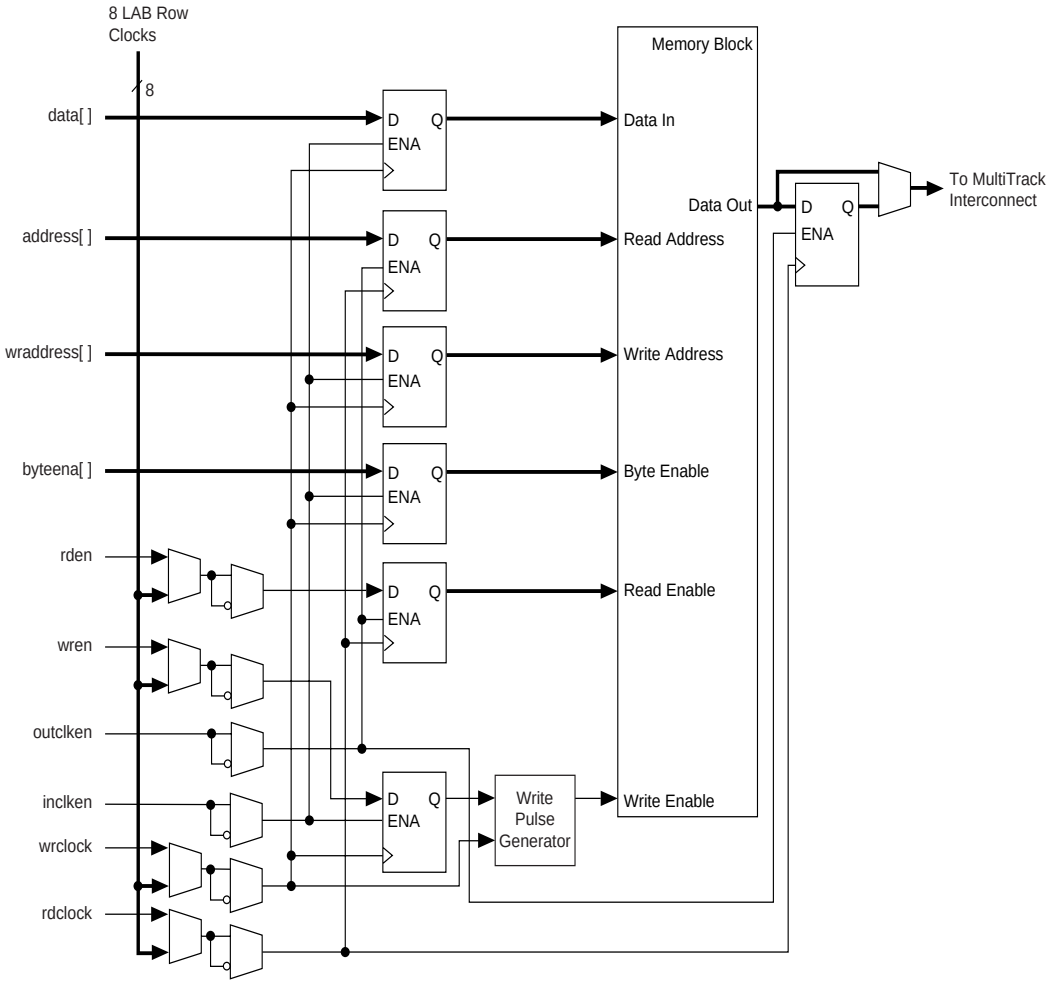
Note to Figure 37:

(1) All registers shown except the `rden` register have asynchronous clear ports.

Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. The designer can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 38 shows a memory block in read/write clock mode.

Figure 38. Read/Write Clock Mode in Simple Dual-Port Mode *Note (1)*

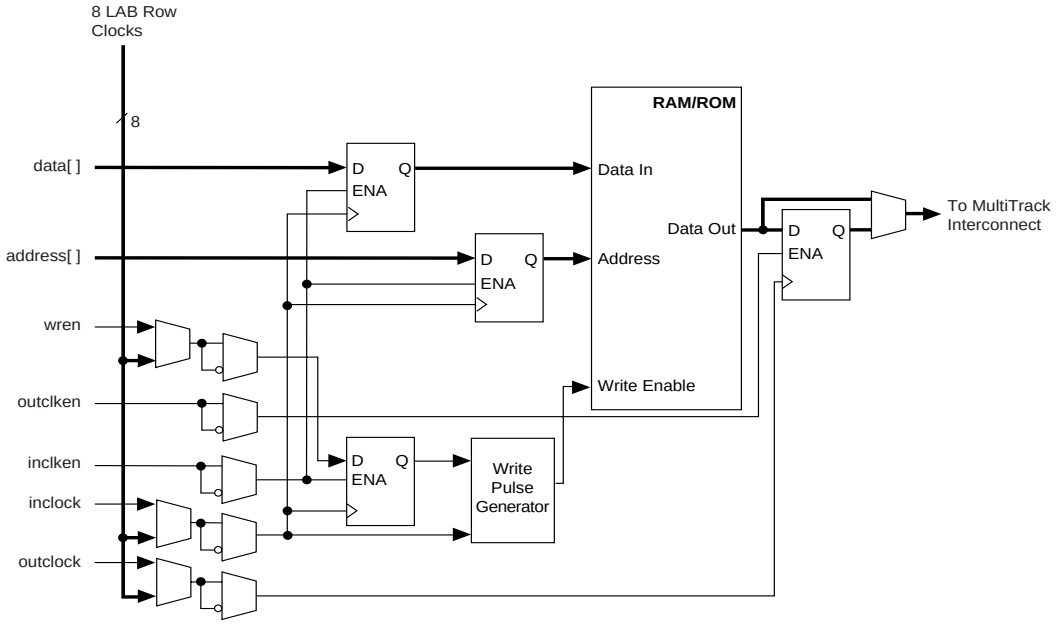


Note to Figure 38:
(1) All registers shown except the `rden` register have asynchronous clear ports.

Single-Port Mode

The memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 39. A single block in a memory block can support up to two single-port mode RAM blocks in the M4K RAM blocks if each RAM block is less than or equal to 2K bits in size.

Figure 39. Single-Port Mode



Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix GX device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix GX devices have more DSP blocks per column (see Table 32). Each DSP block can be configured to support:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

Figure 40 shows one of the columns with surrounding LAB rows.

Figure 40. DSP Blocks Arranged in Columns

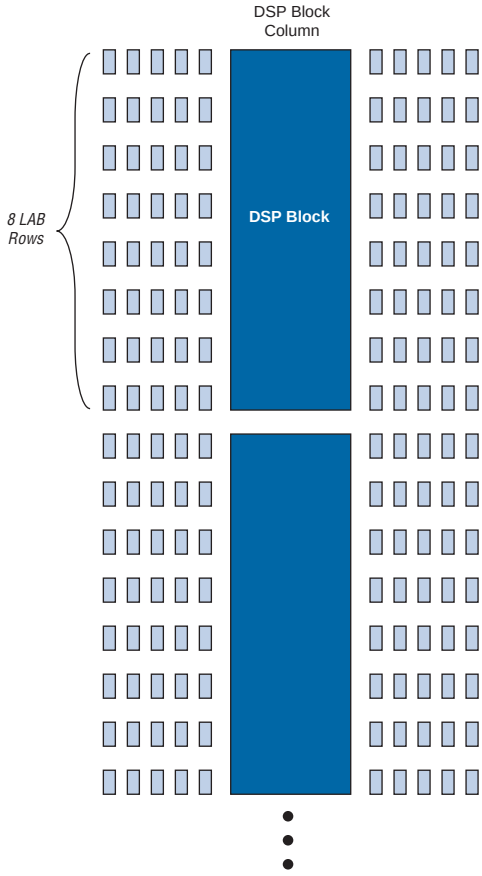


Table 32 shows the number of DSP blocks in each Stratix GX device.

Table 32. DSP Blocks in Stratix GX Devices *Note (1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP1SGX10	6	48	24	6
EP1SGX25	10	80	40	10
EP1SGX40	14	112	56	14

Note to Table 32:

(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

DSP block multipliers can optionally feed an adder/subtractor or accumulator within the block depending on the configuration. This makes routing to LEs easier, saves LE routing resources, and increases performance, because all connections and blocks are within the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications.

Figure 41 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode. Figure 42 shows the 9 × 9-bit multiplier configuration of the DSP block.

Figure 41. DSP Block Diagram for 18 × 18-Bit Configuration

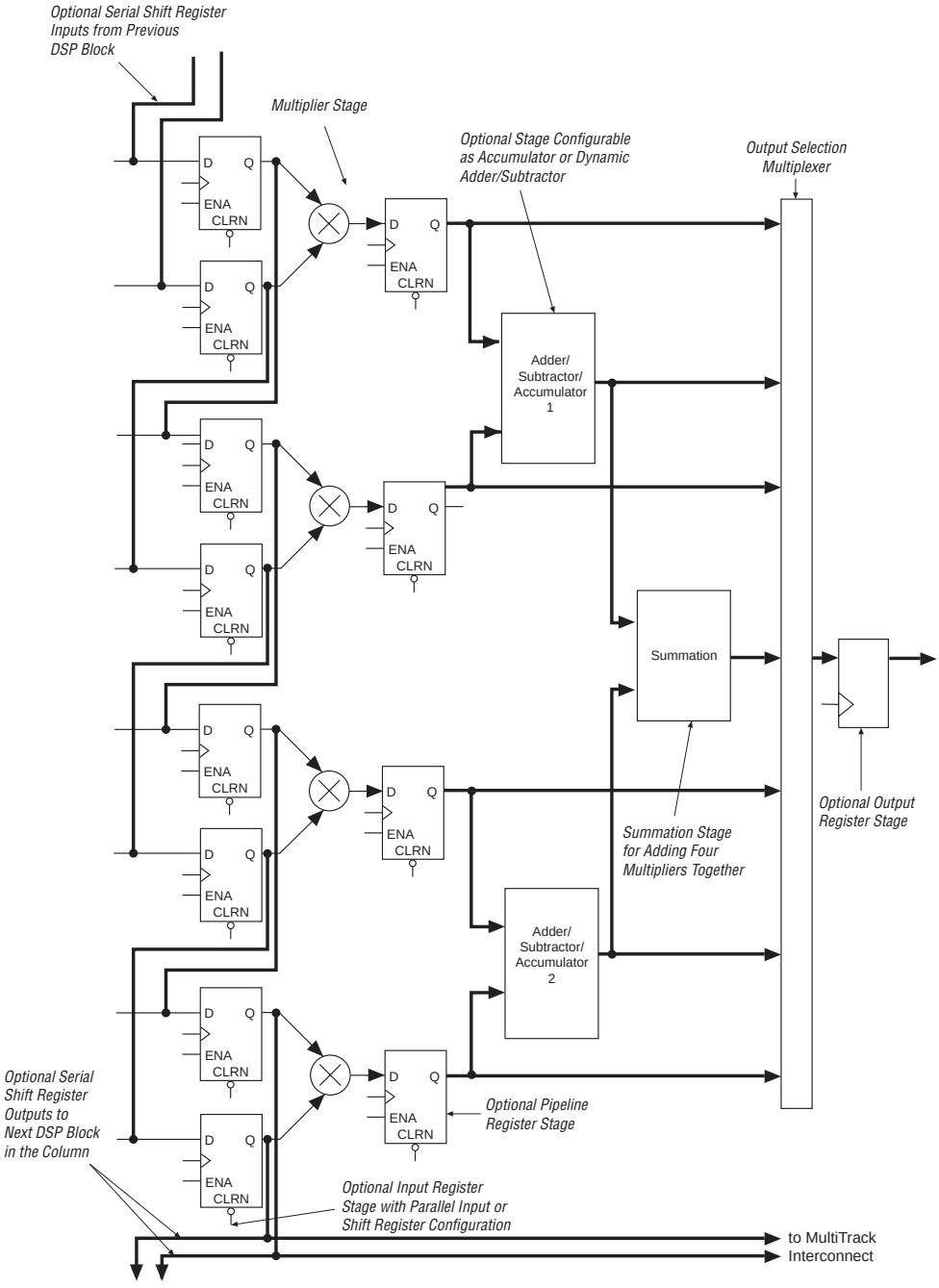
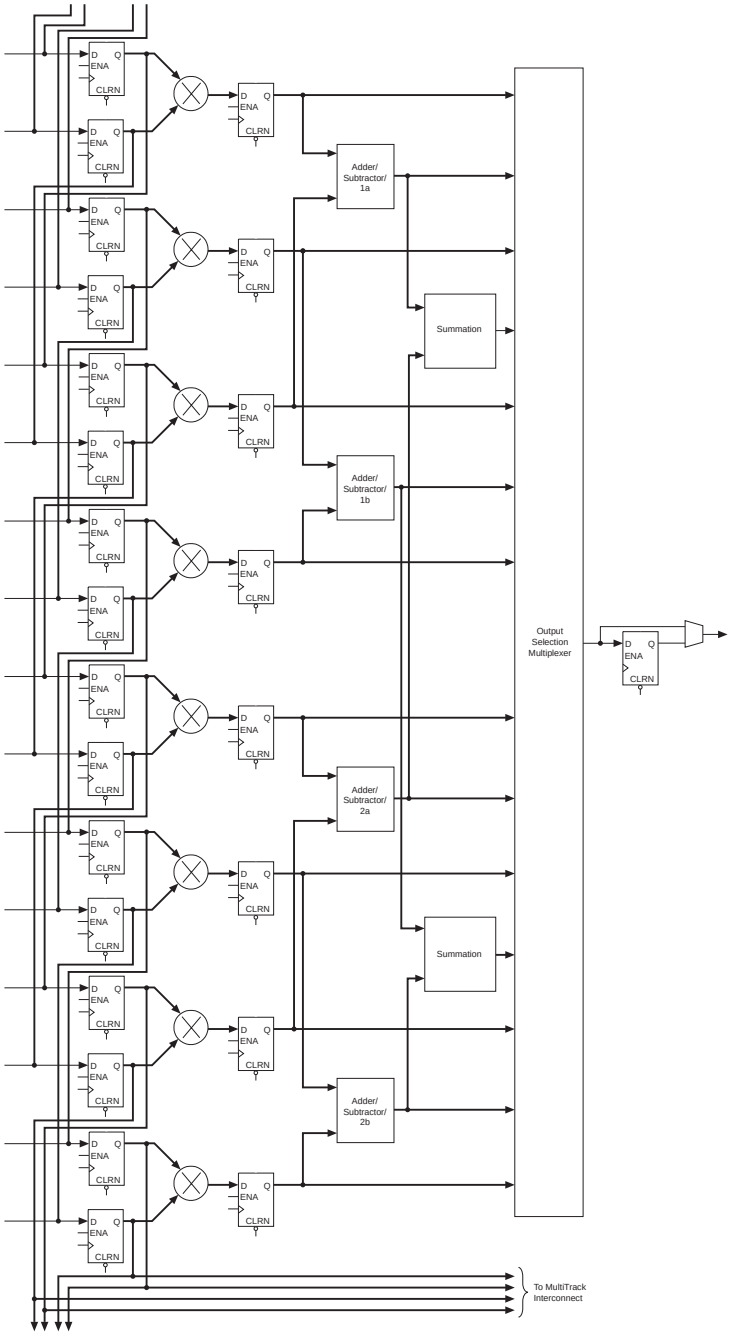


Figure 42. DSP Block Diagram for 9 × 9-Bit Configuration



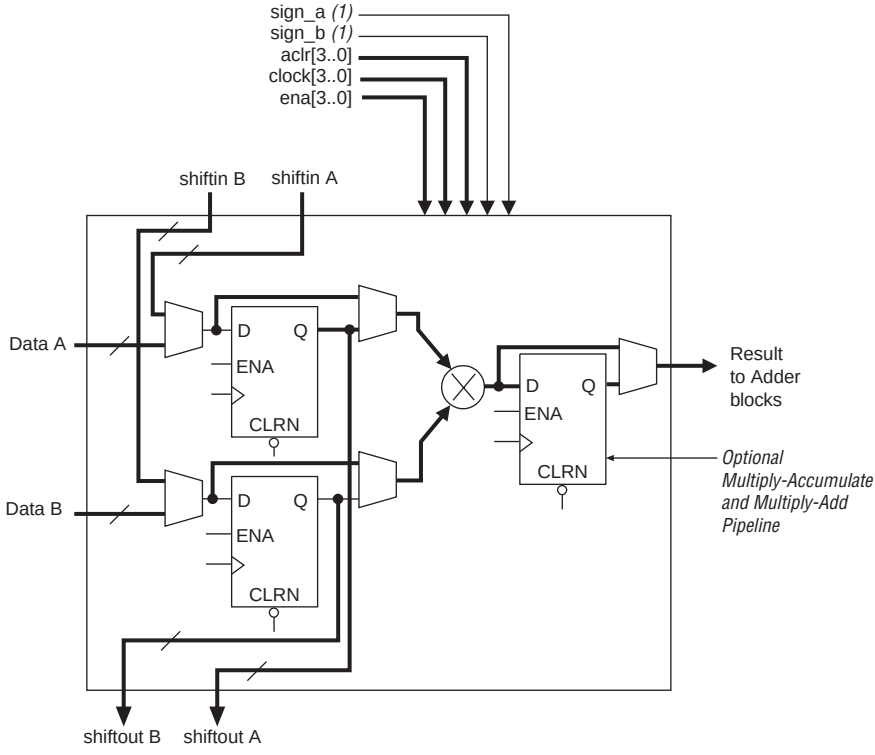
The DSP block consists of the following elements:

- Multiplier block
- Adder/output block

Multiplier Block

The DSP block multiplier block consists of the input registers, a multiplier, and pipeline register for pipelining multiply-accumulate and multiply-add/subtract functions as shown in Figure 43.

Figure 43. Multiplier Sub-Block within Stratix GX DSP Block



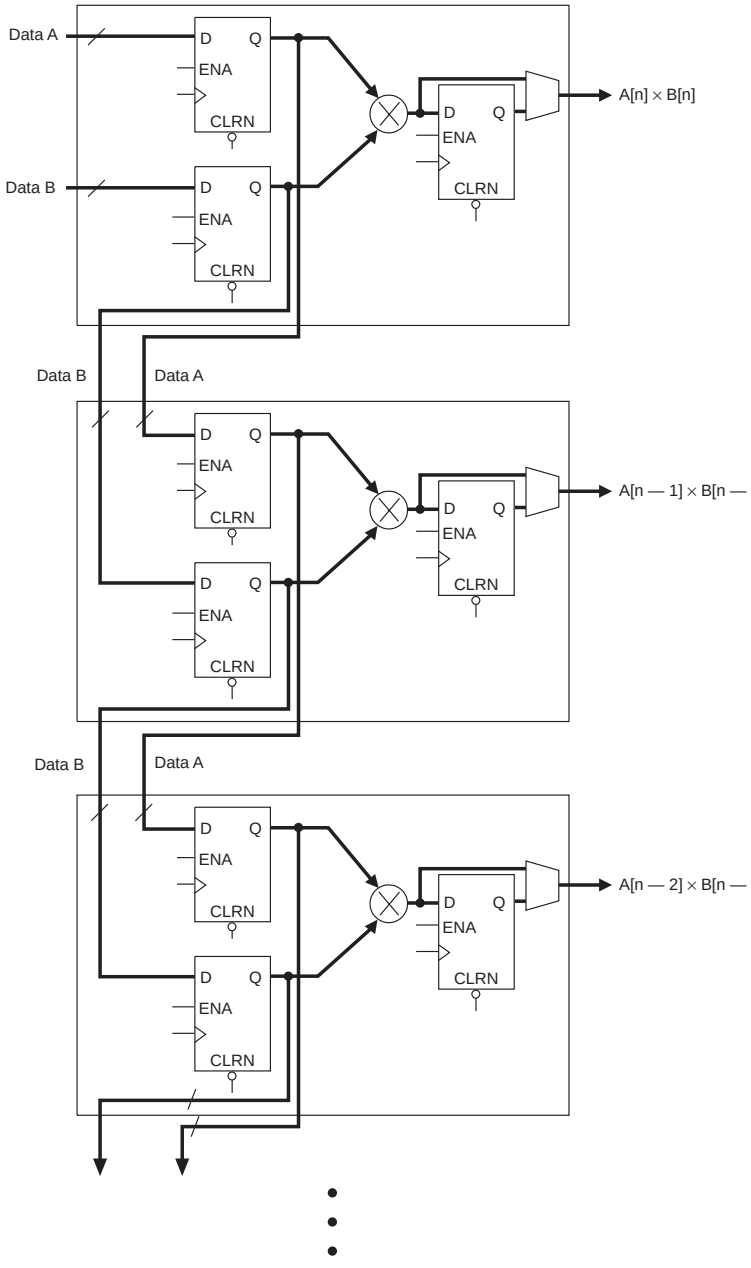
Note to Figure 43:
(1) These signals can be unregistered or registered once to match data path pipelines if required.

Input Registers

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. Designers can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. Designers select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

Designers can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in Figure 44, to form a shift register chain. This chain can terminate in any block, i.e., designers can create any length of shift register chain up to 224 registers. The designer can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9 × 9- and 18 × 18-bit multipliers, the designer does not need to implement external shift registers in LAB LEs. The designer implements all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36 × 36-bit multipliers.

Figure 44. Multiplier Sub-Blocks Using Input Shift Register Connections *Note (1)*



Note to Figure 44:

(1) Either Data A or Data B input can be set to parallel input for constant coefficient multiplication.

Table 33 shows the summary of input register modes for the DSP block.

Table 33. Input Register Modes

Register Input Mode	9 × 9	18 × 18	36 × 36
Parallel input	✓	✓	✓
Shift register input	✓	✓	

Multiplier

The multiplier supports 9 × 9-, 18 × 18-, or 36 × 36-bit multiplication. Each DSP block supports eight possible 9 × 9-bit or smaller multipliers. There are four multiplier blocks available for multipliers larger than 9 × 9 bits but smaller than 18 × 18 bits. There is one multiplier block available for multipliers larger than 18 × 18 bits but smaller than or equal to 36 × 36 bits. The ability to have several small multipliers is useful in applications such as video processing. Large multipliers greater than 18 × 18 bits are useful for applications such as the mantissa multiplication of a single-precision floating-point number.

The multiplier operands can be signed or unsigned numbers, where the result is signed if either input is signed as shown in Table 34. The `sign_a` and `sign_b` signals provide dynamic control of each operand's representation: a logic 1 indicates the operand is a signed number, a logic 0 indicates the operand is an unsigned number. These sign signals affect all multipliers and adders within a single DSP block and designers can register them to match the data path pipeline. The multipliers are full precision (i.e., 18 bits for the 18-bit multiply, 36-bits for the 36-bit multiply, etc.) regardless of whether `sign_a` or `sign_b` set the operands as signed or unsigned numbers.

Table 34. Multiplier Signed Representation

Data A	Data B	Result
Unsigned	Unsigned	Unsigned
Unsigned	Signed	Signed
Signed	Unsigned	Signed
Signed	Signed	Signed

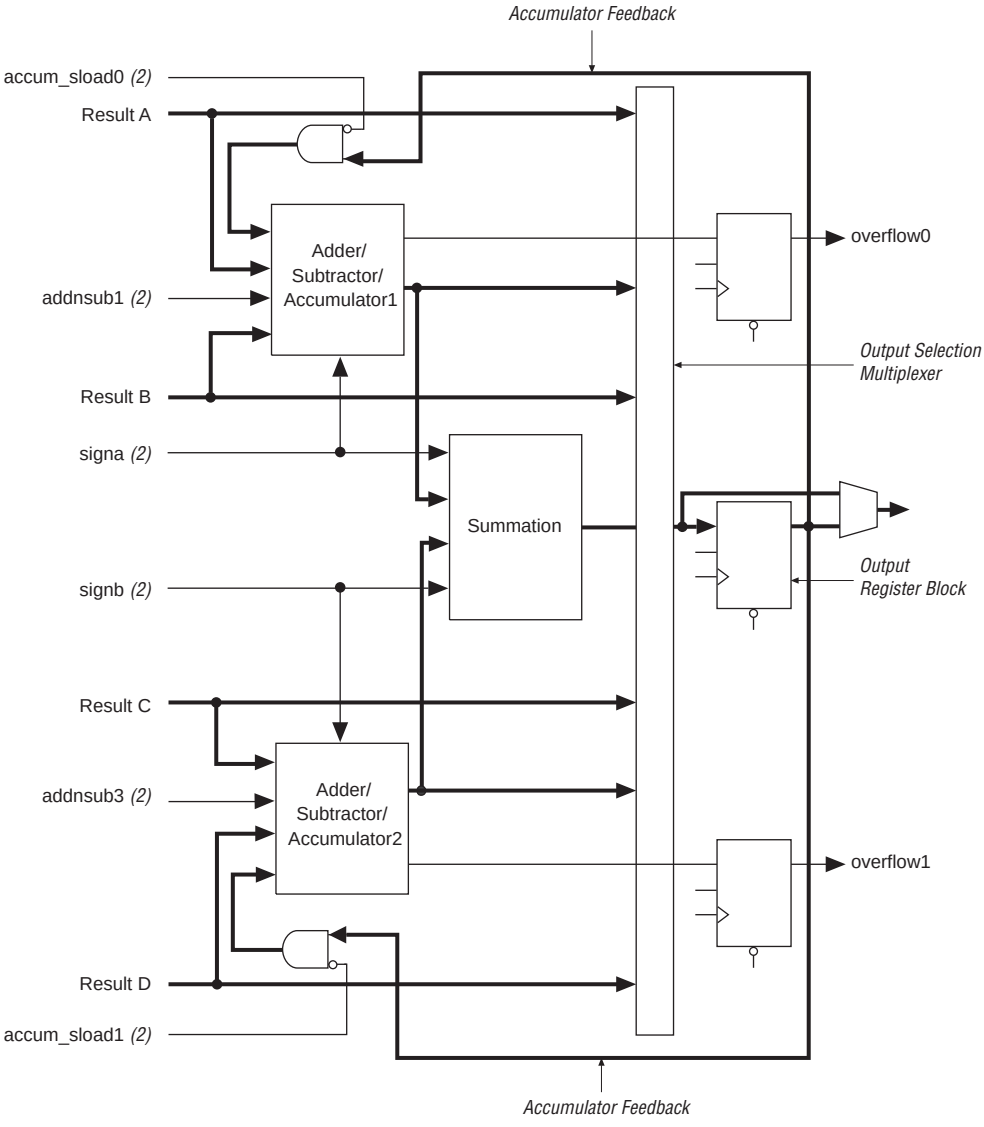
Pipeline/Post Multiply Register

The output of 9 × 9- or 18 × 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 × 36-bit multipliers, this register will pipeline the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. The designer can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 45 shows the adder and output stages.

Figure 45. Adder/Output Blocks *Note (1)*



Notes to Figure 45:

(1) Adder/output block shown in Figure 45 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

Adder/Subtractor/Accumulator

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

Adder/Subtractor

Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 × 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 × 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

Accumulator

When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 45. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

Summation

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 × 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 × 9-bit multipliers. In 18 × 18-bit mode, there is one summation providing the sum of one set of four 18 × 18-bit multipliers.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

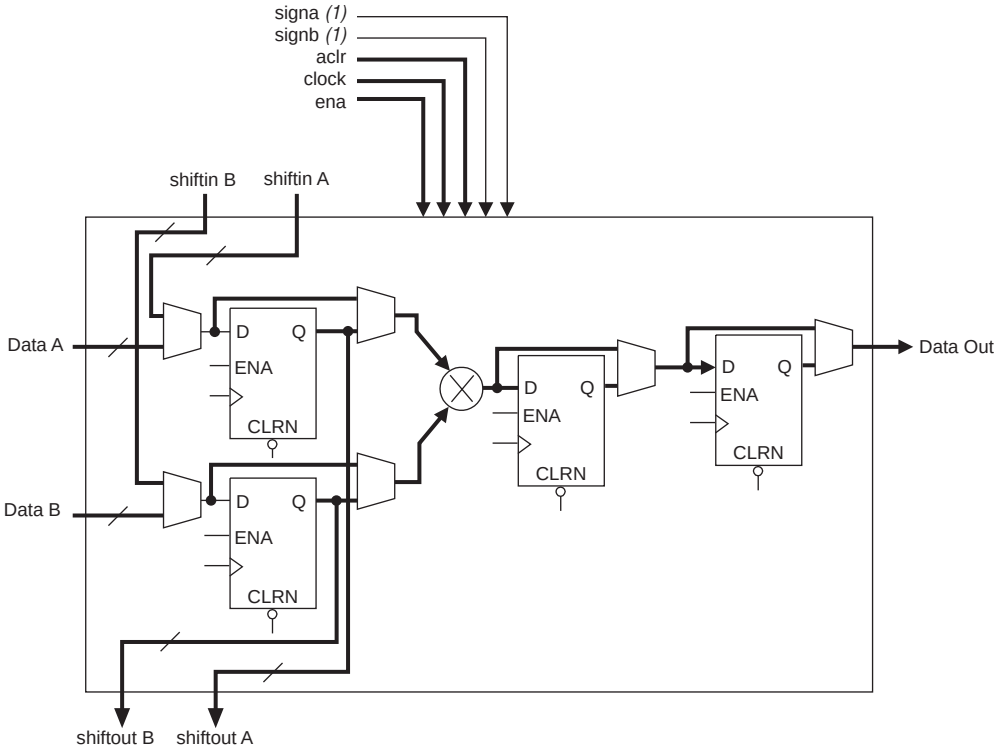
The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Simple Multiplier Mode

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18×18-bit multipliers or eight 9×9-bit multipliers can drive their results directly out of one DSP block. See Figure 46.

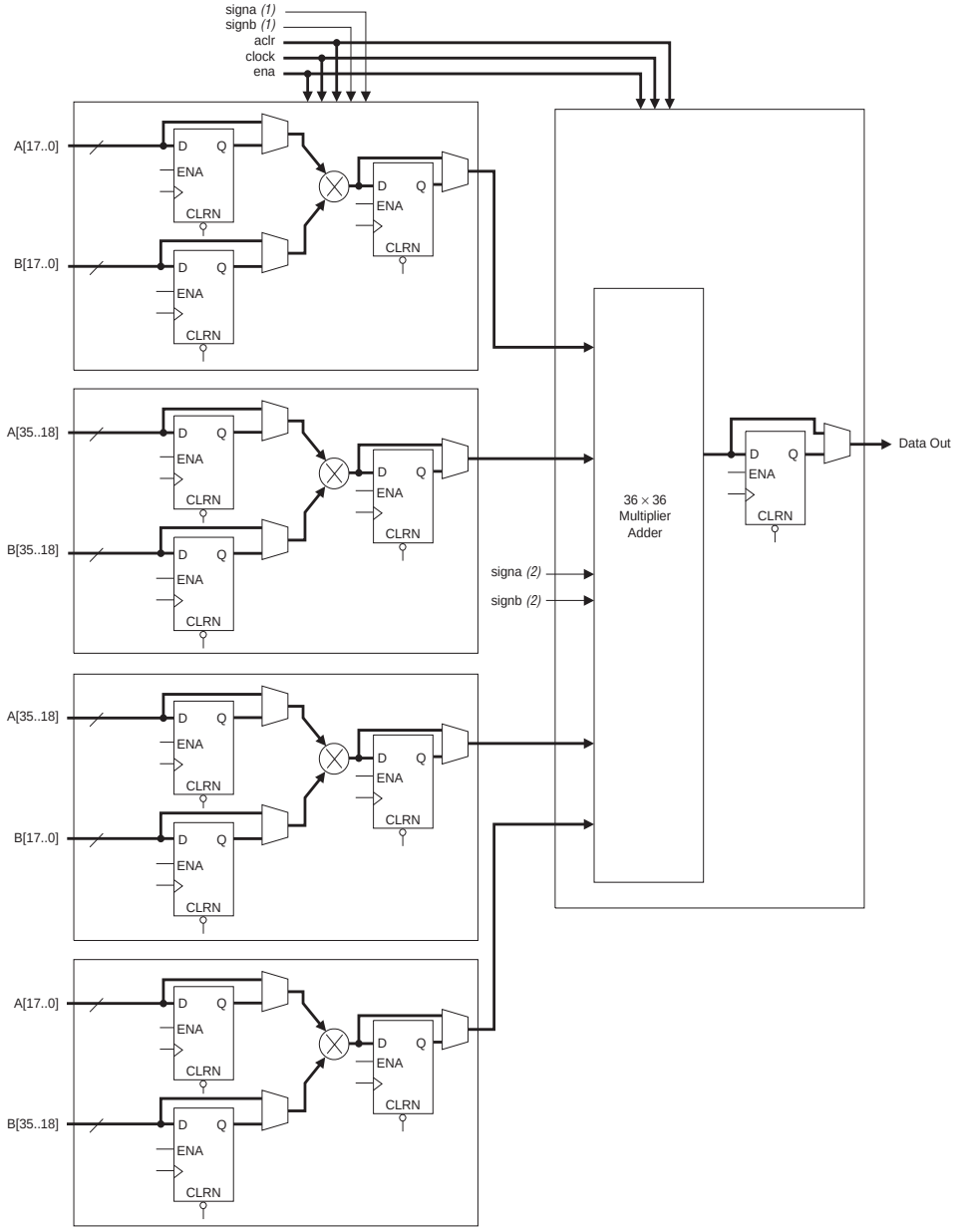
Figure 46. Simple Multiplier Mode



Note to Figure 46:
(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 × 36-bit multiplier in multiplier mode. DSP blocks use four 18 × 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 × 36-bit multiplier. In 36 × 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 × 36-bit multiplier. Figure 47 shows the 36 × 36-bit multiply mode.

Figure 47. 36 × 36 Multiply Mode



Notes to Figure 47:

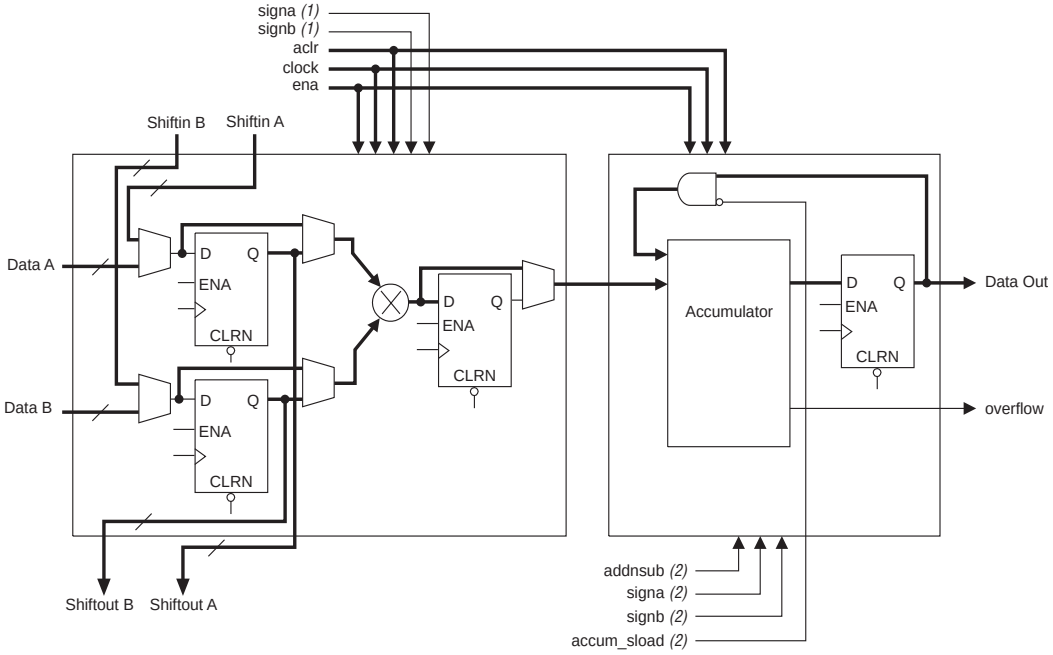
(1) These signals are not registered or registered once to match the pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

Multiply-Accumulator Mode

In multiply-accumulator mode (see Figure 48), the DSP block drives multiplied results to the adder/subtractor/accumulator block configured as an accumulator. A designer can implement one or two multiply-accumulators up to 18 × 18 bits in one DSP block. The first and third multiplier sub-blocks are unused in this mode, since only one multiplier can feed one of two accumulators. The multiply-accumulator output can be up to 52 bits—a maximum of a 36-bit result with 16 bits of accumulation. The `accum_sload` and `overflow` signals are only available in this mode. The `addnsub` signal can set the accumulator for decimation and the `overflow` signal will indicate underflow condition.

Figure 48. Multiply-Accumulate Mode



Notes to Figure 48:
(1) These signals are not registered or registered once to match the data path pipeline.
(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Two-Multipliers Adder Mode

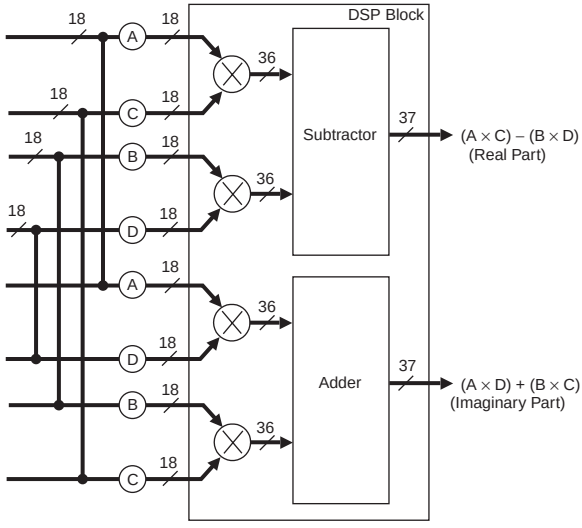
The two-multipliers adder mode uses the adder/subtractor/accumulator block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. A single DSP block can implement two sums or differences from two 18 × 18-bit multipliers each or four sums or differences from two 9 × 9-bit multipliers each.

Designers can use the two-multipliers adder mode for complex multiplications, which are written as:

$$(a + jb) \times (c + jd) = [(a \times c) - (b \times d)] + j \times [(a \times d) + (b \times c)]$$

The two-multipliers adder mode allows a single DSP block to calculate the real part $[(a \times c) - (b \times d)]$ using one subtractor and the imaginary part $[(a \times d) + (b \times c)]$ using one adder, for data widths up to 18 bits. Two complex multiplications are possible for data widths up to 9 bits using four adder/subtractor/accumulator blocks. Figure 49 shows an 18-bit two-multipliers adder.

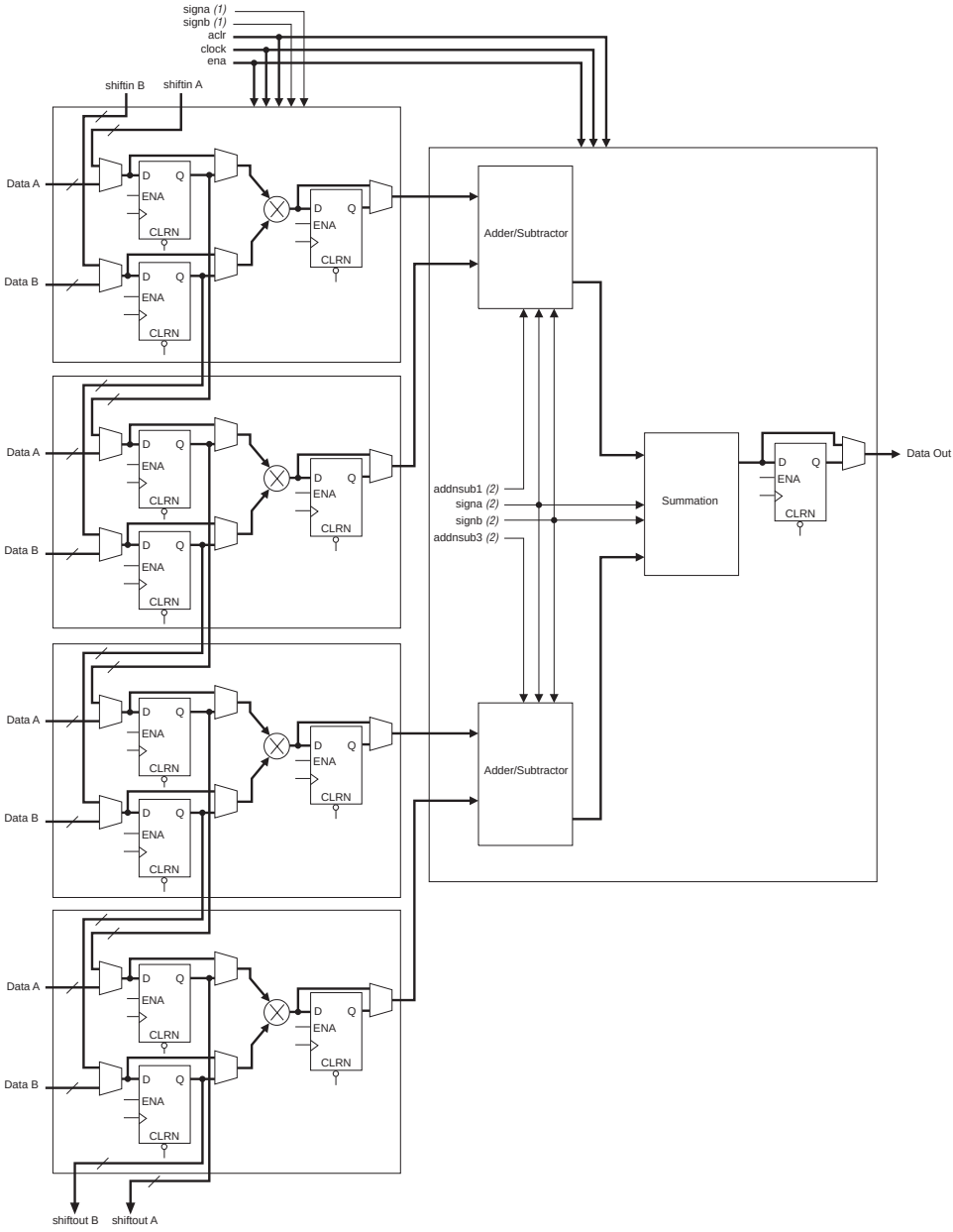
Figure 49. Two-Multipliers Adder Mode Implementing Complex Multiply



Four-Multipliers Adder Mode

In the four-multipliers adder mode, the DSP block adds the results of two first -stage adder/subtractor blocks. One sum of four 18 × 18-bit multipliers or two different sums of two sets of four 9 × 9-bit multipliers can be implemented in a single DSP block. The product width for each multiplier must be the same size. The four-multipliers adder mode is useful for FIR filter applications. Figure 50 shows the four multipliers adder mode.

Figure 50. Four-Multipliers Adder Mode



Notes to Figure 50:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (i.e., implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 35 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 35. Multiplier Size & Configurations per DSP block

DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

DSP Block Interface

Stratix GX device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. The designer can cascade DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

The DSP block is divided into eight block units that interface with eight LAB rows on the left and right. Each block unit can be considered half of an 18 × 18-bit multiplier sub-block with 18 inputs and 18 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 10 direct link interconnects from the LAB to the left or right of the DSP block in the same row. All row and column routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Nine outputs from the DSP block can drive to the left LAB through direct link interconnects and nine can drive to the right LAB though direct link interconnects. All 18 outputs can drive to all types of row and column routing. Outputs can drive right- or left-column routing. Figures 51 and 52 show the DSP block interfaces to LAB rows.

Figure 51. DSP Block Interconnect Interface

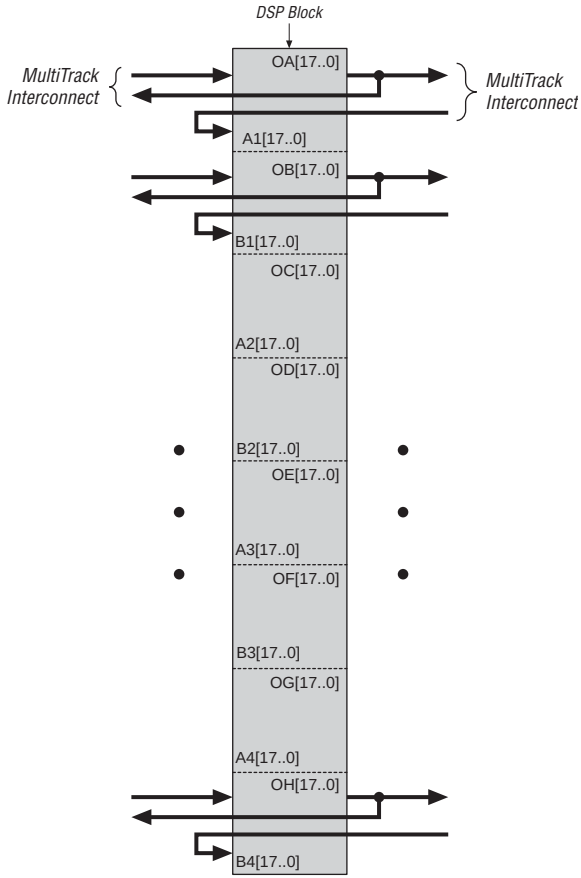
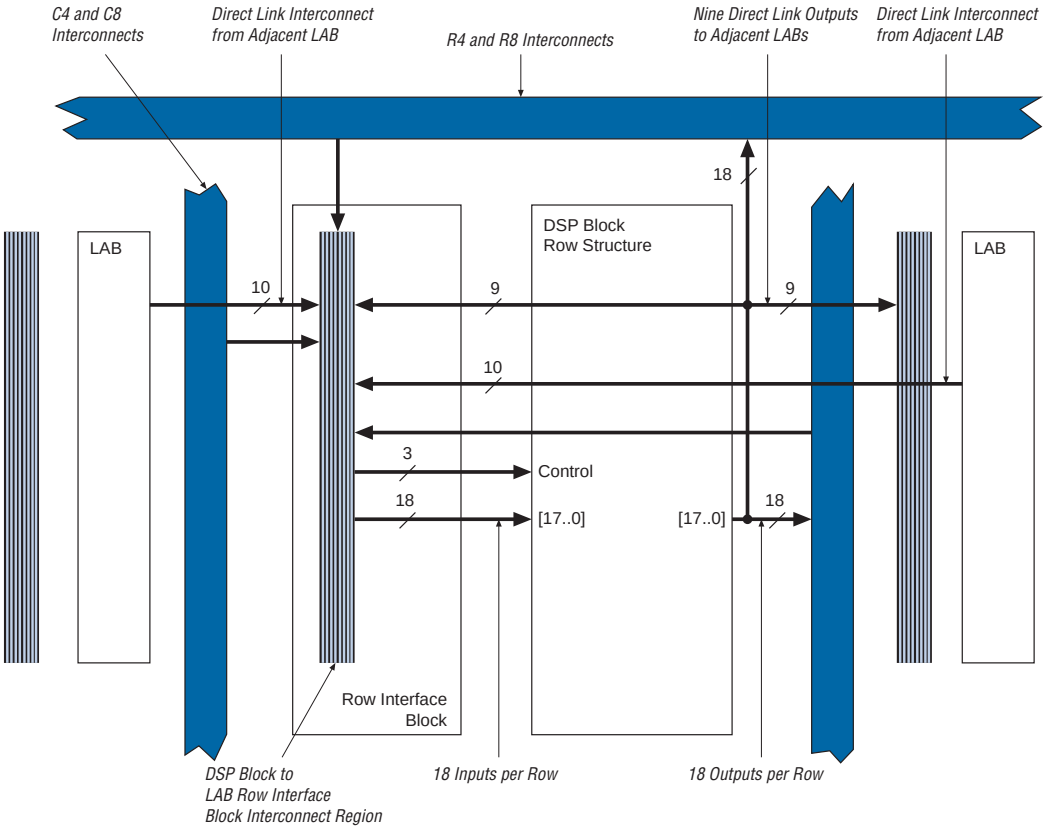


Figure 52. DSP Block Interface to Interconnect



A bus of 18 control signals feeds the entire DSP block. These signals include clock[0..3] clocks, aclr[0..3] asynchronous clears, ena[1..4] clock enables, signa, signb signed/unsigned control signals, addnsub1 and addnsub3 addition and subtraction control signals, and accum_sload[0..1] accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 36.

Table 36. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
1	signa	A1[17..0]	OA[17..0]
2	aclr0 accum_sload0	B1[17..0]	OB[17..0]
3	addnsub1 clock0 ena0	A2[17..0]	OC[17..0]
4	aclr1 clock1 ena1	B2[17..0]	OD[17..0]
5	aclr2 clock2 ena2	A3[17..0]	OE[17..0]
6	sign_b clock3 ena3	B3[17..0]	OF[17..0]
7	clear3 accum_sload1	A4[17..0]	OG[17..0]
8	addnsub3	B4[17..0]	OH[17..0]

PLLs & Clock Networks

Stratix GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution. Stratix GX devices contain up to four enhanced PLLs and up to four fast PLLs.

Global & Hierarchical Clocking

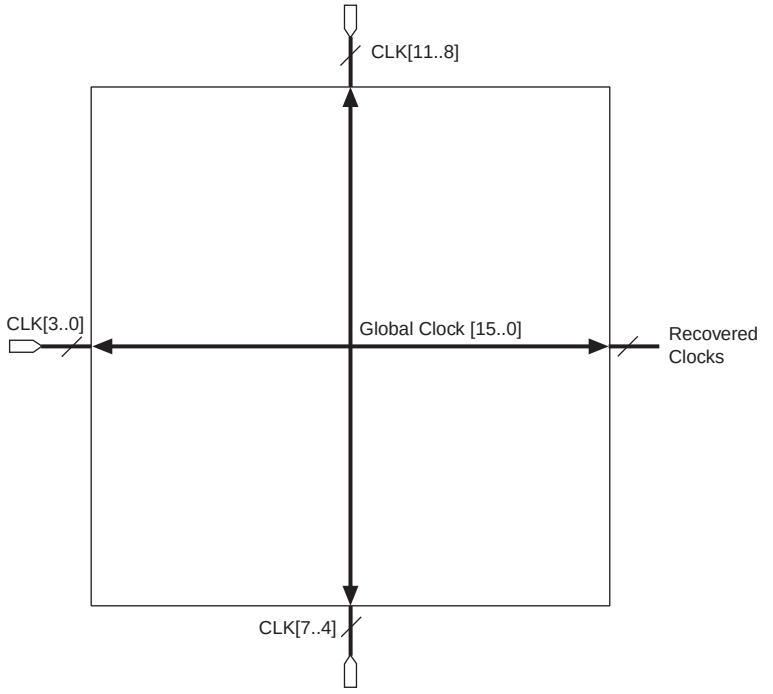
Stratix GX devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks. These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix GX devices.

There are 12 dedicated clock pins (`CLK[11..0]`) to drive either the global or regional clock networks. Three clock pins drive the top, bottom, and left side of the device. Enhanced and fast PLL outputs as well as an I/O interface can also drive these global and regional clock networks. The recovered clocks from the transceiver blocks drive the additional global clock networks (`CLK[15..12]`), as shown in Figures 53 and 54.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device—IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 53 shows the 12 dedicated `CLK` pins and the recovered clock driving global clock networks.

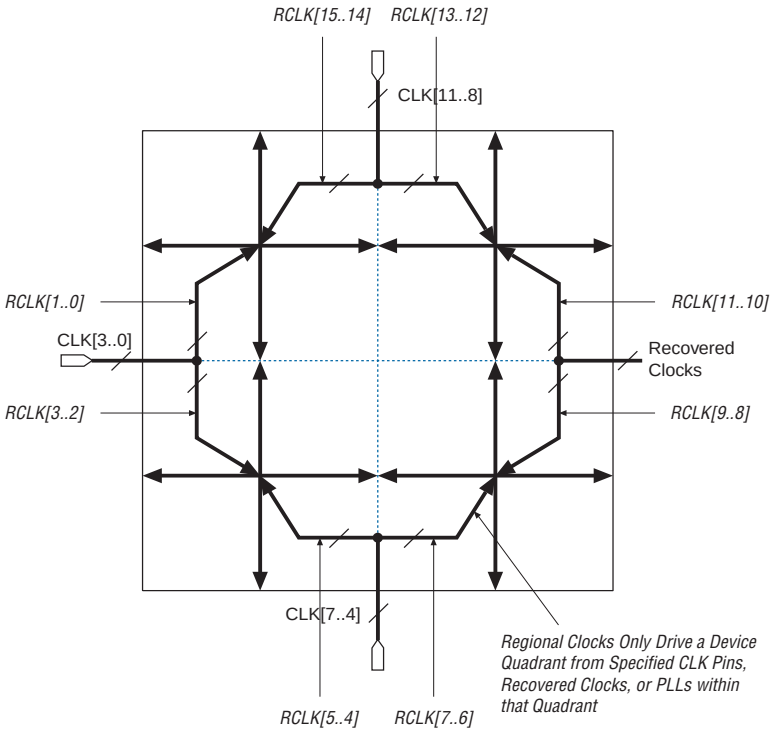
Figure 53. Global Clock Resources



Regional Clock Network

There are four regional clock networks RCLK[3..0] within each quadrant of the Stratix GX device that are driven by the same dedicated CLK[11..0] input pins, PLL outputs, or recovered clocks from the transceiver blocks. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. The CLK clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 54.

Figure 54. Regional Clocks



Fast Regional Clock Network

In EP1SGX25 and EP1SGX10 devices, there are two fast regional clock networks, FCLK[1..0], within each quadrant, fed by input pins to fast regional clock networks that can connect to fast regional clock networks (see Figure 55). In EP1SGX40 devices, there are two fast regional clock networks within each half-quadrant (see Figure 56). The FCLK[1..0] clocks can also be used for high fanout control signals, such as asynchronous clears, presets, clock enables, or protocol control signals such as TRDY and IRDY for PCI. Dual-purpose FCLK pins drive the fast clock networks. All devices have eight FCLK pins to drive fast regional clock networks. Any I/O pin can drive a clock or control signal onto any fast regional clock network with the addition of a delay. The I/O interconnect drives this signal.

Figure 55. EP1SGX25 & EP1SGX10 Device Fast Clock Pin Connections to Fast Regional Clocks

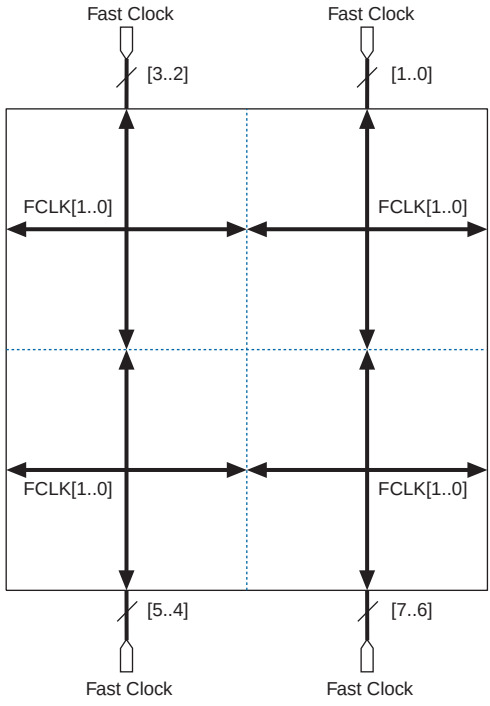
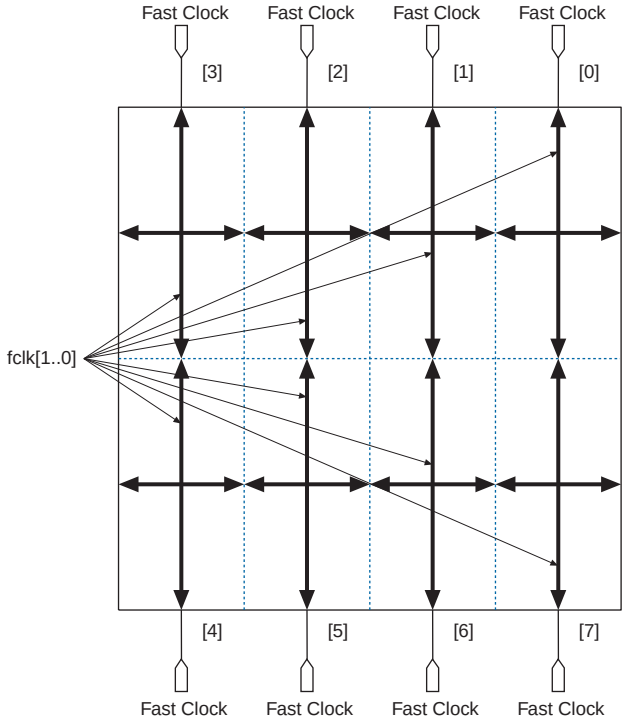


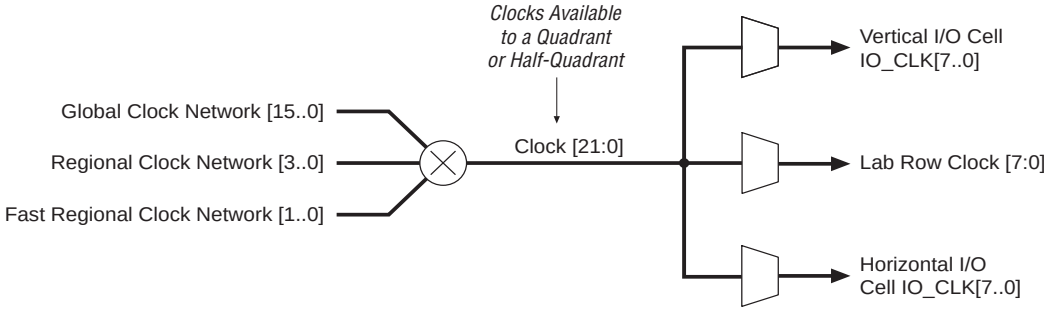
Figure 56. A-5 Device Fast Regional Clock Pin Connections to Fast Regional Clocks



Combined Resources

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, four regional clock lines, and two fast regional clock lines. Multiplexers are used with these clocks to form eight bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select two of the eight row clocks to feed the LE registers within the LAB. See Figure 57.

Figure 57. Regional Clock Bus



IOE clocks have horizontal and vertical block regions that are clocked by eight I/O clock signals chosen from the 22 quadrant or half-quadrant clock resources. Figures 58 and 59 show the quadrant and half-quadrant relationship to the I/O clock regions, respectively. The vertical regions (column pins) have less clock delay than the horizontal regions (row pins).

Figure 58. EP1SGX25 & EP1SGX10 Device I/O Clock Groups

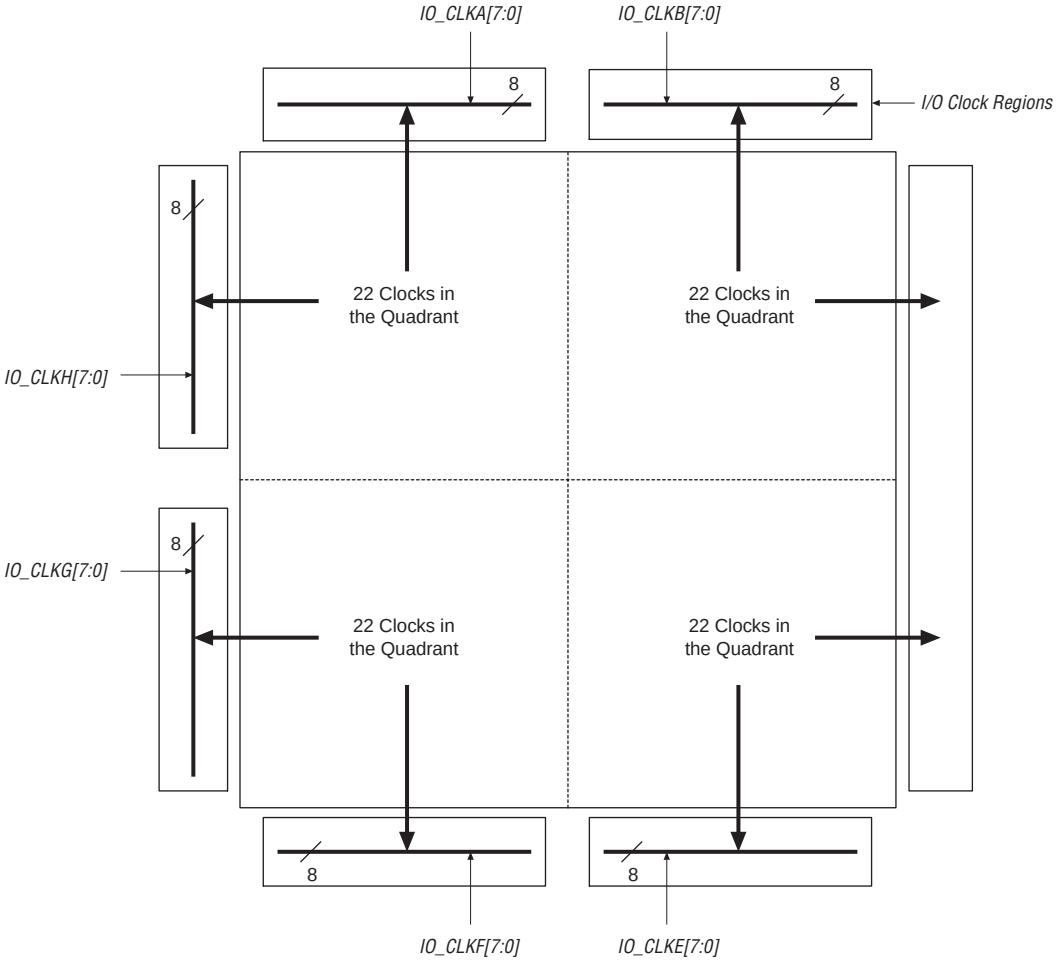
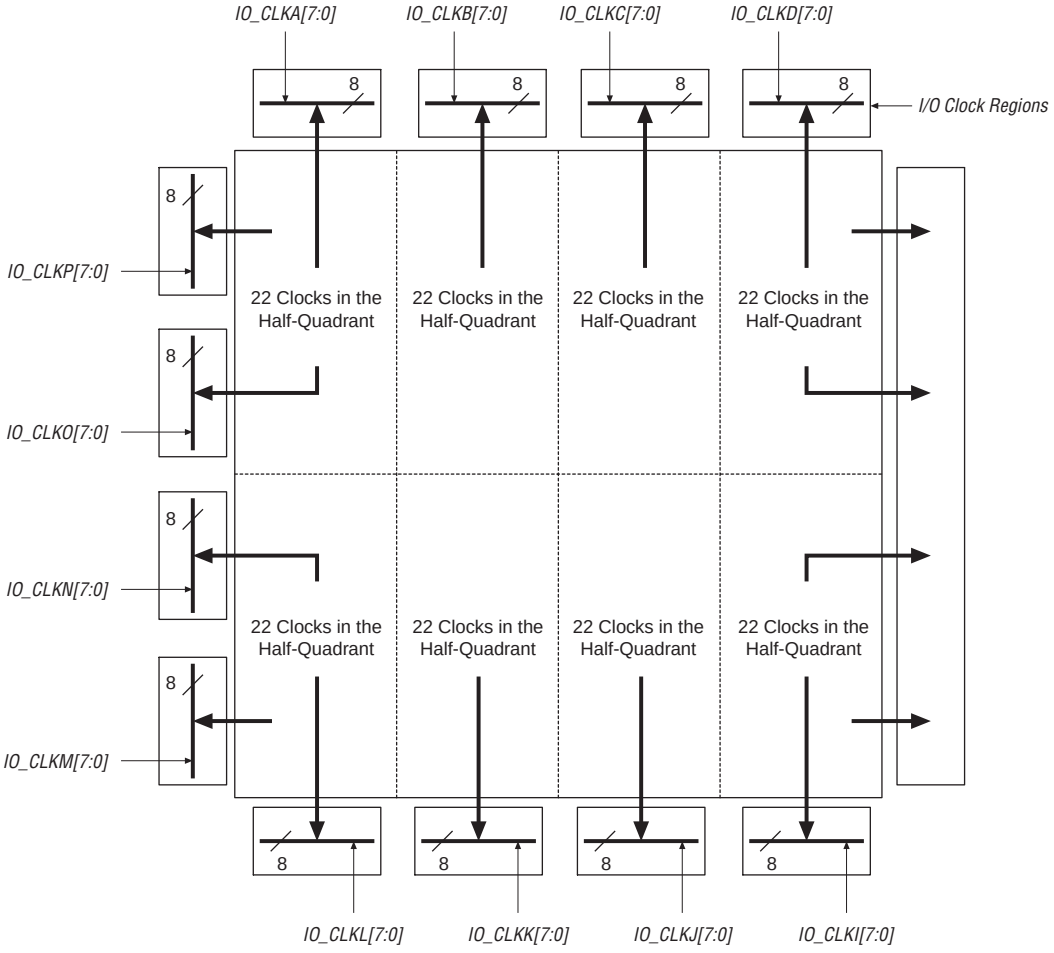


Figure 59. EP1SGX40 Device I/O Clock Groups



Designers can use the Quartus II software to control whether a clock input pin is either global, regional, or fast regional. The Quartus II software automatically selects the clocking resources if not specified.

Enhanced & Fast PLLs

Stratix GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. Stratix GX devices also have up to four additional PLLs that are used for CDR (for more information on these additional PLLs, see "Transceiver Blocks" on page 8). These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread spectrum clocking, programmable bandwidth, phase and delay control, and PLL reconfiguration, the Stratix GX device's enhanced PLLs provide designers with complete control of their clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 37 shows which PLLs are available for each Stratix GX device and their type. Table 38 shows the enhanced PLL and fast PLL features in Stratix GX devices.

Table 37. Stratix GX Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3 *(1)*	4 *(1)*	7	8	9 *(1)*	10 *(1)*	5 *(2)*	6 *(2)*	11 *(3)*	12 *(3)*
EP1SGX10	✓	✓							✓	✓		
EP1SGX25	✓	✓							✓	✓		
EP1SGX40	✓	✓			✓	✓			✓	✓	✓	✓

Notes to Table 37:

(1) PLLs 3, 4, 9, and 10 are not available in Stratix GX devices. However, these PLLs are listed in Table 37 because the Stratix GX PLL numbering scheme is consistent with Stratix devices.
(2) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.
(3) PLLs 11 and 12 each have one single-ended output.

Table 38. Stratix GX PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(post-scale counter) *(2)*
Phase shift	Down to 160-ps increments *(3)*, *(4)*	Down to 150-ps increments*(3)*, *(4)*
Delay shift	250-ps increments for ±3 ns	
Clock switchover	✓	
PLL reconfiguration	✓	
Programmable bandwidth	✓	
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	3 *(5)*
Number of external clock outputs	Four differential/eight singled-ended or one single-ended *(6)*	*(7)*
Number of feedback clock inputs	4 *(8)*	

Notes to Table 38:

(1) For enhanced PLLs, *m* and *n* are counters ranging from 1 to 512.
(2) For fast PLLs, *m* and post-scale counters range from 1 to 16.
(3) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix GX devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) PLLs 7 and 8 have two output ports per PLL. PLLs 1 and 2 have three output ports per PLL.
(6) Every Stratix GX device has two enhanced PLLs with eight single-ended or four differential outputs each. Two additional enhanced PLLs in EP1SGX40 devices each have one single-ended output.
(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(8) Every Stratix GX device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 60 shows a top-level diagram of the Stratix GX device and the PLL floorplan.

Figure 60. PLL Locations

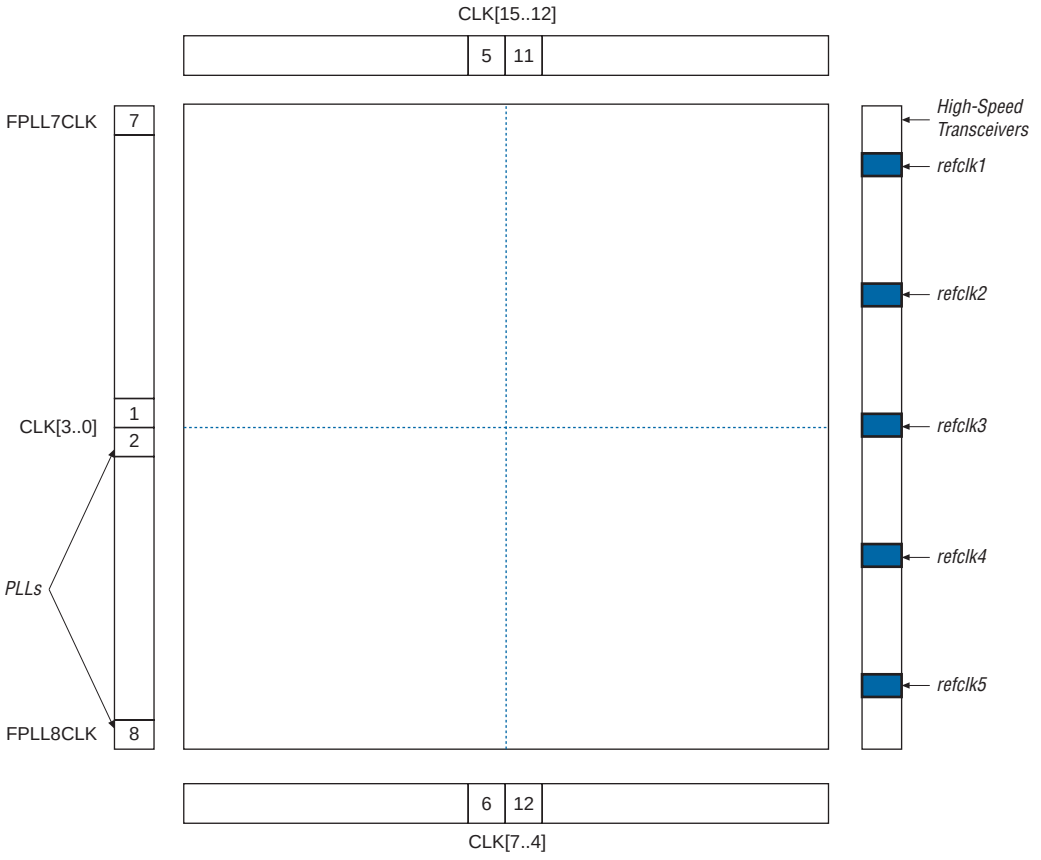
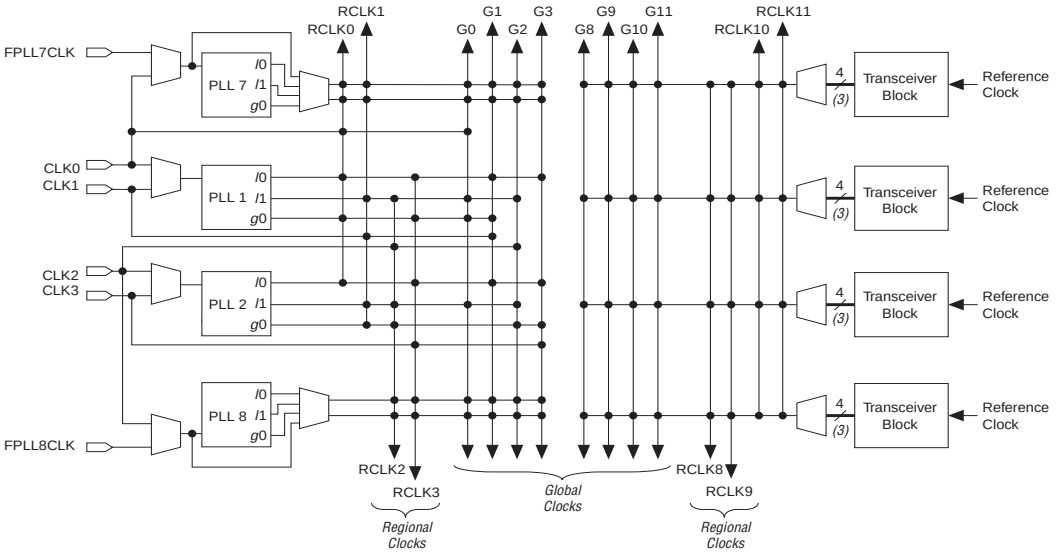


Figure 61 shows the global and regional clock connections from the PLL outputs and the CLK pins.

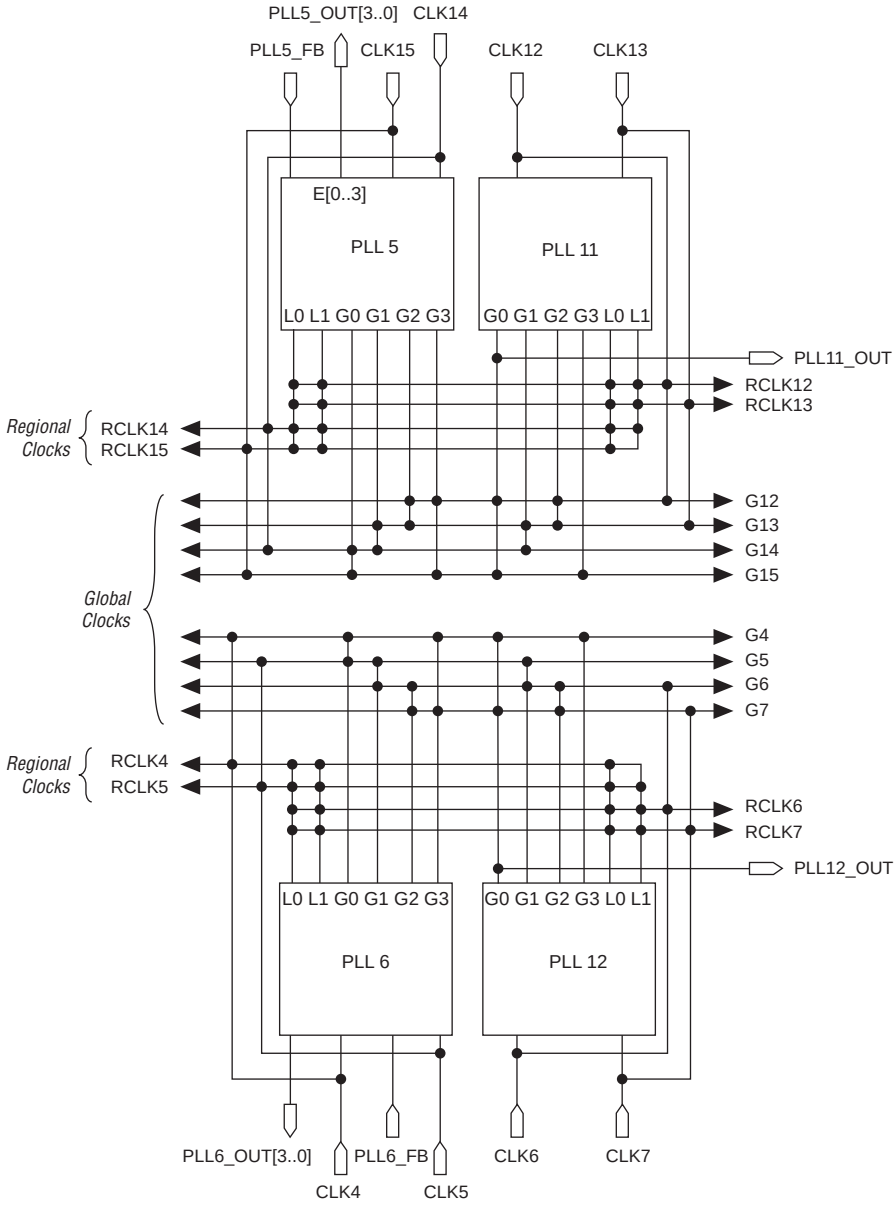
Figure 61. Global & Regional Clock Connections from Side Pins & Fast PLL Outputs (EP1SGX40 Device)
Notes (1), (2)



Notes to Figure 61:
(1) PLLs 1,2 7, and 8 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs. PLLs 7 and 8 do not drive global clocks.
(2) In EP1SGX40 devices that have five transceiver blocks, only four transceiver blocks can drive the global and local clock networks.
(3) The high-speed serial data stream in each transceiver block generates the recovered clocks. Each transceiver block has four recovered clocks from the four transceiver channels. One of the four clocks drive the global and local clock networks.

Figure 62 shows the global and regional clocking from enhanced PLL outputs and top CLK pins.

Figure 62. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs *Note (1)*



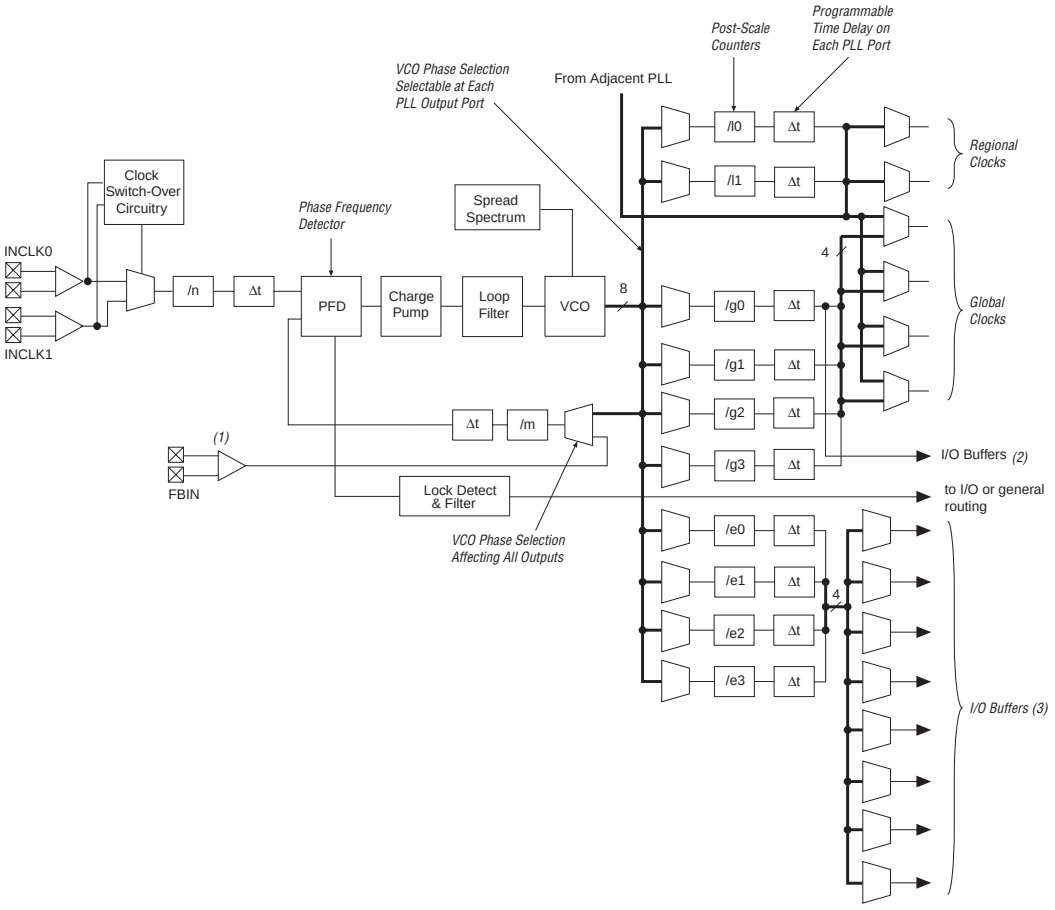
Note to Figure 62:

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs (these PLLs are not shown in Figure 62). PLLs 5, 6, 11, and 12 are enhanced PLLs.

Enhanced PLLs

Stratix GX devices contain up to four enhanced PLLs with advanced clock management features. Figure 63 shows a diagram of the enhanced PLL.

Figure 63. Stratix GX Enhanced PLL



Notes to Figure 63:

(1) External feedback is available in PLLs 5 and 6.
(2) This external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.

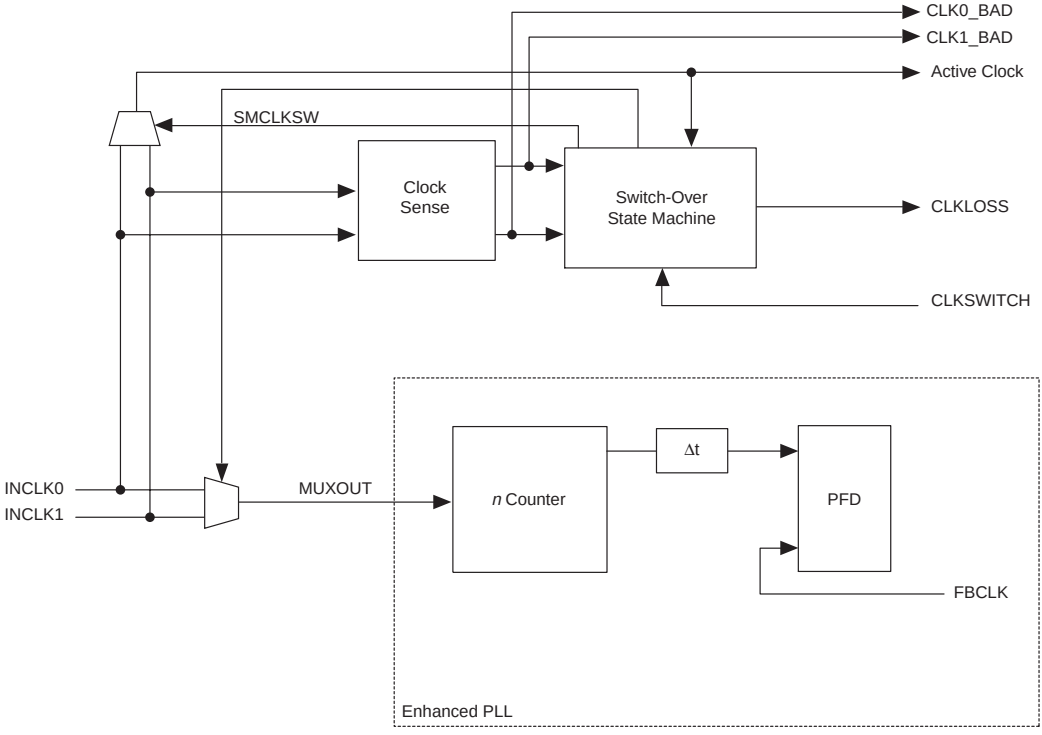
Clock Multiplication & Division

Each Stratix GX device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \times (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale divider, n, and one multiply divider, m, per PLL, with a range of 1 to 512 on each. There are two post-scale dividers (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 512. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix GX device enhanced PLLs support a flexible clock switchover capability. Figure 64 shows a block diagram of the switchover circuit. The switchover circuit is configurable, so the designer can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

Figure 64. Clock Switchover Circuitry



Note to Figure 64:
(1) PFD: phase frequency detector.

There are at least three possible ways to use the clock switch-over feature.

- Designers can use the switch-over circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 64. In this case, the secondary clock becomes the reference clock for the PLL.

- Designers can use the `extswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `extclk0` is 66 MHz and `extclk1` is 100 MHz, the designer must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation.

- If the PLL loses lock for some reason, designers can set the gated lock to control switchover. The gated lock signal goes low to force the switch-over state machine to switch to the secondary clock. If an external PLL is driving the Stratix GX device PLL, excessive jitter on the clock input could cause the PLL to lose lock. Since the switch-over circuit still senses clock edges, it might not sense a switch condition. In this case, the designer can control switchover using the gated version of the locked signal based on the loss of the primary clock.

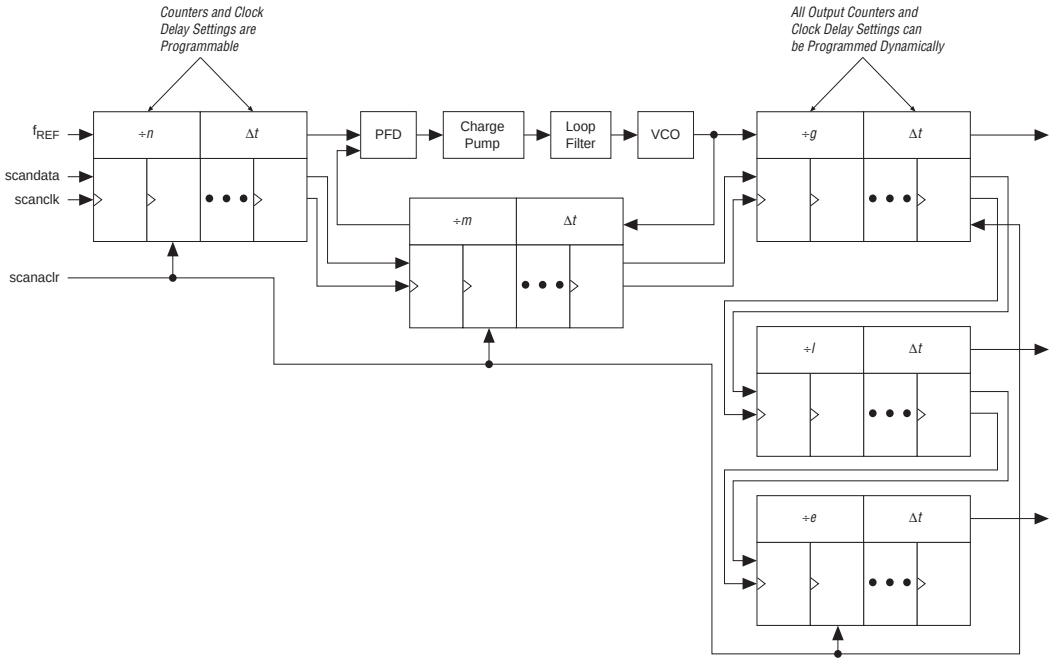
During switch over, the PLL VCO continues to run and will slow down, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The preliminary specification for the maximum time to relock is 100 µs.

PLL Reconfiguration

The PLL reconfiguration feature enables system logic to change Stratix GX device enhanced PLL counters and delay elements without reloading a Programmer Object File (**.pof**). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. The designer can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or t_{CO} delays in end systems.

Clock delay elements at each PLL output port implement variable delay. Figure 65 shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20 µs for the enhanced PLL using a input shift clock rate of 25 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

Figure 65. Dynamically Programmable Counters & Delays in Stratix GX Device Enhanced PLLs



PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.

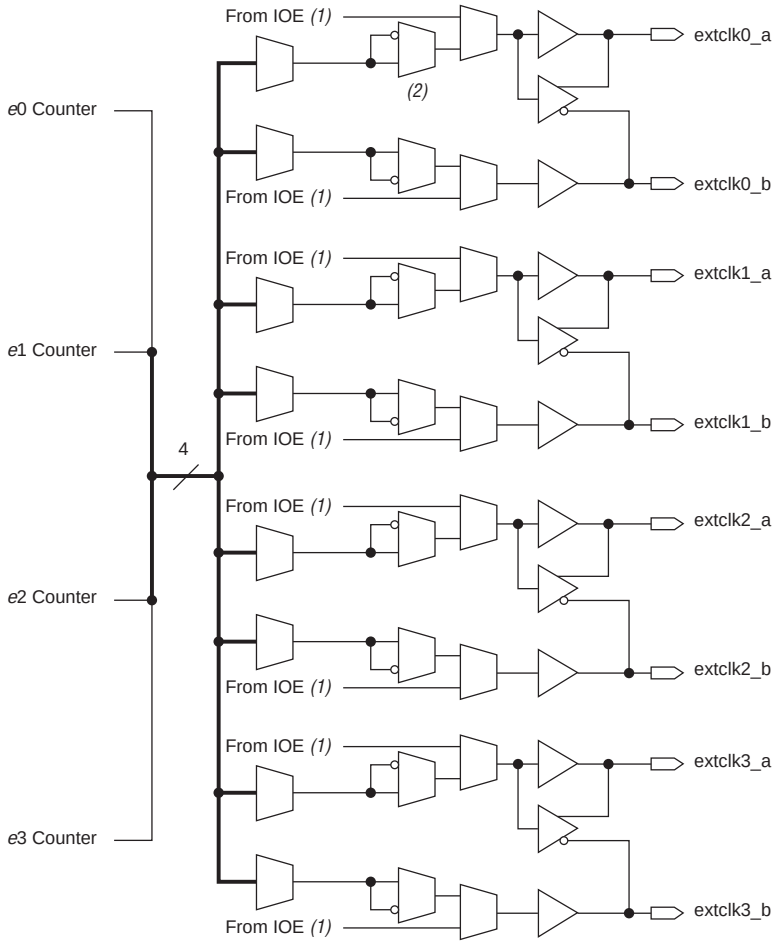
Programmable Bandwidth

The designer has advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also will allow a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL will take longer to lock, but it will attenuate all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and *m* counter value. Designers can manually adjust these values if desired. Bandwidth is programmable from 200 kHz to 1.5 MHz.

External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). See Figure 66.

Figure 66. External Clock Outputs for PLLs 5 & 6



Notes to Figure 66:

(1) Each external clock output pin can be used as a general purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated VCC and GND pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

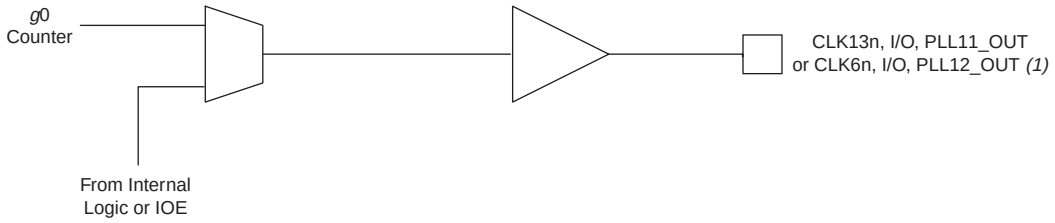
For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, 3.3-V PCML, HyperTransport technology, differential HSTL, and differential SSTL. Table 39 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, the two outputs operate off the same power supply. Both outputs use the same standards in single-ended mode to maintain performance. Designers can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

Table 39. I/O Standards Supported for Enhanced PLL Pins

I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓		✓
1.8 V	✓	✓		✓
1.5 V	✓	✓		✓
3.3-V PCI	✓	✓		✓
3.3-V PCI-X	✓	✓		✓
LVPECL	✓	✓		✓
3.3-V PCML	✓	✓		✓
LVDS	✓	✓		✓
HyperTransport technology	✓	✓		✓
Differential HSTL	✓			✓
Differential SSTL				✓
3.3-V GTL	✓	✓		✓
3.3-V GTL+	✓	✓		✓
1.5-V HSTL class I	✓	✓		✓
1.5-V HSTL class II	✓	✓		✓
SSTL-18 class I	✓	✓		✓
SSTL-18 class II	✓	✓		✓
SSTL-2 class I	✓	✓		✓
SSTL-2 class II	✓	✓		✓
SSTL-3 class I	✓	✓		✓
SSTL-3 class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

Enhanced PLLs 11 and 12 support one single-ended output each (see Figure 67). These outputs do not have their own VCC and GND signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

Figure 67. External Clock Outputs for Enhanced PLLs 11 & 12



Note to Figure 67:
(1) For PLL 11, this pin is CLK13n; for PLL 12 this pin is CLK7n.

Stratix GX devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

Clock Feedback

The following four feedback modes in Stratix GX device enhanced PLLs allow multiplication and/or phase and delay shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay.
- External feedback: The external feedback input pin, FBIN, is phase-aligned with the clock input, CLK, pin. Aligning these clocks allows the designer to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one *e* counter feeds back to the PLL FBIN input, becoming part of the feedback loop.
- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode. The designer defines which internal clock output from the PLL should be phase-aligned to the internal clock pin.
- No compensation: In this mode, the PLL will not compensate for any clock networks or external clock outputs.

Phase & Delay Shifting

Stratix GX device enhanced PLLs provide advanced programmable phase and clock delay shifting. For phase shifting, designers can specify a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Phase-shifting values in time units are allowed with a resolution range of 160 to 420 ps. This resolution is a function of frequency input and the multiplication and division factors – i.e., it is a function of the VCO period equal to an eighth of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps. Designers can use this clock output counter along with an initial setting on the post-scale counter to achieve a phase shift range for the entire period of the output clock. The phase tap feedback to the *m* counter can shift all outputs to a single phase or delay. The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entered.

In addition to the phase shift feature, the fine tune clock delay shift feature provides advanced time delay shift control on each of the four PLL outputs. Each PLL output shifts in 250-ps increments for a range of –3.0 ns to +3.0 ns between any two outputs using discrete delay elements. Total delay shift between any two PLL outputs must be less than 3 ns. For example, shifts on outputs of –1 and +2 ns is allowed, but not –1 and +2.5 ns. There is some delay variation due to process, voltage, and temperature. Only the clock delay shift blocks can be controlled during system operation for dynamic clock delay control.

Spread-Spectrum Clocking

Stratix GX device enhanced PLLs use spread-spectrum technology to reduce electromagnetic interference generation from a system by distributing the energy over a broader frequency range. The enhanced PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread-spectrum for a PLL affects all of its outputs.

Lock Detect & Programmable Gated Locked

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. A designer may need to gate the lock signal for use as a system control. The enhanced PLL includes a programmable counter that holds the lock signal low for a user-selected number of input clock transitions. This allows the PLL to lock before enabling the lock signal. The designer can use the Quartus II software to set the 20-bit counter value. Either a gated lock signal or an ungated lock signal from the locked port can drive the logic array or an output pin. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or assertion of `pllenable`.

Designers can also combine the lock detection with the `CONF_DONE` signal. This signal indicates that the configuration is complete. This feature holds the `CONF_DONE` signal low until the PLL(s) lock.

Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. The designer can use these signals to control PLL resynchronization and the ability to gate PLL output clocks for low power applications.

The `PLLENABLE` pin is a dedicated pin that enables/disables both enhanced and fast PLLs. When the `PLLENABLE` pin is low, the clock output ports are driven by GND and all the PLLs go out of lock. When the `PLLENABLE` pin goes high again, the PLLs relock and resynchronize to the input clocks.

The `areset` signals are reset/resynchronization inputs for each enhanced PLL. The Stratix GX device can drive these input signals from an input pin or from LEs. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. When driven low again, the PLL will resynchronize to its input as it relocks.

The scanaclr signals are resets for the input shift chain registers used in PLL reconfiguration. When high, the entire register chain is cleared. When low, scanclk will clock in the serial data to the input shift register.

The pfdena signals control the PFD output with a programmable gate. If the designer disables the PFD, the VCO will operate at its last set value of control voltage and frequency with some drift, and the system will continue running when the PLL goes out of lock or the input clock disables. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. The designer can either use their own control signal or clk_loss or gated locked status signals to trigger pfdena.

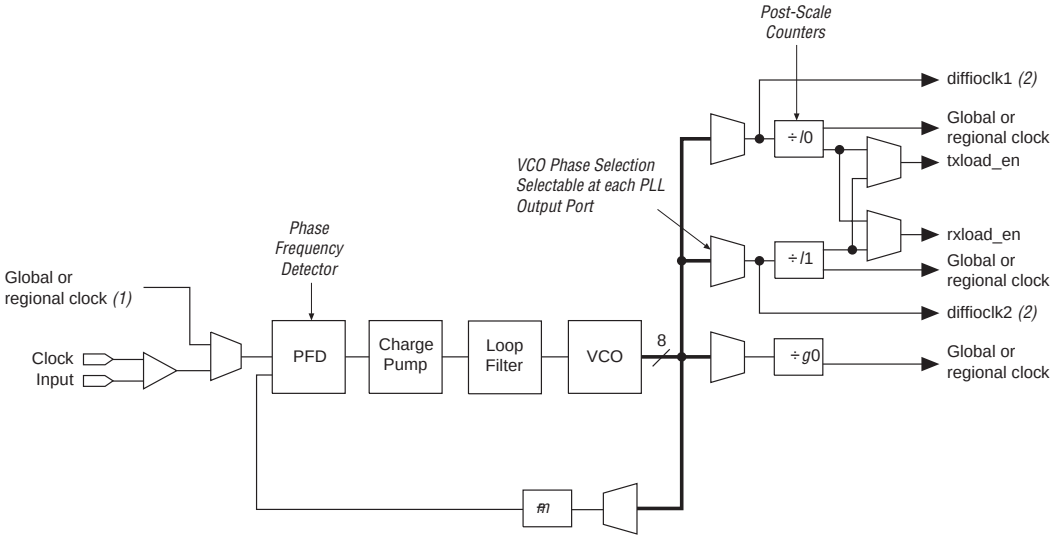
The clkena signals control the regional, global, and external outputs of the enhanced PLL. Each regional, global, and external output port has its own clkena signal. The clkena signals synchronously disable or enable the clock at the PLL output port so the PLL can maintain lock independent of the clkena signals. This feature is useful for applications that require low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The extclkena signals work in the same way as the clkena signals, but they control the external clock output counters ($e0$, $e1$, $e2$, and $e3$). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the FBIN pin.

Fast PLLs

Stratix GX devices contain up to four fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 68 shows a diagram of the fast PLL.

Figure 68. Stratix GX Device Fast PLL



Notes to Figure 68:

(1) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix GX devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(2) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

Stratix GX device fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, the designer can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank.

Table 40 shows the I/O standards supported by fast PLL input pins.

Table 40. Fast PLL Port Input Pin I/O Standards

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL		
Differential SSTL		
3.3-V GTL	✓	
3.3-V GTL+	✓	
1.5V HSTL class I	✓	
1.5V HSTL class II	✓	
SSTL-18 class I	✓	
SSTL-18 class II	✓	
SSTL-2 class I	✓	
SSTL-2 class II	✓	
SSTL-3 class I	✓	
SSTL-3 class II	✓	
AGP (1× and 2×)	✓	
CTT	✓	

Phase Shifting

Stratix GX device fast PLLs have advanced clock shift capability that enables programmable phase shifts. Designers can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can perform phase shifting in time units with a resolution range of 150 to 400 ps. This resolution is a function of the VCO period.

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL. Unlike enhanced PLLs, fast PLLs do not have a programmable gated lock signal.

For more information on high-speed differential I/O support, see "Source-Synchronous Differential I/O Support" on page 31.

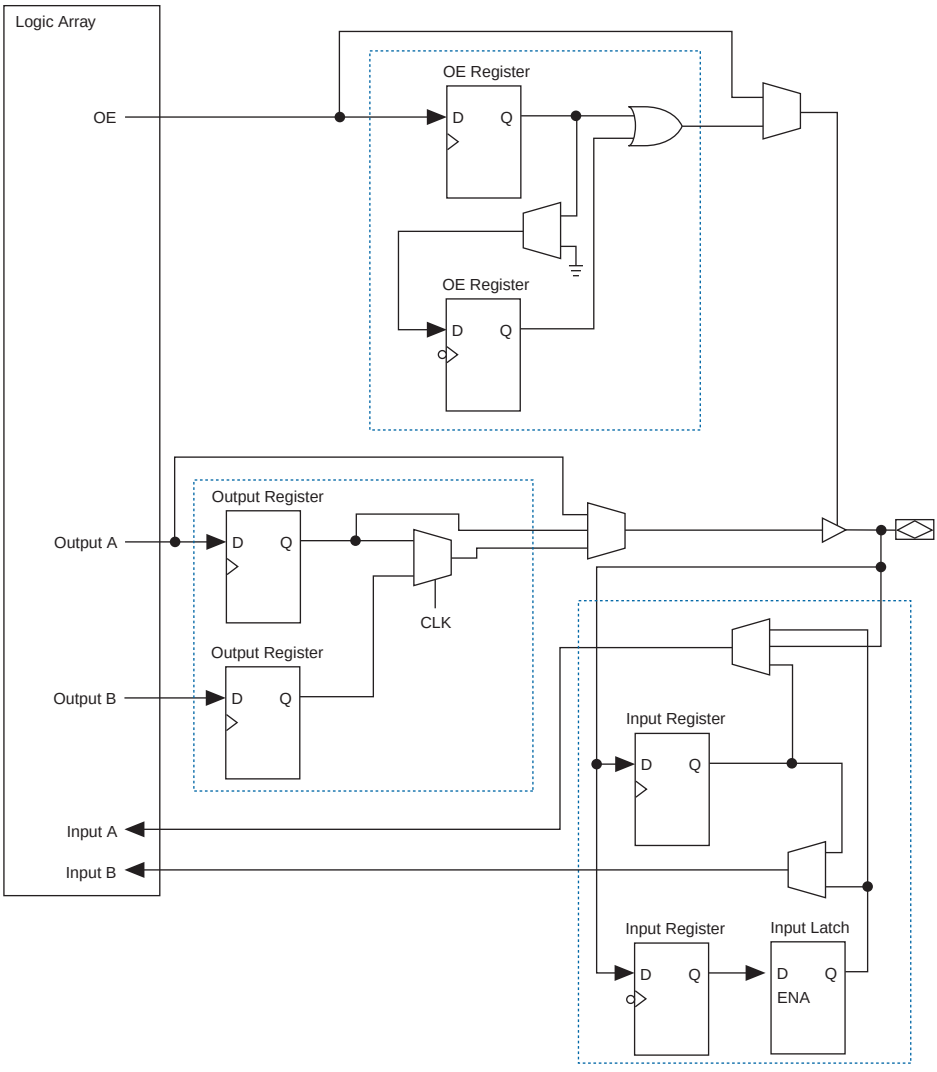
I/O Structure

IOEs are located on the left, top, and bottom of the Stratix GX devices and provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Driver impedance matching
- On-chip termination for differential and single-ended standards
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins

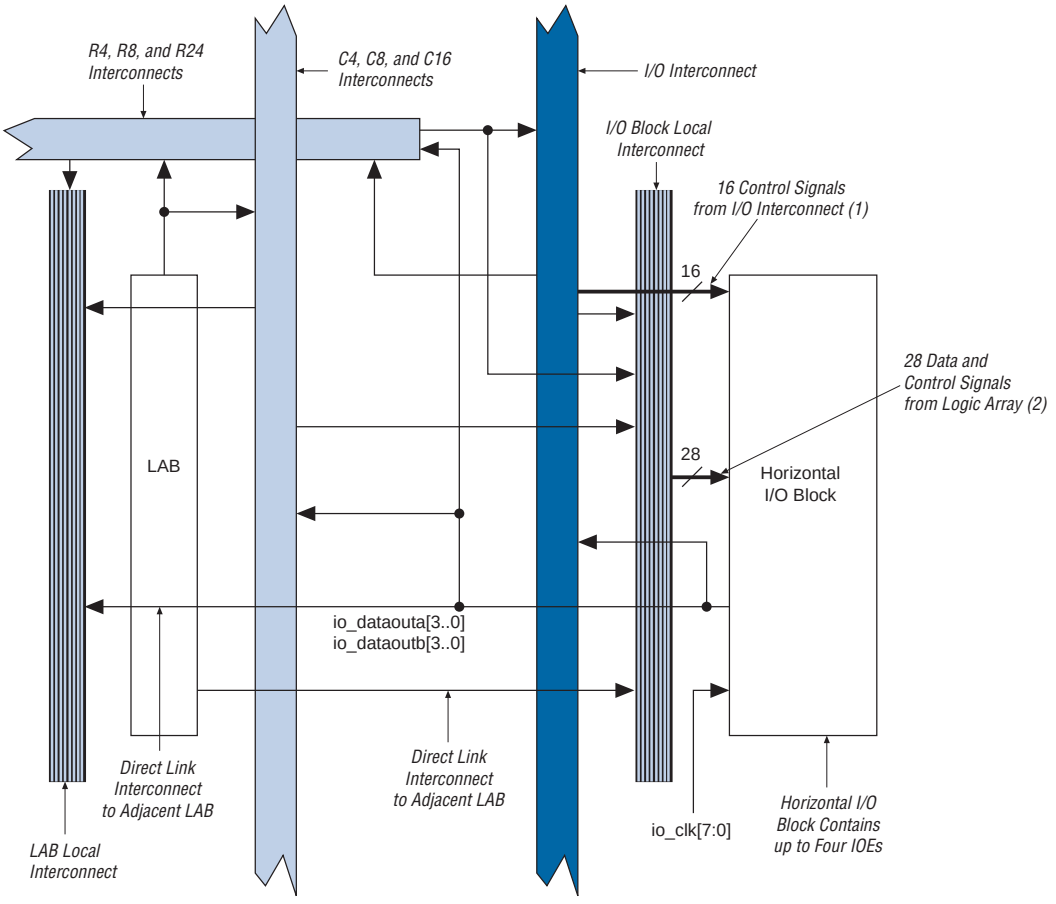
The IOE in Stratix GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 69 shows the Stratix GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins. The I/O banks on the right side of the devices do not have IOEs. However, the connection to the I/O interconnect is similar, as shown in Figure 69.

Figure 69. Stratix GX IOE Structure



The IOEs are located in I/O blocks on the left, top, and bottom of the Stratix GX device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects to the logic array. Figure 70 shows how a row I/O block connects to the logic array. Figure 71 shows how a column I/O block connects to the logic array.

Figure 70. Row I/O Block Connection to the Interconnect

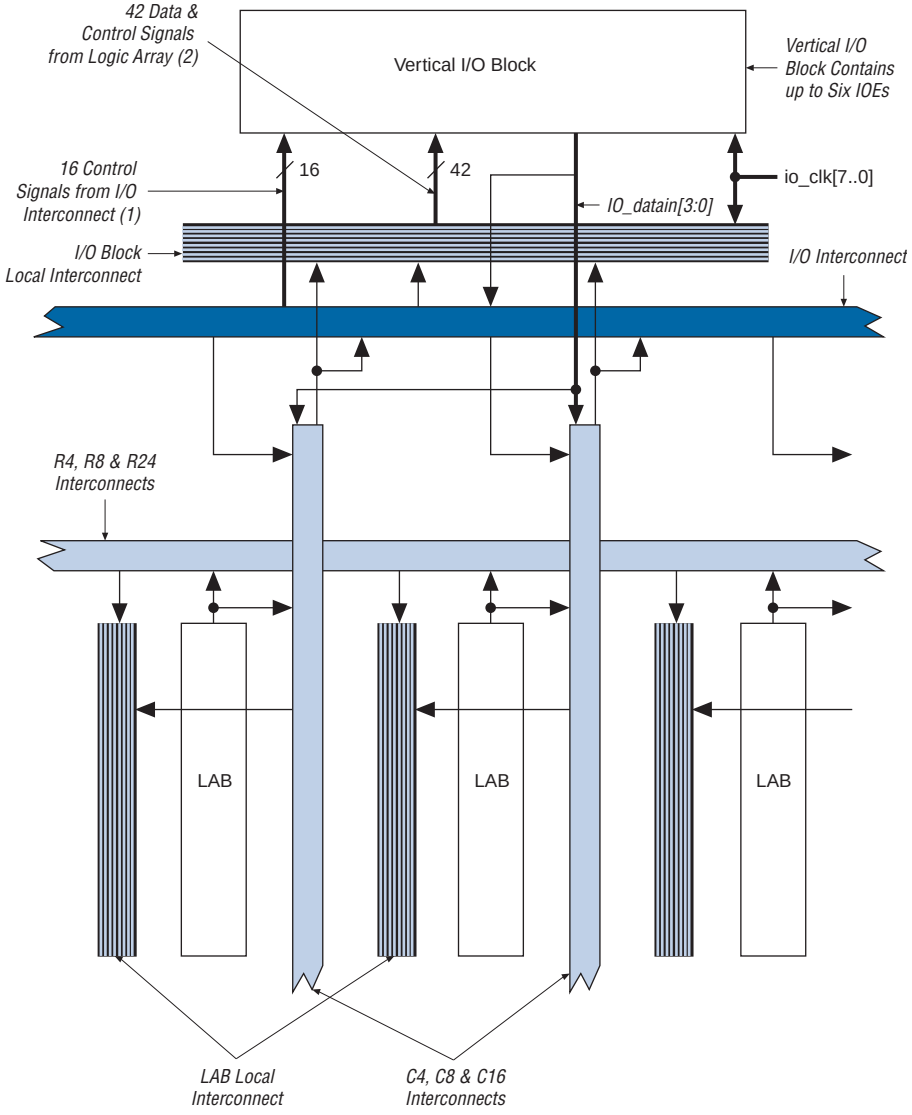


Notes to Figure 70:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_clk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 28 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_coe[3..0]`, four input clock enables `io_cce_in[3..0]`, four output clock enables `io_cce_out[3..0]`, four clocks `io_cclk[3..0]`, and four clear signals `io_cclr[3..0]`.

Figure 71. Column I/O Block Connection to the Interconnect



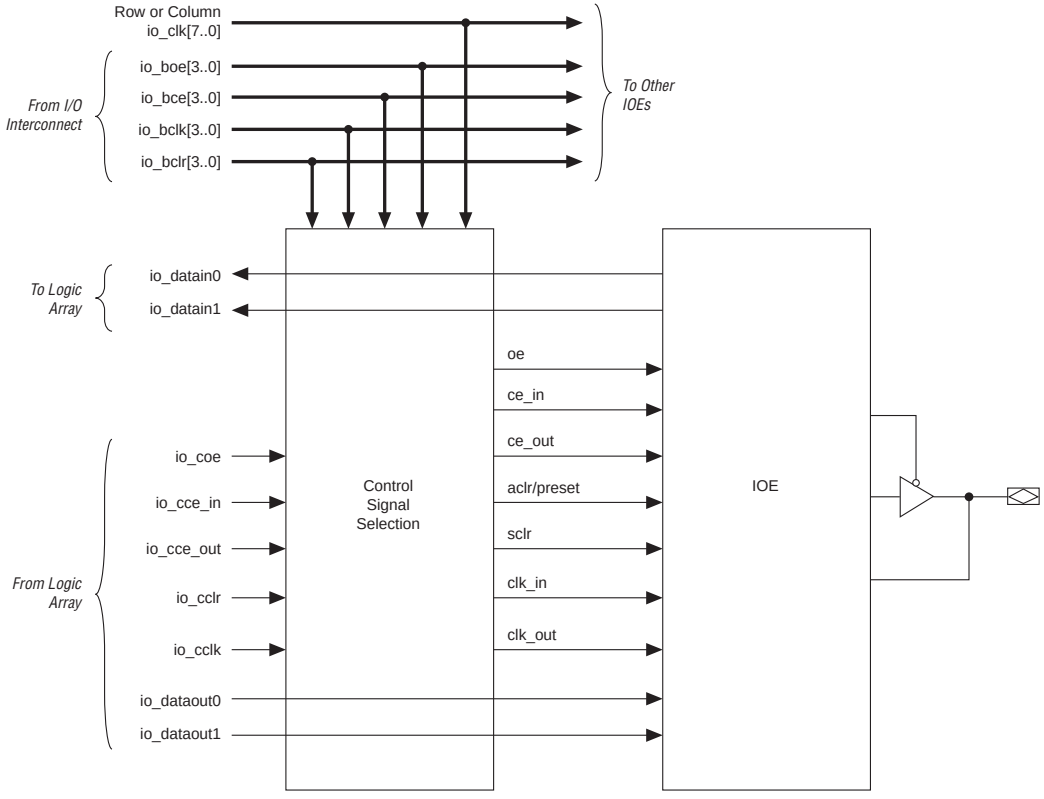
Notes to Figure 71:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

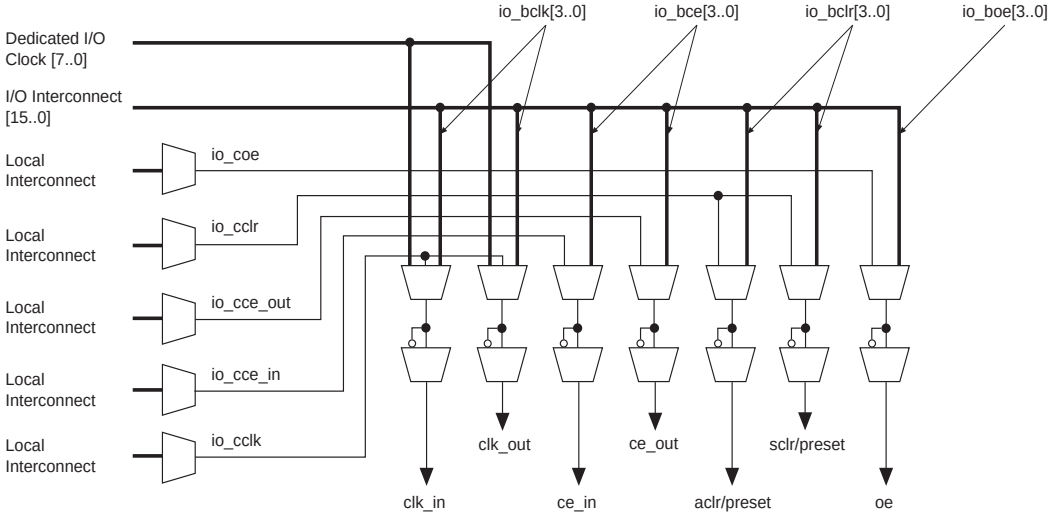
Stratix GX devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 109). Figure 72 illustrates the signal paths through the I/O block.

Figure 72. Signal Path through the I/O Block



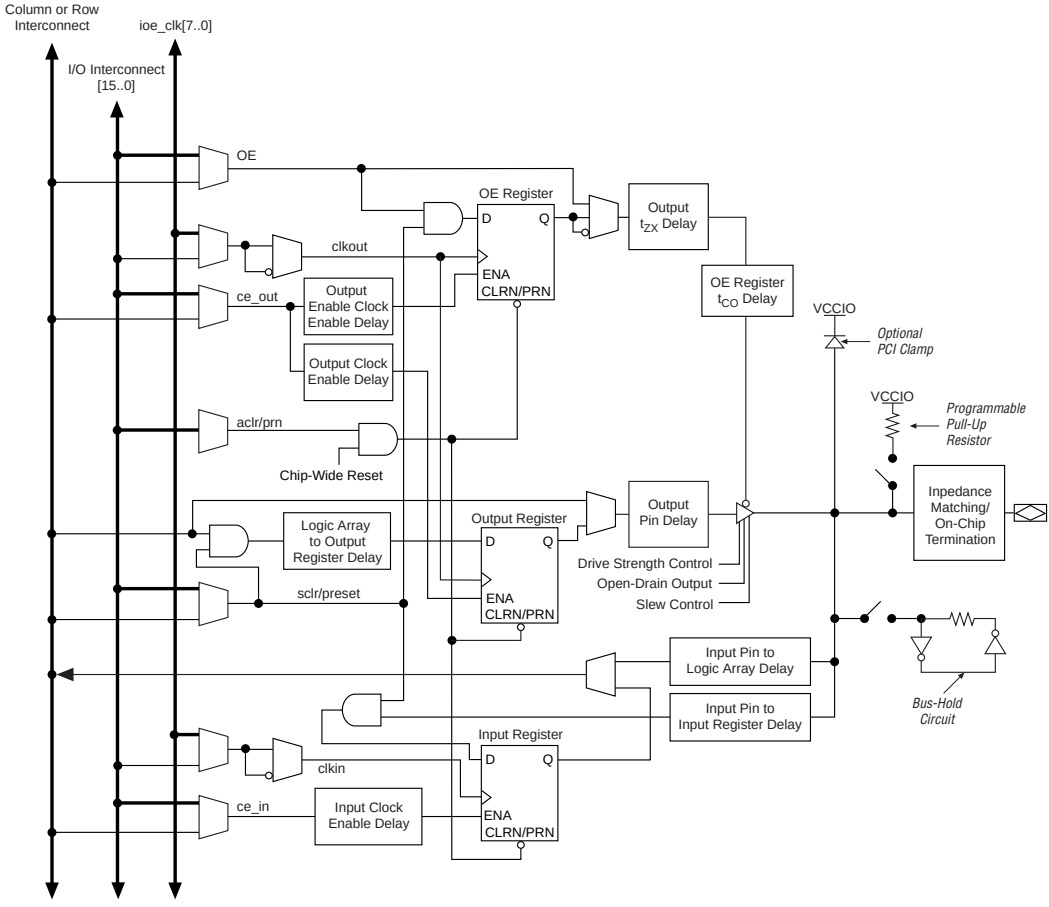
Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 73 illustrates the control signal selection.

Figure 73. Control Signal Selection per IOE



In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 74 shows the IOE in bidirectional configuration.

Figure 74. Stratix GX IOE in Bidirectional I/O Configuration



The Stratix GX device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. A programmable delay exists to increase the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 41 shows the programmable delays for Stratix GX devices.

Table 41. Stratix GX Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output pin delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register
Output enable clock enable delay	Increase output enable clock enable delay

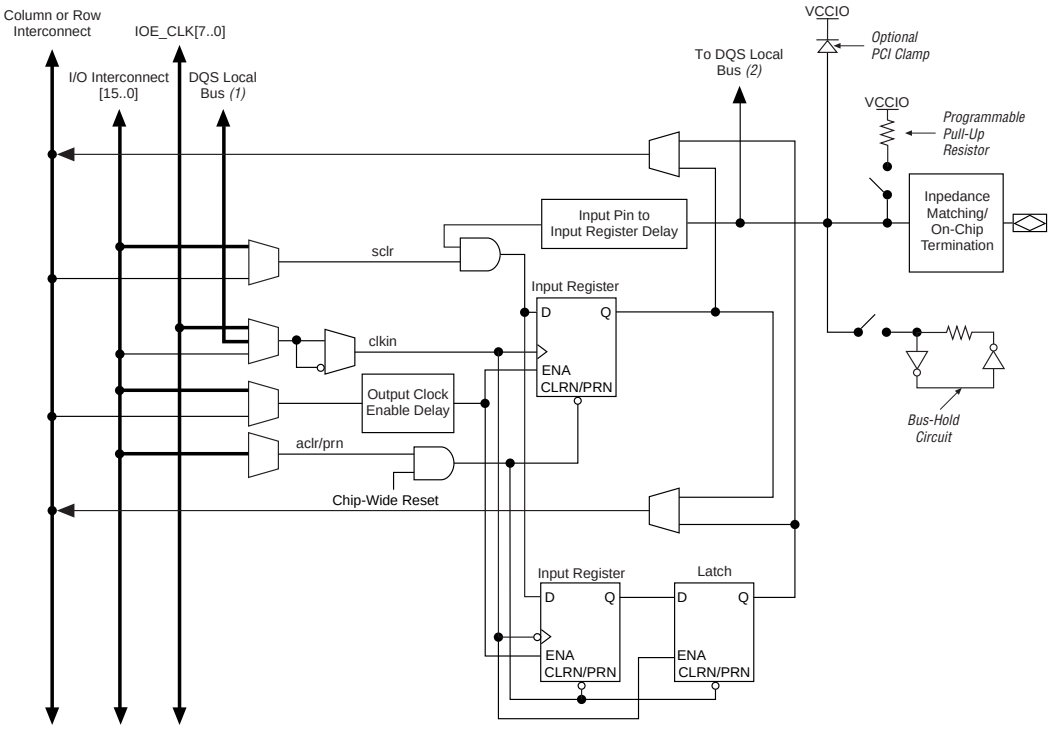
The IOE registers in Stratix GX devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available to the designer for the IOE registers.

Double-Data Rate I/O Pins

Stratix GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes, which are available on the left, top, and bottom of the device.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 75 shows an IOE configured for DDR input.

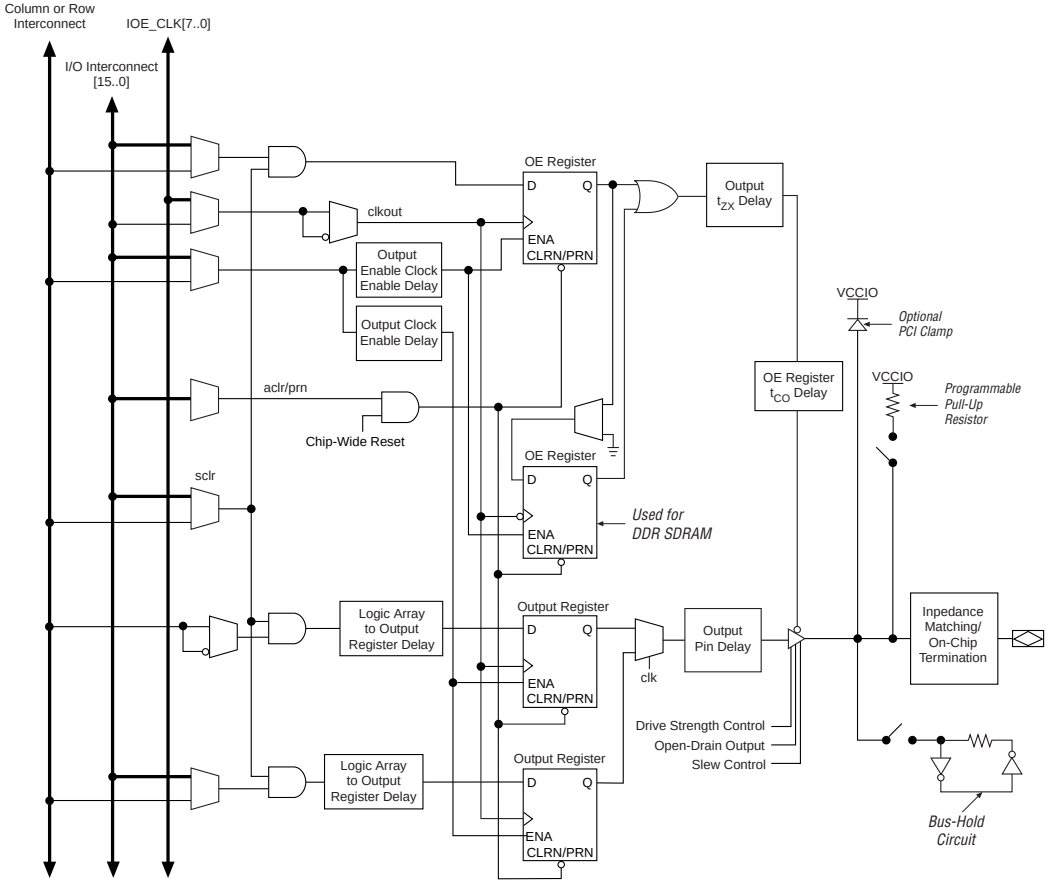
Figure 75. Stratix GX IOE in DDR Input I/O Configuration



Notes to Figure 75:
(1) This signal connection is only allowed on dedicated DQ function pins.
(2) This signal is for dedicated DQS function pins only.

When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 76 shows the IOE configured for DDR output.

Figure 76. Stratix GX IOE in DDR Output I/O Configuration



The Stratix GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix GX device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix GX devices support DDR SDRAM at up to 200 MHz, fast cycle RAM (FCRAM) at up to 200 MHz through dedicated circuitry, and QDR and QDRII SRAM interfaces up to 167 MHz.

DDR SDRAM & FCRAM

In addition to six I/O registers in the IOE for interfacing to these high-speed memory interfaces, Stratix GX devices also have dedicated circuitry for interfacing with DDR SDRAM and FCRAM. In every Stratix GX device, the I/O banks at the top and bottom of the device support DDR SDRAM and FCRAM I/O pins. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32.

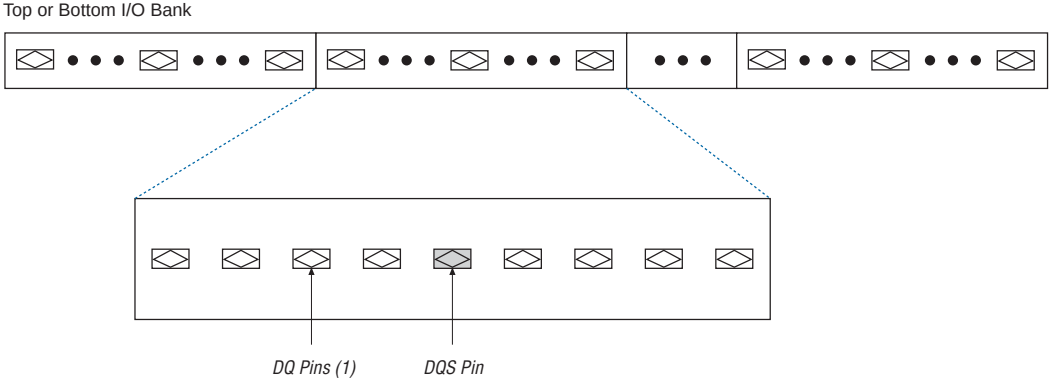
For ×8 mode, there are 20 groups of programmable DQS and DQ pins—10 groups in the top banks and 10 groups in the bottom banks. Each group consists of one DQS pin and a set of at least eight DQ pins (see Figure 77). Each DQS pin drives the set of eight DQ pins within that group.

For ×16 mode, there are eight groups of programmable DQS and DQ pins in the top and bottom banks that are a subset of ×8 DQ pins. Each group consists of one DQS and at least 16 DQ pins.

For ×32 mode, there are four groups of programmable DQS and DQ pins in the top and bottom banks that are also subset of ×8 DQ pins. Each group consists of one DQS and at least 32 DQ pins.

A self-compensated delay element on each DQS pin allows for a 90° phase shift or a 72° phase shift when interfacing to FCRAM. The DQS signals drive onto a local DQS bus within the top and bottom I/O banks. This bus is an additional resource to the I/O Clocks and is used to clock DQ input registers with the DQS signal. See Figure 77. These dedicated circuits combine with enhanced PLL clocking and phase shift ability to provide a complete hardware solution for interfacing to high-speed memory.

Figure 77. Stratix GX Device DQ & DQS Groups in ×8 Mode



Note to Figure 77:
(1) There are at least eight DQ pins per group. Some devices may have more.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, Stratix GX device I/O pins can also interface with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) delay ensures that the t_{ZX} is greater than the clock-to-high-impedance time (t_{XZ}). Stratix GX devices can meet ZBT t_{CO} and t_{SU} times by controlling phase delay in clocks to the OE/output and input registers using an enhanced PLL.

Programmable Drive Strength

The output buffer for each Stratix GX device I/O pin on the left, top, and bottom sides of the device has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 42 shows the possible settings for the I/O standards with drive strength control.

Table 42. Programmable Drive Strength

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
LVTTL (3.3 V)	4
	8
	12
	16
	24
LVCMOS (3.3 V)	2
	4
	8
	12
	24 *(1)*
LVTTL (2.5 V)	2
	8
	12
	16
LVTTL (1.8 V)	2
	8
	12
LVTTL (1.5 V)	2
	4
	8

Note to Table 42:
(1) Banks 1, 2, 5, and 6 do not support this setting.

Open-Drain Output

Stratix GX devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin on the left, top, and bottom sides of the device. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each Stratix GX device I/O pin on the left, top, and bottom sides of the device has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. The I/O pins on the left, top, and bottom sides of the device have an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Bus Hold

Each Stratix GX device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, the designer does not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. Table 86 on page 187 gives the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

The Stratix GX device I/O pins on the left, top, and bottom sides of the device provide an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the output pin's bank.

Advanced I/O Standard Support

Stratix GX device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X
- 3.3-V AGP (1× and 2×)
- LVDS
- LVPECL
- 3.3-V PCML
- 1.5-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output clocks only)
- GTL/GTL+
- HSTL class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II
- CTT

Table 43 describes the I/O standards supported by Stratix GX devices.

Table 43. Stratix GX Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	N/A
1.5-V PCML	Differential	N/A	3.3	N/A
HyperTransport technology	Differential	N/A	2.5	N/A
Differential HSTL	Differential	N/A	1.5	N/A
Differential SSTL	Differential	N/A	2.5	N/A
GTL / GTL+	Voltage-referenced	1.0	N/A	1.5
HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

For more information on I/O standards supported by Stratix GX devices, see *AN 201: Using Selectable I/O Standards in Stratix Devices*.

Stratix GX devices contain seven I/O banks. The two I/O banks on the left of the device contain circuitry to support source-synchronous differential I/O standards with LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. Additionally, these two I/O banks support all I/O standards listed in Table 43 except PCI I/O pins or PCI-X, GTL, SSTL-18 Class II, and HSTL Class II outputs.

The two I/O banks on the right side of the device support high-speed differential I/O standards with 1.5-V PCML inputs and outputs. The top and bottom I/O banks support all single-ended I/O standards. Table 44 shows I/O standard support for each I/O bank.

Table 44. I/O Support by Bank

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)	Right Banks (5 & 6)
LVTTL	✓	✓	
LVCMOS	✓	✓	
2.5 V	✓	✓	
1.8 V	✓	✓	
1.5 V	✓	✓	
3.3-V PCI	✓		
3.3-V PCI-X	✓		
LVPECL		✓	
3.3-V PCML		✓	
1.5-V PCML			✓
LVDS		✓	
HyperTransport		✓	
Differential HSTL (clock inputs/outputs)	✓		
Differential SSTL (clock outputs)	✓		
3.3-V GTL	✓	(1)	
3.3-V GTL+	✓	✓	
1.5-V HSTL class I	✓	✓	
1.5-V HSTL class II	✓	(1)	
SSTL-18 class I	✓	✓	
SSTL-18 class II	✓	(1)	
SSTL-2 class I	✓	✓	
SSTL-2 class II	✓	✓	
SSTL-3 class I	✓	✓	
SSTL-3 class II	✓	✓	
AGP (1× and 2×)	✓	(1)	
CTT	✓	✓	

Note to Table 44:
(1) These I/O standards are only supported for input pins.

The I/O banks on the left, top, and bottom of the device have their own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; these banks can each support a different standard independently. Each of these banks also has dedicated VREF pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

The I/O banks on the left, top, and bottom of the device can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Terminator Technology

Terminator technology provides on-chip parallel and differential termination and impedance matching (series termination) to reduce reflections and maintain signal integrity. Terminator technology simplifies board design by minimizing the number of external termination resistors required. These resistors can be placed inside the package, eliminating small stubs that can still lead to reflections. Additionally, the terminator technology provides constant calibration of the internal resistor values after configuration and during normal operation via two external reference resistors. The constant calibration allows the termination resistors to compensate for process, temperature, and voltage variation, providing a robust termination scheme. There is one set of reference resistors for each I/O bank.

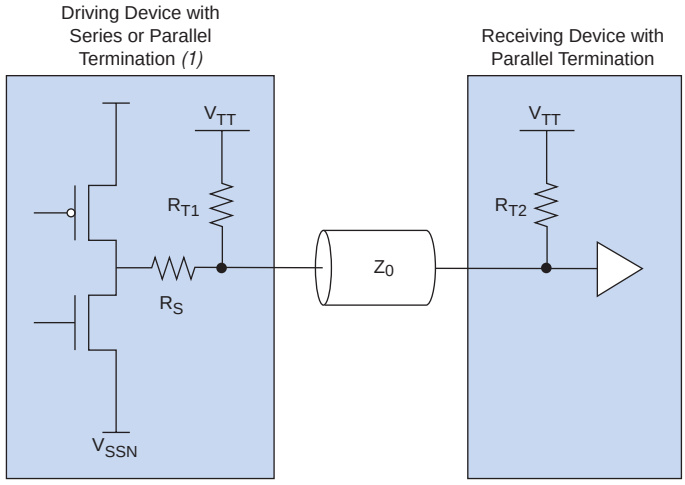
Three types of termination are available in the device:

- Series Termination (R_S) and Impedance Matching
- Parallel Termination (R_T)
- Differential Termination (R_D)

Stratix GX devices support series termination for SSTL-3 and SSTL-2 signals to meet SSTL specifications. Stratix GX devices also support driver impedance matching through series termination for LVTTL and LVCMOS signals to match the impedance of the transmission lines, typically 25 or 50 Ω. When used with the output drivers, the terminator technology sets the output driver impedance to 25 or 50 Ω as specified by the external reference resistors, resulting in significantly reduced reflections.

Parallel termination is supported for SSTL-3, SSTL-2, HSTL, GTL, GTL+, and CTT signals as defined by the respective I/O standards. Figure 78 illustrates the possible termination schemes for single-ended I/O pins.

Figure 78. Termination Schemes for Single-Ended I/O Pins

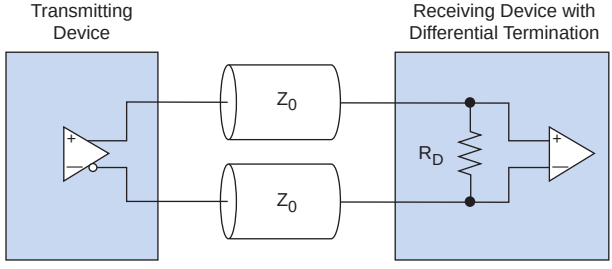


Note to Figure 78:

(1) In the transmitting device, only one type of termination, series or parallel termination, is possible. For standards that require both terminations, such as SSTL 2 Class II, an external parallel termination resistor must be provided.

Stratix GX devices support differential termination with a 100-Ω resistor for LVDS signals. Figure 79 shows the device with differential termination.

Figure 79. Differential LVDS Input On-Chip Termination



Terminator technology can only support one type of termination per I/O bank, although some different I/O standards can be mixed within a given I/O bank. I/O banks at the top and bottom of the device support series termination and impedance matching and parallel termination. I/O banks on the left side of the device support series termination and impedance matching and LVDS far-end differential termination. The I/O banks on the left, top, and bottom sides of the device using on-chip termination must connect two external reference resistors, R_{UP} and R_{DN}, to the designated pins in the I/O bank. The designer sets which pins are terminated and match the reference resistors. After configuration and during normal operation, the device periodically samples the external resistor values and updates the internal resistor values. Table 45 shows the Terminator technology support within each I/O bank.

I/O banks on the right side of Stratix GX devices do not support Terminator technology.

Table 45. Terminator Technology Support by I/O Banks

Terminator Technology Support	Top & Bottom Banks (3, 4, 7 & 8)	Left Banks (1 & 2)
Series termination	✓	✓
Impedance matching (LVTTL/LVCMOS)	✓	✓
Parallel termination *(1)*	✓	
Differential termination		✓

Note to Table 45:
(1) Clock pins `CLK[0..3]` and `CLK[8..11]` do not support parallel termination.

Table 46 summarizes the external resistor values required for terminator technology.

Table 46. External Resistor Values

Parameter	R_{UP}	R_{DN}
Series termination	250 Ω	250 Ω
Impedance matching (LVTTL/LVCMOS)	250 Ω / 500 Ω	250 Ω / 500 Ω
Parallel termination *(1)*	1,000 Ω	1,000 Ω
Differential termination	*(2)*	*(2)*

Notes to Table 46:
(1) Stratix GX devices support parallel termination on the top and bottom I/O banks only.
(2) No external resistor is necessary.

MultiVolt I/O Interface

The Stratix GX architecture supports the MultiVolt I/O interface feature, which allows Stratix GX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and eight sets for I/O output drivers (VCCIO).

The Stratix GX VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 47 summarizes Stratix GX MultiVolt I/O support.

Table 47. Stratix GX MultiVolt I/O Support *Note (1)*

VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8		✓	✓	✓		✓ (2)	✓			
2.5			✓	✓		✓ (3)	✓ (3)	✓		
3.3			✓	✓	✓ (4)	✓ (5)	✓ (5)	✓ (5)	✓	✓

Notes to Table 47:
(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2) When V_{CCIO} = 1.8 V, a Stratix GX device can drive a 1.5-V device with 1.8-V tolerant inputs.
(3) When V_{CCIO} = 2.5 V, a Stratix GX device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(4) Stratix GX devices can be 5.0-V tolerant with the use of an external resistor and internal PCI clamp diode.
(5) When V_{CCIO} = 3.3 V, a Stratix GX device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Stratix GX devices include a dedicated pin, VCCSEL, to set the JTAG pins to accept 3.3 V/2.5 V or 1.8 V during configuration. Setting the pin to high (1.5/1.8/2.5/3.3 V) sets the configuration and JTAG I/O pins to accept 1.8 V, while low (0 V) sets them to accept 3.3/2.5 V.

Electrical Specifications

Stratix GX devices meet the protocol specifications for 10-Gigabit Ethernet, InfiniBand, and 1000BASE-X Ethernet interfaces (see Table 48). Table 49 lists the driver specifications for Stratix GX devices.

Table 48. Driver Specifications (Part 1 of 2) *Note (1)*

Parameter	10-Gigabit Ethernet			InfiniBand			1000BASE-X Ethernet			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply voltage		1.5			1.5			1.5		V
Baud rate		3.125			2.5			1.25		Gigabaud
Unit interval (UI) *(2)*		320			400			800		ps
Differential output voltage ($V_{OD} = V_{POS} - V_{NEG}$)	400		800	500		800	550		1,000	mV
V_{OD} with power off									85	mV
Sleep/standby mode differential output				0 *(3)*	*(3)*	800 *(3)*				
Absolute output voltage limits	–0.4		2.3							V
Output common mode voltage (V_{OCM})	Only AC-coupled			0.5 *(4)*	*(4)*	1 *(4)*	Only AC-coupled			V

Table 48. Driver Specifications (Part 2 of 2) *Note (1)*

Parameter	10-Gigabit Ethernet			InfiniBand			1000BASE-X Ethernet			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
AC common mode voltage	Only AC-coupled					25	Only AC-coupled			mV
AC common mode current						5				µA
Differential skew (within differential pair)			15						25	ps
Differential skew (pair-to-pair)						500				ps
Rise/fall times (20% to 80%) *(5)*	60		130	100			85		327	ps
Differential output return loss			10							dB
Common mode output return loss			6							dB
Duty cycle	45		55	45		55	45		55	%
Differential output impedance		100		75	100	125				Ω
Single-ended output impedance				30	50	75		75		Ω
Single-ended output impedance matching within single pair						10				%

Notes to Table 48:
(1) Contact Altera Applications for information on package constraints.
(2) UI = one bit period.
(3) Driver outputs must be static.
(4) InfiniBand interface can be either AC- or DC-coupled.
(5) These values are for loaded outputs.

Table 49. Additional Driver Specifications (Part 1 of 2) *Note (1)*

Parameter	1-Gigabit Fibre Channel			Serial RapidIO			Units
	Min	Typ	Max	Min	Typ	Max	
Supply voltage		1.5			1.5		V
Baud rate		1.0625			1.25/2.5/ 3.125		Gigabaud
UI *(2)*		941			800/400/ 320		ps

Table 49. Additional Driver Specifications (Part 2 of 2) *Note (1)*

Parameter	1-Gigabit Fibre Channel			Serial RapidIO			Units
	Min	Typ	Max	Min	Typ	Max	
Differential output voltage ($V_{OD} = V_{POS} – V_{NEG}$)	300		800	250/250/250		1,000/500/500	mV
	550		1,000	400/500/500		1,000/800/800	
V_{OD} with power off			85				mV
Sleep/standby mode differential output							
Absolute output voltage limits							V
Output common mode voltage (V_{OCM})	Only AC-coupled			Only AC-coupled			V
AC common mode voltage	Only AC-coupled			Only AC-coupled			mV
AC common mode current							µA
Differential skew (within differential pair)			25			25/20/15	ps
Differential skew (pair-to-pair)						1,000	ps
Rise/fall times (20% to 80%) *(3)*	100		385	100/100/60			ps
Differential output return loss							dB
Common mode output return loss							dB
Duty cycle	45		55				%
Differential output impedance							Ω
Single-ended output impedance		75					Ω
Single-ended output impedance matching within single pair							%

Notes to Table 49:
(1) Contact Altera Applications for information on package constraints.
(2) UI = one bit period.
(3) These values are for loaded outputs.

Table 50. Receiver Specifications *Note (1)*

Parameter	10-Gigabit Ethernet			InfiniBand			1000BASE-X Ethernet			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply voltage		1.5			1.5			1.5		V
Baud rate		3.125			2.5			1.25		Gigabaud
UI		320			400			800		ps
Differential input voltage ($V_{ID} = V_{POS} – V_{NEG}$)	100		1,250	42.5		800	200		1,000	mV
Input common mode voltage (V_{ICM})	Only AC-coupled			0.25 *(2)*	*(2)*	1.25 *(2)*	Only AC-coupled			V
Differential skew (within differential pair)			75						175	ps
Differential skew (pair-to-pair)						24				ns
Eye opening		112			140			320		ps
Differential output return loss			10			10				dB
Common mode output										
Return loss			6			6				dB
Duty cycle	40		60	40		60	40		60	%
Bit error rate (BER)			10^{-12}			10^{-12}			10^{-12}	
Off current *(3)*				–50		50				mA
Hot plug voltage *(4)*				–0.5		1.6				V
Termination to V_{TT} (Z_{RTERM})				40		62.5				Ω
Termination voltage (V_{TT}) *(5)*				1		0.5				V
V_{TT} impedance (Z_{VTT})						30				Ω
Input impedance		50								Ω
Differential input impedance		100								Ω

Notes to Table 50:
(1) Receiver inputs must be internally biased for AC-coupled systems.
(2) The InfiniBand interface can be either AC- or DC-coupled.
(3) This value is the current into a pin with the power off.
(4) This value is the voltage applied with the power on or off.
(5) This does not apply when DC-blocking capacitors are present between the termination resistors and the pins.

Table 51. Additional Receiver Specifications *Note (1)*

Parameter	1-Gigabit Fibre Channel			Serial RapidIO			Units
	Min	Typ	Max	Min	Typ	Max	
Supply voltage		1.5			1.5		V
Baud rate		1.063			1.25/2.5/ 3.125		Gigabaud
Unit interval (UI)		941			800/400/ 320		ps
Differential input voltage ($V_{ID} = V_{POS} - V_{NEG}$)	200		800	87.5/87.5/ 100		1,000/800/ 800	mV
Input common mode voltage (V_{ICM})							V
Differential skew (within differential pair)	Only AC-coupled			Only AC-coupled			ps
Differential skew (pair-to-pair)			200			75	ns
Eye opening						24/24/24	ps
Differential output return loss		395.2					dB
Common mode output							
Return loss							dB
Duty cycle	40		60				%
BER			10^{-12}			10^{-12}	
Off current *(2)*							mA
Hot plug voltage *(3)*							V
Termination to V_{TT} (Z_{RTERM})							Ω
Termination voltage (V_{TT}) *(4)*							V
V_{TT} impedance (Z_{VTT})		75					Ω
Input impedance							Ω
Differential input impedance							Ω

Notes to Table 51:
(1) Receiver inputs must be internally biased for AC-coupled systems.
(2) This value is the current into a pin with the power off.
(3) This value is the voltage applied with the power on or off.
(4) This does not apply when DC-blocking capacitors are present between the termination resistors and the pins.

Power Sequencing & Hot Socketing

Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the VCCIO and VCCINT power supplies may be powered in any order.

Signals can be driven into Stratix GX devices before and during power-up without damaging the device. In addition, Stratix GX devices do not drive out during power-up. Once operating conditions are reached and the device is configured, Stratix GX devices operate as specified by the user.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Stratix GX devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix GX devices can also use the JTAG port for configuration together with either the Quartus II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix GX devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode. Designers can use this ability for JTAG testing before configuration when some of the Stratix GX pins drive or receive from other devices on the board using voltage-referenced standards. Because the Stratix GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows full designers to fully test I/O connection to other devices.

The enhanced PLL reconfiguration bits are part of the JTAG chain before configuration and after power-up. After device configuration, the PLL reconfiguration bits are not part of the JTAG chain.

Stratix GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. Stratix GX devices support the JTAG instructions shown in Table 52.

Table 52. Stratix GX JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring a Stratix GX device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
PULSE_NCONFIG	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	Allows the IOE standards to be configured through the JTAG chain. Stops configuration if executed during configuration. Can be executed before or after configuration.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 52:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The Stratix GX device instruction register length is 10 bits, and the USERCODE register length is 32 bits. Tables 53 and 54 show the boundary-scan register length and device IDCODE information for Stratix GX devices.

Table 53. Stratix GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1SGX10	1,029
EP1SGX25	1,665
EP1SGX40	1,941

Table 54. 32-Bit Stratix GX Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1SGX10	0000	0010 0000 0100 0001	000 0110 1110	1
EP1SGX25	0000	0010 0000 0100 0011	000 0110 1110	1
EP1SGX40	0000	0010 0000 0100 0101	000 0110 1110	1

Notes to Table 54:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 80 shows the timing requirements for the JTAG signals.

Figure 80. Stratix GX JTAG Waveforms

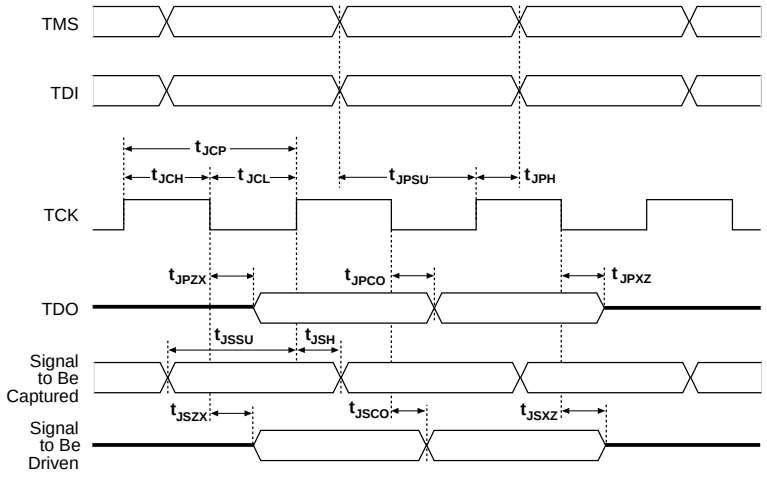


Table 55 shows the JTAG timing parameters and values for Stratix GX devices.

Table 55. Stratix GX JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information on JTAG, see the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

SignalTap Embedded Logic Analyzer

Stratix GX devices feature the SignalTap embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix GX architecture are configured with CMOS SRAM elements. Stratix GX devices are reconfigurable and are 100% tested prior to shipment. As a result, the designer does not have to generate test vectors for fault coverage purposes, and can instead focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs. Stratix GX devices can be configured on the board for the specific functionality required.

Stratix GX devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices that configure Stratix GX devices via a serial data stream. Stratix GX devices can be configured in under 100 ms using 8-bit parallel data at 100 MHz. The Stratix GX device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix GX devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Stratix GX device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Operating Modes

The Stratix GX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

A built-in weak pull-up resistor pulls all user I/O pins to V_{CCIO} before and during device configuration.

SRAM configuration elements allow Stratix GX devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

Configuration Schemes

Designers can load the configuration data for a Stratix GX device with one of five configuration schemes (see Table 56), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix GX device. A configuration device can automatically configure a Stratix GX device at system power-up.

Multiple Stratix GX devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 56. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	ByteBlasterMV or MasterBlaster download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC file (**.jam** or **.jbc**)

Partial Reconfiguration

The enhanced PLLs within the Stratix GX device family support partial reconfiguration of their multiply, divide, and time delay settings without reconfiguring the entire device. Designers can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL. See "Enhanced PLLs" on page 123 for more information on Stratix GX PLLs.

Remote Update Configuration Modes

Stratix GX devices also support remote configuration using an Altera enhanced configuration device (e.g., EPC16, EPC8, and EPC4 devices) with page mode selection. Factory configuration data is stored in the default page of the configuration device. This is the default configuration which contains the design required to control remote updates and handle or recover from errors. The designer writes the factory configuration once into the flash memory or configuration device. Remote update data can update any of the remaining pages of the configuration device. If there is an error or corruption in a remote update configuration, the configuration device reverts back to the factory configuration information.

There are two remote configuration modes: remote and local configuration. Designers can use the remote update configuration mode for all three configuration modes: serial, parallel synchronous, and parallel asynchronous. Configuration devices (e.g., EPC16 devices) only support serial and parallel synchronous modes. Asynchronous parallel mode allows remote updates when an intelligent host is used to configure the Stratix GX device. This host must support page mode settings similar to an EPC16 device.

Remote Update Mode

When the Stratix GX device is first powered-up in remote update programming mode, it loads the configuration located at page address `000`. The factory configuration should always be located at page address `000`, and should never be remotely updated. The factory configuration contains the required logic to perform the following operations:

- Determine the page address/load location for the next application's configuration data
- Recover from a previous configuration error
- Receive new configuration data and write it into the configuration device

The factory configuration is the default and takes control if an error occurs while loading the application configuration.

While in the factory configuration, the factory-configuration logic performs the following operations:

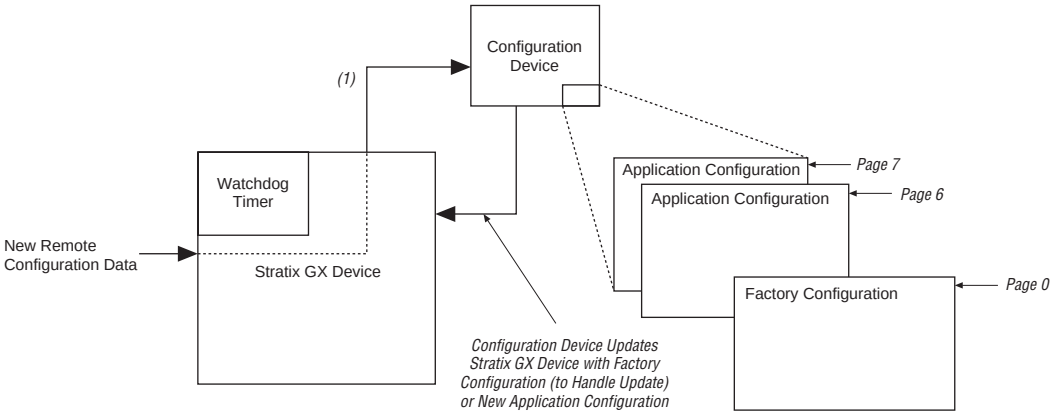
- Loads a remote update-control register to determine the page address of the new application configuration
- Determines whether to enable a user watchdog timer for the application configuration
- Determines what the watchdog timer setting should be if it is enabled

The user watchdog timer is a counter that must be continually reset within a specific amount of time in the user mode of an application configuration to ensure that valid configuration occurred during a remote update. Only valid application configurations designed for remote update can reset the user watchdog timer in user mode. If a valid application configuration does not reset the user watchdog timer in a specific amount of time, the timer updates a status register and loads the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

If an error occurs in loading the application configuration, the configuration logic writes a status register to specify the cause of the reconfiguration. Once this occurs, the Stratix GX device automatically loads the factory configuration, which reads the status register and determines the reason for reconfiguration. Based on the reason, the factory configuration will take appropriate steps and will write the remote update control register to specify the next application configuration page to be loaded.

When the Stratix GX device successfully loads the application configuration, it enters into user mode. The Stratix GX device then executes the main application of the user. Intellectual property (IP), such as a Nios™ embedded processor, can help the Stratix GX device determine when remote update is coming. The Nios embedded processor or user logic receives incoming data, writes it to the configuration device, and loads the factory configuration. The factory configuration will read the remote update status register and determine the valid application configuration to load. Figure 81 shows the Stratix GX remote update. Figure 82 shows the transition diagram for remote update mode.

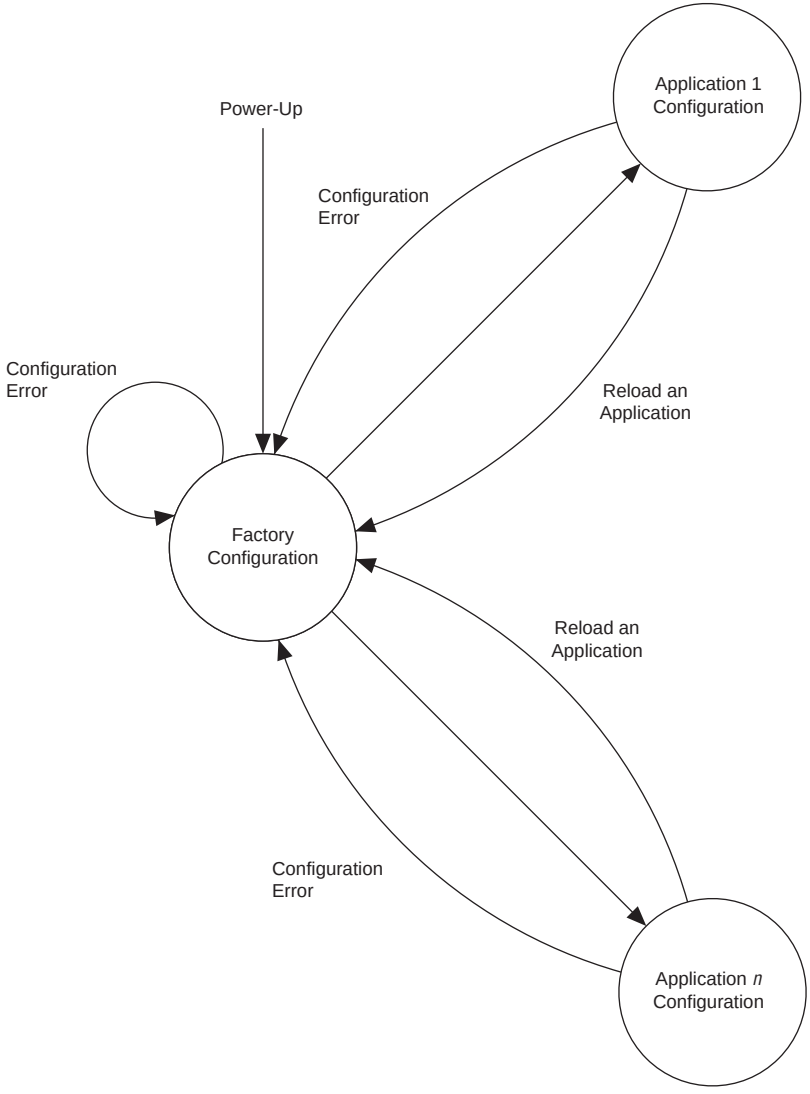
Figure 81. Stratix GX Device Remote Update



Note to Figure 81:

(1) When the Stratix GX device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Figure 82. Remote Update Transition Diagram *Notes (1), (2)*



Notes to Figure 82:

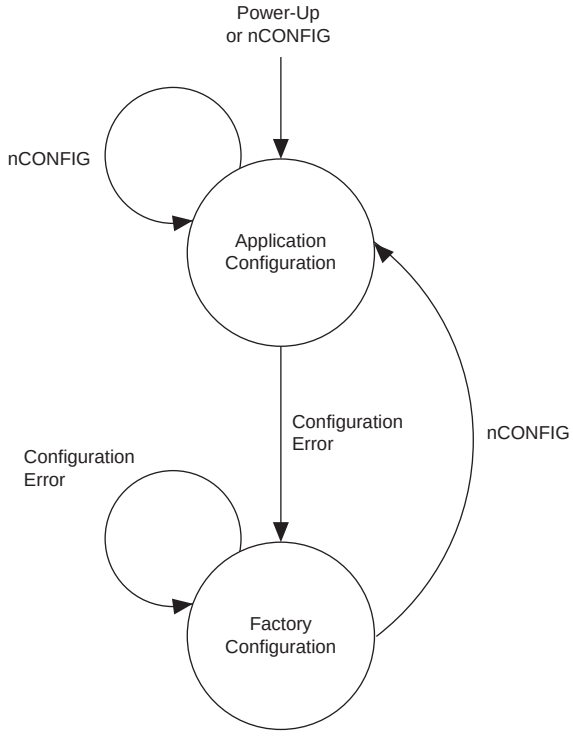
(1) Remote update of Application Configuration is controlled by a Nios embedded processor or user logic programmed in the Factory or Application configurations.

(2) Up to seven pages can be specified allowing up to seven different configuration applications.

Local Update Mode

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power-up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 83 shows the transition diagram for local update mode.

Figure 83. Local Update Transition Diagram



Temperature-Sensing Diode

Stratix GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix GX device to connect to the external temperature-sensing device, as shown in Figure 84. The temperature-sensing diode is a passive element and therefore can be used before the Stratix GX device is powered. Table 57 shows the specifications for bias voltage and current of the Stratix GX temperature-sensing diode.

Figure 84. External Temperature-Sensing Diode

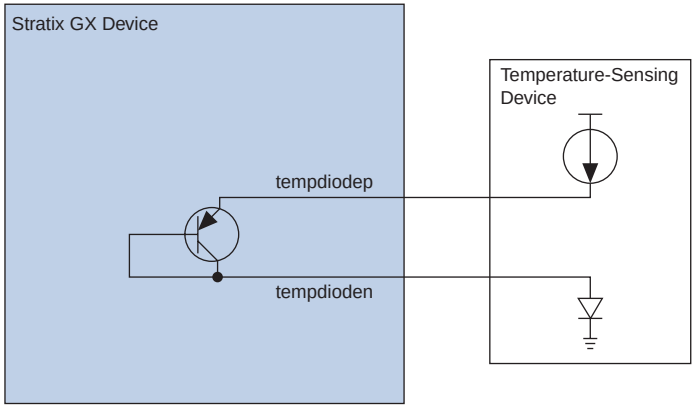
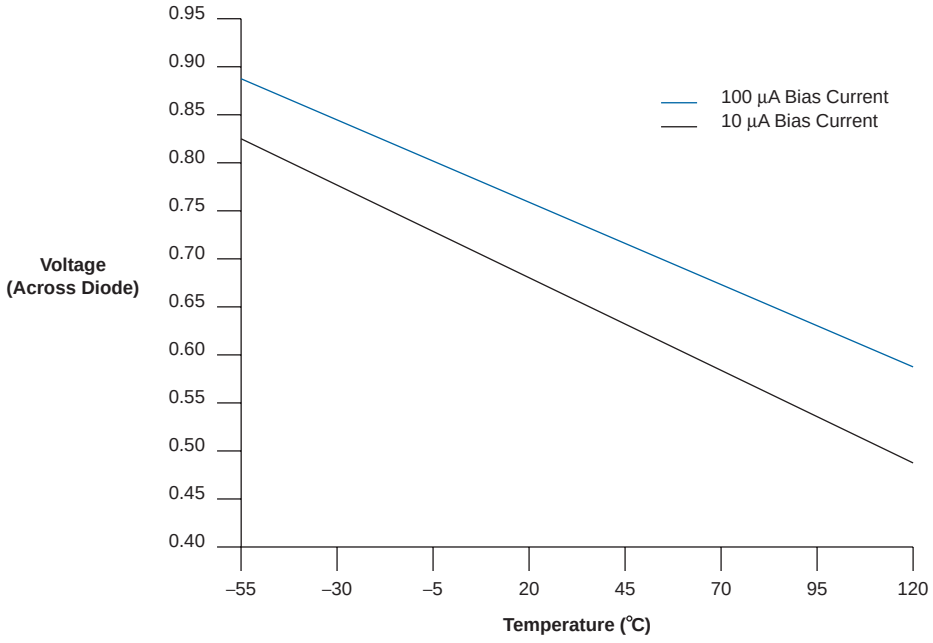


Table 57. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Units
I_{BIAS} high	80	100	120	µA
I_{BIAS} low	8	10	12	µA
$V_{BP} - V_{BN}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 85.

Figure 85. Temperature vs. Temperature-Sensing Diode Voltage



Operating Conditions

Stratix GX devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 58 through 87 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, specifications and capacitance for 1.5-V Stratix GX devices.

Table 58. Stratix GX Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 59. Stratix GX Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 60. Stratix GX Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs				mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 61. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 62. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 63. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA *(10)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OH} = 1 mA		0.4	V
		I_{OH} = 2 to 16 mA *(10)*		0.7	V

Table 64. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	2.25	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 65. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 66. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		450	mV
ý V_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ý V_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor		90	100	110	Ω

Table 67. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.3	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage				V_{CCIO} – 0.3	V
V_{OH}	High-level output voltage		V_{CCIO}			V
V_T	Output termination voltage			V_{CCIO}		V
V_{OD}	Differential output voltage		300	450	600	mV
V_{TH}	Differential input threshold		100			mV
R_O	Output load			100		Ω
R_L	Receiver pull-up resistor		45	50	55	Ω

Table 68. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		0		2,200	mV
V_{IH}	High-level input voltage		100		2,880	mV
V_{OL}	Low-level output voltage		1,450		1,650	mV
V_{OH}	High-level output voltage		2,175		2,420	mV
V_{ID}	Differential input voltage		100	600	970	mV
V_{OD}	Differential output voltage		525	800	970	mV

Table 69. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage		380	600	820	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	500	600	700	mV
V_{ID}	Differential input voltage		300	600	900	mV
V_{ICM}	Input common mode voltage		450	600	750	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Table 70. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 71. PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 72. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(10)*			0.65	V

Table 73. GTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.14	1.2	1.26	V
V_{REF}	Reference voltage		0.74	0.8	0.86	V
V_{IH}	High-level input voltage		V_{REF} + 0.05			V
V_{IL}	Low-level input voltage				V_{REF} – 0.05	V
V_{OL}	Low-level output voltage	I_{OL} = 40 mA *(10)*			0.4	V

Table 74. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(10)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(10)*			V_{TT} – 0.475	V

Table 75. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(10)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(10)*			V_{TT} – 0.630	V

Table 76. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(10)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(10)*			V_{TT} – 0.57	V

Table 77. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(10)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(10)*			V_{TT} – 0.76	V

Table 78. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(10)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(10)*			V_{TT} – 0.6	V

Table 79. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(10)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(10)*			V_{TT} – 0.8	V

Table 80. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			$0.1 \times V_{CCIO}$	V

Table 81. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			$0.1 \times V_{CCIO}$	V

Table 82. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(10)*			0.4	V

Table 83. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(10)*			0.4	V

Table 84. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 85. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤ V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 86. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)			30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)			–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}				200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}				–200		–300		–500	µA

Table 87. Stratix GX Device Capacitance

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
C_{IN}	Input capacitance on I/O pins in banks 1, 2, 5, and 6	V_{IN} = 0 V, f = 1.0 MHz			pF
	Input capacitance on I/O pins in banks 3, 4, 7, and 8	V_{IN} = 1.0 V, f = 1.0 MHz			
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF

Notes to Tables 58 – 87:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Conditions beyond those listed in Table 58 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –0.5 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.
(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.
(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.
(10) Drive strength is programmable according to values in Table 42 on page 150.
(11) V_{REF} specifies the center point of the switching range.

Power Consumption

Detailed power consumption information for Stratix GX devices will be released when available.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus II software displays an informational message during the design compilation if the timing models are preliminary. Table 88 shows the status of the Stratix GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 88. Stratix GX Device Timing Model Status

Device	Preliminary	Final
EP1SGX10	✓	
EP1SGX25	✓	
EP1SGX40	✓	

Performance

Table 89 shows Stratix GX performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

Table 89. Stratix GX Performance (Part 1 of 2) *Notes (1), (2)*

Applications		Resources Used			Performance			
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
LE	16-to-1 multiplexer *(3)*							ns
	32-to-1 multiplexer *(3)*							ns
	16-to-1 multiplexer *(4)*							MHz
	32-to-1 multiplexer *(4)*							MHz
	16-bit counter							MHz
	64-bit counter							MHz
TriMatrix memory M512 block	Simple dual-port RAM 32 × 18 bit							MHz
	FIFO 32 × 18 bit							MHz
TriMatrix memory M4K block	Simple dual-port RAM 128 × 36 bit							MHz
	True dual-port RAM 128 × 36 bit							MHz
	FIFO 128 × 36 bit							MHz

Table 89. Stratix GX Performance (Part 2 of 2) *Notes (1), (2)*

Applications		Resources Used			Performance			
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	Units
TriMatrix memory M-RAM block	Simple dual-port RAM 4K × 144 bit							MHz
	True dual-port RAM 8K × 72 bit							MHz
DSP block	9 × 9-bit multiplier *(5)*	0	0	1		281		MHz
	18 × 18-bit multiplier *(5)*	0	0	1		232		MHz
	36 × 36-bit multiplier *(5)*	0	0	1		135		MHz
	36 × 36-bit multiplier *(6)*	0	0	1		232		MHz
	18-bit, 4-tap FIR filter	0	0	1				
Larger designs	8-bit, 16-tap parallel FIR filter							MHz
	8-bit, 512-point FFT function							MHz

Notes to Table 89:

(1) These design performance numbers were obtained using the Quartus II software.
(2) Numbers not listed will be included in a future version of this data sheet.
(3) This performance number reflects the combinatorial input and output path without pins.
(4) This application uses registered inputs and outputs.
(5) This application uses registered input and output stages within the DSP block.
(6) This application uses registered input, pipeline, and output stages within the DSP block.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 90 through 96 describe the Stratix GX device internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 90. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 91. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	IOE input and output register setup time before clock
t_{H}	IOE input and output register hold time after clock
t_{CO}	IOE input and output register clock-to-output delay
t_{COOUT}	IOE output register clock-to-output delay
$t_{PIN2COMBOUT}$	Input pin to IOE combinatorial output
$t_{COMBIN2PIN}$	IOE data input to combinatorial output
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 92. DSP Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	Input, pipeline, and output register setup time before clock
t_{H}	Input, pipeline, and output register hold time after clock
t_{CO}	Input, pipeline, and output register clock-to-output delay
$t_{INREG2PIPE18}$	Input Register to DSP Block pipeline register in 18 × 18-bit mode
$t_{INREG2PIPE9}$	Input Register to DSP Block pipeline register in 9 × 9-bit mode
$t_{PIPE2OUTREG2ADD}$	DSP Block Pipeline Register to output register delay in Two-Multipliers Adder mode
$t_{PIPE2OUTREG4ADD}$	DSP Block Pipeline Register to output register delay in Four-Multipliers Adder mode
t_{PD9}	Combinatorial input to output delay for 9 × 9
t_{PD18}	Combinatorial input to output delay for 18 × 18
t_{PD36}	Combinatorial input to output delay for 36 × 36
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Minimum clock high or low time

Table 93. M512 Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Minimum clock high or low time
$t_{M512CLR}$	Minimum clear pulse width
$t_{M512PRE}$	Minimum preset pulse width

Table 94. M4K Block Internal Timing Microparameter Descriptions

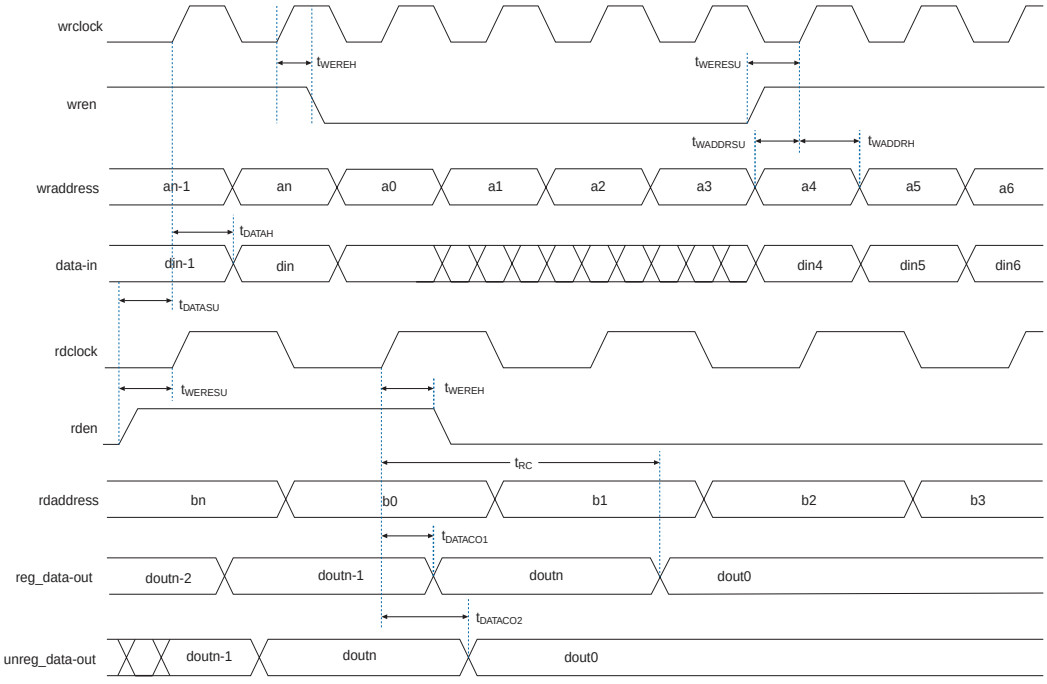
Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATASU}$	Data setup time before clock
$t_{M4KDATAH}$	Data hold time after clock
$t_{M4KWADDRSU}$	Write address setup time before clock
$t_{M4KWADDRH}$	Write address hold time after clock
$t_{M4KRADDRSU}$	Read address setup time before clock
$t_{M4KRADDRH}$	Read address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Minimum clock high or low time
t_{M4KCLR}	Minimum clear pulse width
t_{M4KPRE}	Minimum preset pulse width

Table 95. M-RAM Block Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{MEGARC}	Synchronous read cycle time
t_{MEGAWC}	Synchronous write cycle time
$t_{MEGAWERESU}$	Write or read enable setup time before clock
$t_{MEGAWEREH}$	Write or read enable hold time after clock
$t_{MEGABESU}$	Byte enable setup time before clock
$t_{MEGABEH}$	Byte enable hold time after clock
$t_{MEGADATASU}$	Data setup time before clock
$t_{MEGADATAH}$	Data hold time after clock
$t_{MEGAWADDRSU}$	Write address setup time before clock
$t_{MEGAWADDRH}$	Write address hold time after clock
$t_{MEGARADDRSU}$	Read address setup time before clock
$t_{MEGARADDRH}$	Read address hold time after clock
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers
$t_{MEGADATACO2}$	Clock-to-output delay without output registers
$t_{MEGACLKHL}$	Minimum clock high or low time
$t_{MEGACLR}$	Minimum clear pulse width
$t_{MEGAPRE}$	Minimum preset pulse width

Table 96. Routing Delay Internal Timing Microparameter Descriptions	
Symbol	**Parameter**
t_{R4}	Delay for an R4 line with one load; covers a distance of four LAB columns
t_{R8}	Delay for an R8 line with one load; covers a distance of eight LAB columns
t_{R24}	Delay for an R24 line with one load; covers a distance of 24 LAB columns
t_{C4}	Delay for an C4 line with one load; covers a distance of four LAB rows
t_{C8}	Delay for an C8 line with one load; covers a distance of eight LAB rows
t_{C16}	Delay for an C24 line with one load; covers a distance of 16 LAB rows
t_{LOCAL}	Local interconnect delay

Figure 86 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 93 through 95 above.

Figure 86. Dual-Port RAM Timing Microparameter Waveform



Tables 97 through 103 show the internal timing microparameters for all Stratix GX devices.

Table 97. LE Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
t_{SU}						
t_{H}						
t_{CO}						
t_{LUT}						
t_{CLR}						
t_{PRE}						
t_{CLKHL}						

Table 98. IOE Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
t_{SU}						
t_{H}						
t_{CO}						
t_{COOUT}						
$t_{PIN2COMBOUT}$						
$t_{COMBIN2PIN}$						
t_{CLR}						
t_{PRE}						
t_{CLKHL}						

Table 99. DSP Block Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
t_{SU}						
t_{H}						
t_{CO}						
$t_{INREG2PIPE18}$						
$t_{INREG2PIPE9}$						
$t_{PIPE2OUTREG2ADD}$						
$t_{PIPE2OUTREG4ADD}$						
t_{PD9}						
t_{PD18}						
t_{PD36}						
t_{CLR}						
t_{PRE}						
t_{CLKHL}						

Table 100. M512 Block Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
$t_{M512WESU}$						
$t_{M512RESU}$						
$t_{M512BESU}$						
$t_{M512DATASU}$						
$t_{M512RDADDRSU}$						
$t_{M512WRADDRSU}$						
$t_{M512DATACO1}$						
$t_{M512DATACO2}$						
$t_{M512CLKHL}$						
$t_{M512CLR}$						
$t_{M512PRE}$						

Table 101. M4K Block Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
$t_{M4KWESU}$						
$t_{M4KRESU}$						
$t_{M4KBESU}$						
$t_{M4KDATASU}$						
$t_{M4KRDADDRSU}$						
$t_{M4KWRADDRSU}$						
$t_{M4KDATACO1}$						
$t_{M4KDATACO2}$						
$t_{M4KCLKHL}$						
t_{M4KCLR}						
t_{M4KPRE}						

Table 102. M-RAM Block Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
$t_{MEGAWESU}$						
$t_{MEGARESU}$						
$t_{MEGABESU}$						
$t_{MEGADATASU}$						
$t_{MEGARDADDRSU}$						
$t_{MEGAWRADDRSU}$						
$t_{MEGADATACO1}$						
$t_{MEGADATACO2}$						
$t_{MEGACLKHL}$						
$t_{MEGACLR}$						
$t_{MEGAPRE}$						

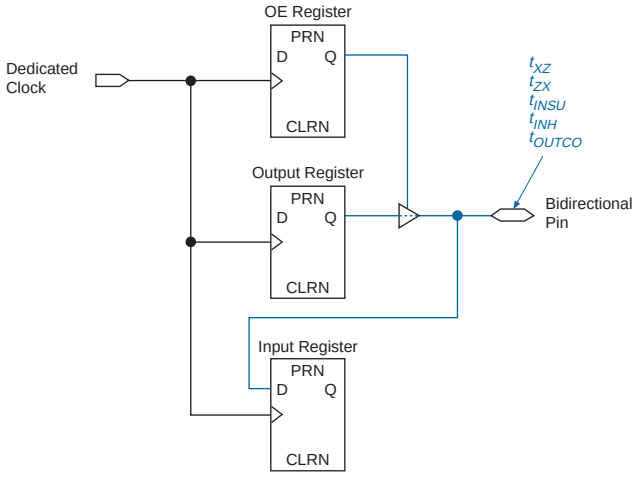
Table 103. Routing Delay Internal Timing Microparameters

Symbol	-5		-6		-7	
	Min	Max	Min	Max	Min	Max
t_{R4}						
t_{R8}						
t_{R24}						
t_{C4}						
t_{C8}						
t_{C16}						
t_{LOCAL}						

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 87 shows the timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 87. External Timing in Stratix GX Devices



All external I/O timing parameters shown are for 3.3-V LVTTL or LVCMOS I/O standards with the maximum current strength. For external I/O timing using standards other than LVTTL or LVCMOS use the I/O standard input and output delay adders in Tables 116 through 118.

Table 104 shows the external I/O timing parameters when using fast regional clock networks.

Table 104. Stratix GX Fast Regional Clock External I/O Timing Parameters Notes (1), (2)		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with fast regional clock fed by FCLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with fast regional clock fed by FCLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with fast regional clock fed by FCLK pin	
t_{XZ}	Synchronous column IOE output enable register to output pin disable delay using fast regional clock fed by FCLK pin	
t_{ZX}	Synchronous column IOE output enable register to output pin enable delay using fast regional clock fed by FCLK pin	

Notes to Table 104:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device and speed grade and whether it is t_{CO} or t_{SU}. Designers should use the Quartus II software to verify the external timing for any pin.

Table 105 shows the external I/O timing parameters when using regional clock networks.

Table 105. Stratix GX Regional Clock External I/O Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock fed by CLK pin	
t_{XZ}	Synchronous column IOE output enable register to output pin disable delay using regional clock fed by CLK pin	
t_{ZX}	Synchronous column IOE output enable register to output pin enable delay using regional clock fed by CLK pin	
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with regional clock fed by Enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with regional clock Enhanced PLL with default phase setting	
t_{XZPLL}	Synchronous column IOE output enable register to output pin disable delay using regional clock fed by Enhanced PLL with default phase setting	
t_{ZXPLL}	Synchronous column IOE output enable register to output pin enable delay using regional clock fed by Enhanced PLL with default phase setting	

Notes to Table 105:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. Designers should use the Quartus II software to verify the external timing for any pin.

Table 106 shows the external I/O timing parameters when using global clock networks.

Table 106. Stratix GX Global Clock External I/O Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions
t_{INSU}	Setup time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{INH}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by CLK pin	
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock fed by CLK pin	
t_{XZ}	Synchronous column IOE output enable register to output pin disable delay using global clock fed by CLK pin	
t_{ZX}	Synchronous column IOE output enable register to output pin enable delay using global clock fed by CLK pin	
$t_{INSUPLL}$	Setup time for input or bidirectional pin using column IOE input register with global clock fed by Enhanced PLL with default phase setting	
t_{INHPLL}	Hold time for input or bidirectional pin using column IOE input register with global clock fed by enhanced PLL with default phase setting	
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using column IOE output register with global clock enhanced PLL with default phase setting	
t_{XZPLL}	Synchronous column IOE output enable register to output pin disable delay using global clock fed by enhanced PLL with default phase setting	
t_{ZXPLL}	Synchronous column IOE output enable register to output pin enable delay using global clock fed by enhanced PLL with default phase setting	

Notes to Table 106:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column IOE pins. Row IOE pins are 100- to 250-ps slower depending on device, speed grade, and the specific parameter in question. Designers should use the Quartus II software to verify the external timing for any pin.

Tables 107 through 109 show the external timing parameters for EP1SGX10 devices.

Table 107. EP1SGX10 Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							

Table 108. EP1SGX10 Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

Table 109. EP1SGX10 Global Clock External I/O Timing Parameters							
Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

Tables 110 through 112 show the external timing parameters for EP1SGX25 devices.

Table 110. EP1SGX25 Fast Regional Clock External I/O Timing Parameters							
Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							

Table 111. EP1SGX25 Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

Table 112. EP1SGX25 Global Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

Tables 113 through 115 show the external timing parameters for EP1SGX40 devices.

Table 113. EP1SGX40 Fast Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							

Table 114. EP1SGX40 Regional Clock External I/O Timing Parameters

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

Table 115. EP1SGX40 Global Clock External I/O Timing Parameters							
Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}							
t_{INH}							
t_{OUTCO}							
t_{XZ}							
t_{ZX}							
$t_{INSUPLL}$							
t_{INHPLL}							
$t_{OUTCOPLL}$							
t_{XZPLL}							
t_{ZXPLL}							

External Delay Parameters

External delay parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density.

Tables 116 through 118 show the adder delays associated with I/O standards. If the designer selects an I/O standard other than LVTTL/LVCMOS, add the selected delay to the external t_{CO} and t_{SU} I/O parameters shown in Tables 97 through 103.

Table 116. Stratix GX I/O Standard Input Delay Adders

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS							
3.3-V LVTTL							
2.5-V LVTTL							
1.8-V LVTTL							
1.5-V LVTTL							
GTL LVTTL							
GTL+							
3.3-V PCI							
3.3-V PCI-X							
Compact PCI							
AGP 1×							
AGP 2×							
CTT							
SSTL-3 class I							
SSTL-3 class II							
SSTL-2 class I							
SSTL-2 class II							
SSTL-18 class I							
SSTL-18 class II							
HSTL class I							
HSTL class II							
LVDS							
LVPECL							
3.3-V PCML							
HyperTransport							

Table 117. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate (Part 1 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA							
	4 mA							
	8 mA							
	12 mA							
	24 mA							
3.3-V LVTTL	4 mA							
	8 mA							
	12 mA							
	16 mA							
	24 mA							
2.5-V LVTTL	2 mA							
	8 mA							
	12 mA							
	16 mA							
1.8-V LVTTL	2 mA							
	8 mA							
	12 mA							
1.5-V LVTTL	2 mA							
	4 mA							
	8 mA							
GTL								
GTL+								
3.3-V PCI								
3.3-V PCI-X								
Compact PCI								
AGP 1×								
AGP 2×								
CTT								
SSTL-3 class I								
SSTL-3 class II								
SSTL-2 class I								
SSTL-2 class II								
SSTL-18 class I								
SSTL-18 class II								
HSTL class I								

Table 117. Stratix GX I/O Standard Output Delay Adders for Fast Slew Rate (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
HSTL class II							
LVDS							
LVPECL							
3.3-V PCML							
HyperTransport							

Table 118. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate (Part 1 of 2)

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA							
	4 mA							
	8 mA							
	12 mA							
	24 mA							
3.3-V LVTTL	4 mA							
	8 mA							
	12 mA							
	16 mA							
	24 mA							
2.5-V LVTTL	2 mA							
	8 mA							
	12 mA							
	16 mA							
1.8-V LVTTL	2 mA							
	8 mA							
	12 mA							
1.5-V LVTTL	2 mA							
	4 mA							
	8 mA							
GTL								
GTL+								
3.3-V PCI								
3.3-V PCI-X								
Compact PCI								

Table 118. Stratix GX I/O Standard Output Delay Adders for Slow Slew Rate (Part 2 of 2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
AGP 1×							
AGP 2×							
CTT							
SSTL-3 class I							
SSTL-3 class II							
SSTL-2 class I							
SSTL-2 class II							
SSTL-18 class I							
SSTL-18 class II							
HSTL class I							
HSTL class II							
LVDS							
LVPECL							
3.3-V PCML							
HyperTransport							

Table 119 shows the adder delays for the IOE programmable delays. These delays are controlled with the Quartus II software options listed in the Parameter column.

Table 119. Stratix GX IOE Programmable Delays

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	On							
	Small							
	Medium							
	Large							
Decrease input delay to input register	On							
Decrease input delay to output register	On							
Increase delay to output pin	On							
Increase delay to output enable pin	On							
Increase output clock enable delay	On							
Increase input clock enable delay	On							
Increase t_{ZX} delay to output pin	On							
Increase output enable clock enable delay	On							

PLL Timing

Table 120 describes the Stratix GX device enhanced PLL specifications.

Table 120. Enhanced PLL Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency *(1)*	3		462	MHz
$f_{IN\ DUTY}$	Input clock duty cycle	40		60	%
$f_{EIN\ DUTY}$	External feedback clock input duty cycle	40		60	%
$t_{IN\ JITTER}$	Input clock cycle-to-cycle jitter			±150	ps
$t_{EIN\ JITTER}$	External feedback clock cycle-to-cycle jitter			±150	ps
t_{FCOMP}	External feedback clock compensation time *(2)*			6	ns
f_{OUT}	PLL output frequency	0.6		462	MHz
$t_{OUT\ DUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	PLL external clock cycle-to-cycle output jitter *(3)*			±100	ps
t_{DLOCK}	Time required to lock dynamically (after switchover or counter value change)	*(4)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration	10		1,000	µs
f_{VCO}	PLL internal VCO operating range	300		800	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	150		500	kHz
% spread	Percentage spread for spread spectrum frequency *(5)*		0.5		%

Notes to Table 120:

(1) Actual PLL performance depends on the settings made.
(2) t_{FCOMP} can also equal 50% of the input clock period multiplied by n.
(3) Actual jitter performance may vary based on the system configuration.
(4) Lock time is a function of PLL configuration and may be significantly faster.
(5) Exact, user-controllable value depends on the PLL settings.

Table 121 describes the Stratix GX device fast PLL specifications.

Table 121. Fast PLL Specifications

Symbol	Parameter	Min	Max	Unit
f_{IN} *(1)*	CLKIN frequency (for *m* = 9, 10)	33	84	MHz
	CLKIN frequency (for *m* = 7, 8)	43	105	MHz
	CLKIN frequency (for *m* = 4, 5, 6)	75	140	MHz
	CLKIN frequency (for *m* = 2)	150	420	MHz
	CLKIN frequency (for *m* = 1)	300	644.5	MHz
t_{INDUTY}	CLKIN duty cycle	40	60	%
$t_{INJITTER}$	Cycle-to-cycle jitter for CLKIN pin		±100	ps
t_{DUTY}	Duty cycle for DFFIO 1× CLKOUT pin	40	60	%
t_{JITTER}	Cycle-to-cycle jitter for DIFFIO clock out *(2)*		±100	ps
	Cycle-to-cycle jitter for internal global or regional clock		±100	ps
t_{LOCK}	Time required for PLL to acquire lock	10	100	µs
f_{VCO}	VCO operating frequency	300	840	MHz
m *(3)*	Multiplication factors for *m* counter	1	32	Integer
*l*0, *l*1, *g*0 *(3)*	Multiplication factors for *l*0, *l*1, and *g*0 counter	1	32	Integer

Notes to Table 121:

(1) PLLs 7, 8, 9, and 10 support up to 462-MHz input clock frequency. PLLs 1, 2, 3, and 4 support up to 644.5-MHz input clock frequency on the CLK0, CLK2, CLK9, and CLK11 pins only.
(2) This parameter is for high-speed differential I/O mode only.
(3) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16. High-speed differential I/O mode supports 1, 2, 4, 8, or 10.

Software

Stratix GX devices are supported by the Altera Quartus II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® logic analysis, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows 2000/NT/98, Sun Solaris, Linux Red Hat v6.2 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Device Pin-Outs

Device pin-outs for Stratix GX devices will be released on the Altera web site (**www.altera.com**).

Ordering Information

Ordering information will be available in a future version of this data sheet.

Revision History

The information contained in the *Stratix GX FPGA Family Data Sheet* version 1.2 supersedes information published in previous versions.

Version 1.2

The following changes were made to the *Stratix GX FPGA Family Data Sheet* version 1.2: updated Table 1.

Version 1.1

The following changes were made to the *Stratix GX FPGA Family Data Sheet* version 1.1:

- Updated Table 2.
- Updated Figure 4.
- Updated Tables 53 and 54.

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