2.5V Wide-Range Frequency Clock Driver (60MHz – 200MHz)

Features

- Low skew; low jitter PLL clock driver.
- 1 to 10 differential clock distribution (SSTL_2).
- Feedback pins for input to output synchronization.
- PDB for power management.
- Spread spectrum tolerant inputs.
- Auto-PD when input signal removed.
- Choice of static phase offset for easy board tuning:
  - -XXX = device pattern number for options listed below:
  - PCV857-025 - 0 ps
  - PCV857-1300 - +50 ps

Product Description

This PLL clock buffer is designed for a V_{DD} of 2.5V, AV_{DD} of 2.5V and differential data input and output levels. ASM5CVF857 is a zero-delay buffer that distributes a differential clock input pair (CLK_INT, CLK_INC) to ten differential pairs of clock outputs (CLKT[0:9], CLKC[0:9]) and one differential pair feedback clock output (FB_OUT, FB_OUTC). The clock outputs are controlled by the input clocks (CLK_INT, CLKINC), the feedback clocks (FB_INT, FB_INC), the 2,5V LVCMOS input (PDB), and the analog power input (AV_{DD}). When input (PDB) is low while power is applied, the receivers are disabled, the PLL is turned off, and the differential clock outputs are tri-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

When the input frequency is less than the operating frequency of the PLL, approximately 20MHz, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as and when the PDB input is low. When the input frequency increases to greater than approximately 20MHz, the PLL will be turned back on, the inputs and outputs will be enabled, and the PLL will obtain phase lock between the feedback clock pair (FB_INT, FB_INC) and the input clock pair (CLK_INT, CLK_INC).

The PLL in the ASM5CVF857 clock driver uses the input clocks (CLK_INT, CLKINC) and the feedback clocks (FB_INT, FB_INC) to provide high-performance, low-skew, low-jitter output differential clocks (CLKT[0:9], CLKC[0:9]). ASM5CVF857 is also able to track spread spectrum clock (SSC) for reduced EMI.

ASM5CVF857 is characterized for operation from 0°C to 85°C.

Applications

- DDR Memory Modules / Zero Delay Board Fan Out.
- Provides complete DDR DIMM logic solution with ASM4SSTVF16857, ASM4SSTVF16859 & ASM4SSTVF32852.

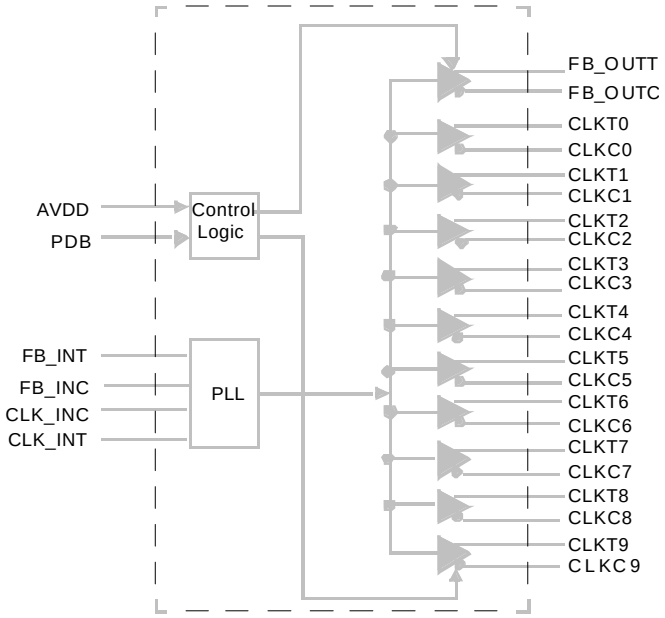
Specifications

- Meets PC3200 specification for DDR-I 400 support.
- Covers all DDRI speed grades.

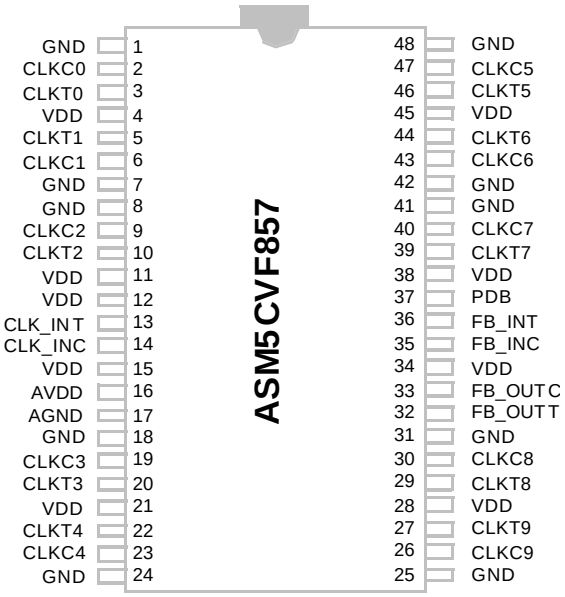
Switching Characteristics

- CYCLE-CYCLE jitter : <50ps.
- OUT-OUTPUT skew: <40ps.
- Period jitter: ±30ps.

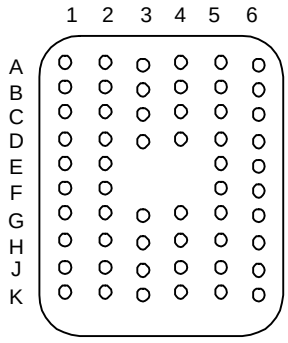
Block Diagram



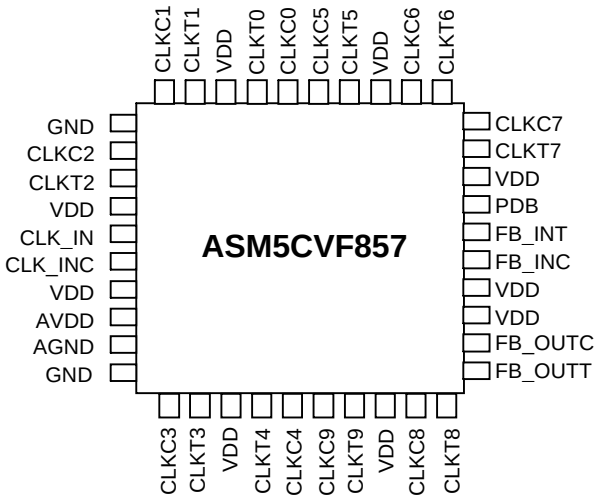
Pin Configuration



56-BALL BGA



56-BALL BGA
(SEE TABLE BELOW)



40-PIN MLF

	1	2	3	4	5	6
A	CLKT0	CLKC0	GND	GND	CLKC5	CLKT5
B	CLKC1	CLKT1	VDD	VDD	CLKT6	CLKC6
C	GND	GND	NC	NC	GND	GND
D	CLKT2	CLKC2	NC	NC	CLKC7	CLKC7
E	VDD	VDD	NB	NB	VDD	PDB
F	CLK_INT	CLK_INC	NB	NB	FB_INC	FB_INT
G	VDD	AVDD	NC	NC	FB_OUTC	VDD
H	AGND	GND	NC	NC	GND	FB_OUTT
J	CLKC3	CLKT3	VDD	VDD	CLKT8	CLKC8
K	CLKT4	CLKC4	GND	GND	CLKC9	CLKT9

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
4, 11, 12, 15, 21, 28, 34, 38, 45	VDD	P	Power supply, 2.5V
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	P	Ground.
16	AVDD	P	Analog power supply, 2.5V.
17	AGND	P	Analog ground.
27, 29, 39, 44, 46, 22, 20, 10, 5, 3	CLKT(9:0)	O	“True” clock of differential pair outputs.
26, 30, 40, 43, 47, 23, 19, 9, 6, 2	CLKC(9:0)	O	“Complementary” clocks of differential pair outputs.
14	CLK_INC	I	“Complementary” reference clock input.
13	CLK_INT	I	“True” reference clock input.
33	FB_OUTC	O	“Complementary” feedback output dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INC.
32	FB_OUTT	O	“True” feedback output dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
36	FB_INT	I	“True” feedback input provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.
35	FB_INC	I	“Complementary” feedback input provides signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.
37	PDB	I	Power down. LVCMOS input.

Functionality

Inputs				Outputs				PLL State
AVDD	PDB	CLK_INT	CLK_INC	CLKT	CLKC	FB_OUTT	FB_OUTC	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
2.5V (nom)	L	L	H	Z	Z	Z	Z	off
2.5V (nom)	L	H	L	Z	Z	Z	Z	off
2.5V (nom)	H	L	H	L	H	L	H	on
2.5V (nom)	H	H	L	H	L	H	L	on
2.5V (nom)	X	<20 MHz		Z	Z	Z	Z	off

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage (VDD and AVDD)	-0.5	3.6	V
Logic Inputs	GND - 0.5	VDD + 0.5	V
Ambient Operating Temperature	0	85	ûC
Storage Temperature	-65	150	ûC
These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged periods may affect device reliability.			

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0°76C to 85°C. Supply voltage AV_{DD} and V_{DD}=2.5V ± 0.2V (unless otherwise stated).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high current	I_{IH}	$V_I = V_{DD}$ or GND	5			µA
Input low current	I_{IL}	$V_I = V_{DD}$ or GND			5	µA
Operating supply current	I_{DDQ}	C_L = 0pF, R_L = 120Ω, F_{CLK_IN} = 200MHz			310	mA
	I_{DDPD}	PDB = GND, FCLK_IN=0MHz		100	200	µA
Supply Current on AVDD	I_{ADD}	F_{CLK_IN} = 200MHz		9	12	mA
Input clamp voltage	V_{IK}	V_{DDQ}=2.3V I_{IN} = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -100µA	V_{DD}-0.1			V
		I_{OH} = -12mA	1.7			V
Low-level output voltage	V_{OL}	I_{OL} = 100µA			0.1	V
		I_{OL} = 12mA			0.6	V
Input capacitance*	C_{IN}	V_I = GND or V_{DD}	2		3.5	pF
Input capacitance variation	$C_{I(\Delta)}$	V_{OUT} = GND or V_{DD}	-0.25		0.25	pF

***** Guaranteed by design at 200MHz; not 100% tested in production.

Recommended Operating Conditions

T_A = 0°C to 85°C. Supply voltage AV_{DD} and V_{DD}=2.5V ± 0.2V (unless otherwise stated).

Parameter**	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, A_{VDD}		2.3	2.5	2.7	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_INT, FB_INC		0.4	V_{DD}/2 - 0.18	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_INT, FB_INC	V_{DD}/2 + 0.18	2.1		V
		PDB	1.7		V_{DD} + 0.3	V
DC input signal voltage#	V_{IN}		-0.3		V_{DD} + 0.3	V
Differential input signal voltage$	V_{ID}	DC: CLK_INT, CLK_INC, FB_INT, FB_INC	0.36		V_{DD} + 0.6	V
		AC: CLK_INT, CLK_INC, FB_INT, FB_INC	0.7		V_{DD} + 0.6	V
Output differential cross voltage@	V_{OX}		V_{DD}/2 - 0.15		V_{DD}/2 + 0.15	V
Input differential cross voltage	V_{IX}		V_{DD}/2 - 0.2		V_{DD}/2 + 0.2	V
High-level output current	I_{OH}				-12	mA
Low-level output current	I_{OL}				12	mA
Operating free-air temperature	T_A		0		85	°C

**: Unused inputs must be held high or low to prevent them from floating.
#: DC input signal voltage specifies the allowable DC execution of differential
$: Differential inputs signal voltages specify the differential voltage [VTR-VCP] required for switching where VTR is the true input level and VCT is the complementary input level.
@: Differential cross-point voltage is expected to track variations of V_{DD} and is the voltage at which the differential signal must be crossing.

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Timing Requirements**

Parameter	Symbol	Conditions	Min	Max	Units
Operating clock frequency	$freq_{op}$	2.5V ± 0.2V	60	220	MHz
Application Frequency Range	$freq_{app}$	2.5V ± 0.2V	95	220	MHz
Input clock duty cycle	d_{tin}		40	60	%
CLK stabilization	T_{STAB}			100	µs

Switching Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low-to-high level propagation delay time	t_{PLH}*	CLK_IN to any output		3.5		ns
High-to-low level propagation delay time	t_{PHL}*	CLK_IN to any output		3.5		ns
Output enable time	t_{en}	PDB to any output		3		ns
Output disable time	t_{dis}	PDB to any output		3		ns
Period Jitter	$t_{jit(per)}$	100MHz to 200MHz	-30		30	ps
Half-period jitter	$t_{jit(hper)}$	100MHz to 200MHz	-75		75	ps
Input clock slew rate	$t_{sl(I)}$		1		4	v/ns
Output clock slew rate	$t_{sl(o)}$	100/133/167/200 MHz	1		2	v/ns
Cycle-to-cycle jitter	t_{cyc}-t_{cyc}	100 MHz to 200MHz	-50		50	ps
Static phase offset	$t_{(phase\ error)}$#		-50	0	50	ps
Output-to-output skew	t_{skew}			40	60	ps
The PLL on the ASM5CVF857 is capable of meeting all the above parameters while supporting SSC synthesizers with the following parameters.						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		-0.50	%
	PLL loop bandwidth		2			MHz
	Phase angle				-0.031	°

*: Refers to transition on non-inverting output in PLL bypass mode.
#: Static phase offset does not include jitter.

** T_A = 0 – 85°C. Supply voltage AV_{DD}, V_{DD}=2.5V ± 0.2V (unless otherwise stated).

Note: While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/tC where the cycle (t_C) decreases as the frequency goes up.

Note: Switching characteristics guaranteed for application frequency range.

Parameter Measurement Information

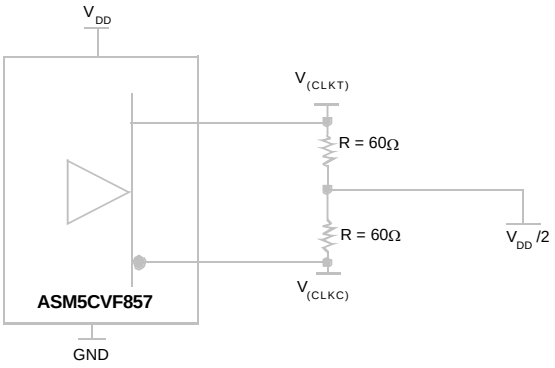


Figure 1: IBIS Model Output Load

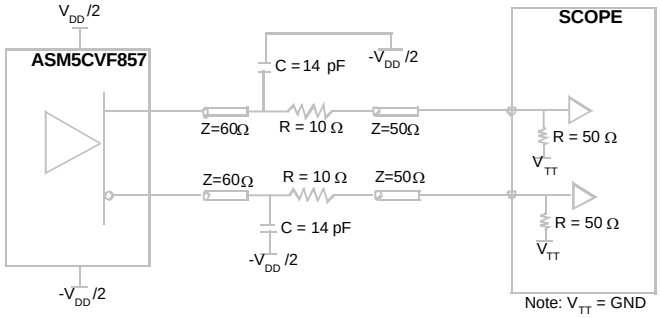


Figure 2: Output Load Test Circuit

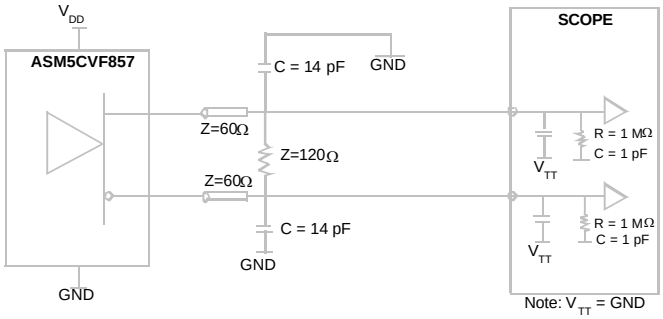


Figure 3: Output Load Test Circuit for Crossing Point

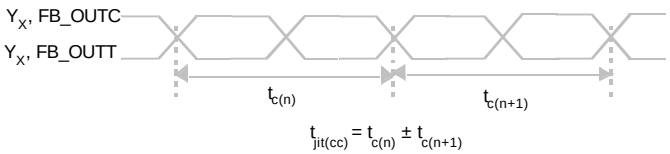
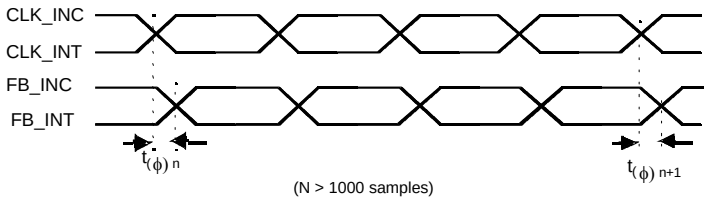


Figure 4: Cycle-to-Cycle Jitter Period



(N > 1000 samples)

Figure 5: Static Phase Offset

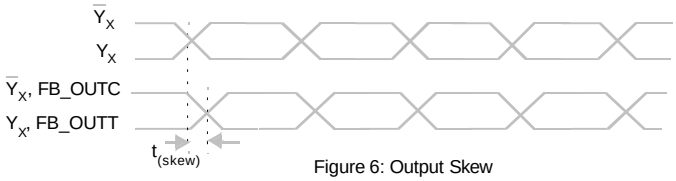
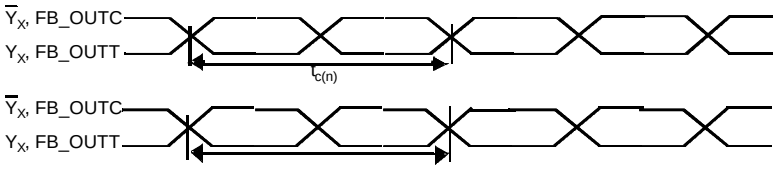
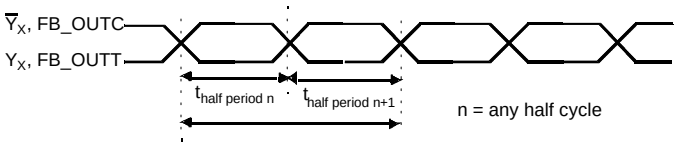


Figure 6: Output Skew



f_o= average input frequency measured at CLK_INT/CLK_INC

Figure 7: Period Jitter



f_o= average input frequency measured at CLK_INT/CLK_INC

Figure 8: Half-Period Jitter

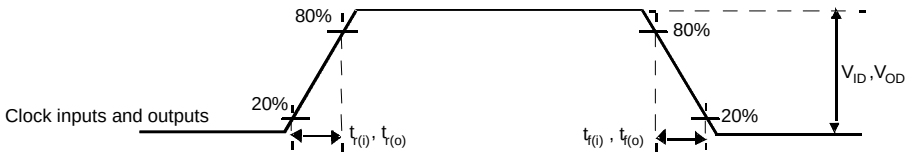


Figure 9: Input and Output Slew rates

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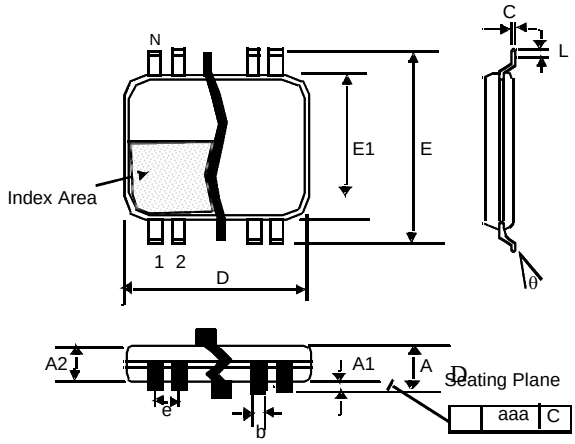
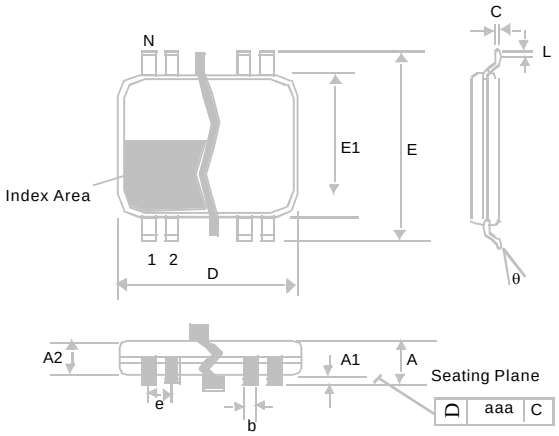
Package Dimensions (6.10mm (240 mil) body, 0.50mm (0.020 mil) pitch TSSOP)



Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.20	-	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.0035	0.008
D	See Variations			
E	8.10 Basic		0.319 Basic	
E1	6.00	6.20	0.236	0.244
e	0.50 Basic		0.20 Basic	
L	0.45	0.75	0.018	0.030
N	See Variations			
θ	0°	8°	0°	8°
aaa	-	0.10	-	0.004

	D (MM)		D(inch)	
	Min	Max	Min	Max
48	12.40	12.60	0.488	0.496

Package Dimensions (4.40mm (1713 mil) body, 0.40 mm (16 mil) pitch TVSOP)



Symbol	Dimensions (mm)		Dimensions (inches)	
	Min	Max	Min	Max
A	-	1.20	-	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.0035	0.008
D	See Variations			
E	8.10 Basic		0.319 Basic	
E1	6.00	6.20	0.236	0.244
e	0.50 Basic		0.20 Basic	
L	0.45	0.75	0.018	0.030
N	See Variations			
θ	0°	8°	0°	8°
aaa	-	0.10	-	0.004

N	D (MM)		D(inch)	
	Min	Max	Min	Max
48	12.40	12.60	0.488	0.496

Ordering Codes

Ordering Number	Marking	Package Type	Quantity Per Reel	Temperature
ASM5CVF857-48TT	AS5CVF857T	48-pin TSSOP, tube		0°C to 70°C
ASM5CVF857-48TR	AS5CVF857T	48-pin TSSOP, tape & reel	2500	0°C to 70°C
ASM5CVF857-48VT	AS5CVF857V	48-pin TVSOP, tube		0°C to 70°C
ASM5CVF857-48VR	AS5CVF857V	48-pin TVSOP, tape & reel	2500	0°C to 70°C
ASM5CVF857-56BT	AS5CVF857B	56-pin Ball BGA, tube		0°C to 70°C
ASM5CVF857-56BR	AS5CVF857B	56-pin Ball BGA, tape & reel	2500	0°C to 70°C
ASM5CVF857-40QT	AS5CVF857M	40-pin QFN, tube		0°C to 70°C
ASM5CVF857-40QR	AS5CVF857M	40-pin QFN, tape & reel	2500	0°C to 70°C

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Advance Information
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