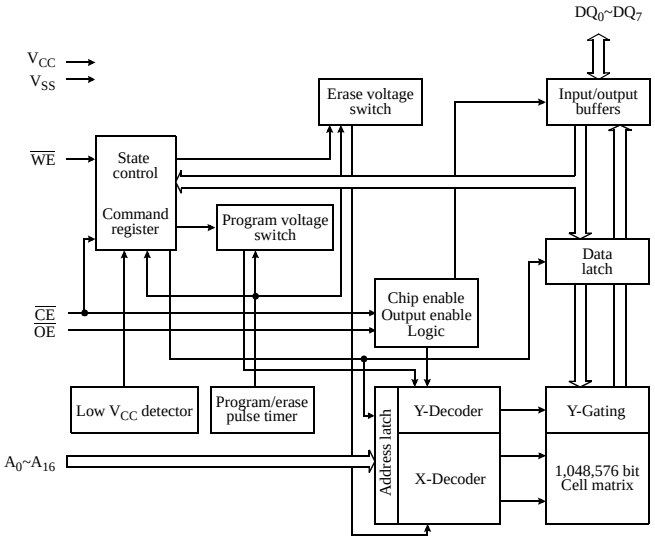
5V 128K×8 CMOS Flash EEPROM

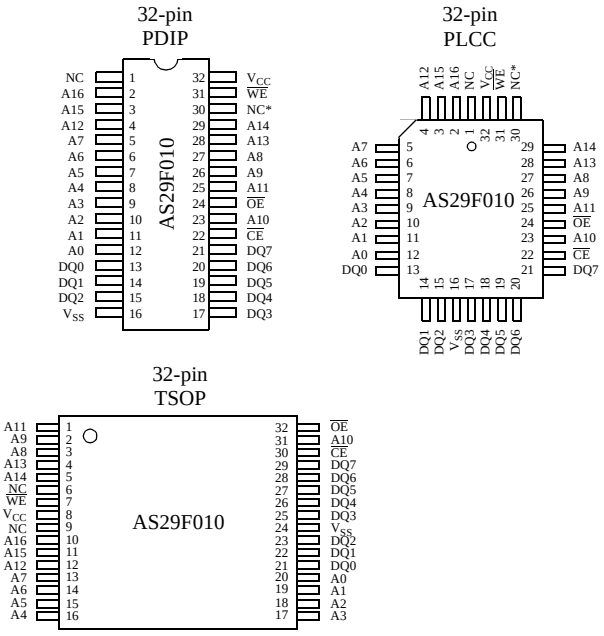
Features

- Organization: 128K × 8 bits
- Sector Erase architecture
  - Four 32K × 8 sectors
- Single 5.0±0.5V power supply for read/write operations
- High speed 120/150 ns address access time
- Low power consumption:
  - 30 mA maximum read current
  - 50 mA maximum program current
  - 1.5 mA maximum standby current
  - 1 mA maximum standby current (low power)
- 10,000 write/erase cycle endurance
- JEDEC standard write cycle commands
  - protects data from accidental changes
- Program/erase cycle end signals:
  - $\overline{\text{Data}}$ polling
  - DQ6 toggle
- Low V_{CC} write lock-out below 3.2V
- JEDEC standard packages and pinouts:
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP

Logic block diagram



Pin arrangement



Selection guide

		AS29F010-120	AS29F010-150	Unit
Maximum access time	t_{AA}	120	150	ns
Chip enable access time	t_{CE}	120	150	ns
Output enable access time	t_{OE}	50	50	ns

Functional description

The AS29F010 is a high performance 1 megabit 5 volt-only Flash memory organized as 128K bytes of 8 bits each. It is divided into four sectors of 32K bytes each. Each sector is separately erased and programmed without affecting data in the other sectors. All program, erase, and verify operations are 5-volt only, and require no external 12V supply pin. All required features for in-system programmability are provided.

The AS29F010 provides high performance with a maximum access time of 120, or 150 ns. Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and Write Enable ($\overline{WE}$) pins allow easy interface with the system bus.

Program, erase, and verify operations are controlled with an on-chip command register using a JEDEC standard Write State Machine approach to enter commands. Each command requires four write cycles to be executed. Address and data are latched internally during all write, erase, and verify operations, and an internal timer terminates each command. The chip has a typical timer period of 200 µs for all commands but Erase, which has a typical period of 800 ms. Under nominal conditions, a sector can be completely programmed and verified in less than 12 seconds. To program, erase, and verify a sector typically takes less than 18 seconds.

Data protection is provided by a low-V_{CC} lockout and by error checking in the Write State Machine. $\overline{DATA}$ polling and Toggle Bit modes are used to show that the chip is executing a command when the AS29F010 is read during a write or erase operation. After Erase or Program commands, Verify-1 and Verify-0 command modes ensure sufficient margin for reliable operation. (See command summary on page 5.)

The AS29F010 is packaged in 32-pin DIP, PLCC and TSOP packages with JEDEC standard pinouts for one megabit Flash memories.

Array architecture and data polarity

The array consists of 128K (131,072) bytes divided into four sectors of 32K bytes each. Addresses A15 and A16 select the four sectors:

Sector	Address range
0	00000h–07FFFh
1	08000h–0FFFFh
2	10000h–17FFFh
3	18000h–1FFFFh

Address pins	Function
A0–A5	CA: Column addresses 00–3Fh
A6–A14	RA: Row addresses 000–1FFh
A15–A16	SA: Sector addresses 0–3h

The AS29F010 is shipped in the erased state with all bits set to 1. Programmed bits are set to 0. Data is programmed into the array one byte at a time. All programmed bits remain set to 0 until the sector is erased and verified using the Sector Erase and Verify algorithm. Erase returns all bytes in a 32K sector to the erased state FFh, or all bits set to 1. Each sector is erased individually with no effect on the other sectors.

Operating modes

The AS29F010 is controlled by a Write State Machine (WSM) that interprets and executes commands. At power-up the WSM is reset to normal read mode. Once a command is initiated by writing data into the DQ pins with the $\overline{WE}$ pin, the WSM enters the command mode and keeps the chip powered up until the command is finished. After the command is terminated by the internal timer, the WSM returns to the normal read mode.

Mode table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A9	DQ
Read	L	L	H	A0	A9	D_{OUT}
Output disable	L	H	H	X	X	High Z
Standby	H	H	H	X	X	High Z
Mfr. code	L	L	H	L	Vh	52h
Device code	L	L	H	H	Vh	CODE (03h,04h,06h)
Write command	L	H	L	A0	A9	D_{IN}

†Key: L =Low (<VIL); H = High (>VIH); Vh = 11.5–12.5V; X =Don't care

Read mode: Selected with CE and OE low, WE high. Data is valid tAA after addresses are stable, tCE after CE is low and tOE after OE is low.

Output disable: Part remains powered up; but outputs disabled with OE pulled high.

Standby: Part is powered down, and ICC reduced to 1.5 mA for TTL input levels (<1.0 mA for CMOS input levels).

Mfr. (manufacturer) code, Device code: Selected by A9 = 11.5–12.5V. When CE and OE are pulled low the outputs are enabled and a data byte is read out. When A0 is pulled low the output data = 52h, a unique Mfr. code for Alliance Semiconductor Flash products. When A0 is high DOUT = 03h,04h, 06h, the Alliance device codes for the AS29F010.

Write command: Selected by CE and WE pulled low, OE pulled high. Initiates command mode in the WSM and latches addresses and data into the chip. Once a write command starts, the WSM stays in command mode until the command is completed or it times out. Addresses are latched on the falling edge of $\overline{WE}$ and $\overline{CE}$, whichever occurs later; data is latched on the rising edge o $\overline{WE}$ and $\overline{CE}$, whichever occurs first. The $\overline{WE}$ signal is filtered to prevent spurious events from being detected as write commands.

Command format

All commands require four bus write cycles to execute. After four write cycles the command is executed until terminated by the i nternal timer. For verify commands a read operation after $Write_{[4]}$ in a write command bus cycle reads out the data from thearray. For manufacturer and device code commands the ID code is read out. For other operations a read operation reads out a status byte on the outputs.

	Address in	Data in
Bus $write_{[1]}$	5555h	AAh
Bus $write_{[2]}$	2AAAh	55h
Bus $write_{[3]}$	5555h	Command code
Bus $write_{[4]}$	Address in	Data in
Bus read	Address in	D_{OUT}

Command timeout: For each operation the address and data are latched at bus $Write_{[4]}$ and held until the operation completes and times-out. After time-out the WSM returns the AS29F010 to normal mode. Each individual operation requires the 4-cycle write command sequence to execute. The AS29F010 does not remain in command mode after time-out. When a command times-out only the error flag is not reset.

Errors and timeout: Any of the following conditions sets the error flag.

- Any write command which does not match the sequence above for $Write_{[1]}$. $Write_{[2]}$, and $Write_{[3]}$.
- Any write cycle that follows more than 150 µs after the previous write cycle.
- The command $Data_{[3]}$ in $Write_{[3]}$ has more than one bit set high. This indicates conflicting commands.
- V_{CC} drops below V_{LKO} during command execution.

Once the error flag is set, the AS29F010 times out and returns to normal Readmode. The error flag remains until it is cleared by a reset command. The error flag can be read by executing a status command and reading the status byte.

Command codes and time out

The Command Code table displays the bus cycles required for each command mode. Read delay is the minimum delay after $Write_{[4]}$ during a write command bus cycle before a valid read may be executed. Timeout indicates the maximum delay before the WSM returns the AS29F010 to normal mode. Erase has a longer timeout than the other modes. Status byte can be read almost immediately after a $Write_{[4]}$, but the verify commands require a 25 µs delay to read valid data.

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Command code table

Mode	$D_{IN[3]}$ $Write_{[3]}$ data	$A_{IN[4]}$ $Write_{[4]}$ address	$D_{IN[4]}$ data	Read address	Read data		Read delay	Maximum time out
Reset	00h	x	x	0000h	Status		100 ns	250 µs
Status	01h	x	x	0000h	Status		100 ns	250 µs
ID Read code	02h	0000h 0001h	x x	0000h 0001h	Mfr. code Device code	52h 04h	100 ns 100 ns	250 µs
Verify-0	04h	A_{IN}	x	A_{IN}	D_{OUT}		25 µs	250 µs
Verify-1	08h	A_{IN}	x	A_{IN}	D_{OUT}		25 µs	250 µs
Converge	10h	A_{IN}	00h	A_{IN}	Status		100 ns	250 µs
Program	40h	A_{IN}	D_{IN}	A_{IN}	Status		100 ns	250 µs
Erase	80h	A_{IN}	FFh	A_{IN}	Status		100 ns	1000 µs

Command algorithms

Individual write commands are used together in eight program and erase algorithms to guarantee the AS29F010 operating margins for the life of the part. Refer to the AS29F010 Programming Specification for details on the algorithms for program and erase operation .

Recommended operating conditions

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	-	V_{CC} + 1.0	V
	V_{IL}	–0.5	-	0.8	V

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage (Input or DQ pin)	V_{IN}	–1.0	V_{CC} + 1.0	V
Input voltage (A9 pin)	V_{IN}	–1.0	+13.0	V
Output voltage	V_{OUT}	–1.0	V_{CC} + 1.0	V
Power supply voltage	V_{CC}	+4.5	+5.5	V
Operating temperature	T_{OPR}	–55	+125	°C
Storage temperature (plastic)	T_{STG}	–65	+125	°C
Short circuit output current	I_{OUT}	-	100	mA
Latch-up current	I_{IN}	-	±100	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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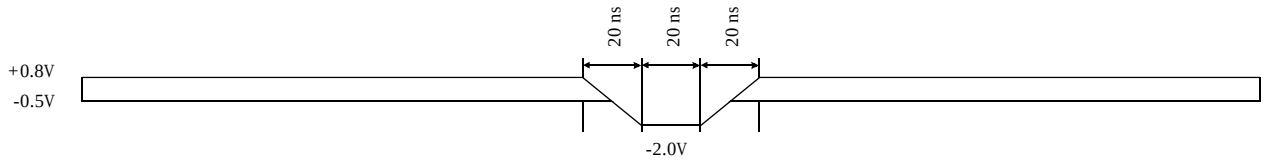
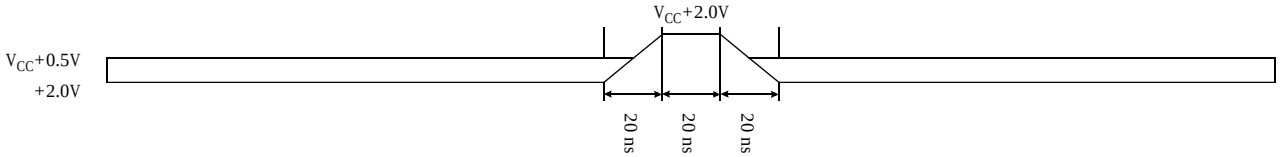
Maximum negative overshoot waveform



Maximum positive overshoot waveform



DC electrical characteristics

(V_{CC} = 5.0±0.5V, V_{SS} = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test conditions	Min	Max	Unit
Input load current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{SS} = V_{MAX}$	-	±1	µA
Output leakage current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{SS} = V_{MAX}$	-	±1	µA
Output short circuit current	I_{OS}	V_{OUT} = 0.5V	-	100	mA
Active current, read @ 6MHz	I_{CC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	30	mA
Active current, program/erase	I_{CCPRG}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	-	50	mA
Standby current	I_{SB1} (TTL)	$\overline{CE} = V_{IH}$	-	1.5	mA
	I_{SB2} (CMOS)	$\overline{CE} = V_{CC}$	-	1.0	mA
	I_{CCPD}	$\overline{RP}$ = 0V	-	2	µA
Input: low level	V_{IL}		0.5	0.8	V
Input: high level	V_{IH}		2.0	V_{SS} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 12mA	-	0.45	V
Output high level	V_{OH1}	I_{OH} = -2.5 mA	2.4	-	V
	V_{OH2}	I_{OH} = -100 µA	V_{CC} - 0.4	-	V
Low V_{CC} lock out voltage	V_{LKO}		3.2	4.2	V
Input HV select voltage	V_{ID}		11.5	12.5	V

Notes

1 Not more than one output tested simultaneously. Duration of the short circuit must not be >1 second. $_{OUT}$ = 0.5V was selected to avoid test problems caused by tester ground degradation. (This parameter is sampled and not 100% tested, but guaranteed by characterization.)

2 The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 6 MHz). The frequency componenttypically is less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.

3 I_{CC} active while program or erase operations are in progress.

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AC parameters — read cycle

(V_{CC} = 5.0±0.5V, V_{SS} = 0V, T_a = 0°C to +70°C)

JEDEC symbol	Std symbol	Parameter	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{RC}	Read cycle time	120	-	150	-	ns
t_{AVQV}	t_{ACC}	Address to output delay	-	120	-	150	ns
t_{ELQV}	t_{CE}	Chip enable to output	-	120	-	150	ns
t_{GLQV}	t_{OE}	Output enable to output	-	50	-	50	ns
t_{EHQZ}	t_{DF}	Chip enable to output High Z	-	30	-	30	ns
t_{GHQZ}	t_{DF}	Output enable to output High Z	-	30	-	30	ns
t_{AXQX}	t_{OH}	Output hold time from addresses, first occurrence of $\overline{CE}$ or $\overline{OE}$	0	-	0	-	ns

AC parameters — write cycle

(V_{CC} = 5.0±0.5V, V_{SS} = 0V, T_a = 0°C to +70°C)

JEDEC symbol	Std symbol	Parameter	-120 Min	-120 Max	-150 Min	-150 Max	Unit
t_{AVAV}	t_{WC}	Write cycle time	120	-	150	-	ns
t_{AVWL}	t_{AS}	Address setup time	0	-	0	-	ns
t_{WLAX}	t_{AH}	Address hold time	50	-	50	-	ns
t_{DVWH}	t_{DS}	Data setup time	50	-	50	-	ns
t_{WHDX}	t_{DH}	Data hold time	0	-	0	-	ns
	t_{OES}	Output enable setup time	0	-	0	-	ns
	t_{OEH}	Output enable hold time: Read	0	-	0	-	ns
		Output enable hold time: Toggle and $\overline{DATA}$ polling	10	-	10	-	ns
t_{GHWL}	t_{GHWL}	Read recover time before write	0	-	0	-	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ setup time	0	-	0	-	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ hold time	0	-	0	-	ns
t_{WLWH}	t_{WP}	Write pulse width	80	-	80	-	ns
t_{WHWL}	t_{WPH}	Write pulse width high	20	-	20	-	ns
t_{WHWH1}	t_{WHWH1}	Programming pulse time	250	-	250	-	µs
t_{WHWH2}	t_{WHWH2}	Erase pulse time	1000	-	1000	-	µs
	t_{VCS}	V_{CC} setup time	2	-	2	-	µs

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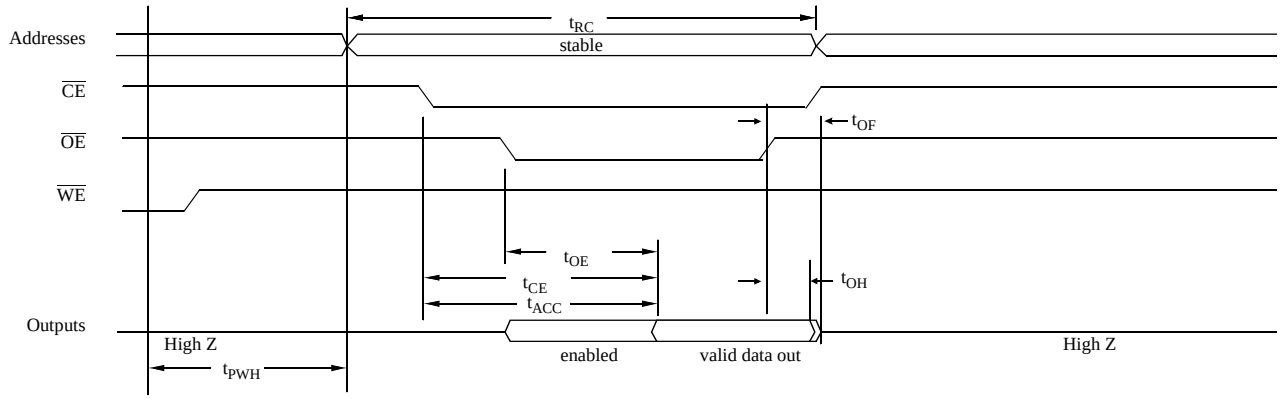
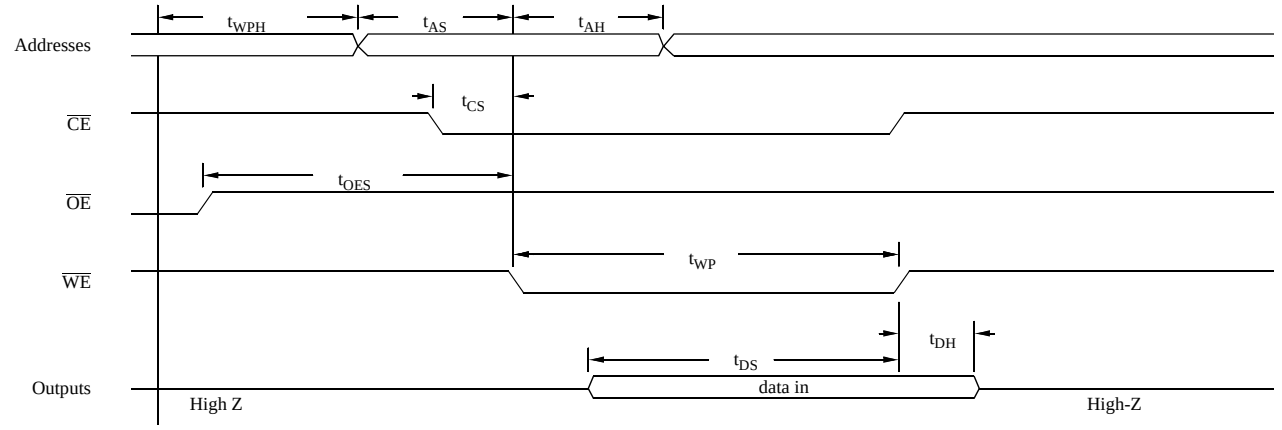
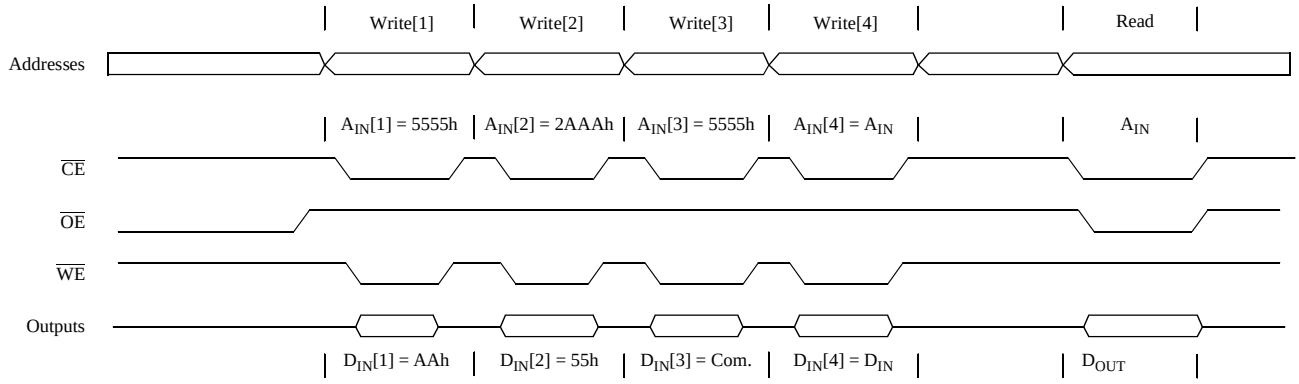
Read waveform



Write command waveform



Write command bus waveform



For all waveforms, $A_{IN[4:1]}$, and $D_{IN[4:1]}$ = Address and Data for write cycles 1–4; D_{IN} = Data to be programmed at address A_{IN}; Com. = Command byte input on the DQ pins during $Write_{[3]}$; D_{OUT} = Status byte, Manufacturer ID code, or array data for verify.

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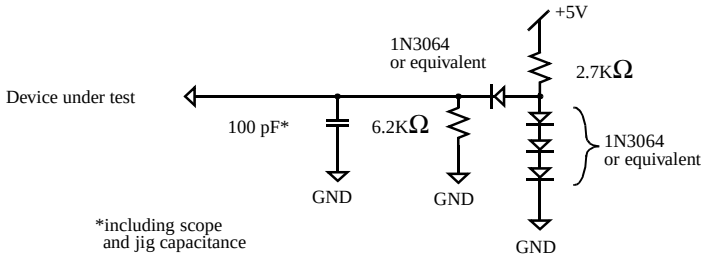
AC test conditions



Latchup tolerance

Parameter	Min	Max	Unit
Input voltage with respect to V_{SS} on pin A9	-1.0	+13.5	V
Input voltage with respect to V_{SS} on all DQ pins	-1.0	V_{CC}+1.0	V
Current	-100	+100	mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0V, one pin at a time.

TSOP pin capacitance

(f = 1 MHz, T_a = 25°C)

Symbol	Parameter	Test setup	Typical	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	7.5	9	µF

PLCC and PDIP pin capacitance

(f = 1 MHz, T_a = 25°C)

Symbol	Parameter	Test setup	Typical	Max	Unit
CIN	Input capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	8	12	µF

Erase and programming performance

(f = 1 MHz, T_a = room temperature, V_{CC} = 5V±10%)

	Limits			
Parameter	Min	Typical	Max	Unit
Sector erase and Verify-1 time (excludes 00h programming prior to erase)	-	6.0	8.2	sec
Sector programming time	-	-	8.2	sec
Chip programming time	-	48	80	sec
Erase program cycles	-	10,000	-	cycles
Byte program time	-	200	250	µs
Byte verify-0 time	-	200	250	µs

Data retention

Parameter	Temperature	Min	Unit
Minimum pattern data retention time	150°	10	years
	125°	20	years

AS29F010 ordering information

Package \ Access time	120 ns	150 ns
Plastic DIP, 600 mil, 32-pin	AS29F010-120PC	AS29F010-150PC
PLCC, 0.55 × 0.45" 32-pin	AS29F010-120LC	AS29F010-150LC
TSOP, 8×20 mm, 32-pin	AS29F010-120TC	AS29F010-150TC

AS29F010 part numbering system

AS29F	010	–XXX	X	C
Flash EEPROM prefix	Device number	Address access time	Package: P = PDIP L = PLCC T = TSOP	Commercial temperature range, 0°C to 70 °C