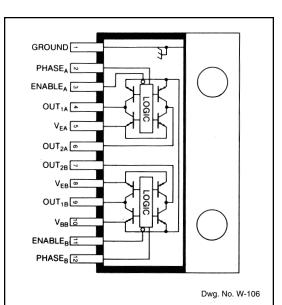
2998

DUAL FULL-BRIDGE MOTOR DRIVER



ABSOLUTE MAXIMUM RATINGS at T $_{\rm I} \le +150^{\circ}{\rm C}$

Supply Voltage, V_{BB} 50 V
Output Current, $I_{OUT}\left(\text{continuous}\right)\ \pm 2\ A$
(peak) ±3 A
Sink Driver Emitter Voltage, $V_{\rm E}$ $~1.5~V$
Logic Input Voltage Range, V_{PHASE} or V_{ENABLE} 0.3 V to 15 V Package Power Dissipation, P_D See Graph Operating Temperature Range, T_A 20°C to +85°C
Storage Temperature Range, T _S 55°C to +150°C
NOTE: Output current rating may be limited by chopping frequency, ambient tempera- ture, air flow, or heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of +150°C.

As an interface between low-level logic and solenoids, dc (brush) motors, or stepper motors, the UDN2998W dual full-bridge driver will operate inductive loads up to 50 V with continuous output currents of up to 2 A per bridge or peak (start-up) currents to 3 A. The control inputs are compatible with TTL, DTL, and 5 V CMOS logic. Except for a common supply voltage and thermal shutdown, the two drivers in each package are completely independent.

For external PWM control, an Output Enable for each bridge circuit is provided and the sink driver emitters are pinned out for connection to external current-sensing resistors. The chopper drive mode is characterized by low power dissipation levels and maximum efficiency. A PHASE input to each bridge determines load-current direction.

Extensive circuit protection is provided on-chip. Both groundclamp and flyback diodes for each bridge are provided. A thermal shutdown circuit disables the load drive if chip temperature rating (package power dissipation) is exceeded. Internally-generated delays provide crossover-current protection.

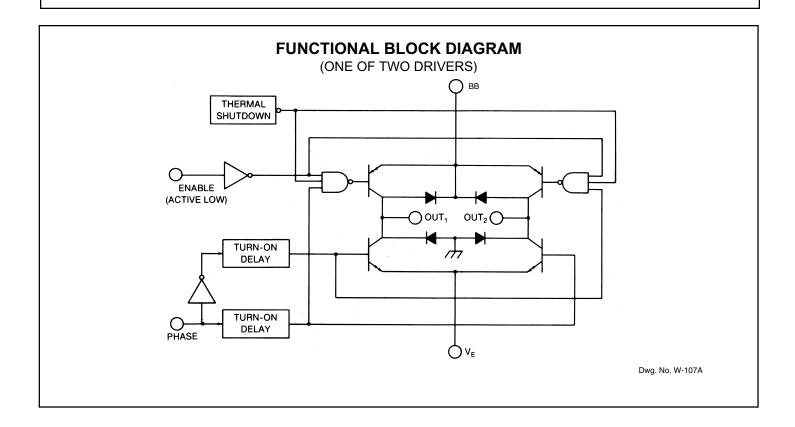
The UDN2998W is packaged in a 12-pin single in-line power-tab package for high power capabilities. Driving either of the bridges at the full 2 A dc rating requires the use of an external heat sink. The tab is at ground potential and needs no insulation.

FEATURES

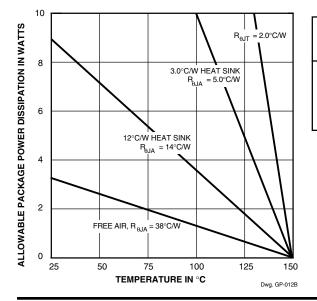
- ±3 A Peak Output Current
- Output Voltage to 50 V
- Integral Output Suppression Diodes
- Output Current Sensing
- TTL/CMOS Compatible Inputs
- Internal Thermal Shutdown Circuitry
- Crossover-Current Protected
- Automotive Capable

Always order by complete part number: **UDN2998W**.





To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.





ENABLE INPUT	PHASE INPUT	OUTPUT 1	OUTPUT 2
Low	High	High	Low
Low	Low	Low	High
High	High	Open	Low
High	Low	Low	Open



115 Northeast Cutoff, Box 15036 Worcester, Massachusetts 01615-0036 (508) 853-5000 Copyright © 1985, 2000 Allegro MicroSystems, Inc.

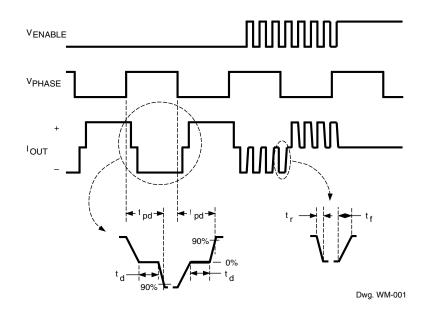
ELECTRICAL CHARACTERISTICS at T_A = +25°C, T_J \leq +150°C, V_{BB} = 50 V

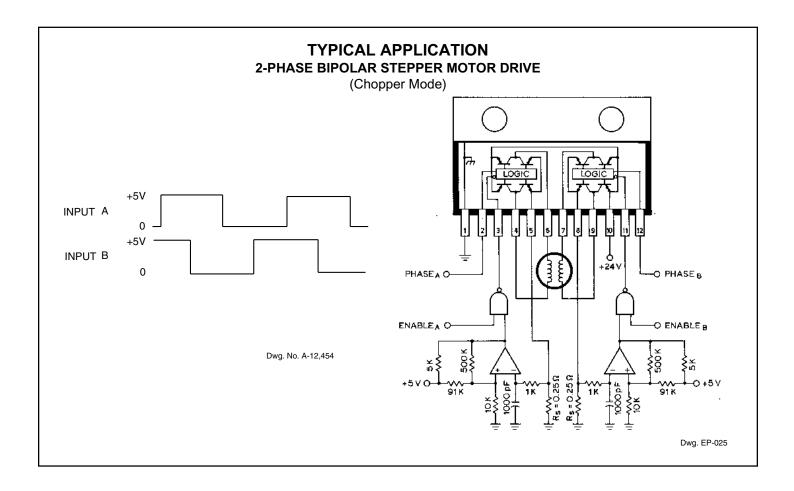
	Symbol			Limits			
Characteristic		Test Conditions	Min.	Тур.	Max.	Units	
Output Drivers							
Operating Voltage Range	V _{BB}		10	—	50	V	
Output Leakage Current	I _{CEX}	V _{OUT} = 50 V, V _{ENABLE} = 2.0 V, Note 2	_	<5.0	50	μA	
		V_{OUT} = 0, V_{ENABLE} = 2.0 V, Note 2	_	<-5.0	-50	μA	
Output Saturation Voltage	V _{CE(SAT)}	I _{OUT} = 1 A, Sink Driver	_	1.2	1.4	V	
		I _{OUT} = 2 A, Sink Driver	_	1.7	1.9	V	
		I _{OUT} = -1 A, Source Driver	_	1.7	1.9	V	
		I _{OUT} = -2 A, Source Driver	_	2.0	2.2	V	
Output Sustaining Voltage	V _{CE(sus)}	I _{OUT} = ±2 A, L = 3.5 mH, Note 2	50	—		V	
Source Driver Rise Time	t _r	I _{OUT} = -2 A	_	500	_	ns	
Source Driver Fall Time	t _f	I _{OUT} = -2 A	_	750		ns	
Deadtime	t _d	$I_{OUT} = \pm 2 A$	_	2.5		μs	
Clamp Diode Leakage Current	I _R	V _R = 50 V	_	<5.0	50	μA	
Clamp Diode Forward Voltage	V _F	I _F = 2 A	_	1.5	2.0	V	
Supply Current	I _{BB}	$V_{\text{ENABLE}(1)} = V_{\text{ENABLE}(2)} = 0.8 \text{ V}$	_	30	35	mA	
Control Logic (PHASE or ENA	BLE)						
Logic Input Voltage	V _{IN(0)}		_		0.8	V	
	V _{IN(1)}		2.0	_		V	
Logic Input Current	I _{IN(0)}	V_{PHASE} or V_{ENABLE} = 0.8 V	_	-5.0	-25	μA	
	I _{IN(1)}	V_{PHASE} or V_{ENABLE} = 2.0 V		<1.0	10	μA	
Turn-On Delay Time	t _{pd0}	ENABLE Input to Source Drivers		0.4	1.0	μs	
Turn-Off Delay Time	t _{pd1}	ENABLE Input to Source Drivers	_	2.0	4.0	μs	

NOTES: 1. Each driver is tested separately.

2. Test is performed with $V_{PHASE} = 0.8 \text{ V}$ and then repeated for $V_{PHASE} = 2.0 \text{ V}$.

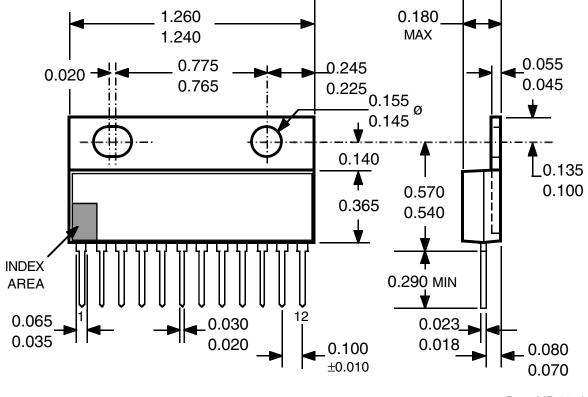
3. Negative current is defined as coming out of (sourcing) the specified device pin.







115 Northeast Cutoff, Box 15036 Worcester, Massachusetts 01615-0036 (508) 853-5000



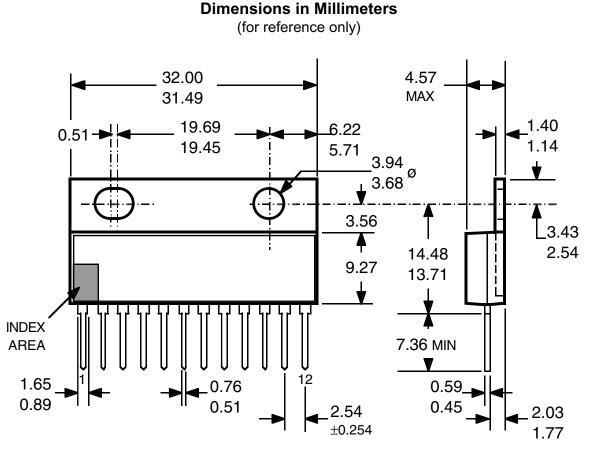
Dimensions in Inches

(controlling dimensions)

Dwg. MP-007 in

NOTES: 1. Lead thickness is measured at seating plane or below.

- 2. Lead spacing tolerance is non-cumulative.
- 3. Exact body and lead configuration at vendor's option within limits shown.
- 4. Lead gauge plane is 0.030" below seating plane.
- 5. Supplied in standard sticks/tubes of 15 devices.



Dwg. MP-007 mm

NOTES: 1. Lead thickness is measured at seating plane or below.

- 2. Lead spacing tolerance is non-cumulative.
- 3. Exact body and lead configuration at vendor's option within limits shown.
- 4. Lead gauge plane is 0.762 mm below seating plane.
- 5. Supplied in standard sticks/tubes of 15 devices.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

