Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

# T7698 Quad T1/E1 Line Interface and Octal T1/E1 Monitor

## Features

- Integrated quad T1/E1 line interface and octal T1/E1 receive frame monitor with HDLC processor provides system QoS capabilities.
- Hardware and software reset options.
- 3-state outputs.
- 0.35 µm, low-power CMOS technology.
- Compliant with:

  **AT&T**
  CB119 (10/79)

  **Bellcore**
  TR-54016 (89)
  TR-TSY-000170 (10/97)
  TR-TSY-000009 (5/86)
  GR-499-CORE (12/95)
  GR-253-CORE (12/95)

  **ANSI**
  T1.102 (93)
  T1.231 (93)
  T1.403 (95)

  **ITU-T**
  G.703 (88)
  G.704 (91)
  G.706 (91)
  G.732 (88)
  G.735-9 (88)
  G.775 (11/94)
  G.823-4 (3/93)
  G.826 (11/93)
  I.431 (3/93)

  **ETSI**
  TBR 12 (12/93)
  TBR 13 (1/96)
- –40 °C to +85 °C operating temperature range.
- Fine-pitch (25 mil spacing) surface-mount package, 100-pin BQFP.

### T1/E1 Line Interface Features

- Transmitter includes transmit encoder (B8ZS or HDB3), pulse shaping, and line driver.
- Compatible with the Lucent Technologies Microelectronics Group T7690 line interface.
- Five pulse equalization settings for template compliance at DSX cross connect.
- Receive includes equalization, digital clock and data recovery (immune to false lock), and receive decoder (B8ZS or HDB3).
- CEPT/E1 interference immunity as required by G.703.
- Transmit jitter <0.02 UI.
- Receive generated jitter <0.05 UI.
- Jitter attenuator selectable for use in transmit or receive path. Jitter attenuation characteristics are data pattern independent.
- For use with 100 Ω DS1 twisted-pair, 120 Ω E1 twisted-pair, and 75 Ω E1 coaxial cable.
- Common transformer for transmit/receive.
- Analog LOS alarm for signals less than –18 dB for greater than 1 ms or 10 bit symbol periods to 255 bit symbol periods (selectable).
- Digital LOS alarm for 100 zeros (DS1) or 255 zeros (CEPT).
- Diagnostic loopback modes.
- Ultralow power consumption.

### T1/E1 Frame Monitor Features

- Framing formats
  - — DS1 extended superframe (ESF)
  - — DS1 superframe (SF): D4 (domestic, Japanese); *SLC*®-96; T1DM DDS with FDL access
  - — Compliant to ITU-CEPT framing recommendation:
    1. CEPT basic frame format
    2. CEPT with CRC-4 multiframe search algorithm and 100 ms timer
    3. CEPT with CRC-4 multiframe search algorithm and 400 ms timer for interworking of CRC-4 and non-CRC-4 equipment
    4. CEPT with loss of frame condition upon detection of ≥915 CRC-4 submultiframe errors out of 1000 CRC-4 submultiframe checks

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## Features (continued)

### T1/E1 Frame Monitor Features (continued)

- Alarm reporting, performance monitoring, and maintenance
  - — Status registers for detection of red alarm, remote frame alarm, and alarm indication signal conditions, errors, and violations
  - — 16-bit counter registers for counting:
    1. Line format violations (bipolar, coding, excessive zeros)
    2. Framing bit errors
    3. CRC errors
    4. CEPT E bit = 0 conditions
    5. CEPT Sa6 codes
    6. Errored seconds
    7. Bursty errored seconds
    8. Severely errored seconds
    9. Unavailable seconds
  - — Selectable errored event monitoring for errored and severely errored seconds processing with optional programmable thresholds for errored seconds, bursty errored seconds, and severely errored seconds
- Compatible with the receive section of Lucent's T7630

### Facility Data Link Features

- HDLC or transparent mode
- 64-byte receive FIFO capable of holding multiple frames
- Detection of the ANSI ESF bit-oriented messages
- Monitoring of the ANSI performance report messages

### User-Programmable Microprocessor Interface

- 16 MHz read and write access with no wait-states
- 4-bit address, 8-bit data interface
- Programmable *Intel** or *Motorola*† interface modes
- Demultiplexed or multiplexed address and data bus

## Applications

- T1/E1 network performance monitoring
- SONET/SDH multiplexers
- Asynchronous multiplexers (M13)
- Digital access cross connects (DACs)
- Channel banks
- Digital radio base stations, remote wireless modules
- PBX interfaces

## Description

The T7698 is an integrated quad line interface containing four line transmit and receive channels and an octal frame monitor for use in both North American (T1/DS1) and European (E1/CEPT) applications. The line interface unit has the same functions as the Lucent T7690, and the frame monitors are compatible with the receive section of the Lucent T7630. Included is a parallel microprocessor interface that allows the user to define the architecture, initiate loopbacks, and monitor alarms. The interface is compatible with many commercially available microprocessors. The functional block diagram of the T7698 is shown in Figure 1.

The block diagram of the line interface unit is shown in Figure 4. The line receiver performs clock and data recovery using a fully integrated digital phase-locked loop. This digital implementation prevents false lock conditions that are common when recovering sparse data patterns with analog phase-locked loops. Equalization circuitry in the receiver guarantees a high level of interference immunity. As an option, the raw sliced data (no retiming) can be output on the receive data pins. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. The quad device will interface to the digital cross connect (DSX) at lengths of up to 655 ft. for DS1 operation or to line impedances of 75 Ω or 120 Ω for CEPT operation.

A selectable jitter attenuator may be placed in the receive signal path for low-bandwidth line-synchronous applications, or it may be placed in the transmit path for multiplexer applications where DS1/CEPT signals are demultiplexed from higher rate signals. The jitter attenuator will perform the clock smoothing required on the resulting demultiplexed gapped clock.

* *Intel* is a registered trademark of Intel Corporation.
† *Motorola* is a registered trademark of Motorola, Inc.

## Features (continued)

The octal frame monitor section frames on the eight channels (four in the transmit direction and four in the receive direction, as shown in Figure 1) and performs monitoring, alarm reporting, and maintenance signalling. Registers and counters (unique to each one of the eight channels) report on bipolar violations, frame bit errors, CRC errors, and alarms. The block diagram of the octal frame monitor is shown in Figure 16. Both DS1 (D4, *SLC*-96, DDS, ESF) and CEPT (with and without CRC-4) framing formats are supported. The facility data link section allows extraction of data from the facility data link in the *SLC*-96, DDS, ESF, and CEPT framing formats. Both HDLC and transparent mode are supported. Access to the facility data link is through a 64-byte FIFO which is capable of holding multiple frames. The facility data link also monitors the ANSI performance report messages (PRM) and detects the ANSI ESF bit-oriented messages.

## Block Diagram

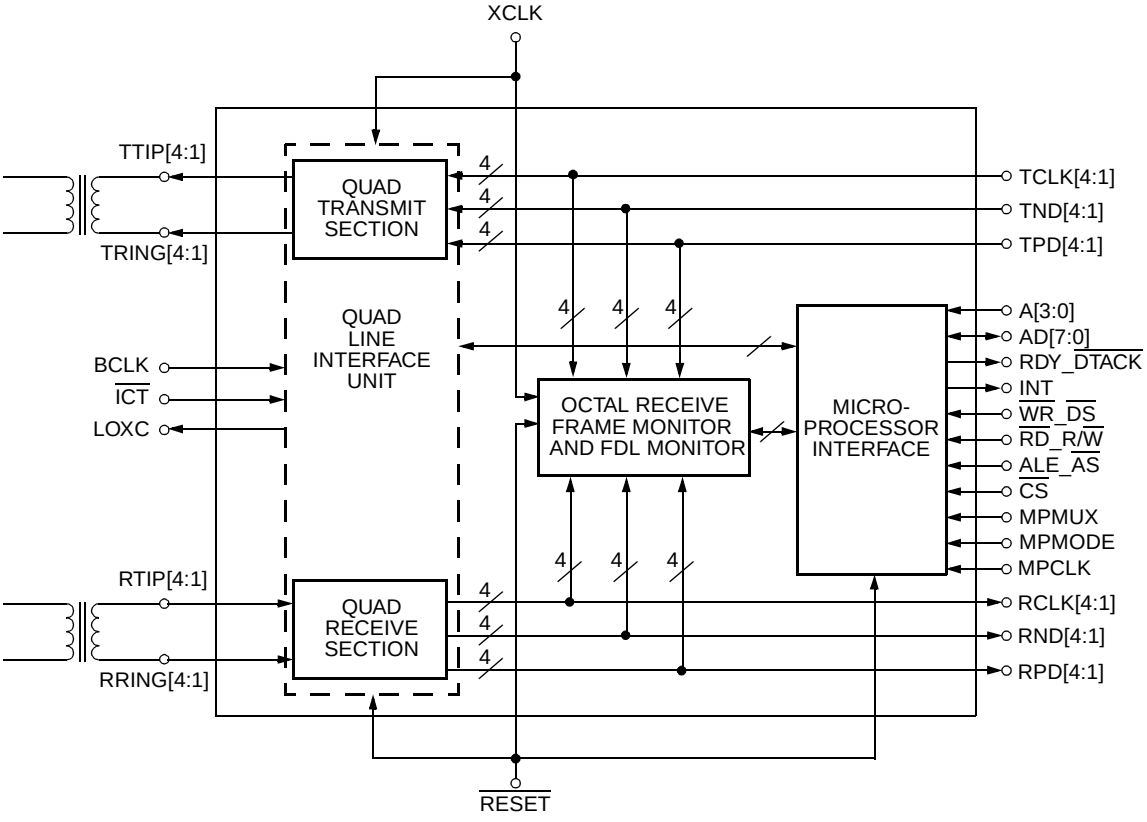


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**Figure 1. T7698 Block Diagram**

## Pin Information

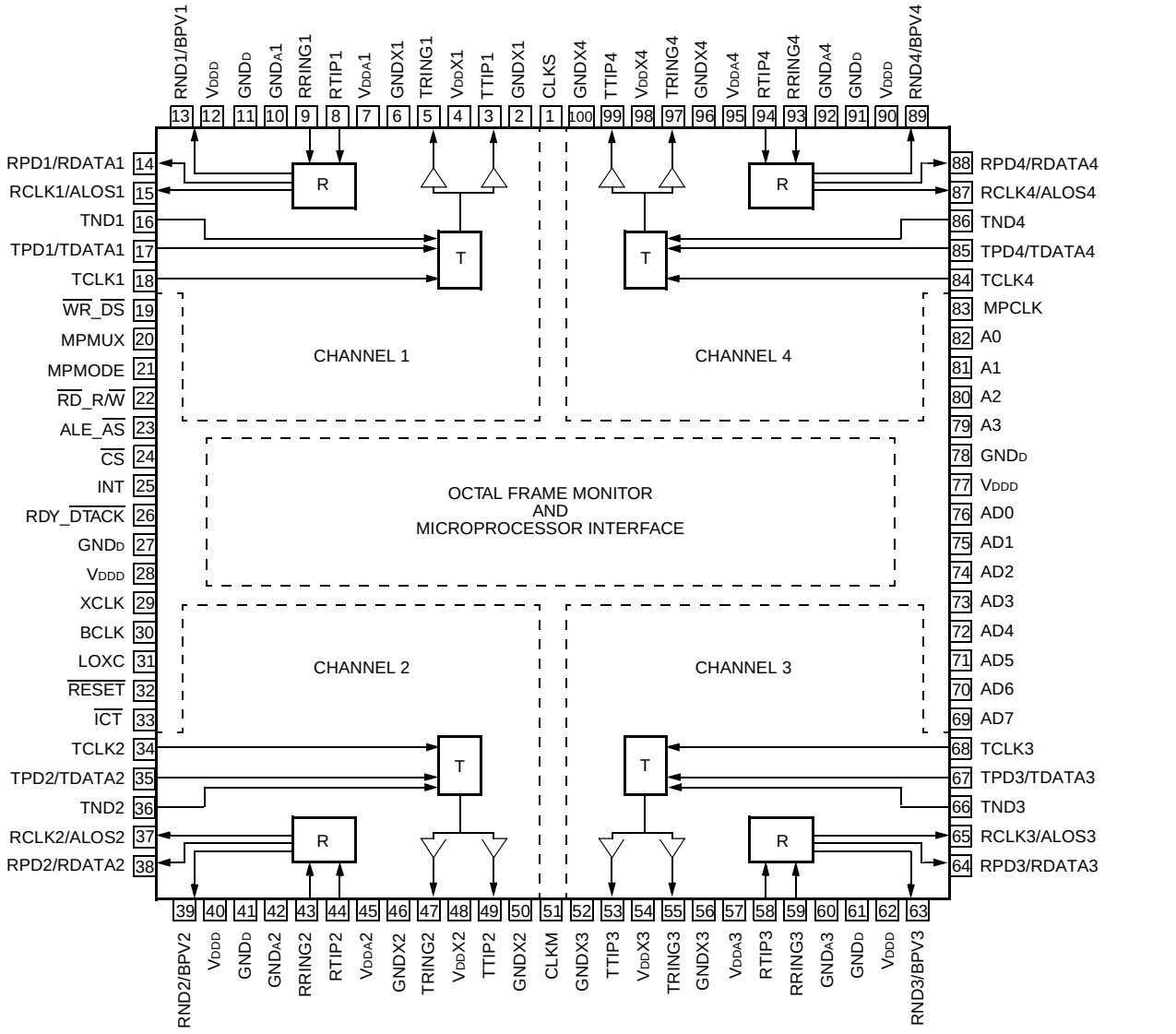


**Figure 2. T7698 Pin Diagram**

## Pin Information (continued)

**Table 1. Pin Descriptions**

| Pin | Symbol | Type* | Name/Description |
|---|---|---|---|
| 1 | CLKS | $I^d$ | **XCLK Select.** This pin selects either a 16x rate clock for XCLK (CLKS = 0) or a primary line rate clock for XCLK (CLKS = 1). |
| 51 | CLKM | $I^d$ | **XCLK Mode.** This pin must be set appropriately when using a primary line rate clock for XCLK.<br>CEPT: CLKM = 1.<br>DS1: CLKM = 0. |
| 2, 6 | GNDX1 | P | **Ground Reference for Line Drivers.** |
| 46, 50 | GNDX2 | | |
| 52, 56 | GNDX3 | | |
| 96, 100 | GNDX4 | | |
| 3 | TTIP1 | O | **Transmit Bipolar Tip.** Positive bipolar transmit data to the analog line interface. |
| 49 | TTIP2 | | |
| 53 | TTIP3 | | |
| 99 | TTIP4 | | |
| 4 | $V_{DD}$X1 | P | **Power Supply for Line Drivers.** The T7698 device requires a 5 V ± 5% power supply on these pins. |
| 48 | $V_{DD}$X2 | | |
| 54 | $V_{DD}$X3 | | |
| 98 | $V_{DD}$X4 | | |
| 5 | TRING1 | O | **Transmit Bipolar Ring.** Negative bipolar transmit data to the analog line interface. |
| 47 | TRING2 | | |
| 55 | TRING3 | | |
| 97 | TRING4 | | |
| 7 | $V_{DDA}$1 | P | **Power Supply for Analog Circuitry.** The T7698 device requires a 5 V ± 5% power supply on these pins. |
| 45 | $V_{DDA}$2 | | |
| 57 | $V_{DDA}$3 | | |
| 95 | $V_{DDA}$4 | | |
| 8 | RTIP1 | I | **Receive Bipolar Tip.** Positive bipolar receive data from the analog line interface. |
| 44 | RTIP2 | | |
| 58 | RTIP3 | | |
| 94 | RTIP4 | | |
| 9 | RRING1 | I | **Receive Bipolar Ring.** Negative bipolar receive data from the analog line interface. |
| 43 | RRING2 | | |
| 59 | RRING3 | | |
| 93 | RRING4 | | |
| 10 | $GND_A$1 | P | **Ground Reference for Analog Circuitry.** |
| 42 | $GND_A$2 | | |
| 60 | $GND_A$3 | | |
| 92 | $GND_A$4 | | |

* $I^u$ indicates an internal pull-up; $I^d$ indicates an internal pull-down.

## Pin Information (continued)

**Table 1. Pin Descriptions** (continued)

| Pin | Symbol | Type* | Name/Description |
|---|---|---|---|
| 13, 39, 63, 89 | RND/BPV[4:1] | O | **Receive Negative Data.** When in dual-rail (DUAL = 1: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the received negative NRZ data to the terminal equipment. When in data slicing mode (CDR = 0), this signal is the raw sliced negative data of the front end. For frame monitor operation, clock recovery mode (CDR = 1) must be chosen.<br>**Bipolar Violation.** When in single-rail (DUAL = 0: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), and CODE = 1 (register 5, bit 3), this signal is asserted high to indicate the occurrence of a code violation in the receive data stream. A code violation is a bipolar violation that is not part of a zero substitution code. If CODE = 0, this signal is asserted to indicate the occurrence of a bipolar violation in the received data. |
| 14, 38, 64, 88 | RPD/ RDATA[4:1] | O | **Receive Positive Data.** When in dual-rail (DUAL = 1: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the received positive NRZ data to the terminal equipment. When in data slicing mode (CDR = 0), this signal is the raw sliced positive data of the front end. For frame monitor operation, clock recovery mode (CDR = 1) must be chosen.<br>**Receive Data.** When in single-rail (DUAL = 0: register 5, bit 4) clock recovery mode (CDR = 1: register 5, bit 0), this signal is the received NRZ data. |
| 15, 37, 65, 87 | RCLK/ ALOS[4:1] | O | **Receive Clock.** In clock recovery mode (CDR = 1: register 5, bit 0), this signal is the recovered receive clock for the terminal equipment. The duty cycle of RCLK is 50% ± 5%.<br>**Analog Loss of Signal.** In data slicing mode (CDR = 0: register 5, bit 0), this signal is asserted high to indicate low amplitude receive data at the RTIP/ RRING inputs. |
| 16, 36, 66, 86 | TND[4:1] | I | **Transmit Negative Data.** This signal is the transmit negative NRZ data from the terminal equipment. |
| 17, 35, 67, 85 | TPD/ TDATA[4:1] | I | **Transmit Positive Data.** When in dual-rail mode (DUAL = 1: register 5, bit 4), this signal is the transmit positive NRZ data from the terminal equipment.<br>**Transmit Data.** When in single-rail mode (DUAL = 0: register 5, bit 4), this signal is the transmit NRZ data from the terminal equipment. |
| 18, 34, 68, 84 | TCLK[4:1] | I | **Transmit Clock.** DS1 (1.544 MHz ± 32 ppm) or CEPT (2.048 MHz ± 50 ppm) clock signal from the terminal equipment. |

* $I^u$ indicates an internal pull-up; $I^d$ indicates an internal pull-down.

## Pin Information (continued)

**Table 1. Pin Descriptions** (continued)

| Pin | Symbol | Type* | Name/Description |
|---|---|---|---|
| 21 | MPMODE | I | **Microprocessor Mode.** When MPMODE = 1, the device uses the address latch enable type microprocessor read/write protocol with separate read and write controls. Setting MPMODE = 0 allows the device to use the address strobe type microprocessor read/write protocol with a separate data strobe and a combined read/write control. |
| 20 | MPMUX | I | **Microprocessor Multiplex Mode.** Setting MPMUX = 1 allows the microprocessor interface to accept multiplexed address and data signals. Setting MPMUX = 0 allows the microprocessor interface to accept demultiplexed (separate) address and data signals. |
| 19 | $\overline{WR}$_$\overline{DS}$ | I | **Write (Active-Low).** If MPMODE = 1 (pin 21), this pin is asserted low by the microprocessor to initiate a write cycle.<br>**Data Strobe (Active-Low).** If MPMODE = 0 (pin 21), this pin becomes the data strobe for the microprocessor. When R/$\overline{W}$ = 0 (pin 22) initiating a write, a low applied to this pin latches the signal on the data bus into internal registers. |
| 22 | $\overline{RD}$_R/$\overline{W}$ | I | **Read (Active-Low).** If MPMOD = 1 (pin 21), this pin is asserted low by the microprocessor to initiate a read cycle.<br>**Read/Write.** If MPMODE = 0 (pin 21), this pin is asserted high by the microprocessor to initiate a read cycle or asserted low to initiate a write cycle. |
| 23 | ALE_$\overline{AS}$ | I | **Address Latch Enable.** If MPMODE = 1 (pin 21), this pin becomes the address latch enable for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers.<br>**Address Strobe (Active-Low).** If MPMODE = 0 (pin 21), this pin becomes the address strobe for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers. |
| 24 | $\overline{CS}$ | $I^u$ | **Chip Select (Active-Low).** This pin is asserted low by the microprocessor to enable the microprocessor interface. If MPMUX = 1 (pin 20), $\overline{CS}$ can be externally tied low to use the internal chip selection function. An internal 100 kΩ pull-up is on this pin. |
| 25 | INT | O | **Interrupt.** This pin is asserted high to indicate an interrupt produced by an alarm condition in register 0 or 1. The activation of this pin can be masked by microprocessor registers 2, 3, and 4. |
| 26 | RDY_$\overline{DTACK}$ | O | **Ready.** If MPMODE = 1 (pin 21), this pin is asserted high to indicate the device has completed a read or write operation. This pin is in a 3-state condition when $\overline{CS}$ (pin 24) is high.<br>**Data Transfer Acknowledge (Active-Low).** If MPMODE = 0 (pin 21), this pin is asserted low to indicate the device has completed a read or write operation. |
| 11, 27, 41, 61, 78, 91 | $GND_D$ | P | **Ground Reference for Microprocessor Interface and Digital Circuitry.** |
| 12, 28, 40, 62, 77, 90 | $V_{DDD}$ | P | **Power Supply for Microprocessor Interface and Digital Circuitry.** The T7698 device requires a 5 V ± 5% power supply on these pins. |

* $I^u$ indicates an internal pull-up; $I^d$ indicates an internal pull-down.

## Pin Information (continued)

**Table 1. Pin Descriptions** (continued)

| Pin | Symbol | Type* | Name/Description |
|---|---|---|---|
| 29 | XCLK | $I^u$ | **Reference Clock**. The clock signal used for clock and data recovery and jitter attenuation. This clock must be ungapped and free of jitter.<br>For CLKS = 0, a 16x clock (for DS1, XCLK = 24.704 MHz ± 100 ppm and for CEPT, XCLK = 32.768 MHz ± 100 ppm).<br>For CLKS = 1, a 1x clock (for DS1, XCLK = 1.544 MHz ± 100 ppm and for CEPT, XCLK = 2.048 MHz ± 100 ppm).<br>To meet TBR 12/13 jitter accommodation requirements, clock tolerances must be reduced to ±20 ppm. An internal 100 kΩ pull-up is on this pin. |
| 30 | BCLK | $I^u$ | **Blue Clock**. Input clock signal used to transmit the AIS signal (all 1s data pattern). In DS1 mode, this clock is 1.544 MHz ± 32 ppm, and in CEPT mode, this clock is 2.048 MHz ± 50 ppm. An internal 100 kΩ pull-up is on this pin. |
| 31 | LOXC | O | **Loss of XCLK**. This pin is asserted high when the XCLK signal (pin 29) is not present. |
| 32 | $\overline{\text{RESET}}$ | $I^u$ | **Hardware Reset (Active-Low)**. If $\overline{\text{RESET}}$ is forced low, all internal states in the line interface paths are reset and data flow through each channel will be momentarily disrupted. The $\overline{\text{RESET}}$ pin must be held low for a minimum of 10 µs. An internal 50 kΩ pull-up is on this pin. |
| 33 | $\overline{\text{ICT}}$ | $I^u$ | **In-Circuit Test Control (Active-Low)**. If $\overline{\text{ICT}}$ is forced low, certain output pins are placed in a high-impedance state. Which output pins are affected is controlled by the ICTMODE bit (register 4, bit 3). An internal 50 kΩ pull-up is on this pin. |
| 69—76 | AD7—AD0 | I/O | **Microprocessor Interface Address/Data Bus.** If MPMUX = 0 (pin 20), these pins become the bidirectional, 3-statable data bus. If MPMUX = 1, these pins become the multiplexed address/data bus. In this mode, only the lower 4 bits (AD[3:0]) are used for the internal register addresses. |
| 79—82 | A3—A0 | I | **Microprocessor Interface Address.** If MPMUX = 0 (pin 20), these pins become the address bus for the microprocessor interface registers. If MPMUX = 1 (pin 20) and $\overline{\text{CS}}$ = 0 (pin 24), A3 (pin 79) can be externally tied high to use the internal chip selection function. The state of A[2:0] determines the address of the device. The device is addressed when the state of pins AD[6:4] matches the device address of A[2:0]. If this function is not used, A[3:0] must be externally tied low. |
| 83 | MPCLK | I | **Microprocessor Interface Clock.** Microprocessor interface clock rates from twice the frequency of the line clock (3.088 MHz for DS1 operation, 4.096 MHz for CEPT operation) to 16.384 MHz are supported. |

* $I^u$ indicates an internal pull-up; $I^d$ indicates an internal pull-down.

## T7698 Device Overview

The T7698 is a four-channel device with a shared microprocessor interface. Each of the four channels consists of a line interface unit (LIU) and two frame monitors with facility data links (FDL). The LIUs convert bipolar line data pulses into logic level terminal data, with options for monitoring of the line integrity, clock and data recovery or raw sliced data, timing for the data and clock recovery, jitter attenuation, equalization, zero bit coding, loopbacks, and other functions. The frame monitors monitor line performance providing data on integrity of the frame structure, perform cyclical redundancy checks for bit errors, and extract alarm and data link signaling for operations and maintenance functions.

## System Interface Pin Options

The system interface can be configured to operate in a number of different modes. The different modes change the functionality of the system interface pins, as shown in Table 2. Dual-rail or single-rail operation is possible using the DUAL control bit (register 5, bit 4). Dual-rail mode is enabled when DUAL = 1; single-rail mode is enabled when DUAL = 0. In dual-rail operation, data received from the line interface on RTIP and RRING appears on RPD (pins 14, 38, 64, 88) and RND (pins 13, 39, 63, 89) at the system interface and data transmitted from the system interface on TPD (pins 17, 35, 67, 85) and TND (pins 16, 36, 66, 86) appears on TTIP and TRING at the line interface. In single-rail operation, data received from the line interface on RTIP and RRING appears on RDATA (pins 14, 38, 64, 88) at the system interface and data transmitted from the system interface on TDATA (pins 17, 35, 67, 85) appears on TTIP and TRING at the line interface.

In both dual-rail and single-rail operation, the clock/data recovery mode is selectable via the CDR bit (register 5, bit 0). When CDR = 1, the clock and data recovery is enabled and the system interface operates in a nonreturn-to-zero (NRZ) digital format, recovering the clock and data from the incoming pulses. When CDR = 0, the clock and data recovery is disabled and the system interface operates on unretimed sliced data in RZ data format. No clock is recovered, freeing up the RCLK pin to be used to indicate an analog loss of signal (ALOS). If the incoming pulse height falls below –18 dB, the ALOS pin (15, 37, 65, 87) is asserted high, and remains high until the signal rises above –14 dB.

In single-rail mode only, B8ZS/HDB3 encoding/decoding may be selected by setting the control bits properly (see the Zero Substitution Decoding (CODE) section, page 23, and the Zero Substitution Encoding (CODE) section, page 31). When a coding violations occurs, the BPV pin (pins 13, 39, 63, 89) is asserted high.

**Table 2. System Interface Pin Mapping**

| Configuration | RCLK/ ALOS | RPD/ RDATA | RND/BPV | TPD/ TDATA | TND |
|---|---|---|---|---|---|
| Dual-rail with Clock Recovery (DUAL = 1, CDR = 1) | RCLK | RPD | RND | TPD | TND |
| Dual-rail with Data Slicing (DUAL = 1, CDR = 0) | ALOS | RPD | RND | | |
| Single-rail with Clock Recovery (DUAL = 0, CDR = 1) | RCLK | RDATA | BPV | TDATA | Not Used |
| Single-rail with Data Slicing (DUAL = 0, CDR = 0) | ALOS | RPD | RND | | |

# Microprocessor Interface

## Overview

The device is equipped with a microprocessor interface that can operate with most commercially available microprocessors. Inputs MPMUX and MPMODE (pins 20 and 21) are used to configure this interface into one of four possible modes, as shown in Table 3. The MPMUX setting selects either a multiplexed 8-bit address/data bus (AD[7:0]) or a demultiplexed 4-bit address bus (A[3:0]) and an 8-bit data bus (AD[7:0]). The MPMODE setting selects the associated set of control signals required to access a set of registers within the device.

When the microprocessor interface is configured to operate in the multiplexed address/data bus modes (MPMUX = 1), the user has access to an internal chip select function that allows the microprocessor to selectively read/write a specific T7698 in a multiple T7698 environment (see the Internal Chip Select Function section).

The microprocessor interface can operate at speeds up to 16.384 MHz in interrupt-driven or polled mode without requiring any wait-states. For microprocessors operating at greater than 16.384 MHz, the RDY_$\overline{\text{DTACK}}$ output is used to introduce wait-states in the read/write cycles.

In the interrupt-driven mode, one or more device alarms will assert the active-high INT output (pin 25) once per alarm activation. After the microprocessor reads the alarm status registers, the INT output will deassert. In the polled mode, however, the microprocessor monitors the various device alarm status by periodically reading the alarm status registers without the use of INT (pin 25). A variety of LIU mask controls are available for control of the INT pin.

## Microprocessor Configuration Modes

Table 3 highlights the four microprocessor modes controlled by the MPMUX and MPMODE inputs (pins 20 and 21).

**Table 3. Microprocessor Configuration Modes**

| Mode | MPMODE | MPMUX | Address/Data Bus | Generic Control, Data, and Output Pin Names |
|---|---|---|---|---|
| MODE 1 | 0 | 0 | deMUXed | $\overline{\text{CS}}$, $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, A[3:0], AD[7:0], INT, $\overline{\text{DTACK}}$ |
| MODE 2 | 0 | 1 | MUXed | $\overline{\text{CS}}$, $\overline{\text{AS}}$, $\overline{\text{DS}}$, R/$\overline{\text{W}}$, AD[7:0], INT, $\overline{\text{DTACK}}$ |
| MODE 3 | 1 | 0 | deMUXed | $\overline{\text{CS}}$, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A[3:0], AD[7:0], INT, RDY |
| MODE 4 | 1 | 1 | MUXed | $\overline{\text{CS}}$, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, AD[7:0], INT, RDY |

## Microprocessor Interface (continued)

### Microprocessor Interface Pinout Definitions

The MODE 1—MODE 4 specific pin definitions are given in Table 4. Note that the microprocessor interface uses the same set of pins in all modes.

**Table 4. MODE [1—4] Microprocessor Pin Definitions**

| Configuration | Pin Number | Device Pin Name | Generic Pin Name | Pin_Type | Assertion Sense | Function |
|---|---|---|---|---|---|---|
| MODE 1 | 19 | $\overline{WR}$_$\overline{DS}$ | $\overline{DS}$ | Input | Active-Low | Data Strobe |
| | 22 | $\overline{RD}$_R/$\overline{W}$ | R/$\overline{W}$ | Input | — | Read/Write<br>R/$\overline{W}$ = 1 => Read<br>R/$\overline{W}$ = 0 => Write |
| | 23 | ALE_$\overline{AS}$ | $\overline{AS}$ | Input | — | Address Strobe |
| | 24 | $\overline{CS}$ | $\overline{CS}$ | Input | Active-Low | Chip Select |
| | 25 | INT | INT | Output | Active-High | Interrupt |
| | 26 | RDY_$\overline{DTACK}$ | $\overline{DTACK}$ | Output | Active-Low | Data Acknowledge |
| | 69—76 | AD[7:0] | AD[7:0] | I/O | — | Data Bus |
| | 79—82 | A[3:0] | A[3:0] | Input | — | Address Bus |
| | 83 | MPCLK | MPCLK | Input | — | Microprocessor Clock |
| MODE 2 | 19 | $\overline{WR}$_$\overline{DS}$ | $\overline{DS}$ | Input | Active-Low | Data Strobe |
| | 22 | $\overline{RD}$_R/$\overline{W}$ | R/$\overline{W}$ | Input | — | Read/Write<br>R/$\overline{W}$ = 1 => Read<br>R/$\overline{W}$ = 0 => Write |
| | 23 | ALE_$\overline{AS}$ | $\overline{AS}$ | Input | — | Address Strobe |
| | 24 | $\overline{CS}$ | $\overline{CS}$ | Input | Active-Low | Chip Select |
| | 25 | INT | INT | Output | Active-High | Interrupt |
| | 26 | RDY_$\overline{DTACK}$ | $\overline{DTACK}$ | Output | Active-Low | Data Acknowledge |
| | 69—76 | AD[7:0] | AD[7:0] | I/O | — | Address/Data Bus |
| | 83 | MPCLK | MPCLK | Input | — | Microprocessor Clock |
| MODE 3 | 19 | $\overline{WR}$_$\overline{DS}$ | $\overline{WR}$ | Input | Active-Low | Write |
| | 22 | $\overline{RD}$_R/$\overline{W}$ | $\overline{RD}$ | Input | Active-Low | Read |
| | 23 | ALE_$\overline{AS}$ | ALE | Input | — | Address Latch Enable |
| | 24 | $\overline{CS}$ | $\overline{CS}$ | Input | Active-Low | Chip Select |
| | 25 | INT | INT | Output | Active-High | Interrupt |
| | 26 | RDY_$\overline{DTACK}$ | RDY | Output | Active-High | Ready |
| | 69—76 | AD[7:0] | AD[7:0] | I/O | — | Data Bus |
| | 79—82 | A[3:0] | A[3:0] | Input | — | Address Bus |
| | 83 | MPCLK | MPCLK | Input | — | Microprocessor Clock |
| MODE 4 | 19 | $\overline{WR}$_$\overline{DS}$ | $\overline{WR}$ | Input | Active-Low | Write |
| | 22 | $\overline{RD}$_R/$\overline{W}$ | $\overline{RD}$ | Input | Active-Low | Read |
| | 23 | ALE_$\overline{AS}$ | ALE | Input | — | Address Latch Enable |
| | 24 | $\overline{CS}$ | $\overline{CS}$ | Input | Active-Low | Chip Select |
| | 25 | INT | INT | Output | Active-High | Interrupt |
| | 26 | RDY_$\overline{DTACK}$ | RDY | Output | Active-High | Ready |
| | 69—76 | AD[7:0] | AD[7:0] | I/O | — | Address/Data Bus |
| | 83 | MPCLK | MPCLK | Input | — | Microprocessor Clock |

## Microprocessor Interface (continued)

### Microprocessor Clock (MPCLK) Specifications

The microprocessor interface is designed to operate at clock speeds up to 16.384 MHz without requiring any wait-states. Wait-states may be needed if higher microprocessor clock speeds are required. The microprocessor clock (MPCLK, pin 83) specification is shown in Table 5. This clock must be supplied only if the RDY_DTACK and INT outputs are required to be synchronous to MPCLK. Otherwise, the MPCLK pin must be connected to ground.

**Table 5. Microprocessor Input Clock Specifications**

| Name | Symbol | Period and Tolerance | $T_{rise}$ Typ | $T_{fall}$ Typ | Duty Cycle | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min High | Min Low | |
| MPCLK | t1 | 61 to 323 | 5 | 5 | 27 | 27 | ns |

### Internal Chip Select Function

When the microprocessor interface is configured to operate in the multiplexed address/data bus modes (MPUX = 1), the user has access to an internal chip select function. This function allows a microprocessor to selectively read or write a specific T7698 device in a system of up to eight devices on the microprocessor bus. Externally tying $\overline{CS}$ = 0 (pin 24) and A3 = 1 (pin 79) on every device enables the internal chip select function. Individual device addresses are established by externally connecting the other three address pins, A[2:0] (pins 80, 81, 82), to a unique address value in the range of 000 through 111. In order for a device to respond to the register read or write request from the microprocessor, the address data bus AD[6:4] (pins 70, 71, 72) must match the specific address defined on A[2:0]. If $\overline{CS}$ and A3 pins are tied low, the internal chip select function is disabled and all devices will respond to a microprocessor write request. However, if $\overline{CS}$ = 1, none of the devices will respond to the microprocessor read/write request.

The I/O timing specifications for the microprocessor interface are given on page 103.

## Microprocessor Interface (continued)

### Microprocessor Interface Register Architecture

The register bank architecture of T7698 consists of a primary register bank for the quad line interface unit and secondary register banks for the receive frame monitor [1—8] and FDL [1—8]. The primary register bank consists of sixteen 8-bit registers comprising the alarm, control, and configuration registers for the quad line interface unit. Register 13 (1101) of the primary register bank is a global index register used to access the secondary registers (this is needed because the microprocessor address bus is only 4 bits wide). The default (reset) value of register 13 is 00 (hexadecimal) allowing writes to and reads from the primary (LIU) register bank. Writing 01 (hexadecimal) through 08 (hexadecimal) to register 13 allows access to frame monitors [1—8], respectively, and writing 11 (hexadecimal) through 18 (hexadecimal) allows access to FDL [1—8], respectively.

Table 6 shows the primary register bank and Figure 3 shows the secondary register bank architecture.

**Table 6. Primary (LIU) Register Bank**

| Designation | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Alarm Registers (Read Only)** | | | | | | | | | |
| 0 | 0000 | LOTC2 | TDM2 | DLOS2 | ALOS2 | LOTC1 | TDM1 | DLOS1 | ALOS1 |
| 1 | 0001 | LOTC4 | TDM4 | DLOS4 | ALOS4 | LOTC3 | TDM3 | DLOS3 | ALOS3 |
| **Alarm Mask Registers (Read/Write)** | | | | | | | | | |
| 2 | 0010 | MLOTC2 | MTDM2 | MDLOS2 | MALOS2 | MLOTC1 | MTDM1 | MDLOS1 | MALOS1 |
| 3 | 0011 | MLOTC4 | MTDM4 | MDLOS4 | MALOS4 | MLOTC3 | MTDM3 | MDLOS3 | MALOS3 |
| **Global Control Registers (Read/Write)** | | | | | | | | | |
| 4 | 0100 | HIGHZ4 (1) | HIGHZ3 (1) | HIGHZ2 (1) | HIGHZ1 (1) | ICTMODE (0) | LOSSTD | SWRESET(0) | GMASK (1) |
| 5 | 0101 | LOSSD | ACM | ALM | DUAL | CODE | JAT | JAR | CDR |
| **Channel Configuration Registers (Read/Write)** | | | | | | | | | |
| 6 | 0110 | EQA1 | EQB1 | EQC1 | LOOPA1 | LOOPB1 | XAIS1 | MASK1 | PWRDN1 |
| 7 | 0111 | EQA2 | EQB2 | EQC2 | LOOPA2 | LOOPB2 | XAIS2 | MASK2 | PWRDN2 |
| 8 | 1000 | EQA3 | EQB3 | EQC3 | LOOPA3 | LOOPB3 | XAIS3 | MASK3 | PWRDN3 |
| 9 | 1001 | EQA4 | EQB4 | EQC4 | LOOPA4 | LOOPB4 | XAIS4 | MASK4 | PWRDN4 |
| 10 | 1010 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 1011 | 0 | CODE3 | 0 | CODE4 | 0 | 0 | 0 | 0 |
| 12 | 1100 | CODE1 | CODE2 | JABW0 (0) | PHIZALM (0) | PRLALM (0) | PFLALM (0) | RCVAIS (0) | ALTIMER (0) |
| 13 | 1101 | (VERSION)* | 0 | 0 | RI4 | RI3 | RI2 | RI1 | RI0 |
| 14—15 | 1110—1111 | RESERVED | | | | | | | |

* Device version determines reset state of bit. 0 = V1 and V2; 1 = V3.

Notes:
A numerical suffix appended to the bit name identifies the channel number.

Bits shown in parentheses indicate the state forced during a reset condition.

All registers must be configured by the user before the device can operate as required for the particular application.

## Microprocessor Interface (continued)

### Microprocessor Interface Register Architecture (continued)

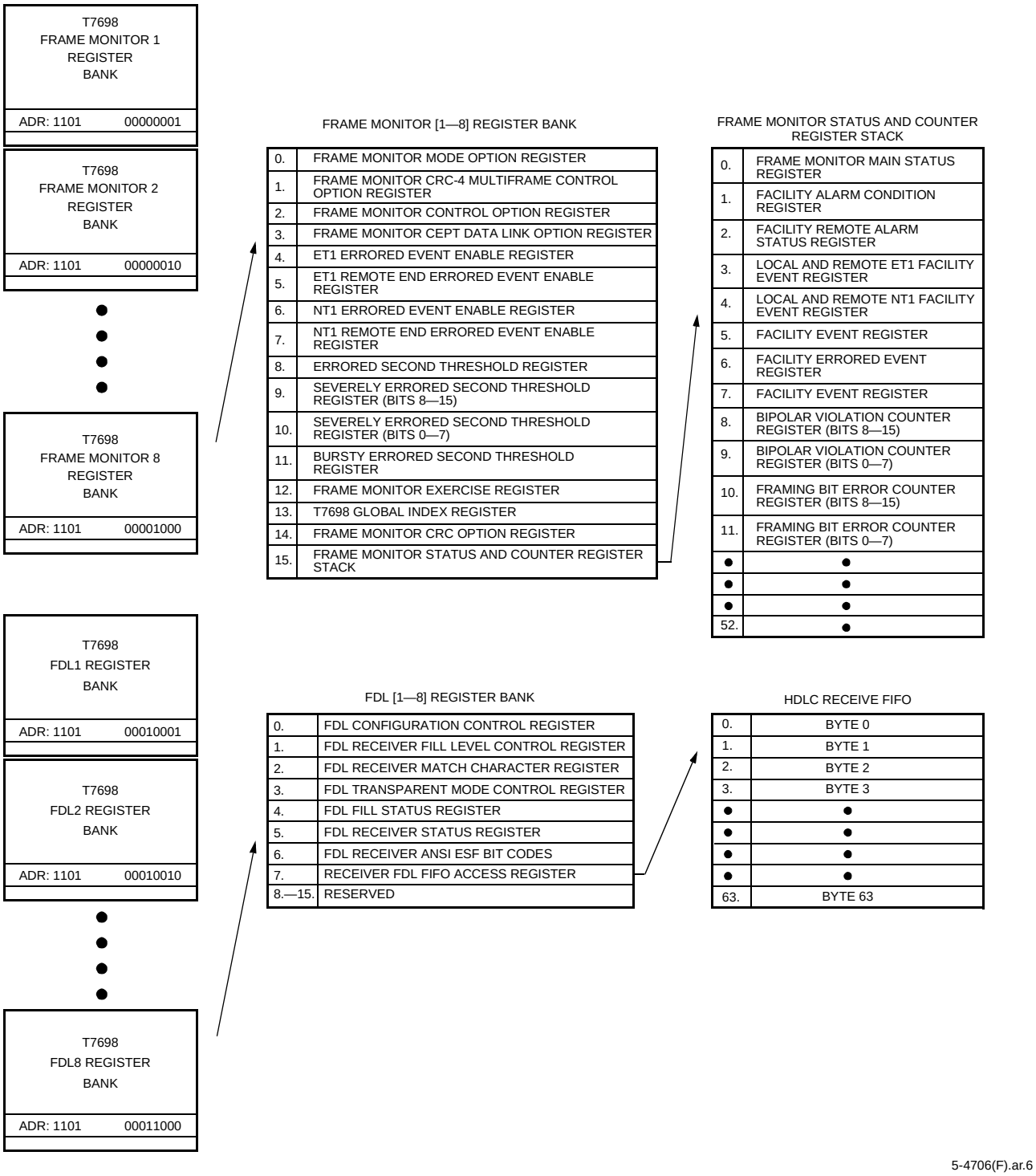


**Figure 3. T7698's Secondary Register Bank Architecture**

## Microprocessor Interface (continued)

### Microprocessor Interface Register Architecture (continued)

#### Examples of Microprocessor Writes and Reads

1. Write 29 (hexadecimal) to register 5 of the LIU.
   Step 1. Write 00 (hexadecimal) to address 1101 (this selects the LIU register bank).
   Step 2. Write 29 (hexadecimal) to address 0101 (this writes 29 to the LIU register 5).
2. Read register 2 of the LIU.
   Step 1. Write 00 (hexadecimal) to address 1101 (this selects the LIU register bank).
   Step 2. Read address 0010 (this reads the LIU register 2).
3. Write 20 (hexadecimal) to register 0 of frame monitor 1.
   Step 1. Write 01 (hexadecimal) to address 1101 (this selects the frame monitor 1 register bank).
   Step 2. Write 20 (hexadecimal) to address 0000 (this writes 20 to the frame monitor 1 register 0).
4. Read register 10 of frame monitor 7.
   Step 1. Write 07 (hexadecimal) to address 1101 (this selects the frame monitor 7 register bank).
   Step 2. Read address 1010 (this reads the frame monitor 7, register 10).
5. Read status registers Framer_SR0—Framer_SR20 of frame monitor 5.
   Step 1. Write 05 (hexadecimal) to 1101 (this selects the frame monitor 5 register bank).
   Step 2. Read address 1111 (this reads the contents of register Framer_SR0).
   Step 3. Read address 1111 (this reads the contents of register Framer_SR1).
   Step 4. Read address 1111 (this reads the contents of register Framer _SR2).
   ⋮
   Step 22. Read address 1111 (this reads the contents of register Framer_SR20).

   Note that every new access to a frame monitor status register (register 15) starts the read at Framer_SR0. The read counter is incremented internally so subsequent read commands read the contents of Framer _SR1, Framer _SR2, etc. Also, the chip select ($\overline{CS}$) must remain low for the entire time that register 15 is being read.
6. Write A6 (hexadecimal) to register 0 of FDL1.
   Step 1. Write 11 (hexadecimal) to address 1101 (this selects the FDL1 register bank).
   Step 2. Write A6 (hexadecimal) to address 0001 (this writes A6 to FDL1 register bank).
7. Read register 6 of FDL3.
   Step 1. Write 13 (hexadecimal) to address 1101 (this selects the FDL3 register bank).
   Step 2. Read address 0110 (this reads the FDL3 register 6).
8. Read 10 bytes from the receive FIFO of FDL8.
   Step 1. Write 18 (hexadecimal) to address 1101 (this selects the FDL8 register bank).
   Step 2. Read address 0111 (this reads the first byte from the FDL8 FIFO).
   Step 3. Read address 0111 (this reads the second byte from the FDL8 FIFO).
   ⋮
   Step 11. Read address 0111 (this reads the tenth byte from the FDL8 FIFO).

   Note that the FIFO pointer keeps track of the location where data has not been read.

## Line Interface Units

The line interface block diagram is shown in Figure 4. For illustration purposes, only one of the four on-chip line interfaces is shown. Pin names that apply to all four channels are followed by the designation [4:1].

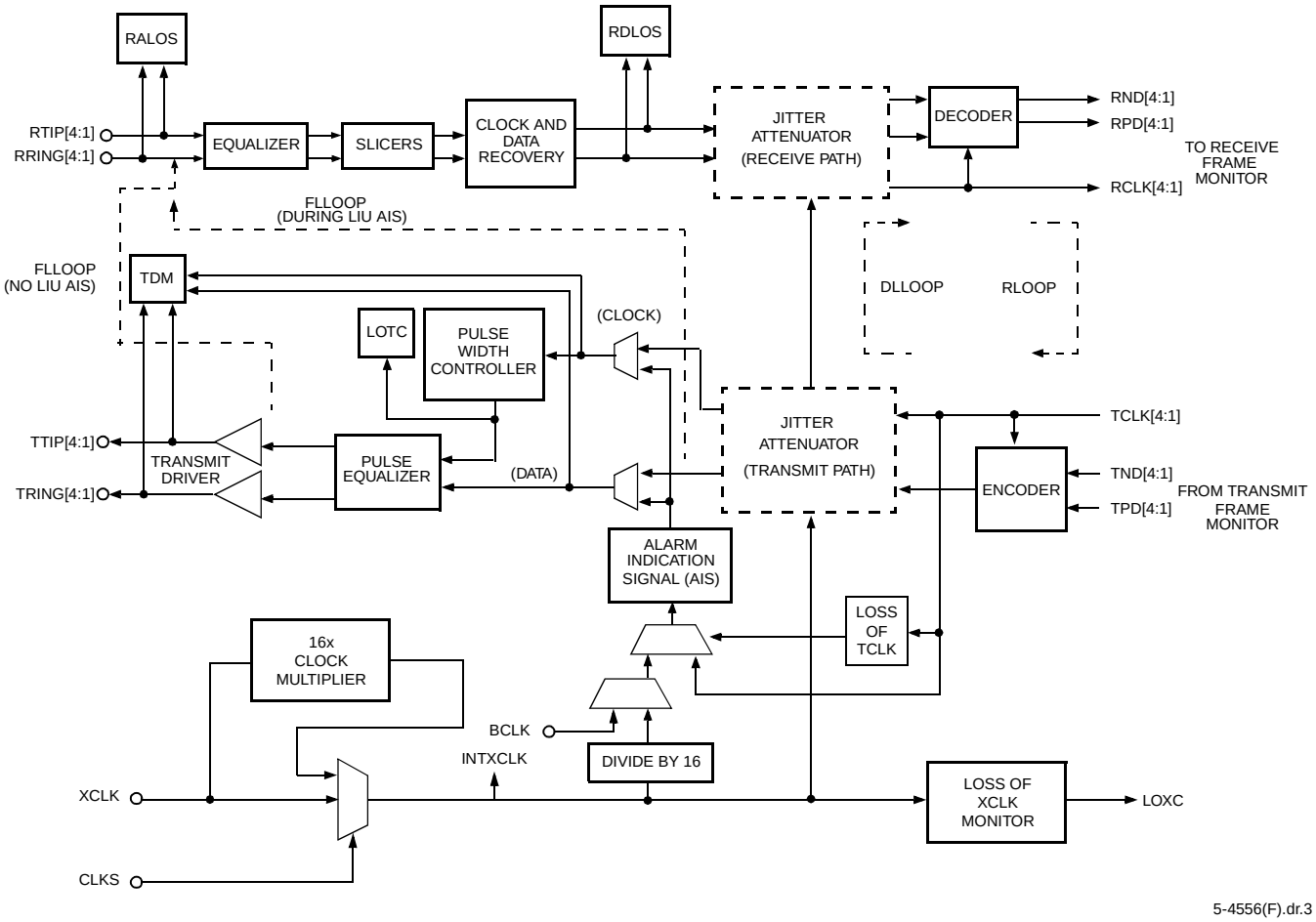


**Figure 4. Block Diagram of the Quad Line Interface Unit (Single Channel)**

# Line Interface Units: Receive

## Data Recovery

The receive line interface unit (RLIU) format is bipolar alternate mark inversion (AMI). The data rate tolerance is ±130 ppm (DS1) or ±80 ppm (CEPT). The receiver first restores the incoming data and detects analog loss of signal. Subsequent processing is optional and depends on the programmable device configuration established within the microprocessor interface registers. The RLIU utilizes an equalizer to operate on line length with up to 15 dB of loss at 772 kHz (DS1) or 13 dB loss at 1.024 MHz (CEPT). The signal is then peak-detected and sliced to produce digital representations of the data.

Selectable clock and data recovery, digital loss of signal, jitter attenuation, and data decoding are performed. For applications bypassing the clock and data recovery function (CDR = 0), the receive digital output format is unretimed sliced data (RZ positive and negative data). For clock and data recovery applications (CDR = 1), the receive digital output format is nonreturn to zero (NRZ) with selectable dual-rail or single-rail system interface. The recovered clock (RCLK, pins 15, 37, 65, 87) is only provided when CDR = 1 (see Table 2 above).

The clock is recovered by a digital phase-locked loop that uses XCLK (pin 29) as a reference to lock to the data rate component. Because the internal reference clock is a multiple of the received data rate, the RCLK output (pins 15, 37, 65, 87) will always be a valid DS1/CEPT clock that eliminates false-lock conditions. During periods with no receive input signal, the free-run frequency of RCLK is defined to be either XCLK/16 or XCLK, depending on the state of CLKS (pin 1). RCLK is always active with a duty-cycle centered at 50%, deviating by no more than ±5%. Valid data is recovered within the first few bit periods after the application of XCLK. The delay of the data through the receive circuitry is approximately 1 to 14 bit periods, depending on the CDR and CODE configurations. Additional delay is introduced if the jitter attenuator is selected for operation in the receive path (see the LIU Delay Values section, page 40).

## Jitter Accommodation and Jitter Transfer Without the Jitter Attenuator

The RLIU is designed to accommodate large amounts of input jitter. The RLIU's jitter performance exceeds the requirements shown in the RLIU Specifications tables (Table 10 and Table 11). Typical receiver performance without the jitter attenuator in the path is shown in Figure 5 through Figure 8. Jitter transfer is independent of input ones density on the line interface.

## Receiver Configuration Modes

### Clock/Data Recovery Mode (CDR)

The clock/data recovery function in the receive path is selectable via the CDR bit (register 5, bit 0). If CDR = 1, the clock and data recovery function is enabled and provides a recovered clock (RCLK) with retimed data (RPD/RDATA, RND). If CDR = 0, the clock and data recovery function is disabled, and the RZ data from the slicers is provided over RPD and RND to the system. In this mode, ALOS is available on the RCLK/ALOS pins, and downstream functions selected by microprocessor register 5 (JAR, ACM, LOSSD) are ignored.

### Zero Substitution Decoding (CODE)

When single-rail operation is selected with DUAL = 0 (register 5, bit 4), the B8ZS/HDB3 decoding can be selected. CODE = 1 selects the B8ZS/HDB3 decoding operation in all four channels, regardless of the state of the CODE[1—4] bits. The B8ZS/HDB3 decoding operation can be selected for individual channels independently by setting CODE = 0 and programming CODE[1—4] bits for the respective channels.

**Note:** Encoding and decoding are not independent. Selecting B8ZS/HDB3 decoding in the receiver selects B8ZS/HDB3 encoding in the transmitter.

**Table 7. Register Map for CODE Bits**

| Name | Location | |
|---|---|---|
| | Register | Bit |
| CODE | 5 | 3 |
| CODE1 | 12 | 7 |
| CODE2 | 12 | 6 |
| CODE3 | 11 | 6 |
| CODE4 | 11 | 4 |

## Line Interface Units: Receive (continued)

### Receiver Configuration Modes (continued)

When decoding is selected for a given channel, decoded receive data and code violations appear on the RDATA and BPV pins, respectively. If coding is not selected, receive data and any bipolar violations (such as two consecutive 1s of the same polarity) appear on the RDATA and BPV pins, respectively.

#### Alternate Logic Mode (ALM)

The alternate logic mode (ALM) control bit (register 5, bit 5) selects the receive and transmit data polarity (i.e., active-high vs. active-low). If ALM = 0, the receiver circuitry (and transmit input) assumes the data to be active-low polarity. If ALM = 1, the receiver circuitry (and transmit input) assumes the data to be active-high polarity. The ALM control is used in conjunction with the ACM control (register 5, bit 6) to determine the receive data retiming mode.

#### Alternate Clock Mode (ACM)

The alternate clock mode (ACM) control bit (register 5, bit 6) selects the positive or negative clock edge of the receive clock (RCLK) for receive data retiming. The ACM control is used in conjunction with ALM (register 5, bit 5) control to determine the receive data retiming modes. If ACM = 1, the receive data is retimed on the positive edge of the receive clock. If ACM = 0, the receive data is retimed on the negative edge of the receive clock. Note that this control does not affect the timing relationship for the transmitter inputs. See Figure 33 on page 109.

### Receive Line Interface Configuration Modes

#### RLIU Alarms

**Analog Loss of Signal (ALOS) Alarm**. An analog signal detector monitors the receive signal amplitude and reports its status in the analog loss of signal alarm bits in registers 0 and 1. Analog loss of signal is indicated (ALOS = 1) if the amplitude at the RRING and RTIP inputs drops below a voltage approximately 18 dB below the nominal signal amplitude. The ALOS alarm condition will clear when the receive signal amplitude returns to greater than 14 dB below normal. The ALOS alarm status bit will latch the alarm and remain set until being cleared by a read (clear on read).

Upon the transition from ALOS = 0 to ALOS = 1, a microprocessor interrupt will be generated if the ALOS interrupt mask bits MALOS in registers 2 and 3 are not set and the GMASK bit (register 4, bit 0) is not set.

The ALOS circuitry provides 4 dB of hysteresis to prevent alarm chattering. The time required to detect ALOS is selectable. When ALTIMER = 0 (register 12, bit 0), ALOS is declared between 1 ms and 2.6 ms after losing signal as required by I.431(3/93) and ETS-300-233 (5/94). If ALTIMER = 1, ALOS is declared between 10 and 255 bit symbol periods after losing signal as required by G.775 (11/95). The timing is derived from the XCLK clock, if XCLK is available or BCLK, if XCLK is not available, as may be the case when CDR = 0. The detection time is independent of signal amplitude before the loss condition occurs. Normally, ALTIMER = 1 would be used only in CEPT mode since no T1/DS1 standards require this mode. In T1/DS1 mode, this bit should normally be zero.

The behavior of the receiver RLIU outputs under ALOS conditions is dependent on the loss shutdown (LOSSD) control bit (register 5, bit 7) in conjunction with the receive alarm indication select control bit (RCVAIS; register 12, bit 1) as described in the Loss Shutdown (LOSSD) and Receiver AIS (RCVAIS) section on page 25.

**Digital Loss of Signal (DLOS) Alarm**. A digital loss of signal (DLOS) detector guarantees the received signal quality as defined in the appropriate ANSI, Bellcore, and ITU standards. The digital loss of signal alarms are reported in the alarm status registers 0 and 1. During DS1 operation, digital loss of signal (DLOS = 1) is indicated if 100 or more consecutive 0s occur in the receive data stream. The DLOS condition is deactivated when the average ones density of at least 12.5% is received in 100 contiguous pulse positions. The DLOS alarm status bit will latch the alarm and remain set until being cleared by a read (clear on read). The LOSSTD control bit (register 4, bit 2) selects the conformance protocols for the DLOS alarm indication per Table 8. Setting LOSSTD = 1 adds an additional constraint that there are less than 15 consecutive zeros in the DS1 data stream before DLOS is deactivated.

## Line Interface Units: Receive (continued)

### Receive Line Interface Configuration Modes (continued)

During CEPT operation, DLOS is indicated when 255 or more consecutive 0s occur in the receive data stream. The DLOS indication is deactivated when the average ones density of at least 12.5% is received in 255 contiguous pulse positions. LOSSTD has no effect in CEPT mode. Upon the transition from DLOS = 0 to DLOS = 1, a microprocessor interrupt will be generated if the DLOS interrupt mask bits (MDLOS; registers 2 and 3, bits 1 and 5 ) are not set and the GMASK bit (register 4, bit 0) is not set.

The DLOS alarm may occur when FLLOOP is activated (see Line Interface Units: Loopbacks on page 39) due to the abrupt change in signal level at the receiver input. Setting the FLLOOP alarm prevention, PFLALM = 1 (register 12, bit 2), prevents the DLOS alarm from occurring when FLLOOP is activated by quickly resetting the receiver's internal peak detector. It will not prevent the DLOS alarm during the FLLOOP period but only avoids the alarm created by the signal amplitude transient.

**Table 8. Digital Loss of Signal Standard Select**

| LOSSTD | DS1 Mode | CEPT Mode |
|---|---|---|
| 0 | T1M1.3/93-005, ITU-T G.775 | ITU-T G.775 |
| 1 | TR-TSY-000009 | ITU-T G.775 |

**Loss Shutdown (LOSSD) and Receiver AIS (RCVAIS).** The loss shutdown control bit (LOSSD; register 5, bit 7) acts in conjunction with the receive alarm indication select (RCVAIS) control bit (register 12, bit 1) to place the digital outputs in a predetermined state when a digital loss of signal (DLOS) or analog loss of signal (ALOS) alarm occurs.

If LOSSD = 0 and RCVAIS = 0, the RND, RPD, and RCLK outputs will be unaffected by the DLOS alarm condition. However, when an ALOS alarm condition is indicated in the alarm status registers, the RPD and RND outputs are forced to their inactive state (dependent on ALM state) and the RCLK free runs (based on XCLK frequency).

If LOSSD = 0, RCVAIS = 1, and a DLOS or an ALOS alarm condition is indicated in the alarm status registers, the RPD and RND outputs will present an alarm indication signal (AIS, all ones) based on the free-running clock frequency, and the RCLK free runs.

If LOSSD = 1, regardless of the state of RCVAIS, and a DLOS or an ALOS alarm condition is indicated in the alarm status registers, the RPD and RND outputs are forced to their inactive state (dependent on ALM state) and the RCLK free runs.

The RND, RPD, and RCLK signals will remain unaffected if any loopback (FLLOOP, RLOOP, DLLOOP) is activated independent of LOSSD and RCVAIS settings.

The LOSSD and RCVAIS behavior is summarized in Table 9.

**Table 9. LOSSD and RCVAIS Control Configurations (Not Valid During Loopback Modes)**

| LOSSD | RCVAIS | ALARM | RPD/RND | RLCK |
|---|---|---|---|---|
| 0 | 0 | ALOS | 0 if ALM = 1, 1 if ALM = 0 | Free Runs |
| 0 | 0 | DLOS | Normal Data | Recovered Clock |
| 0 | 1 | ALOS | AIS (all ones) | Free Runs |
| 0 | 1 | DLOS | AIS (all ones) | Free Runs |
| 1 | X | ALOS | 0 if ALM = 1, 1 if ALM = 0 | Free Runs |
| 1 | X | DLOS | 0 if ALM =1, 1 if ALM = 0 | Free Runs |

**RLIU Bipolar Violation (BPV) Alarm.** The bipolar violation (BPV) alarm is used only in the single-rail mode of operation. When B8ZS(DS1)/HDB3(CEPT) coding is not used (i.e., CODE = 0), any violations in the receive data (such as two or more consecutive 1s on a rail) are indicated on the RND/BPV outputs. When B8ZS(DS1)/HDB3(CEPT) coding is used (i.e., CODE = 1), the HDB3/B8ZS code violations are reflected on the RND/BPV outputs.

## Line Interface Units: Receive (continued)

### DS1 Receiver Specifications

During DS1/T1 operation, the RLIU will perform as specified in Table 10.

**Table 10. DS1 RLIU Specifications**

| Parameter | Min | Typ | Max | Unit | Spec |
|---|---|---|---|---|---|
| Analog Loss of Signal: | | | | | |
| Threshold to Assert | 17.5 | 18 | 23 | dB[1] | I.431 |
| Threshold to Clear | 13.5 | 14 | 17.5 | dB[1] | — |
| Hysteresis | — | 4 | — | dB | — |
| Time to Assert (ALTIMER = 0) | 1.0 | — | 2.6 | ms | I.431 |
| Receiver Sensitivity[2] | 11 | 15 | — | dB | — |
| Jitter Transfer: | | | | | |
| 3 dB Bandwidth | — | 3.84 | — | kHz | Figure 6 on page 27 |
| Peaking | — | — | 0.1 | dB | Figure 12 on page 37 |
| Generated Jitter | — | 0.04 | 0.05 | UIp-p | GR-499-CORE<br>ITU-T G.824 |
| Jitter Accommodation | — | — | — | — | Figure 5 on page 27<br>Figure 11 on page 37 |
| Return Loss[3]: | | | | | |
| 51 kHz to 102 kHz | 14 | — | — | dB | — |
| 102 kHz to 1.544 MHz | 20 | — | — | dB | — |
| 1.544 MHz to 2.316 MHz | 16 | — | — | dB | — |
| Digital Loss of Signal: | | | | | |
| Flag Asserted When Consecutive Bit Positions Contain | 100 | — | — | zeros | ITU-T G.775,<br>T1M1.3/93-005 |
| Flag Deasserted when | | | | | |
| Data Density Is and | 12.5 | — | — | % ones | — |
| Maximum Consecutive Zeros Are | — | — | 15 | zeros | TR-TRY-000009 |
| | — | — | 99 | zeros | ITU-T G.775, T1M1.3/<br>93-005 |

1. Below the nominal pulse amplitude of 3.0 V with the line interface circuitry specified (see Line Interface Unit: Line Circuitry section).
2. Cable loss at 772 kHz.
3. Using Lucent transformer 2795B and components listed in Table 111.

## Line Interface Units: Receive (continued)

### DS1 Receiver Specifications (continued)

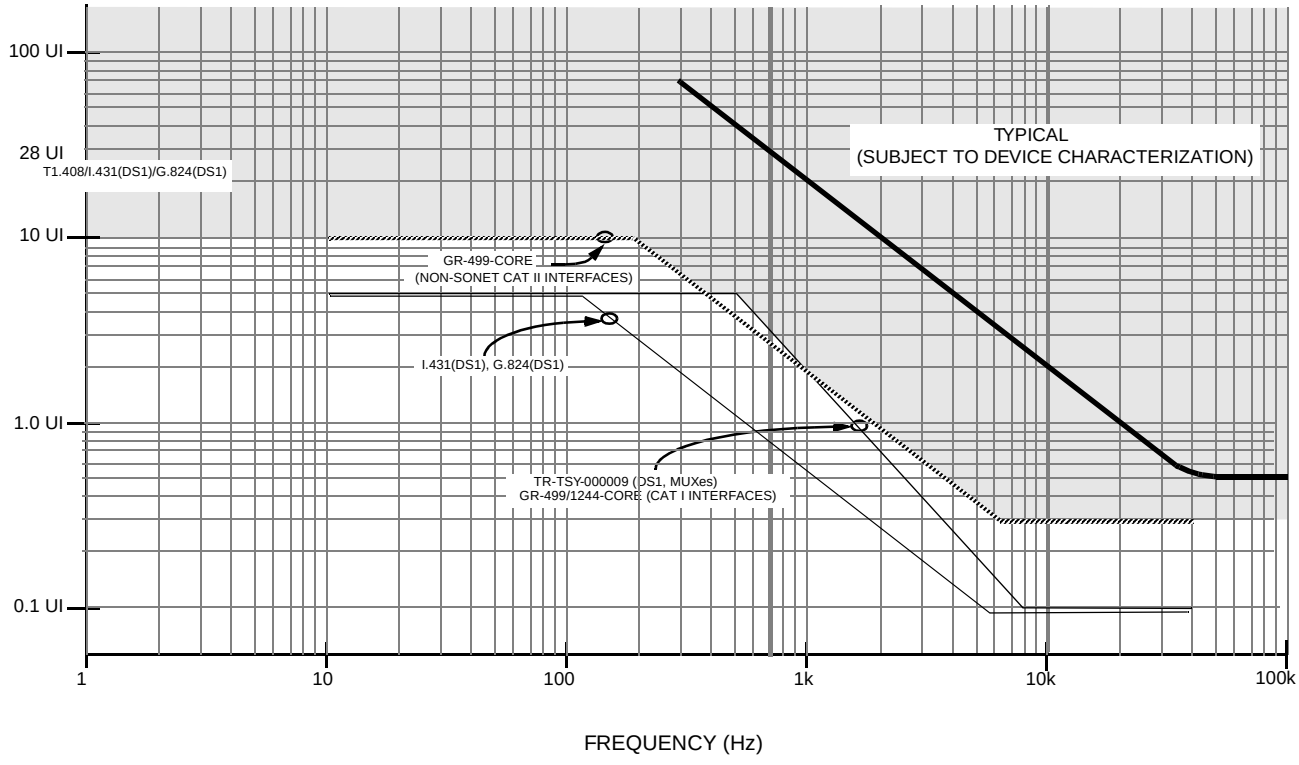


**Figure 5. DS1/T1 Receiver Jitter Accommodation Without Jitter Attenuator**

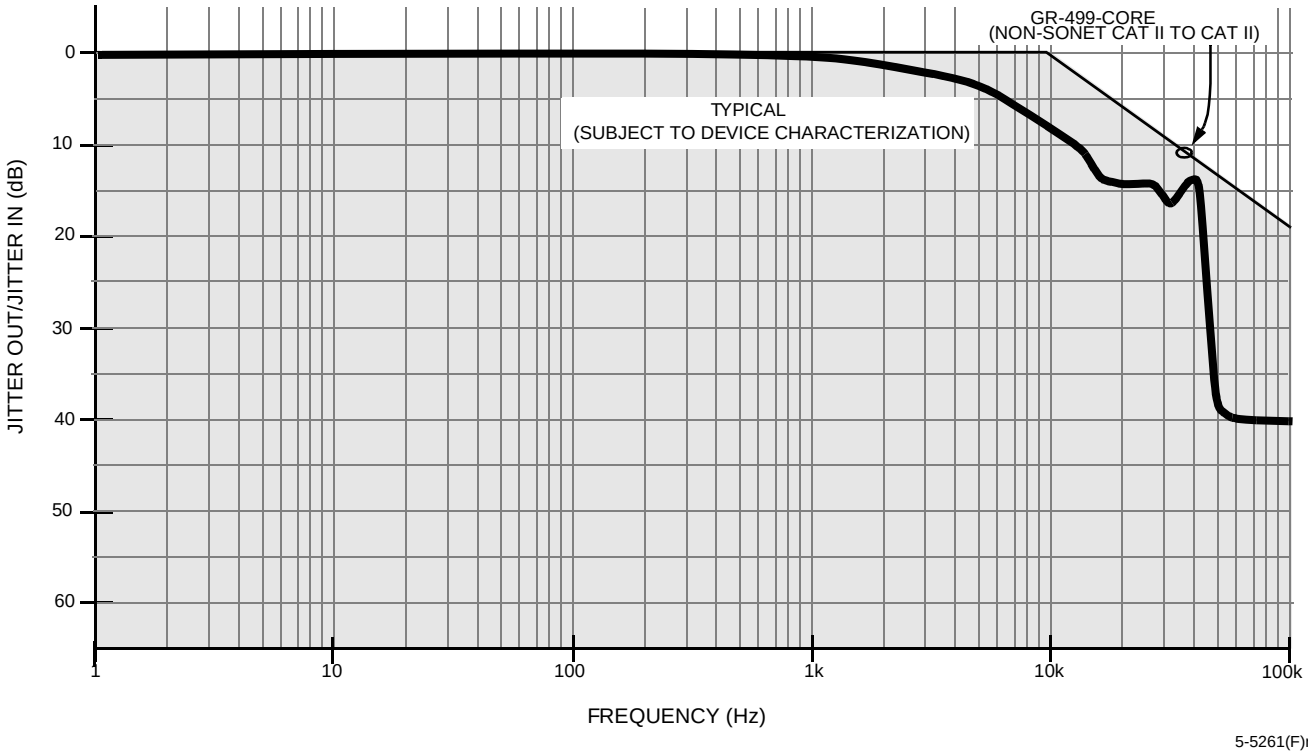


**Figure 6. DS1/T1 Receiver Jitter Transfer Without Jitter Attenuator**

## Line Interface Units: Receive (continued)

### CEPT Receiver Specifications

During CEPT/E1 operation, the RLIU will perform as specified in Table 11.

**Table 11. CEPT RLIU Specifications**

| Parameter | Min | Typ | Max | Unit | Spec |
|---|---|---|---|---|---|
| Analog Loss of Signal: | | | | | |
| Threshold to Assert | 17.5 | 18 | 23 | dB[1] | I.431, ETSI 300 233 |
| Threshold to Clear | 13.5 | 14 | 17.5 | dB[1] | — |
| Hysteresis | — | 4 | — | dB | — |
| Time to Assert (ALTIMER = 0) | 1.0 | — | 2.6 | ms | I.431, ETSI 300 233 |
| Time to Assert (ALTIMER = 1) | 10 | — | 255 | UI | G.775 |
| Receiver Sensitivity[2] | 11 | 13.5 | — | dB | — |
| Interference Immunity[3]: | 9 | 12 | — | dB | ITU-T G.703 |
| Jitter Transfer: | | | | | |
| 3 dB Bandwidth, Single Pole Roll Off | — | 5.1 | — | kHz | Figure 8 on page 29 |
| Peaking | — | — | 0.5 | dB | Figure 14 on page 38 |
| Generated Jitter | — | 0.04 | 0.05 | UIp-p | ITU-T G.823, I.431 |
| Jitter Accommodation | — | — | — | — | Figure 7 on page 29<br>Figure 13 on page 38 |
| Return Loss[4]: | | | | | ITU-T G.703 |
| 51 kHz to 102 kHz | 14 | — | — | dB | |
| 102 kHz to 1.544 MHz | 20 | — | — | dB | |
| 1.544 MHz to 2.316 MHz | 16 | — | — | dB | |
| Digital Loss of Signal: | | | | | |
| Flag Asserted When Consecutive Bit Positions Contain | 255 | — | — | zeros | — |
| Flag Deasserted When Data Density is (LOSSTD = 1) | 12.5 | — | — | %ones | ITU-T G.775 |

1. Below the nominal pulse amplitude of 3.0 V with the line circuitry specified (see Line Interface Unit: Line Circuitry section).
2. Cable loss at 1.024 MHz.
3. Amount of cable loss for which the receiver will operate error-free in the presence of a –18 dB interference signal summing with the intended signal source.
4. Using Lucent transformer 2795D or 2795C and components listed in Table 111.

## Line Interface Units: Receive (continued)

### CEPT Receiver Specifications (continued)

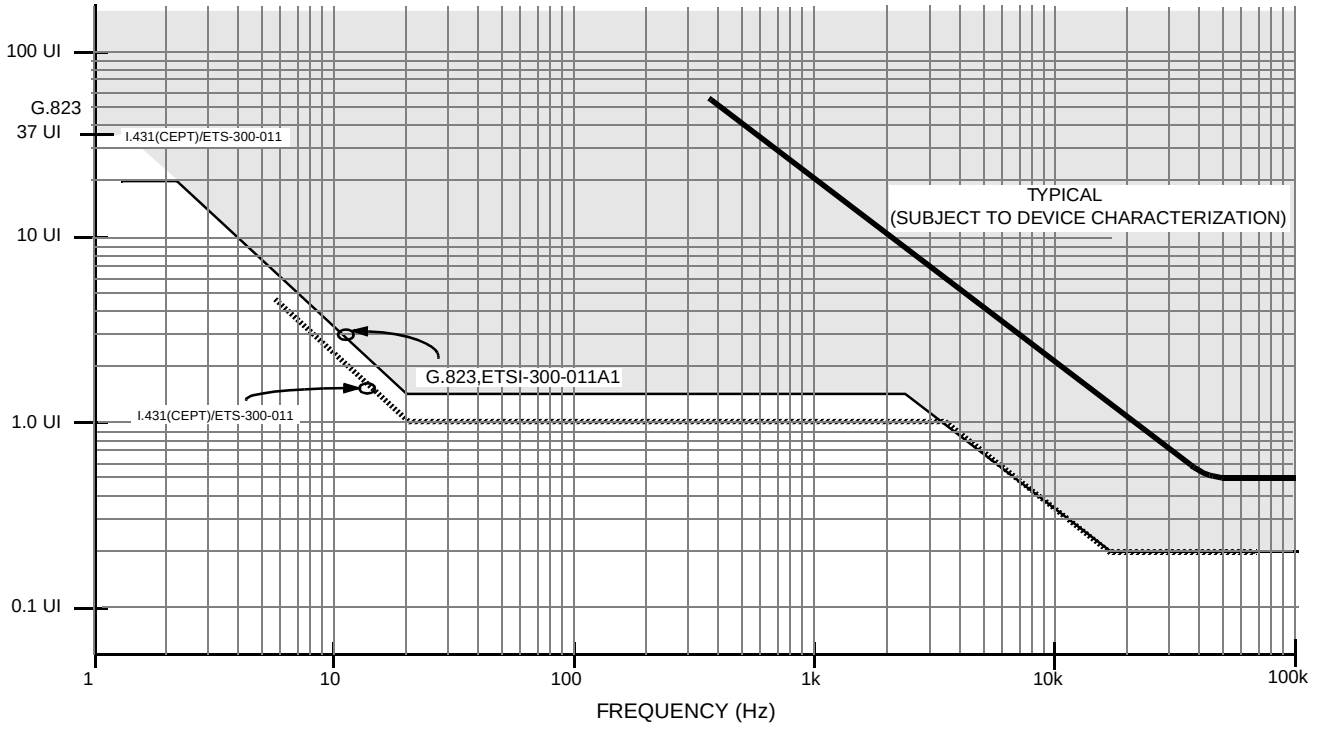


**Figure 7. CEPT/E1 Receiver Jitter Accommodation Without Jitter Attenuator**

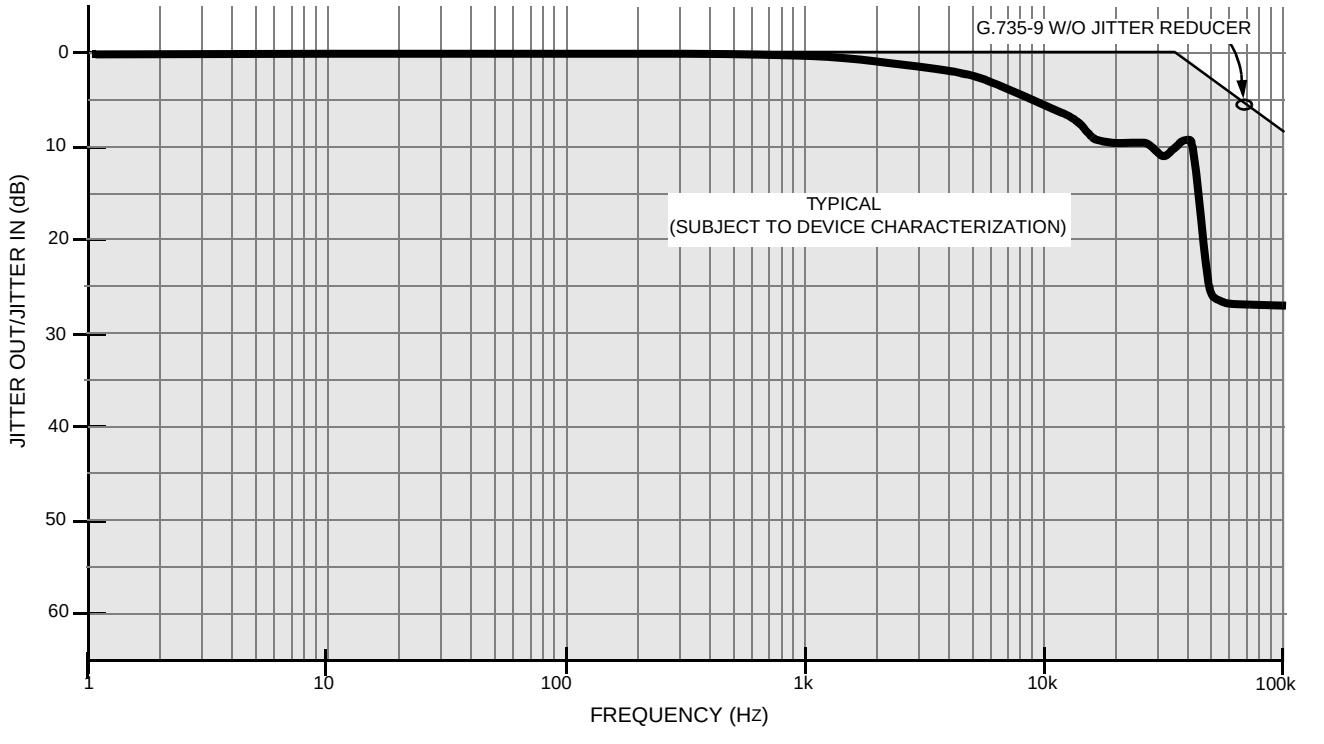


**Figure 8. CEPT/E1 Receiver Jitter Transfer Without Jitter Attenuator**

# Line Interface Units: Transmit

## Output Pulse Generation

The transmitter accepts a clock with NRZ data in single-rail mode (DUAL = 0: register 5, bit 4) or a clock, and positive and negative NRZ data in dual-rail mode (DUAL = 1) from the system. The device converts this data to a balanced bipolar signal (AMI format) with optional B8ZS(DS1)/HDB3(CEPT) encoding and jitter attenuation. Low-impedance output drivers produce these pulses on the line interface. Positive 1s are output as a positive pulse on TTIP, and negative 1s are output as a positive pulse on TRING. Binary 0s are converted to null pulses. The total delay of the data from the system interface to the transmit driver is approximately 3 to 11 bit periods, depending on the code configuration (see the Zero Substitution Decoding (CODE) section, page 23 and the Zero Substitution Encoding (CODE) section, page 31).

Additional delay results if the jitter attenuator is selected for use in the transmit path (see the LIU Delay Values section).

Transmit pulse shaping is controlled by the on-chip pulse-width controller and pulse equalizer. The pulse-width controller produces high-speed timing signals to accurately control the transmit pulse widths. This eliminates the need for a tightly controlled transmit clock duty cycle that is usually required in discrete implementations. The pulse equalizer controls the amplitudes of the pulses. Different pulse equalizations are selected through proper settings of EQA, EQB, and EQC (registers 6 to 9, bits 5 to 7) as described in Table 12.

**Table 12. Equalizer/Rate Control**

| EQA | EQB | EQC | Service | Clock Rate | Transmitter Equalization* | | Maximum Cable Loss† |
|---|---|---|---|---|---|---|---|
| | | | | | Feet | Meters | dB |
| 0 | 0 | 0 | DS1 | 1.544 MHz | 0 ft. to 131 ft. | 0 m to 40 m | 0.6 |
| 0 | 0 | 1 | | | 131 ft. to 262 ft. | 40 m to 80 m | 1.2 |
| 0 | 1 | 0 | | | 262 ft. to 393 ft. | 80 m to 120 m | 1.8 |
| 0 | 1 | 1 | | | 393 ft. to 524 ft. | 120 m to 160 m | 2.4 |
| 1 | 0 | 0 | | | 524 ft. to 655 ft. | 160 m to 200 m | 3.0 |
| 1 | 0 | 1 | CEPT‡ | 2.048 MHz | 75 Ω (Option 2) | | — |
| 1 | 1 | 0 | | | 120 Ω or 75 Ω (Option 1) | | — |
| 1 | 1 | 1 | Not Used | — | — | | — |

* In DS1 mode, the distance to the DSX for 22 gauge PIC (ABAM) cable is specified. Use the maximum cable loss figures for other cable types. In CEPT mode, equalization is specified for coaxial or twisted-pair cable.
† Loss measured at 772 kHz.
‡ In 75 Ω applications, Option 1 is recommended over Option 2 for lower device power dissipation. Option 2 allows for the same transformer as used in CEPT 120 Ω applications.

## Jitter

The intrinsic jitter of the transmit path, i.e., the jitter at TTIP/TRING when no jitter is applied to TCLK (and the jitter attenuator is not selected, JAT = 0), is typically 5 nsp-p and will not exceed 0.02 UIp-p.

## Line Interface Units: Transmit (continued)

### Transmitter Configuration Modes

#### Zero Substitution Encoding (CODE)

Zero substitution B8ZS/HDB3 encoding can be activated only in the single-rail system interface mode (DUAL = 0). CODE = 1 selects the B8ZS/HDB3 encoding operation in all four channels, regardless of the state of the CODE[1—4] bits. The B8ZS/HDB3 encoding operation can be selected for individual channels independently by setting CODE = 0 and programming CODE[1—4] bits for the respective channels.

**Note:** Encoding and decoding are not independent. Selecting B8ZS/HDB3 encoding in the transmitter selects B8ZS/HDB3 decoding in the receiver.

**Table 13. Register Map for CODE Bits**

| Name | Location | |
|---|---|---|
| | Register | Bit |
| CODE | 5 | 3 |
| CODE1 | 12 | 7 |
| CODE2 | 12 | 6 |
| CODE3 | 11 | 6 |
| CODE4 | 11 | 4 |

When coding is selected for a given channel, data transmitted from the system interface on TDATA (pins 17, 35, 67, 85) will be B8ZS/HDB3 encoded before appearing on TTIP and TRING at the line interface.

#### Alarm Indication Signal Generator (XAIS)

When the transmit alarm indication signal control is set (XAIS = 1) for a given channel (registers 6 to 9, bit 2), a continuous stream of bipolar 1s is transmitted to the line interface. The TPD/TDATA and TND inputs are ignored during this mode. The XAIS input is ignored when a remote loopback (RLOOP) is selected using loopback control bits (LOOPA and LOOPB; registers 6 to 9, bits 3 and 4). (See the Line Interface Units: Loopbacks section.)

To maintain application flexibility, the clock source used for the AIS signal is selected by configuring BCLK (pin 30). If a data rate clock is input on the BCLK pin, it will be used to transmit the AIS signal. If BCLK = 0, then TCLK is used to transmit the AIS signal (the smoothed clock from the jitter attenuator is used if JAT = 1 is selected). If BCLK = 1, then the internal XCLK (after being divided by a factor of 16) is used to transmit the AIS signal.

After BCLK is established, a minimum of 16 µs is required for the device to properly select the clock. For any of the above options, the clock tolerance must meet the normal line transmission rates (DS1 1.544 MHz ± 32 ppm; CEPT 2.048 MHz ± 50 ppm).

### Transmitter Alarms

#### Loss of Transmit Clock (LOTC) Alarm

A loss of transmit clock alarm (LOTC = 1; registers 0 and 1, bits 3 and 7) is indicated if any of the clocks in the transmit path disappear. This includes loss of TCLK input, loss of RCLK during remote loopback, loss of jitter attenuator output clock (when enabled), or the loss of clock from the pulse-width controller.

For all of these conditions, a core transmitter timing clock is lost and no data can be driven onto the line. Output drivers TTIP and TRING are placed in a high-impedance state when this alarm condition is active. The LOTC interrupt is asserted between 3 µs and 16 µs after the clock disappears, and deasserts immediately after detecting the first clock edge. The LOTC alarm status bit will latch the alarm and remain set until being cleared by a read (clear on read). Upon the transition from LOTC = 0 to LOTC = 1 a microprocessor interrupt will be generated if the LOTC interrupt mask bit (MLOTC; registers 2 and 3, bits 3 and 7) is not set and the GMASK bit (register 4, bit 0) is not set.

An LOTC alarm may occur when RLOOP is activated and deactivated due to the phase transient that occurs as TCLK switches its source to and from RCLK. Setting the prevent RLOOP alarm bit, (PRLALM = 1; LIU register 12, bit 3) prevents the LOTC alarm from occurring at the activation and deactivation of RLOOP but allows the alarm to operate normally during the RLOOP active period.

#### Transmit Driver Monitor (TDM) Alarm

The transmit driver monitor detects two conditions: a nonfunctional link due to a fault on the primary of the transmit transformer, or periods of no data transmission. The transmit driver monitor alarm (TDM; registers 0 and 1, bits 2 and 6) is the ORed function of both faults and provides information about the integrity of the transmit signal path.

The first monitoring function is provided to detect nonfunctional links and protect the device from damage. The alarm is set (TDM = 1) when one of the transmitter's line drivers (TTIP or TRING) is shorted to power supply or ground, or TTIP and TRING are shorted together.

## Line Interface Units: Transmit (continued)

### Transmitter Alarms (continued)

Under these conditions, internal circuitry protects the device from damage and excessive power supply current consumption by 3-stating the output drivers. The monitor detects faults on the transformer primary, but transformer secondary faults may not be detected.

The monitor operates by comparing the line pulses with the transmit inputs. After 32 transmit clock cycles, the transmitter is powered up in its normal operating mode. The drivers attempt to correctly transmit the next data bit. If the error persists, TDM remains active to eliminate alarm chatter and the transmitter is internally protected for another 32 transmit clock cycles. This process is repeated until the error condition is removed and the TDM alarm is deactivated. The TDM alarm status bit will latch the alarm and remain set until being cleared by a read (clear on read).

The second monitoring function is to indicate periods of no data transmission. The alarm is set (TDM = 1) when 32 consecutive zeros have been transmitted and the alarm condition is cleared on the detection of a single pulse. Again, the TDM alarm status bit will latch the alarm and remain set until being cleared by a read (clear on read). This alarm condition does not alter the state or functionality of the signal path.

Upon the transition from TDM = 0 to TDM = 1 a microprocessor interrupt will be generated if the TDM interrupt mask bit (MTDM; registers 2 and 3, bits 2 and 6) is not set and the GMASK bit (register 4, bit 0) is not set.

A TDM alarm may occur when RLOOP is activated and deactivated. If the prevent RLOOP alarm bit (PRLALM; register 12, bit 3) is not set, then RLOOP may activate an LOTC alarm, which will put the output drivers TTIP and TRING in a high-impedance state as described in Loss of Transmit Clock (LOTC) Alarm on page 31. The high-impedance state of the drivers may in turn generate a TDM alarm. Setting the HIGHZ alarm prevention PHIZALM = 1 (register 12, bit 4) prevents the TDM alarm from occurring when the drivers are in a high-impedance state.

### DS1 Transmitter Pulse Template and Specifications

The DS1 pulse shape template is specified at the DSX (defined by CB119 and ANSI T1.102) and is illustrated in Figure 9. The device also meets the pulse template specified by ITU-T G.703 (not shown).

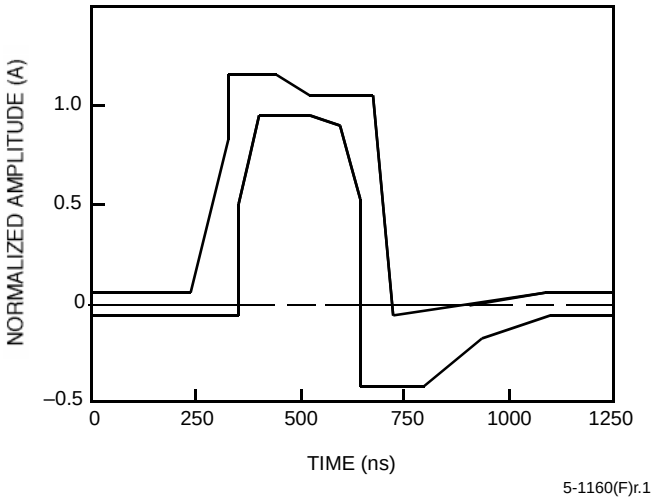


**Figure 9. DSX-1 Isolated Pulse Template**

**Table 14. DSX-1 Pulse Template Corner Points (from CB119)**

| Maximum Curve | | Minimum Curve | |
|---|---|---|---|
| ns | V | ns | V |
| 0 | 0.05 | 0 | –0.05 |
| 250 | 0.05 | 350 | –0.05 |
| 325 | 0.80 | 350 | 0.50 |
| 325 | 1.15 | 400 | 0.95 |
| 425 | 1.15 | 500 | 0.95 |
| 500 | 1.05 | 600 | 0.90 |
| 675 | 1.05 | 650 | 0.50 |
| 725 | –0.07 | 650 | –0.45 |
| 1100 | 0.05 | 800 | –0.45 |
| 1250 | 0.05 | 925 | –0.20 |
| — | — | 1100 | –0.05 |
| — | — | 1250 | –0.05 |

## Line Interface Units: Transmit (continued)

### DS1 Transmitter Pulse Template and Specifications (continued)

During DS1 operation, the TTIP and TRING pins will perform as specified in Table 15.

**Table 15. DS1 Transmitter Specifications**

| Parameter | Min | Typ | Max | Unit | Spec |
|---|---|---|---|---|---|
| Output Pulse Amplitude at DSX[1] | 2.5 | 3.0 | 3.5 | V | AT&T CB119, ANSI T1.102 |
| Output Pulse Width at Line Side of Transformer[1] | 325 | 350 | 375 | ns | |
| Output Pulse Width at Device Pins TTIP and TRING[1] | 330 | 350 | 370 | ns | |
| Positive/Negative Pulse Imbalance[2] | — | 0.1 | 0.4 | dB | |
| Power Levels[3, 4]:<br>772 kHz<br>1.544 MHz[5] | <br>12.6<br>29 | <br>—<br>39 | <br>17.9<br>— | <br>dBm<br>dB | |

1. In accordance with the line circuitry described (see Line Interface Unit: Line Circuitry section).
2. Total power difference.
3. Measured in a 2 kHz band around the specified frequency.
4. Using Lucent transformer 2795B and components in Table 111.
5. Below the power at 772 kHz.

### CEPT Transmitter Pulse Template and Specifications

CEPT pulse shape template is specified at the system output (defined by ITU-T G.703) and is illustrated in Figure 10.

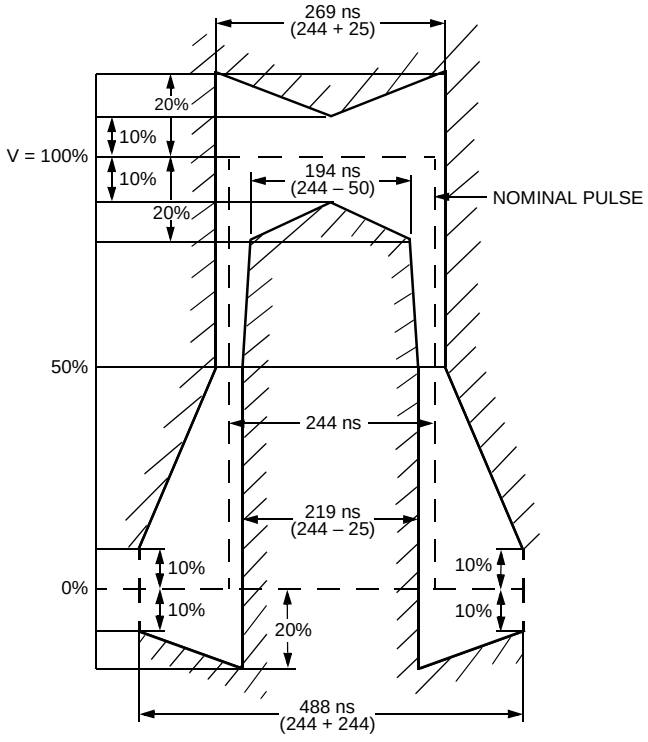


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**Figure 10. ITU-T G.703 Pulse Template**

## Line Interface Units: Transmit (continued)

### CEPT Transmitter Pulse Template and Specifications (continued)

During CEPT operation, the transmitter tip/ring (TTIP/TRING pins) will perform as specified in Table 16.

**Table 16. CEPT Transmitter Specifications**

| Parameter | Min | Typ | Max | Unit | Spec |
|---|---|---|---|---|---|
| Output Pulse Amplitude[1]: | | | | | ITU-T G.703 |
| 75 Ω | 2.13 | 2.37 | 2.61 | V | |
| 120 Ω | 2.7 | 3.0 | 3.3 | V | |
| Output Pulse Width at Line Side of Transformer[1] | 219 | 244 | 269 | ns | |
| Output Pulse Width at Device Pins TTIP and TRING[1] | 224 | 244 | 264 | ns | |
| Positive/Negative Pulse Imbalance: | | | | | |
| Pulse Amplitude | –4 | ±1.5 | 4 | % | |
| Pulse Width | –4 | ±1 | 4 | % | |
| Zero Level (percentage of pulse amplitude) | –5 | 0 | 5 | % | |
| Return Loss[2] (120 Ω): | | | | | CH-PTT |
| 51 kHz to 102 kHz | 9 | — | — | dB | |
| 102 kHz to 2.048 MHz | 15 | — | — | dB | |
| 2.048 MHz to 3.072 MHz | 11 | — | — | dB | |
| Return Loss[2] (75 Ω): | | | | | ETS 300 166: 1993 |
| 51 kHz to 102 kHz | 7 | — | — | dB | |
| 102 kHz to 3.072 MHz | 9 | — | — | dB | |

1. In accordance with the line circuitry described (see Line Interface Unit: Line Circuitry section), measured at the transformer secondary.
2. Using Lucent transformer 2795D or 2795C and components in Table 111.

## Line Interface Units: Jitter Attenuator

A selectable jitter attenuator is provided for narrow-bandwidth jitter transfer function applications. When placed in the LIU receive path, the jitter attenuator provides narrow-bandwidth jitter filtering for line synchronization. The jitter attenuator can also be placed in the transmit path to provide clock smoothing for applications such as synchronous/asynchronous demultiplexers. In these applications, TCLK will have an instantaneous frequency that is higher than the data rate, and some periods of TCLK are suppressed (gapped) in order to set the average long-term TCLK frequency to within the transmit line rate specification. The jitter attenuator will smooth the gapped clock.

### Generated (Intrinsic) Jitter

Generated jitter is the amount of jitter appearing on the output port when the applied input signal has no jitter. The jitter attenuator of this device outputs a maximum of 0.05 UIp-p intrinsic jitter.

### Jitter Transfer Function

The jitter transfer function describes the amount of jitter that is transferred from the input to the output over a range of frequencies. The jitter attenuator exhibits a single-pole roll-off (20 dB/decade) jitter transfer characteristic that has no peaking and a nominal filter corner frequency (3 dB bandwidth) of less than 4 Hz for DS1 operation and approximately 10 Hz for CEPT operation. Optionally, a lower bandwidth of approximately 1.25 Hz can be selected in CEPT operation by setting JABW0 = 1 (register 12, bit 5) for systems desiring compliance with ETSI-TBR12/13 jitter attenuation requirements. When configured to meet ETSI-TBR12/13, the clock connected to the XCLK input must be ±20 ppm. For a given frequency, different jitter amplitudes will cause a slight variation in attenuation because of finite quantization effects. Jitter amplitudes of less than approximately 0.2 UI will have greater attenuation than the single-pole roll-off characteristic. The jitter transfer curve is independent of data patterns. Typical jitter transfer curves of the jitter attenuator are given in Figure 12 and Figure 14.

### Jitter Accommodation

The minimum jitter accommodation of the jitter attenuator occurs when the XCLK frequency and the input clock's long-term average frequency are at their extreme frequency tolerances. When the jitter attenuator is used in the LIU transmit path, the minimum accommodation is 28 UIp-p at the highest jitter frequency of 15 kHz. Typical receiver jitter accommodation curves including the jitter attenuator in the LIU receive path are given in Figure 11 and Figure 13.

When the jitter attenuator is placed in the data path, a difference between the XCLK/16 frequency and the incoming line rate for receive applications, or the TCLK rate for transmit applications, will result in degraded low-frequency jitter accommodation performance. The peak-to-peak jitter accommodation (JAp-p) for frequencies from above the corner frequency of the jitter attenuator (fc) to approximately 100 Hz is given by the following equation:

$$\text{JAp-p} = \left(64 - \frac{2(|\Delta f_{xclk} - \Delta f_{data}|)f_{data}}{2\pi f_c}\right)\text{UI}$$

where:

$f_{data}$ = 1.544 MHz for DS1 or 2.048 MHz for CEPT;
for JABW0 = 0, fc = 3.8 Hz for DS1 or 10 Hz for CEPT,
and for JABW0 = 1, fc = 1.25 Hz for CEPT;
$\Delta f_{xclk}$ = XCLK tolerance in ppm;
$\Delta f_{data}$ = data tolerance in ppm.

Note that for lower corner frequencies, the jitter accommodation is more sensitive to clock tolerance than for higher corner frequencies. When JABW0 = 1 and the jitter attenuator is used in the receive data path, the tolerance on XCLK should be tightened to ±20 ppm in order to meet the jitter accommodation requirements of TBR12/13 as given in G.823 for line data rates of ±50 ppm.

## Line Interface Units: Jitter Attenuator (continued)

### Jitter Attenuator Enable

The jitter attenuator is selected using the JAR and JAT bits (register 5, bits 1 and 2) of the microprocessor interface. These control bits are global and affect all four channels unless a given channel is in the powerdown mode (PWRDN = 1). Because there is only one attenuator function in the device, selection must be made between either the transmit or receive path. If both JAT and JAR are activated at the same time, the jitter attenuator will be disabled.

Note that the power consumption increases slightly on a per-channel basis when the jitter attenuator is active. If jitter attenuation is selected, a valid XCLK (pin 29) signal must be available.

#### Jitter Attenuator Receive Path Enable (JAR)

When the jitter attenuator receive bit is set (JAR = 1), the attenuator is enabled in the receive data path between the clock/data recovery and the decoder (see Figure 4 on page 22). Under this condition, the jitter characteristics of the jitter attenuator apply for the receiver. When JAR = 0, the clock/data recovery outputs bypass the disabled attenuator and directly enter the decoder function. The receive path will then exhibit the jitter characteristics shown in Figure 11 through Figure 14. If CDR = 0 (register 5, bit 0), the JAR bit is ignored because clock recovery will be disabled.

#### Jitter Attenuator Transmit Path Enable (JAT)

When the jitter attenuator transmit bit is set (JAT = 1), the attenuator is enabled in the transmit data path between the encoder and the pulse-width controller/pulse equalizer (see Figure 4 on page 22). Under this condition, the jitter characteristics of the jitter attenuator apply for the transmitter. When JAT = 0, the encoder outputs bypass the disabled attenuator and directly enter the pulse-width controller/pulse equalizer. The transmit path will then pass all jitter from TCLK to line interface outputs TTIP/TRING.

## Line Interface Units: Jitter Attenuator (continued)

### Jitter Attenuator Enable (continued)

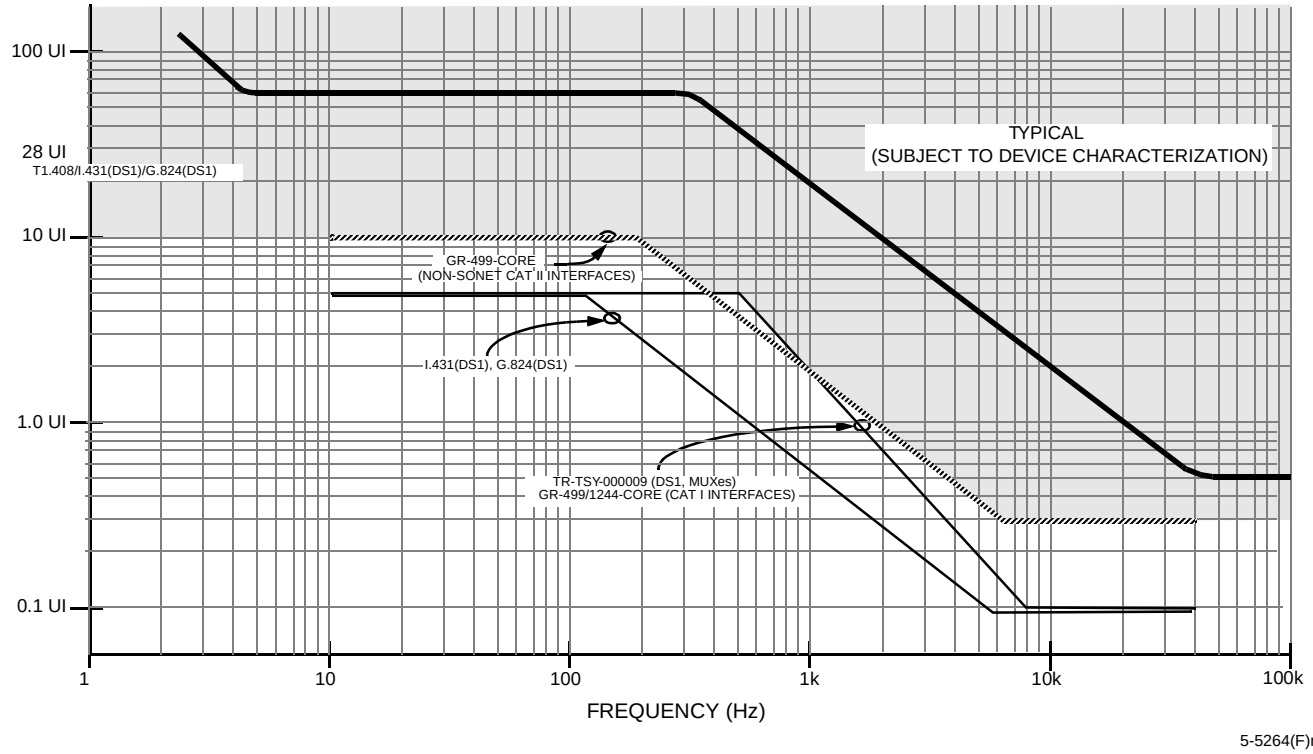



**Figure 11. DS1/T1 Receiver Jitter Accommodation with Jitter Attenuator**

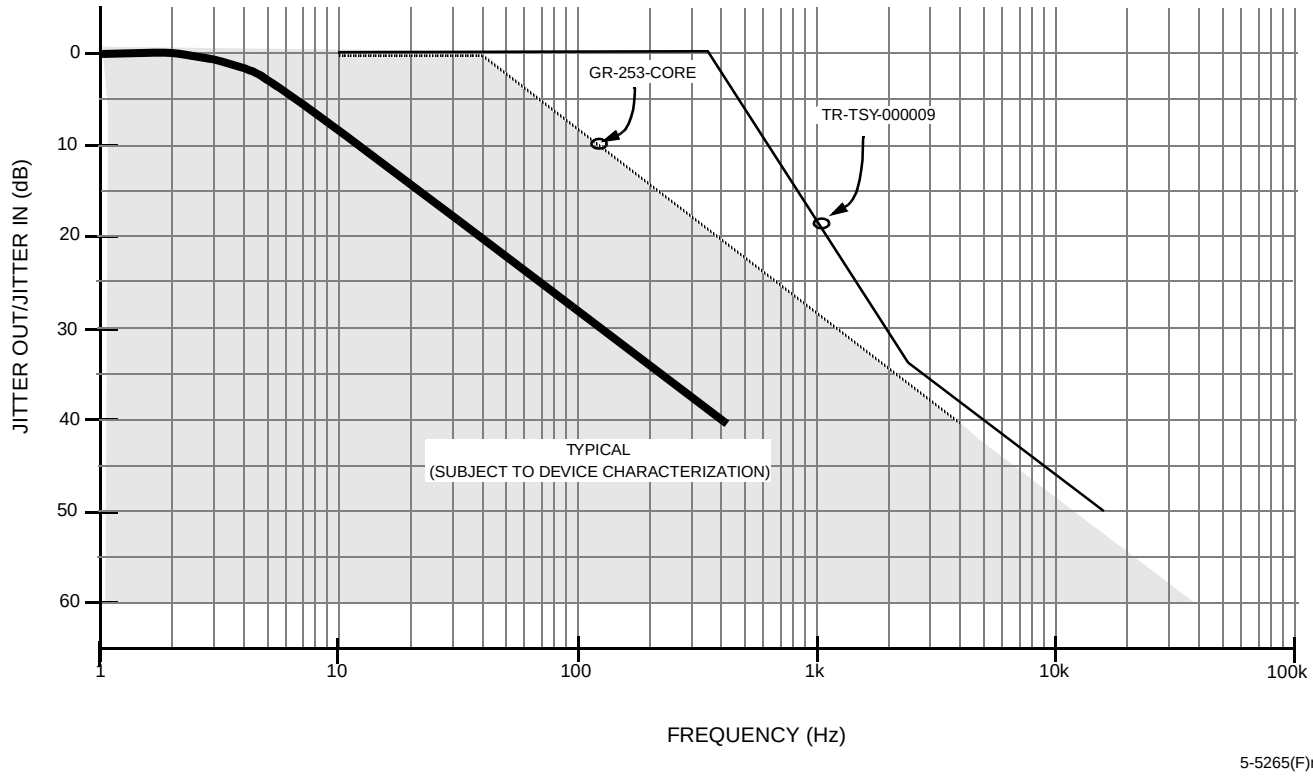



**Figure 12. DS1/T1 Jitter Transfer of the Jitter Attenuator**

## Line Interface Units: Jitter Attenuator (continued)

### Jitter Attenuator Enable (continued)

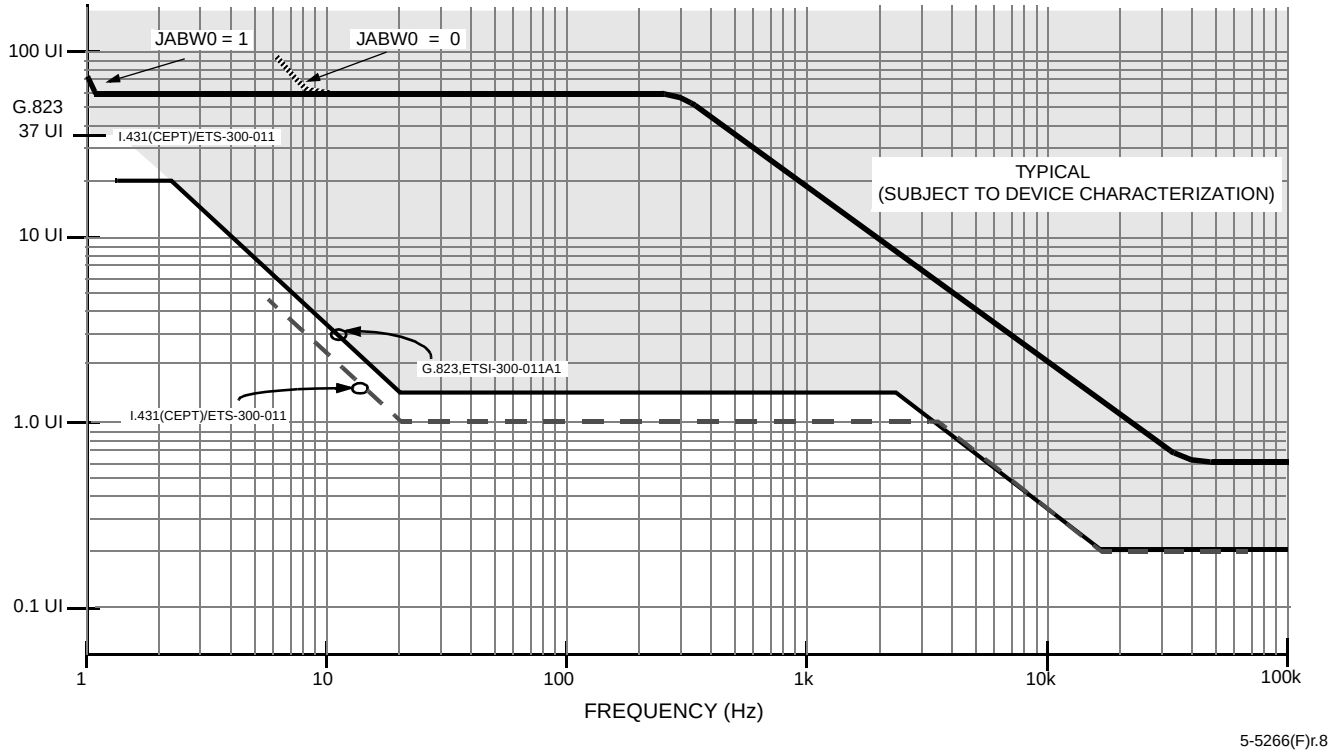



**Figure 13. CEPT/E1 Receiver Jitter Accommodation with Jitter Attenuator**

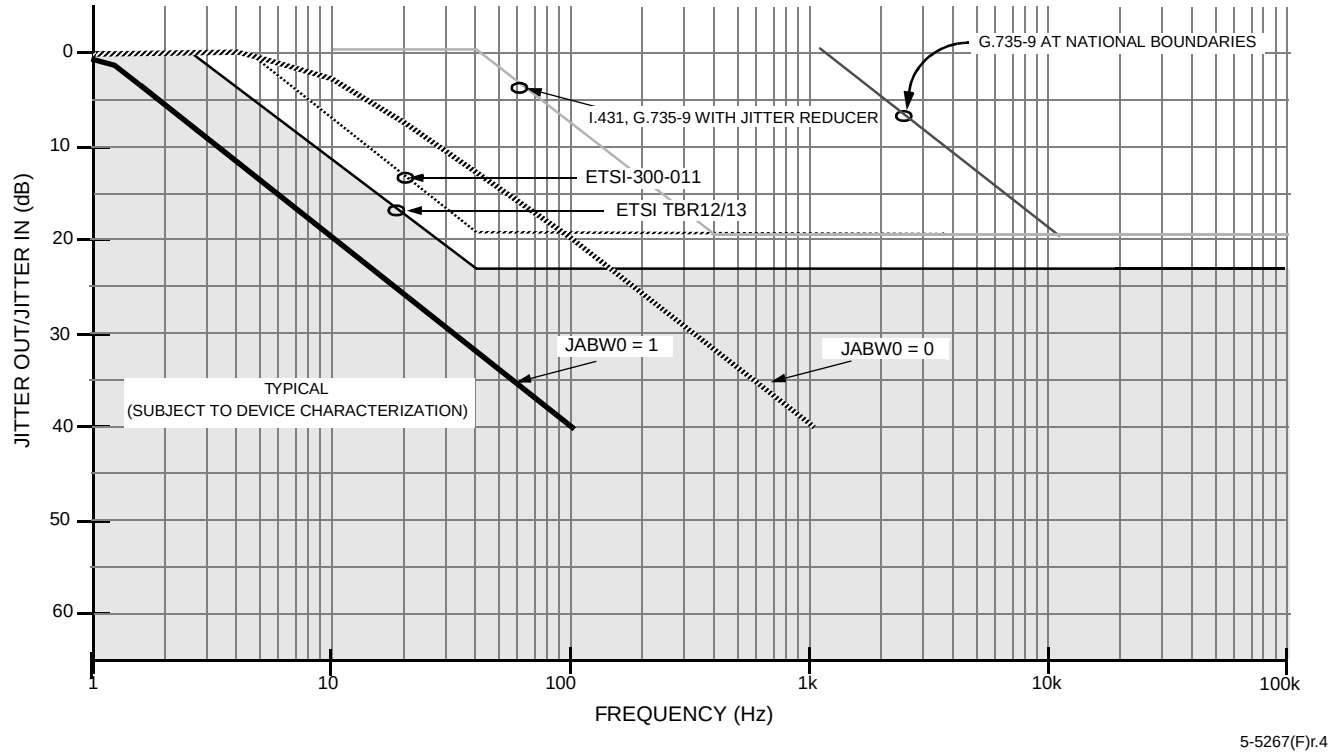



**Figure 14. CEPT/E1 Jitter Transfer of the Jitter Attenuator**

## Line Interface Units: Loopbacks

The device has three independent loopback paths that are activated using LOOPA and LOOPB (registers 6 to 9, bits 3 and 4) as shown in Table 17. The locations of these loopbacks are illustrated in Figure 1.

**Table 17. Loopback Control**

| Operation | Symbol | LOOPA | LOOPB |
|---|---|---|---|
| Normal | — | 0 | 0 |
| Full Local Loopback | FLLOOP* | 0 | 1 |
| Remote Loopback | RLOOP† | 1 | 0 |
| Digital Local Loopback | DLLOOP | 1 | 1 |

* During the transmit AIS condition, the looped data will be the transmitted data from the system and not the all-1s signal.
† Transmit AIS request is ignored.

### Full Local Loopback (FLLOOP)

A full local loopback (FLLOOP) connects the transmit line driver input to the receiver analog front-end circuitry. Valid transmit output data continues to be sent to the network. If the transmit AIS (all-1s signal) is sent to the network, the looped data is not affected. The ALOS alarm continues to monitor the receive line interface signal while DLOS monitors the looped data.

See Digital Loss of Signal (DLOS) Alarm section on page 24 regarding the behavior of the DLOS alarm upon activation of FLLOOP.

### Remote Loopback (RLOOP)

A remote loopback (RLOOP) connects the recovered clock and retimed data to the transmitter at the system interface and sends the data back to the line. The receiver front end, clock/data recovery, encoder/decoder (if enabled) jitter attenuator (if enabled), and transmit driver circuitry are all exercised during this loopback. The transmit clock, transmit data, and XAIS inputs are ignored. Valid receive output data continues to be sent to the system interface. This loopback mode is very useful for isolating failures between systems.

See Loss of Transmit Clock (LOTC) Alarm and Transmit Driver Monitor (TDM) Alarm on page 31 regarding the behavior of the LOTC and TDM alarms upon activation and deactivation of RLOOP.

### Digital Local Loopback (DLLOOP)

A digital local loopback (DLLOOP) connects the transmit clock and data through the encoder/decoder pair to the receive clock and data output pins at the system interface. This loopback is operational if the encoder/decoder pair is enabled or disabled. The AIS signal can be transmitted without any effect on the looped signal.

## Line Interface Units: Other Features

### Powerdown (PWRDN)

Each line interface channel has an independent powerdown mode controlled by PWRDN (registers 6 to 9, bit 0). This provides power savings for systems that use backup channels. If PWRDN = 1, the corresponding channel will be in a standby mode, consuming only a small amount of power. It is recommended that the alarm registers for the corresponding channel be masked with MASK = 1 (registers 6 to 9, bit 1) during powerdown mode. If a line interface channel in powerdown mode needs to be placed into service, the channel should be turned on (PWRDN = 0) approximately 5 ms before data is applied.

If a line interface channel will never be in service, the $V_{DDA}$ and $V_{DDD}$ pins can be connected to the ground plane, resulting in no power consumption.

### RESET ($\overline{\text{RESET}}$, SWRESET)

The device provides both a hardware reset ($\overline{\text{RESET}}$; pin 32) and a software reset (SWRESET; register 4, bit 1) that are functionally equivalent. When the device is in reset, all signal-path and alarm monitor states are initialized to a known starting configuration. The status registers and INT (pin 25) are also cleared. The writable microprocessor interface registers are not affected by reset, with the exception of bits in register 4 (see the Global Control Registers (0100, 0101) section). During a reset condition, data transmission will be interrupted.

The reset condition is initiated by setting $\overline{\text{RESET}}$ = 0 or SWRESET = 1 for a minimum of 10 µs. After leaving the reset condition (with $\overline{\text{RESET}}$ = 1 or SWRESET = 0), the bits in register 4 will be reset and may need to be restored.

### Loss of XCLK Reference Clock (LOXC)

The LOXC output (pin 31) is active when the XCLK reference clock (pin 29) is absent. The LOXC flag is asserted a maximum of 16 µs after XCLK disappears, and deasserts immediately after detecting the first clock edge of XCLK.

During the LOXC alarm condition, the clock recovery and jitter attenuator functions are automatically disabled. Therefore, if CDR = 1 and/or JAR = 1, the RCLK, RPD, RND, and DLOS outputs will be unknown. If CDR = 0, there will be no effect on the receiver. If the jitter attenuator is enabled in the transmit path (JAT = 1) during this alarm condition, then a Loss of Transmit Clock alarm, LOTC = 1, will also be indicated.

### In-Circuit Testing and Driver High-Impedance State ($\overline{\text{ICT}}$)

The function of the $\overline{\text{ICT}}$ input (pin 33) is determined by the ICTMODE bit (register 4, bit 3). If ICTMODE = 0 and $\overline{\text{ICT}}$ is activated ($\overline{\text{ICT}}$ = 0), then all output buffers (TTIP, TRING, RCLK, RPD, RND, LOXC, RDY_$\overline{\text{DTACK}}$, INT, AD[7:0]) are placed in a high-impedance state. For in-circuit testing, the $\overline{\text{RESET}}$ pin can be used to activate ICTMODE = 0 without having to write the bit. If ICTMODE = 1 and $\overline{\text{ICT}}$ = 0, then only the TTIP and TRING outputs of all channels will be placed in a high-impedance state. The TTIP and TRING outputs have a limiting high-impedance capability of approximately 8 kΩ.

### LIU Delay Values

The transmit coder has 5 UI delay whether it is in the path or not and whether it is B8ZS or HDB3. Its delay is only removed when in single-rail mode. The remainder of the transmit path has 4.6 UI delay. The receive decoder has 5 UI delay whether it is in the path or not and whether it is B8ZS or HDB3. Its delay is only removed when in single-rail mode or CDR = 0. The AFE (equalizer plus slicer) delay is nearly 0 UI delay. The jitter attenuator delay is nominally 33 UI but can be 2 UI—64 UI depending on the state. The DPLL used for timing recovery has 8 UI delay.

# Line Interface Units: Line Encoding/Decoding

## Alternate Mark Inversion (AMI)

The default line code used for T1 is alternate mark inversion (AMI). The coding scheme represents a 1 with a pulse or mark on the positive or negative rail and a 0 with no pulse on either rails. This scheme is shown in Table 18.

**Table 18. AMI Encoding**

| | | | | |
|---|---|---|---|---|
| Input Bit Stream | 1011 | 0000 | 0111 | 1010 |
| AMI Data | –0+– | 0000 | 0+–+ | –0+0 |

The T1 ones density rule requires that in every 24 bits of information to be transmitted, there must be at least three pulses, and no more than 15 zeros may be transmitted consecutively.

AT&T Technical Reference 62411 for digital transmissions requires that in every 8 bits of information, at least one pulse must be present.

The frame monitor indicates excessive zeros upon detecting any zero string length greater than 15 contiguous zeros (no pulses on either RPD or RND).

## T1-Binary 8 Zero Code Suppression

Clear channel transmission can be accomplished using Binary 8 Zero Code Suppression (B8ZS). Eight consecutive 0s are replaced with the B8ZS code. This code consists of two bipolar violations in bit positions 4 and 7 and valid bipolar marks in bit positions 5 and 8. The receiving end recognizes this code and replaces it with the original string of eight 0s. Table 19 shows the encoding of a string of 0s using B8ZS. B8ZS is recommended when ESF format is used.

**Table 19. DS1 B8ZS Encoding**

| **Bit Positions** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **—** | **—** | **—** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Before B8ZS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| After B8ZS | 0 | 0 | 0 | V | B | 0 | V | B | B | 0 | B | 0 | 0 | 0 | V | B | 0 | V | B |

The frame monitor indicates excessive zeros upon detecting any zero string length greater than 15 contiguous zeros (no pulses on either RPD or RND).

## Line Interface Units: Line Encoding/Decoding (continued)

### High-Density Bipolar of Order 3 (HDB3)

The line code used for CEPT is described in ITU Rec. G.703 Section 6.1 as high-density bipolar of order 3 (HDB3). HDB3 uses a substitution code that acts on strings of four 0s. The substitute HDB3 codes are 000V and B00V, where V represents a violation of the bipolar rule and B represents as inserted pulse conforming to the AMI rule defined in ITU Rec. G.701, item 9004. The choice of the B00V or 000V is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no direct current (dc) component is introduced. The substitute codes follow each other if the string of 0s continues. The choice of the first substitute code is arbitrary. A line code error is defined as a bipolar violation and consists of two pulses of the same polarity that is not defined as one of the two substitute codes. The frame monitor also indicates a bipolar violation upon detecting a block of four or more consecutive 0s. Both excessive zeros and coding violations are indicated as bipolar violations. An example is shown in Table 20.

**Table 20. ITU HDB3 Coding and DCPAT Binary Coding**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Input Bit Stream | 1011 | 0000 | 01 | 0000 | 0000 | 0000 | 0000 |
| HDB3-Coded Data | 1011 | 000V | 01 | 000V | B00V | B00V | B00V |
| HDB3-Coded Levels | –0+– | 000– | 0+ | 000+ | –00– | +00+ | –00– |

## Line Interface Units: Quad Line Interface Unit Registers

As shown in Table 6, the quad LIU registers consist of sixteen 8-bit registers (some of which are reserved). These registers can be accessed by writing 00 (hexadecimal) to register 13.

Registers 0 and 1 are the alarm registers used for storing the various device alarm status and are read only. All other registers are read/write. Registers 2 and 3 contain the individual mask bits for the alarms in registers 0 and 1. Registers 4 and 5 are designated as the global control registers used to set up the functions for all four channels. The channel configuration registers in registers 6 through 9 and register 12 are used to configure the individual channel functions and parameters. Registers 10 and 11 must be cleared by the user after a powerup for proper device operation; CODE3 and CODE4 may be set as desired. (See Table 26 on page 46.) Register 13 is the global index register. Registers 14 and 15 are reserved for proprietary functions and must not be addressed during operation. The following sections describe these registers in detail.

### Alarm Registers (0000, 0001)

The bits in the alarm registers represent the status of the transmitter and receiver alarms LOTC, TDM, DLOS, and ALOS for all four channels as shown in Table 21. The alarm indicators are active-high and automatically clear on a microprocessor read if the corresponding alarm condition no longer exists. Persistent alarm conditions will cause the bit to remain set. These are read-only registers.

**Table 21. Alarm Registers**

| Bits | Symbol* | Description |
|---|---|---|
| **Alarm Register (0)** | | |
| 4, 0 | ALOS[2:1] | Analog loss of signal alarm for channels 1 & 2. |
| 5, 1 | DLOS[2:1] | Digital loss of signal alarm for channels 1 & 2. |
| 6, 2 | TDM[2:1] | Transmit driver monitor alarm for channels 1 & 2. |
| 7, 3 | LOTC[2:1] | Loss of transmit clock alarm for channels 1 & 2. |
| **Alarm Register (1)** | | |
| 4, 0 | ALOS[4:3] | Analog loss of signal alarm for channels 3 & 4. |
| 5, 1 | DLOS[4:3] | Digital loss of signal alarm for channels 3 & 4. |
| 6, 2 | TDM[4:3] | Transmit driver monitor alarm for channels 3 & 4. |
| 7, 3 | LOTC[4:3] | Loss of transmit clock alarm for channels 3 & 4. |

*The numerical suffix identifies the channel number.

## Line Interface Units: Quad Line Interface Unit Registers (continued)

### Alarm Mask Registers (0010, 0011)

The bits in the alarm mask registers in Table 22 allow the microprocessor to selectively mask each channel alarm and prevent it from generating an interrupt. The mask bits correspond to the alarm status bits in the alarm registers and are active-high to disable the corresponding alarm from generating an interrupt. These registers are read/write registers.

**Table 22. Alarm Mask Registers**

| Bits | Symbol* | Description |
|---|---|---|
| **Alarm Mask Register (2)** | | |
| 4, 0 | MALOS[2:1] | Mask analog loss of signal alarm for channels 1 & 2. |
| 5, 1 | MDLOS[2:1] | Mask digital loss of signal alarm for channels 1 & 2. |
| 6, 2 | MTDM[2:1] | Mask transmit driver monitor alarm for channels 1 & 2. |
| 7, 3 | MLOTC[2:1] | Mask loss of transmit clock alarm for channels 1 & 2. |
| **Alarm Mask Register (3)** | | |
| 4, 0 | MALOS[4:3] | Mask analog loss of signal alarm for channels 3 & 4. |
| 5, 1 | MDLOS[4:3] | Mask digital loss of signal alarm for channels 3 & 4. |
| 6, 2 | MTDM[4:3] | Mask transmit driver monitor alarm for channels 3 & 4. |
| 7, 3 | MLOTC[4:3] | Mask loss of transmit clock alarm for channels 3 & 4. |

*The numerical suffix identifies the channel number.

### Global Control Registers (0100, 0101)

The bits in the global control registers in Table 23 and Table 24 allow the microprocessor to configure the various device functions over all the four channels. All the control bits (with the exception of LOSSTD and ICTMODE) are active-high. These are read/write registers.

**Table 23. Global Control Register (0100)**

| Bits | Symbol | Description |
|---|---|---|
| **Global Control Register (4)** | | |
| 0 | GMASK | The GMASK bit globally masks all the channel alarms when GMASK = 1, preventing all the receiver and transmitter alarms from generating an interrupt. GMASK = 1 after a device reset. |
| 1 | SWRESET | The SWRESET provides the same function as the hardware reset. It is used for device initialization through the microprocessor interface. |
| 2 | LOSSTD | The LOSSTD bit selects the conformance protocol for the DLOS receiver alarm function. |
| 3 | ICTMODE | The ICTMODE bit changes the function of the $\overline{\text{ICT}}$ pin. ICTMODE = 0 after a device reset. |
| 7—4 | HIGHZ[4:1] | A HIGHZ bit is available for each individual channel. When HIGHZ = 1, the TTIP and TRING transmit drivers for the specified channel are placed in a high-impedance state. HIGHZ[4:1] = 1 after a device reset. |

## Line Interface Units: Quad Line Interface Unit Registers (continued)

### Global Control Registers (0100, 0101) (continued)

**Table 24. Global Control Register (0101)**

| Bits | Symbol | Description |
|---|---|---|
| **Global Control Register (5)** | | |
| 0 | CDR | The CDR bit is used to enable and disable the clock/data recovery function. |
| 1 | JAR | The JAR is used to enable and disable the jitter attenuator function in the receive path. The JAR and JAT control bits are mutually exclusive; i.e., either JAR or the JAT control bit can be set, but not both. |
| 2 | JAT | The JAT is used to enable and disable the jitter attenuator function in the transmit path. The JAT and JAR control bits are mutually exclusive; i.e., either JAT or the JAR control bit should be set, but not both. |
| 3 | CODE | The CODE bit is used to enable the B8ZS/HDB3 zero substitution coding. It is used in conjunction with the DUAL bit and is valid only for single-rail operation. |
| 4 | DUAL | The DUAL bit is used to select single or dual-rail mode of operation. |
| 5 | ALM | The ALM bit selects the transmit and receive data polarity (i.e., active-low or active-high). The ALM and ACM bits are used together to determine the transmit and receive data retiming modes. |
| 6 | ACM | The ACM bit selects the positive or negative edge of the receive clock (RCLK[4:1]) for receive data retiming. The ACM and ALM bits are used together to determine the transmit and receive data retiming modes. |
| 7 | LOSSD | The LOSSD bit selects the shutdown function for the digital loss of signal alarm (DLOS). |

### Channel Configuration and Control Registers (0110—1001, 1011, 1100)

The control bits in the channel configuration registers in Table 25 are used to select equalization, loopbacks, AIS generation, channel alarm masking, and the channel powerdown mode for each channel (1—4). The PWRDN[1—4], MASK[1—4], and XAIS[1—4] bits are active-high. These are read/write registers.

Control bits for zero substitution coding for channels 1—4 are listed in Table 27 and Table 26.

**Table 25. Channel Configuration Registers (0110—1001)**

| Bits | Symbol* | Description† |
|---|---|---|
| **Channel Configuration Registers (6—9)** | | |
| 0 | PWRDN[4:1] | The PWRDN bit powers down a channel when not used. |
| 1 | MASK[4:1] | The MASK bit masks all interrupts for the channel. |
| 2 | XAIS[4:1] | The XAIS bit enables transmission of an all-1s signal to the line interface. |
| 3<br>4 | LOOPB[4:1]<br>LOOPA[4:1] | The LOOPB and LOOPA bits select the channel loopback modes. |
| 5<br>6<br>7 | EQC[4:1],<br>EQB[4:1],<br>EQA[4:1] | The EQC, EQB, and EQA bits select the type of service (DS1 or CEPT) and the associated transmitter cable equalization/termination impedances. |

* A numerical suffix identifies the channel number.
† Channel suffix not shown in the description.

## Line Interface Units: Quad Line Interface Unit Registers (continued)

### Channel Configuration and Control Registers (0110—1001, 1011, 1100) (continued)

**Table 26. Channel Configuration Register (1011)**

| Bits | Symbol* | Description |
|---|---|---|
| **Channel Configuration Register (11)** | | |
| 0—3 | — | Reserved. Write to 0. |
| 4 | CODE4 | The CODE4 bit selects B8ZS/HDB3 encoding (transmit) and decoding (receive) in channel 4. |
| 5 | — | Reserved. Write to 0. |
| 6 | CODE3 | The CODE3 bit selects B8ZS/HDB3 encoding (transmit) and decoding (receive) in channel 3. |
| 7 | — | Reserved. Write to 0. |

* A numerical suffix identifies the channel number.

**Table 27. Control Register (1100)**

| Bit | Symbol* | Description |
|---|---|---|
| **Control Register (12)** | | |
| 0 | ALTIMER | The ALTIMER bit is used to select the time required to declare ALOS. ALTIMER = 0 selects 1 ms—2.6 ms. ALTIMER = 1 selects 10 bit—255 bit periods. |
| 1 | RCVAIS | The RCVAIS bit selects the shutdown function for the receiver during analog loss of signal alarm (ALOS). RCVAIS operates in conjunction with the LOSSD bit. |
| 2 | PFLALM | The PFLALM prevents the DLOS alarm from occurring during FLLOOP activation. |
| 3 | PRLALM | The PRLALM prevents the LOTC alarm from occurring during RLOOP activation/ deactivation. |
| 4 | PHIZALM | The PHIZALM prevents the TDM alarm from occurring when the driver is in a high-impedance state. |
| 5 | JABW0 | The JABW0 bit selects the lower bandwidth jitter attenuator option in CEPT mode. |
| 6 | CODE2 | The CODE2 bit selects B8ZS/HDB3 encoding (transmit) and decoding (receive) in channel 2. |
| 7 | CODE1 | The CODE1 bit selects B8ZS/HDB3 encoding (transmit) and decoding (receive) in channel 1. |

* A numerical suffix identifies the channel number.

## Line Interface Units: Quad Line Interface Unit Registers (continued)

### Global Index Register (1101)

Bits RI[4:0] are decoded to index into the primary register bank for the LIU or the secondary register banks for the eight receive frame monitors and eight FDL blocks. Bit 7 identifies the device version.

**Table 28. Global Index Register**

| Bits | Symbol | Description | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Global Index Register (13)** | | | | | | | | |
| 4—0 | RI[4:0] | **RI4** | **RI3** | **RI2** | **RI1** | **RI0** | **Block Name** | **Channel Monitored** |
| | | 0 | 0 | 0 | 0 | 1 | Frame Monitor 1 | Channel 1 transmit side |
| | | 1 | 0 | 0 | 0 | 1 | FDL1 | |
| | | 0 | 0 | 0 | 1 | 0 | Frame Monitor 2 | Channel 1 receive side |
| | | 1 | 0 | 0 | 1 | 0 | FDL2 | |
| | | 0 | 0 | 0 | 1 | 1 | Frame Monitor 3 | Channel 2 transmit side |
| | | 1 | 0 | 0 | 1 | 1 | FDL3 | |
| | | 0 | 0 | 1 | 0 | 0 | Frame Monitor 4 | Channel 2 receive side |
| | | 1 | 0 | 1 | 0 | 0 | FDL4 | |
| | | 0 | 0 | 1 | 0 | 1 | Frame Monitor 5 | Channel 3 transmit side |
| | | 1 | 0 | 1 | 0 | 1 | FDL5 | |
| | | 0 | 0 | 1 | 1 | 0 | Frame Monitor 6 | Channel 3 receive side |
| | | 1 | 0 | 1 | 1 | 0 | FDL6 | |
| | | 0 | 0 | 1 | 1 | 1 | Frame Monitor 7 | Channel 4 transmit side |
| | | 1 | 0 | 1 | 1 | 1 | FDL7 | |
| | | 0 | 1 | 0 | 0 | 0 | Frame Monitor 8 | Channel 4 receive side |
| | | 1 | 1 | 0 | 0 | 0 | FDL8 | |
| 6—5 | — | Reserved. Must be set to 0. | | | | | | |
| 7 | VERSION | Device version determines reset condition.<br>0 = versions 1 and 2<br>1 = version 3 | | | | | | |

## Frame Monitors

The frame monitor section for the T7698 is illustrated in Figure 15. The frame monitor interface consists of two groups of signals. The first group goes to the quad line transmitter and consists of clocks TCLK1—TCLK4, positive data TPD1—TPD4, and negative data TND1—TND4; the second group comes from the quad line receiver and consists of clocks RCLK1—RCLK4, positive data RPD1—RPD4, and negative data RND1—RND4.

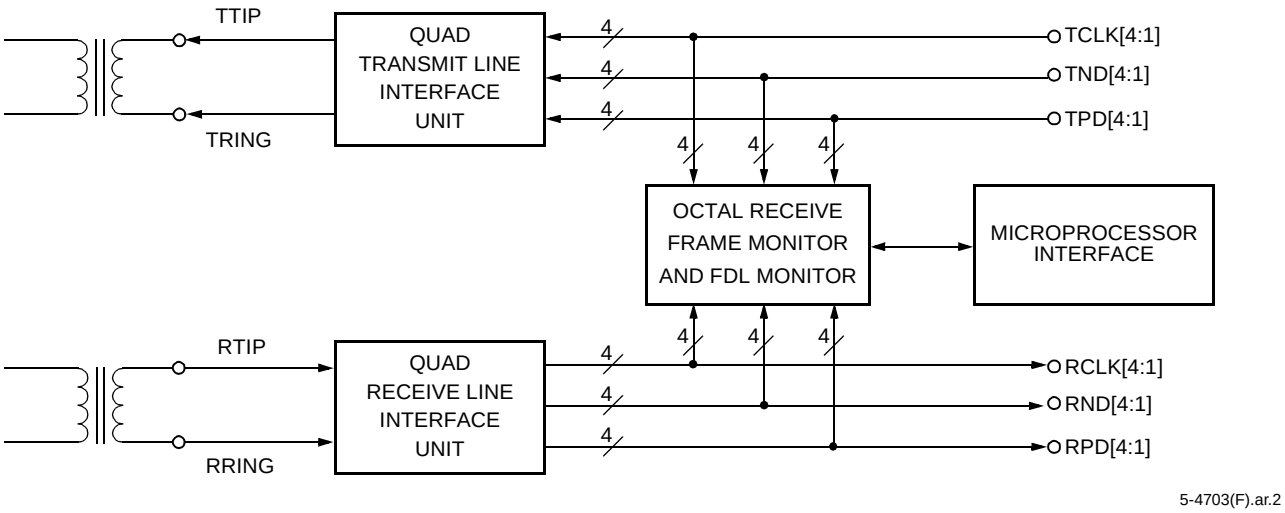



**Figure 15. Block Diagram of the Receive Frame Monitor Section**

## Frame Monitors (continued)

The octal frame monitor diagram is shown in Figure 16, with the details of a frame monitor shown in Figure 17.

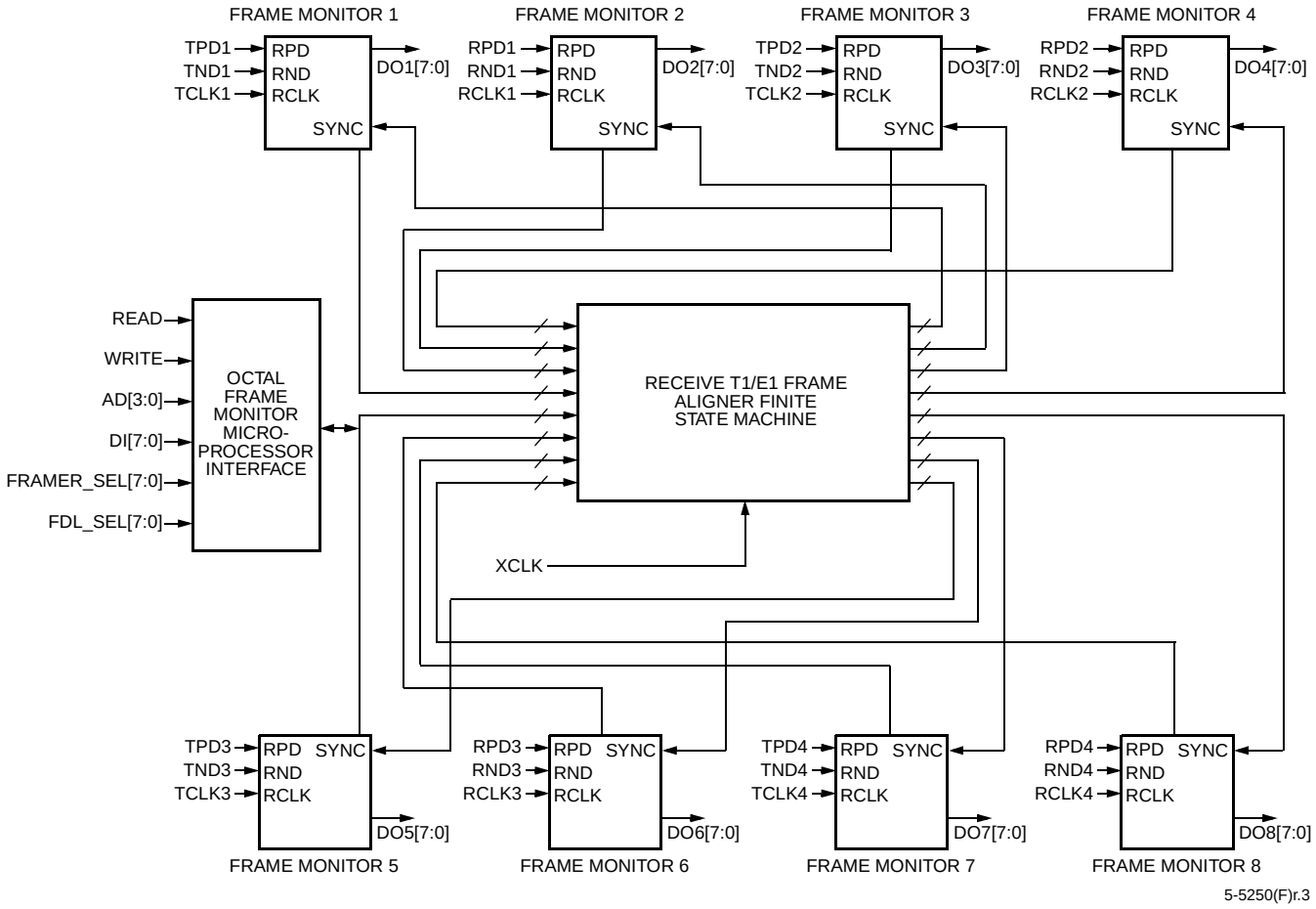



**Figure 16. Block Diagram of the Octal Receive Frame Monitor**

## Frame Monitors (continued)

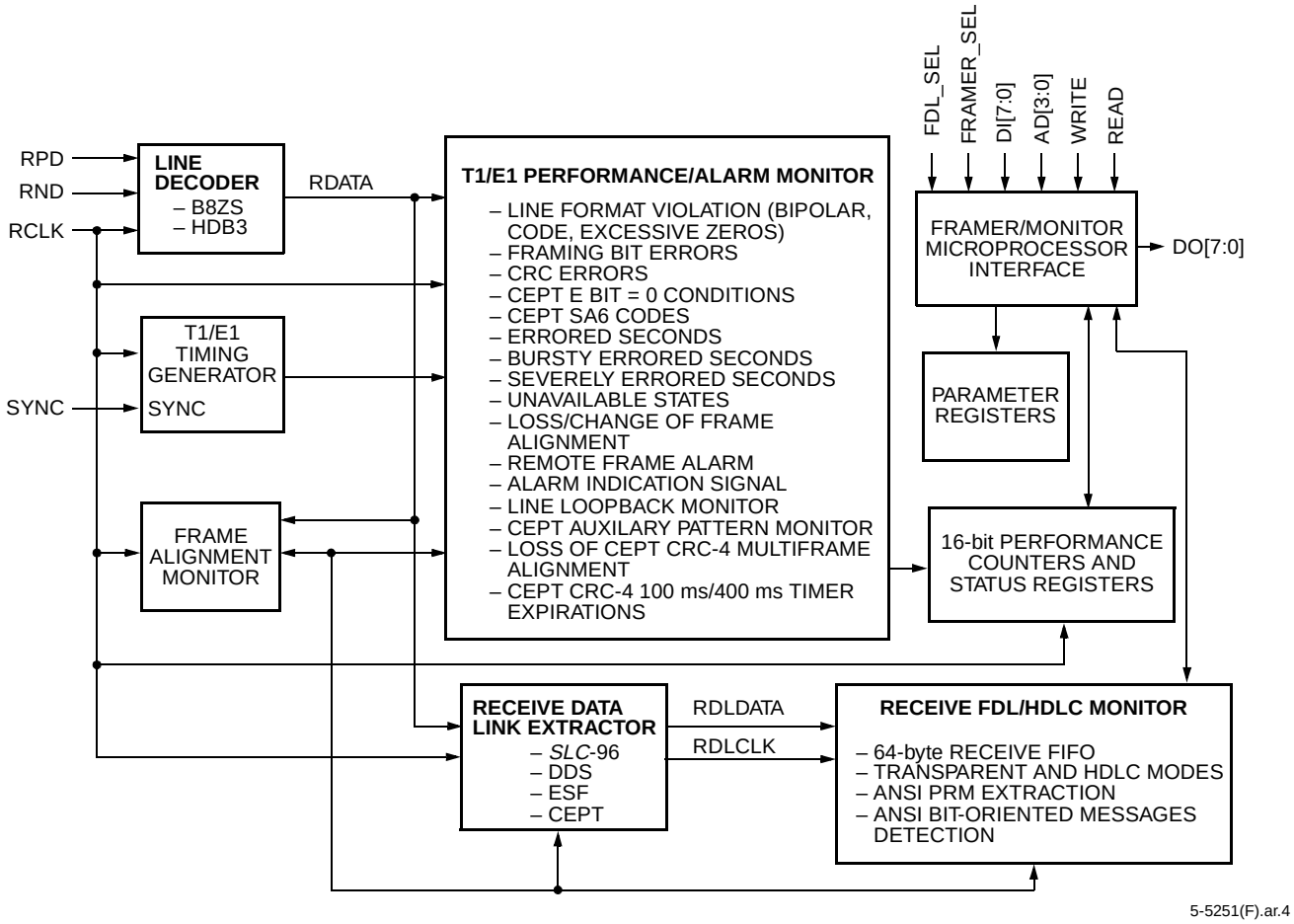



**Figure 17. Block Diagram of the Frame Monitor**

## Frame Monitors (continued)

### Frame Formats

The T7698 supports the North American T1 framing format of superframe (D4, *SLC*-96, DDS), extended superframe (ESF), and the ITU CEPT/E1 basic format with and without CRC-4 multiframe formatting. This section describes the framing formats.

#### T1 Framing Structures

T1 is a digital transmission line which multiplexes twenty-four 64 kbits/s time slots (DS0) onto a serial link. The T1 system is the lowest level of hierarchy on the North American T-carrier system, as shown in Table 29.

**Table 29. T-Carrier Hierarchy**

| T Carrier | DS0 Channels | Bit Rate (Mbits/s) | Signal Hierarchy |
|---|---|---|---|
| T1 | 24 | 1.544 | DS1 |
| T1-C | 48 | 3.152 | DS1C |
| T2 | 96 | 6.312 | DS2 |
| T3 | 672 | 44.736 | DS3 |
| T4 | 4032 | 274.176 | DS4 |

**Frame, Superframe, and Extended Superframe Definitions.** Each time slot (DS0) is comprised of 8 bits sampled every 125 µs (8 kHz). Multiplexing 24 of these 8-bit samples together produces a 192-bit (24 DS0s) frame. A framing bit is added to the beginning of each frame to allow for detection of frame boundaries and the transport of additional maintenance information. This 193-bit frame, also referred to as a DS1 frame, is repeated every 125 µs to yield the 1.544 Mbits/s T1 data rate. Twelve DS1 frames are bundled together to form a superframe and 24 DS1 frames are bundled together to form an extended superframe.

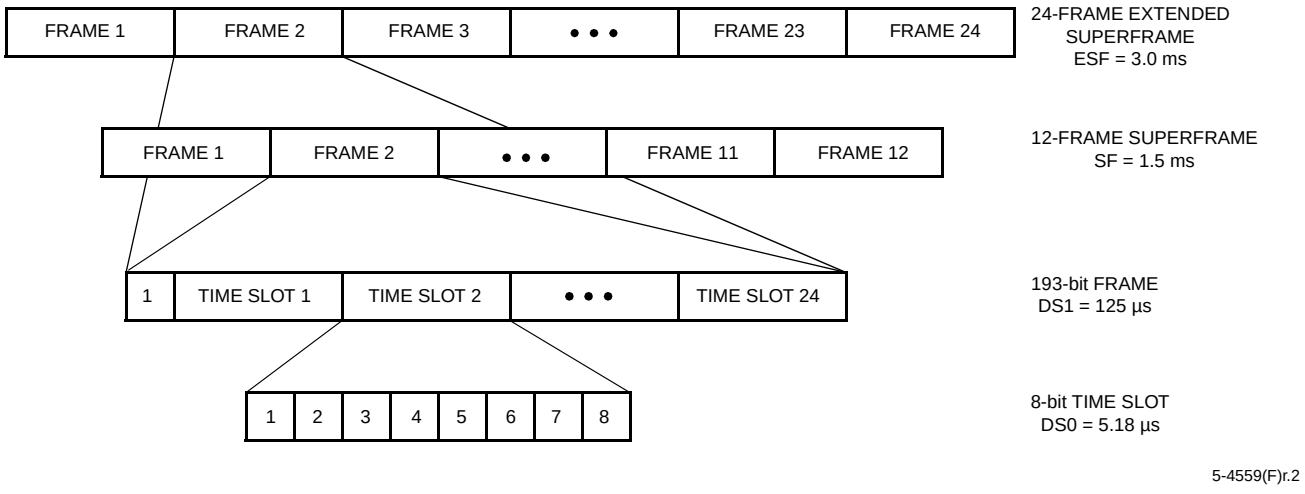



**Figure 18. T1 Frame Structure**

## Frame Monitors (continued)

### Frame Formats (continued)

**D4 Superframe Format.** D4 superframe format consists of 12 DS1 frames. Table 30 shows the framing bit structure of the D4 superframe.

**Table 30. D4 Superframe Format**

| Framing Bits | | | |
|---|---|---|---|
| **Frame Number** | **Bit Number** | **Terminal Frame $F_T$** | **Signal Frame $F_S$** |
| 1 | 0 | 1 | — |
| 2 | 193 | — | 0 |
| 3 | 386 | 0 | — |
| 4 | 579 | — | 0 |
| 5 | 772 | 1 | — |
| 6 | 965 | — | 1 |
| 7 | 1158 | 0 | — |
| 8 | 1351 | — | 1 |
| 9 | 1544 | 1 | — |
| 10 | 1737 | — | 1 |
| 11 | 1930 | 0 | — |
| 12 | 2123 | — | 0 |

Notes:
Frame 1 is transmitted first.

The remote alarm condition forces bit 2 of each time slot to a 0 state when enabled.

The remote alarm-Japanese condition forces framing bit 12 (bit number 2123) to a 1 state when enabled.

The T7698 frame monitor section uses both the $F_T$ and $F_S$ framing bits (excluding the twelfth $F_S$ bit) during its frame alignment procedure.

**Digital Data Service (DDS) Frame Format.** The superframe format for DDS is the same as that given for D4. DDS uses channel 24 to transmit the remote frame alarm and data link bits. The format for channel 24 is shown in Table 31.

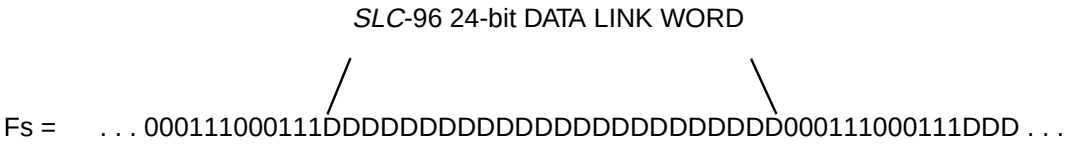
**Table 31. DDS Channel 24 Format**

| | |
|---|---|
| Channel 24 = | 10111YD0 |
| | Y = remote frame alarm: 1 = no alarm state; 0 = alarm state |
| | D = data link bits (8 kbits/s) |

## Frame Monitors (continued)

### Frame Formats (continued)

***SLC*-96 Frame Format.** *SLC*-96 superframe format consists of 12 DS1 frames similar to D4. The FT pattern is exactly the same as D4. The FS uses that same structure as D4 but incorporates a data link 24-bit word every 12 FS bits:



## Frame Monitors (continued)

### Frame Formats (continued)

**Extended Superframe.** The extended superframe format consists of 24 DS1 frames. The frame bits are used for frame and superframe alignment (FE), error checking (CRC-6), and facility data link transport (DL). Table 32 shows the ESF framing bit format.

**Table 32. Extended Superframe (ESF) Structure**

| Frame Bit | | | | |
|---|---|---|---|---|
| **Frame Number** | **Bit Number** | **FE** | **DL** | **CRC-6** |
| 1 | 0 | — | D | — |
| 2 | 193 | — | — | $C_1$ |
| 3 | 386 | — | D | — |
| 4 | 579 | 0 | — | — |
| 5 | 772 | — | D | — |
| 6 | 965 | — | — | $C_2$ |
| 7 | 1158 | — | D | — |
| 8 | 1351 | 0 | — | — |
| 9 | 1544 | — | D | — |
| 10 | 1737 | — | — | $C_3$ |
| 11 | 1930 | — | D | — |
| 12 | 2123 | 1 | — | — |
| 13 | 2316 | — | D | — |
| 14 | 2509 | — | — | $C_4$ |
| 15 | 2702 | — | D | — |
| 16 | 2895 | 0 | — | — |
| 17 | 3088 | — | D | — |
| 18 | 3281 | — | — | $C_5$ |
| 19 | 3474 | — | D | — |
| 20 | 3667 | 1 | — | — |
| 21 | 3860 | — | D | — |
| 22 | 4053 | — | — | $C_6$ |
| 23 | 4246 | — | D | — |
| 24 | 4439 | 1 | — | — |

Notes:
Frame 1 is transmitted first.

The $C_1$ to $C_6$ bits are the cyclic redundancy checksum (CRC-6) bits calculated over the previous extended superframe.

The remote alarm is a repeated 1111111100000000 pattern in the DL when enabled.

The ESF format allows for nondisruptive error detection, monitoring, and diagnostics on T1 circuits. ESF format consist of 24 framing bits: 6 FE bits for framing synchronization (2 kbits/s); 6 CRC-6 bits for error detection (2 kbits/s); and 12 DL bits for in-service monitoring and diagnostics (4 kbits/s). Cyclic redundancy checking is performed over the entire 4632-bit ESF frame (all 24 framing bits are set to 1 during calculations).

## Frame Monitors (continued)

### Frame Formats (continued)

#### T1 Loss of Frame Alignment (LFA)

Loss of frame alignment condition is caused by the inability of the frame monitor to maintain the proper sequence of frame bits. The number of errored framing bits required to detect a loss of frame alignment for the T1 framing formats is given is Table 33. In the case of ESF, excessive CRC-6 errors can also result in LFA by optionally setting register Framer_PR14, bit 0 = 0 (default mode).

**Table 33. T1 Loss of Frame Alignment Criteria**

| Format | Loss of Frame Alignment Condition |
|---|---|
| D4 | 2 errored frame bits ($F_T$) out of 4 consecutive frame bits force loss of frame and superframe alignment. |
| *SLC*-96 | 2 errored frame bits ($F_T$) out of 4 consecutive frame bits force loss of frame and superframe alignment. |
| DDS | 3 errored frame bits ($F_T$ or $F_S$ or channel 24 FAS pattern) out of 12 consecutive frame bits force loss of frame alignment. |
| ESF | Due to framing errors: 2 errored FE bits out of 4 consecutive FE bits.<br>Due to CRC-6 errors (if enabled by setting register Framer_PR14, bit 0 = 0 (default mode)):<br>Option a: Setting Framer_PR14, bit 1 = 0, forces LFA if 32 CRC-6 errors out of 33 CRC-6 checks are detected.<br>Option b: Setting Framer_PR14, bit 1 = 1, forces LFA if more than 320 CRC-6 errors in one second are detected. |

The T7698 indicates the loss of frame and superframe conditions by setting the loss of frame alignment (LFA) and loss of superframe alignment (LSFA) bits, respectively, in the status register Framer_SR1. LFA state can be forced on demand by setting the register Framer_PR2, bit 5 = 1.

## Frame Monitors (continued)

### Frame Formats (continued)

#### T1 Frame Recovery Alignment Algorithms

When in a loss of frame alignment state, the frame monitor searches for a new frame alignment and forces its internal circuitry to this new alignment. The T7698's synchronization circuit inhibits realignment in T1 framing formats when repetitive data patterns emulate the T1 frame alignment patterns. The loss of frame alignment will always force a loss of superframe alignment. T1 frame synchronization will not occur until all frame sequence emulating patterns disappear and only one valid pattern exists. Superframe alignment is established only after frame alignment has been determined in the *SLC*-96 frame format. Table 34 gives the requirements for establishing T1 frame and superframe alignment.

**Table 34. T1 Frame Alignment Procedures**

| Frame Format | Alignment Procedure |
|---|---|
| D4 | Using the $F_T$ frame position as the starting point, frame alignment is established when 24 consecutive $F_T$ and $F_S$ frame bits, excluding the twelfth $F_S$ bit (48 total frames) are received error-free. |
| *SLC*-96 | Using the $F_T$ frame position as the starting point, frame alignment is established when 24 consecutive $F_T$ frame bits (48 total frames) are received error-free. Superframe alignment is achieved on the first valid superframe ($F_S$) bit sequence (000111000111). |
| DDS | Using the $F_T$ frame position as the starting point, frame alignment is established when five consecutive $F_T$/$F_S$ frame bits and the DDS FAS in time slot 24 is received error-free. In the DDS format, there is no search for a superframe structure. |
| ESF | Frame and superframe alignment is established simultaneously using the $F_E$ framing bit. Alignment is established when 24 consecutive $F_E$ bits are received error-free. |

## Frame Monitors (continued)

### Frame Formats (continued)

#### CEPT 2.048 Mbits/s Basic Frame Structure

As defined in ITU Rec. G.704, the CEPT 2.048 Mbits/s frame, CRC-4 multiframe, and channel associated signaling multiframe structures are illustrated in Figure 19.

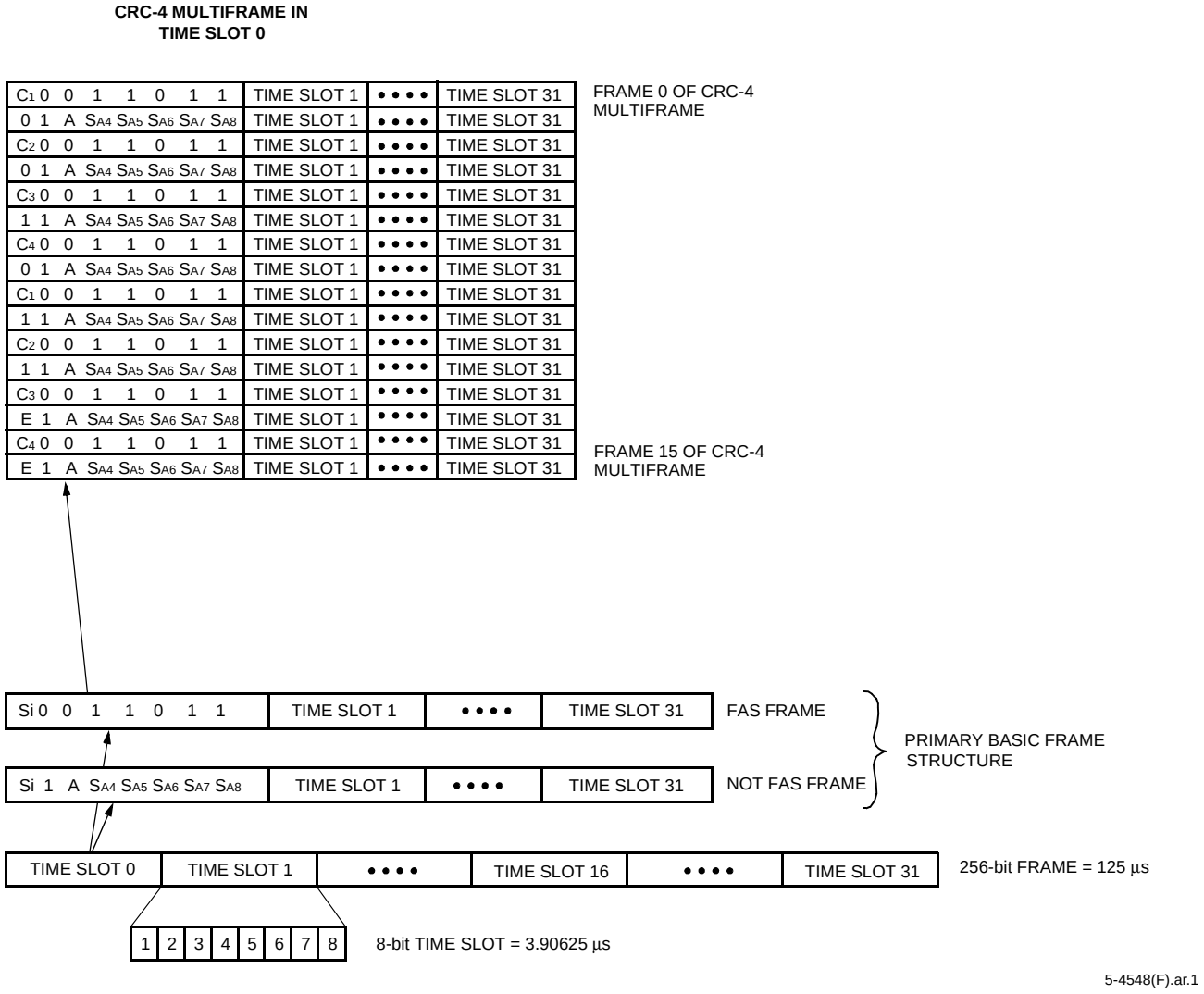



**Figure 19. ITU 2.048 Mbits/s Basic Frame and CRC-4 Multiframe Structures**

## Frame Monitors (continued)

### Frame Formats (continued)

According to the ITU Rec. G.704 Section 2.3.1, the frame length is defined to be 256 bits, numbered 1 to 256. The frame repetition rate is 8 kHz. The allocation of bits numbered 1 to 8 of the frame is shown in Table 35.

**Table 35. Allocation of Bits 1 to 8 of the FAS Frame and the NOT FAS Frame**

| Basic Frames | Bit 1 (MSB) | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 (LSB) |
|---|---|---|---|---|---|---|---|---|
| Frame Alignment Signal (FAS) | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Not Frame Alignment Signal | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

The function of each bit in Table 35 is described below:

1. The Si bits are reserved for international use. A specific use for these bits is described in the CRC-4 Multiframe section. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border.
2. Bit 2 of the frames not containing the FAS (i.e., the NOT FAS frames) is fixed to 1 to prevent emulations of the frame alignment signal.
3. Bit 3 of the NOT FAS is the remote alarm indication (A bit). In undisturbed operation, this bit is set to 0; in alarm condition, set to 1.
4. Bits 4—8 of the NOT FAS may be recommended by ITU for use in specific point-to-point applications. Bit Sa4 may be used as a message-based data link for operations, maintenance, and performance monitoring.
5. MSB = most significant bit and is received first.
6. LSB = least significant bit and is received last.

## Frame Monitors (continued)

### Frame Formats (continued)

#### CEPT Loss of Basic Frame Alignment (LFA)

Frame alignment is assumed to be lost when:

1. As described in ITU Rec. G.706, Section 4.1.1, three (3) consecutive incorrect frame alignment signals have been received.
2. Bit 2 in time slot 0 in NOT FAS frames has been received with an error on three consecutive occasions.
3. Optionally, as described in ITU Rec. G.706, Section 4.3.2, by exceeding a count of 914 errored CRC-4 blocks out of 1000, with the understanding that a count of ≥915 errored CRC blocks indicates false frame alignment.
4. On demand via the control registers (by setting register Framer_PR2, bit 5 = 1).

In the LFA state:

1. No additional FAS or NOT FAS errors are processed.
2. The received remote frame alarm (received A bit) detection is deactivated.
3. All NOT FAS bit (Si bit, A bit and Sa4 to Sa8 bits) processing is halted.
4. Receive Sa6 code monitoring and counting is halted.
5. If CRC-4 is enabled, loss of CRC-4 multiframe alignment is forced.
6. If CRC-4 is enabled, the monitoring and processing of CRC-4 checksum errors is halted.
7. If CRC-4 is enabled, all monitoring and processing of received E-bit information is halted.

#### CEPT Loss of Frame Alignment Recovery Algorithm

The frame monitor begins the search for basic frame alignment one bit position beyond the position where the LFA state was detected. As defined in ITU Rec. G.706, Section 4.1.2, frame alignment will be assumed to have been recovered when the following sequence is detected:

1. For the first time, the presence of the correct frame alignment signal in frame n.
2. The absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a 1 in frame n + 1.
3. For the second time, the presence of the correct frame alignment in the next frame, n + 2.

Failure to meet 2 or 3 above will initiate a new basic frame search in frame n + 2.

## Frame Monitors (continued)

### Frame Formats (continued)

#### CEPT Time Slot 0 CRC-4 Multiframe Structure

The CRC-4 multiframe is in bit 1 of the frame. As described in ITU Rec. G.704 Section 2.3.3.1, where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 of each frame may be used for a cyclic redundancy check-4 (CRC-4) procedure as detailed below. The allocation of bits 1—8 of the frame is shown in Table 36 for the complete CRC-4 multiframe.

**Table 36. ITU CRC-4 Multiframe Structure of the T7698**

| | Submultiframe (SMF) | Frame Number | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| Multiframe | I | 0 | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 1 | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 2 | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 3 | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 4 | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 5 | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 6 | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 7 | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | II | 8 | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 9 | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 10 | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 11 | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 12 | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 13 | E | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| | | 14 | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| | | 15 | E | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

Notes:
C1 to C4 = cyclic redundancy check-4 (CRC-4) bits.
E = CRC-4 error indication bits.
Sa4 to Sa8 = spare bits.
A = remote frame alarm (RFA) bit (active-high); referred to as the A bit.

The CRC-4 multiframe consists of 16 frames numbered 0 to 15 and is divided into two eight-frame submultiframes (SMF), designated SMF-I and SMF-II that signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the CRC-4 block size (2048 bits). In those frames containing the frame alignment signal (FAS), bit 1 contains the CRC-4 bits. There are four CRC-4 bits, designated C1, C2, C3, and C4 in each SMF. In those frames not containing the frame alignment signal (NOT FAS), bit 1 contains the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E). The multiframe alignment signal is defined in ITU Rec. G.704 Section 2.3.3.4, as 001011. The received E bits will always be taken into account, by the receive E-bit processor*, even when the SMF that contains them is found to be errored. In the case where there exists equipment that does not use the E bits, the state of the E bits should be set to a binary 1 state.

The CRC-4 word, located in submultiframe N, is the remainder after multiplication by $x^4$ and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of the submultiframe N – 1.

* The receive E-bit processor will halt the monitoring of the received E bit during the loss of CRC-4 multiframe alignment.

## Frame Monitors (continued)

### Frame Formats (continued)

Representing the contents of the submultiframe check block as a polynomial, the first bit in the block, i.e., frame 0, bit 1 or frame 8, bit 1, is taken as being the most significant bit and the least significant bit in the check block is frame 7 or frame 15, bit 256. Similarly, $C_1$ is defined to be the most significant bit of the remainder and $C_4$, the least significant bit of the remainder. The encoding procedure, as described in ITU Rec. G.704, Section 2.3.3.5.2, follows:

1. The CRC-4 bits in the SMF are replaced by binary 0s.
2. The SMF is then acted upon by the multiplication/division process referred to above.
3. The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

The decoding procedure, as described in ITU Rec. G.704, Section 2.3.3.5.3, follows:

1. A received SMF is acted upon by the multiplication/division process referred to above, after having its CRC-4 bits extracted and replaced by 0s.
2. The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.
3. If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error-free.

## Frame Monitors (continued)

### Frame Formats (continued)

#### CEPT Loss of CRC-4 Multiframe Alignment (LMFA)

Loss of basic frame alignment forces the receive frame monitor into a loss of CRC-4 multiframe alignment state. This state is reported by way of the status registers, and once basic frame alignment is achieved, a new search for CRC-4 multiframe alignment is initiated. During a loss of CRC-4 multiframe alignment state:

1. The CRC-4 error counter is halted.
2. The CRC-4 error monitoring circuit for errored seconds, bursty errored seconds, and severely errored seconds is halted.
3. The received E bit = 0 counter is halted.
4. The received E bit = 0 monitoring circuit for errored seconds, bursty errored seconds, and severely errored seconds at the remote end interface is halted.
5. All receive Sa6 code monitoring and counting functions are halted.
6. Optionally, if LMFA monitoring in the performance counters is enabled (by setting bit 1 high in registers Framer_PR4—Framer_PR7), then these counts are incremented once per second for the duration of the LMFA state.

#### CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms

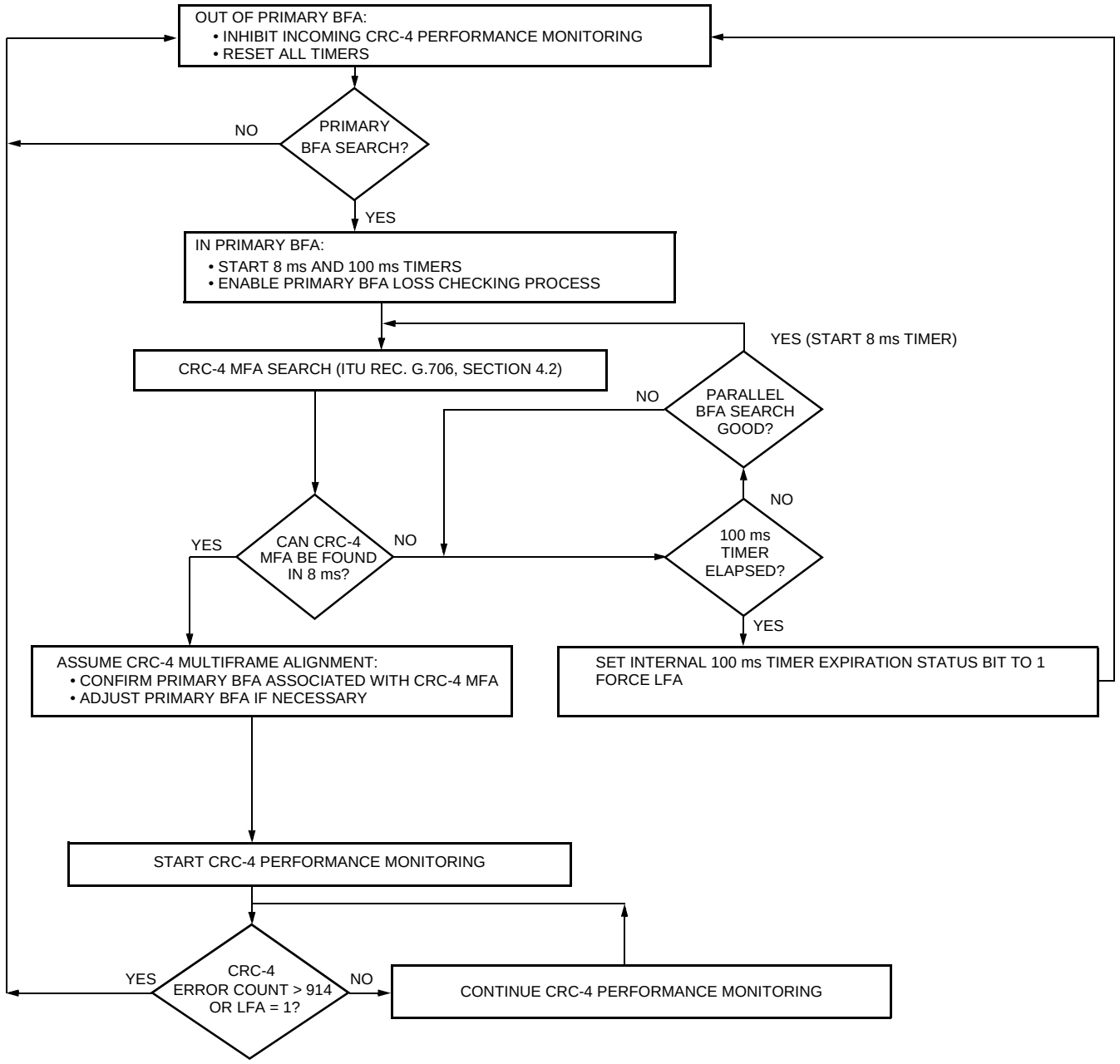
Several optional algorithms exist in the receive frame monitor.

**CRC-4 Multiframe Alignment Algorithm with 8 ms Timer.** The default algorithm is as described in ITU Rec. G.706, Section 4.2. The recommendation states that if a condition of assumed frame alignment has been achieved, CRC-4 multiframe alignment is deemed to have occurred if at least two valid CRC-4 multiframe alignment signals can be located within 8 ms, the time separating two CRC-4 multiframe signals being 2 ms or a multiple of 2 ms. The search for the CRC-4 multiframe alignment signal is made only in bit 1 of NOT FAS frames. If multiframe alignment cannot be achieved within 8 ms, it is assumed that frame alignment is due to a spurious frame alignment signal and a new parallel search for basic frame alignment is initiated. The new search for the basic frame alignment is started at the point just after the location of the assumed spurious frame alignment signal. During this parallel search for basic frame alignment, there is no indication to the system of a loss of frame alignment (LFA) state. The receive frame monitor will continuously search for CRC-4 multiframe alignment if no other CRC-4 multiframe algorithm is used.

**CRC-4 Multiframe Alignment Algorithm with 100 ms Timer.** This CRC-4 multiframe reframe mode starts a 100 ms timer upon detection of basic frame alignment. This is a parallel timer to the 8 ms timer. If CRC-4 multiframe alignment cannot be achieved within the time limit of 100 ms, then a loss of frame alignment occurs.

## Frame Monitors (continued)

### Frame Formats (continued)




Note: BFA = basic frame alignment.

**Figure 20. T7698 Receive CRC-4 Multiframe Search Algorithm Using the 100 ms Internal Timer**

## Frame Monitors (continued)

### Frame Formats (continued)

**CRC-4 Multiframe Alignment Search Algorithm with 400 ms Timer.** This receive CRC-4 multiframe reframe mode is the modified CRC-4 multiframe alignment algorithm described in ITU Rec. 706 Annex B, where it is referred to as CRC-4-to-non-CRC-4 equipment interworking. A flow diagram of this algorithm is illustrated in Figure 21. This algorithm assumes that a valid basic frame alignment signal is consistently present but the CRC-4 multiframe alignment cannot be achieved by the end of the total CRC-4 multiframe alignment search period of 400 ms when the distant end is non-CRC-4 equipment. In this mode, the following consequent actions should be taken by the receiving equipment.

1. An indication that there is no incoming CRC-4 multiframe alignment signal.
2. All CRC-4 processing on the receive 2.048 Mbits/s signal is inhibited.

As described in ITU Rec. G.706, Section B.2.3:

1. A 400 ms timer is triggered on the initial recovery of the primary basic frame alignment.
2. The 400 ms timer is reset if and only if the criteria for loss of basic frame alignment, as described in ITU Rec. G.706 Section 4.1.1, is achieved.
3. A new search for frame alignment is initiated if CRC-4 multiframe alignment cannot be achieved in 8 ms as described in ITU Rec. G.706, Section 4.2. This new search for basic frame alignment will not reset the 400 ms timer or invoke consequent actions associated with loss of the primary basic frame alignment. In particular, all searches for basic frame alignment are carried out in parallel with, and independent of, the primary basic frame loss checking process. All subsequent searches for CRC-4 multiframe alignment are associated with each basic framing sequence found during the parallel search.
4. During the search for CRC-4 multiframe alignment, traffic is allowed through upon, and synchronized to, the initially determined primary basic frame alignment.
5. Upon detection of the CRC-4 multiframe before the 400 ms timer elapsing, the basic frame alignment associated with the CRC-4 multiframe alignment replaces, if necessary, the initially determined basic frame alignment.
6. If CRC-4 multiframe alignment is not found before the 400 ms timer elapses, it is assumed that a condition of interworking between equipment with and without CRC-4 capability exists.

## Frame Monitors (continued)

### Frame Formats (continued)

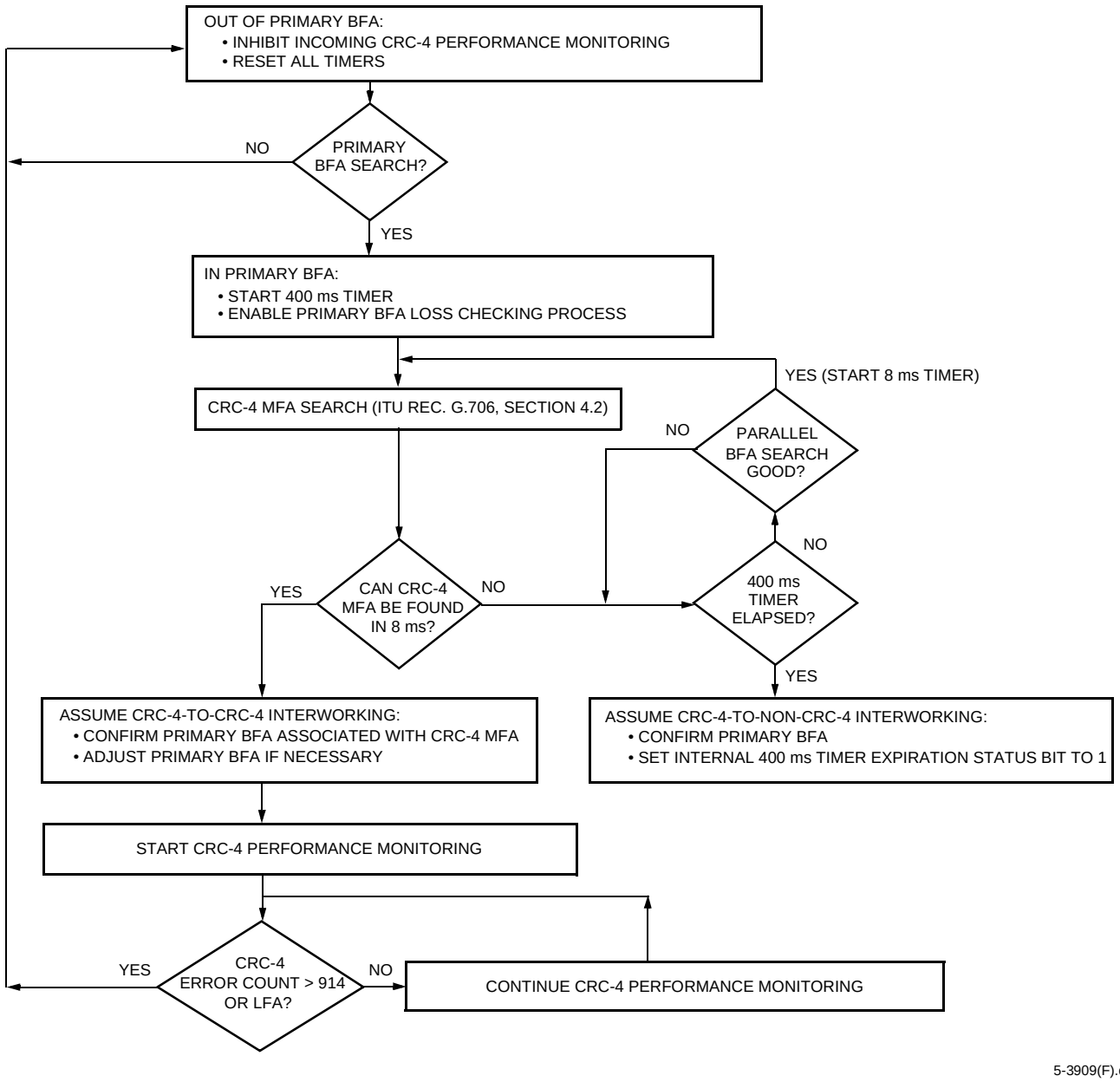



**Figure 21. CEPT Loss of CRC-4 Multiframe Alignment Recovery Algorithms: T7698 Receive CRC-4 Multiframe Search Algorithm for Automatic, CRC-4/ Non-CRC-4 Equipment Interworking as Defined by ITU (from ITU Rec. G.706, Annex B.2.2 - 1991)**

## Frame Monitors (continued)

### Alarms and Performance Monitoring

The T7698 receive frame monitor monitors the receive line data for alarm conditions and error events and presents this information to the system through the microprocessor interface status registers. The updating of the status registers is controlled by the receive line clock signal. When the line clock is lost, then the updating of all status information is corrupted.

The alarm conditions monitored on the received line interface are:

1. **Red alarm** or the **loss of frame alignment** indication. The red alarm indicates that the receive frame alignment for the line has been lost and the data cannot be properly extracted. The loss of frame condition for the various framing formats is defined in Table 37.

**Table 37. Red Alarm Conditions**

| Framing Format | Red Alarm (Loss of Frame Alignment) Condition |
|---|---|
| D4 | Two incorrect received $F_T$ framing bits out of four. |
| *SLC*-96 | Two incorrect received $F_T$ framing bits out of four. |
| DDS | Three incorrect received framing bits ($F_T$, $F_S$, or FAS pattern) out of twelve. |
| ESF | Two incorrect received $F_E$ framing bits out of four, or optionally (if register Framer_PR14, bit 0 = 0):<br>Option a (Framer_PR14, bit 1 = 0): 32 CRC-6 errors out of 33 CRC checks.<br>Option b (Framer_PR14, bit 1 = 1): >320 CRC-6 errors in one second. |
| CEPT | Three consecutive incorrect FAS patterns or three consecutive incorrect NOT FAS patterns, or optionally (if register Framer_PR14, bit 0 = 0) ≥ 915 received CRC-4 submultiframe errors out of 1000 CRC submultiframe checks. |

2. **Severely errored frame (SEF) alarm (DS1 only).** This alarm is determined by examining contiguous time windows for framing bit errors. For D4, DDS, and *SLC*-96 framing modes, the window size is 0.75 ms and only the $F_T$ bits are examined. For ESF, the window size is 3 ms, and only the $F_E$ bits are examined. An SEF defect occurs when two or more framing bit errors in a window are detected. An SEF defect is terminated when the signal is in-frame and there are less than two framing bit errors in a window.
3. **Yellow alarm** or the **remote frame alarm**. This alarm is an indication that the remote end is in a loss of frame alignment state. The T7698 detects an incoming remote frame alarm (commonly referred to as a yellow alarm) for the different framing formats as shown in Table 38.

**Table 38. Remote Frame Alarm Conditions**

| Framing Format | Remote Frame Alarm Format |
|---|---|
| D4 | Bit 2 of all time slots in the 0 state. |
| D4-Japanese | The twelfth (12th) framing bit in the 1 state in two out of three consecutive superframes. |
| DDS | Bit 6 of time slot 24 in the 0 state in all the word-24 occurrences in a superframe. |
| ESF | An alternating pattern of eight ones followed by eight zeros in the ESF data link. |
| CEPT | Bit 3 of the NOT FAS frame (A bit) signals the remote frame alarm.<br>For register Framer_PR2, bit 0 = 0, one A bit = 1 event required.<br>For register Framer_PR2, bit 0 = 1, three consecutive A bit = 1 events required. |

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

4. **Blue alarm** or the **alarm indication signal** (AIS). The alarm indication signal (AIS), sometimes referred to as the blue alarm, is an indication that the remote end is out of service. The T7698 detects an incoming alarm indication signal as defined in Table 39.

**Table 39. Alarm Indication Signal Conditions**

| Framing Format | Remote Frame Alarm Format |
|---|---|
| DS1 | As indicated in ANSI TI.231_1997, the receive frame monitor detects an unframed signal with a 1s density of at least 99.9% for a period of 3 ms. The AIS defect is terminated when a signal is detected as not meeting either the 99.9% 1s density or the unframed signal criteria for a period of 3 ms. |
| CEPT ETSI | As described in Draft prETS 300 233:1992 Section 8.2.2.4, loss of frame alignment occurs and the frame monitor receives a 512 bit period containing two (2) or less binary zeros. |
| CEPT ITU | As described in ITU Rec. G.775, the incoming signal has two (2) or fewer zeros in each of two consecutive double frame periods (512 bits). AIS is cleared if each of two consecutive double frame periods contains three (3) or more zeros or frame alignment signal (FAS) has been found. |

5. The **continuous E-bit** alarm (CON-E) is asserted when the receive frame monitor detects:
   I. Five consecutive seconds where each one-second interval contains ≥991 received E bits = 0 events.
   II. Simultaneously, no LFA or LMFA occurred.
   III. Optionally, no A bit = 1 was received*.
   IV. Optionally, neither Sa6-$F_{hex}$ nor Sa6-$E_{hex}$ codes were detected*.

The five-second timer is started when:
   I. CRC-4 multiframe alignment is achieved, and
   II. Optionally, A = 0 is detected, and
   III. Optionally, neither Sa6_$F_{hex}$ nor Sa6_$E_{hex}$ is detected.

The five-second counter is restarted and the continuous E-bit alarm is disabled when:
   I. LFA or LMFA occurs, or
   II. ≤ 990 E bit = 0 events occurred in 1 second, or
   III. Optionally, an A bit = 1, is detected, or
   IV. Optionally, a valid Sa6_$F_{hex}$ or Sa6_$E_{hex}$ code was detected.

* Options can be set through register Framer_PR1.

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

6. **Failed state** alarm or the **unavailable state alarm**.
   A. The default mode asserts this alarm upon detection of ten consecutive severely errored second events and deasserts this alarm upon detection of ten consecutive seconds which were not severely errored. The corresponding performance counters are incremented appropriately.
   B. Optionally, the T7698 can be programmed according to ITU Rec. G.826 (by setting register Framer_PR2, bit 4 high) to process the unavailable state at the onset of the unavailable state (at the beginning of the ten consecutive severely errored interval), and inhibit the increment of the severely errored and errored second counters for the duration of the unavailable state. In this mode, the contents of the performance counters contain information delayed by ten seconds. Out of unavailable state is entered at the onset of ten consecutive seconds that were not severely errored.
7. The **4-bit Sa6 codes** (Sa6_hex) are asserted if three consecutive 4-bit patterns have been detected. The alarms are disabled when three consecutive 4-bit Sa6 codes have been detected that are different from the pattern previously detected. The receive frame monitors the Sa6 bits for special codes described in ETS Draft prETS 300 233:1992, Section 9.2. The Sa6 codes are defined in Table 40 and Table 41. The Sa6 codes in Table 40 can be recognized as an asynchronous bit stream in either non-CRC-4 or CRC-4 modes as long as the receive frame monitor is in the basic frame alignment state. In the CRC-4 mode, the receive frame monitor can be forced to recognize the received Sa6 codes in Table 40 synchronously to the CRC-4 submultiframe structure as long as the receive frame monitor has achieved CRC-4 multiframe alignment (synchronous Sa6 monitoring can be enabled by setting bit 1 of register Framer_PR2 high).

**Table 40. Sa6 Bit Coding Recognized by the T7698 Receive Frame Monitor**

| Code | First Receive Bit (MSB) | . . . | | Last Received Bit (LSB) |
|---|---|---|---|---|
| Sa6_8hex | 1 | 0 | 0 | 0 |
| Sa6_Ahex | 1 | 0 | 1 | 0 |
| Sa6_Chex | 1 | 1 | 0 | 0 |
| Sa6_Ehex | 1 | 1 | 1 | 0 |
| Sa6_Fhex | 1 | 1 | 1 | 1 |

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

Table 41 defines the 4-bit Sa6 codes that are always detected synchronously to the CRC-4 submultiframe structure, and are only used for counting NT1 events.

**Table 41. Sa6 Bit Coding of NT1 Interface Events Recognized by the T7698 Receive Frame Monitor**

| Code | First Receive Bit (MSB) | . . . | | Last Received Bit (LSB) | Event at NT1 | Counter Size (bits) |
|---|---|---|---|---|---|---|
| Sa6_1hex | 0 | 0 | X | 1 | E = 0 | 16 |
| Sa6_2hex | 0 | 0 | 1 | X | CRC Error | 16 |

The reference points for receive CRC-4, E bit and Sa6 decoding are illustrated in Figure 22.

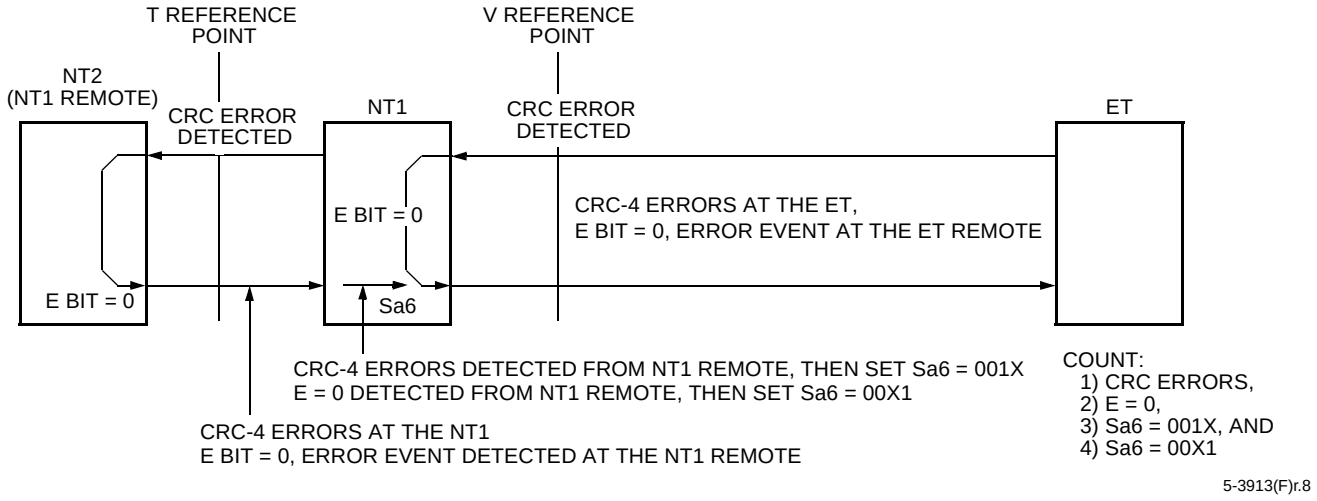



**Figure 22. The T and V Reference Points for a Typical CEPT E1 Application**

8. **CEPT auxiliary pattern alarm (AUXP).** The received auxiliary alarm (AUXP) is asserted when the receive frame monitor is in the LFA state and has detected more than 253 instances of "10" patterns for 512 consecutive bits. In a 512-bit interval, only two non- "10" patterns are allowed for the alarm to be asserted and maintained. The 512-bit interval is a sliding window determined by the first "10" pattern detected. This alarm is disabled when three or more non- "10" patterns are detected in 512 consecutive bits. The search for AUXP is synchronized with the first "10" pattern as illustrated in Table 42.

**Table 42. AUXP Synchronization and Clear Synchronization Process**

| 00 | 10 | 10 | 01 | 11 | 11 | 00 | 00 | 0 | 10 | 00 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| — | sync | — | — | — | clear sync | — | — | — | sync | . . . | . . . |

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

The error events monitored by the T7698 counters are as follows.

**Table 43. T7698 Event Counters Definition**

| Error Event | T7698 Mode | Definition | Counter Size (bits) |
|---|---|---|---|
| Bipolar Violations (BPVs) | AMI | Any bipolar violation or occurrence of any zero string length greater than 15 consecutive zeros. | 16 |
| | B8ZS | Any noncode bipolar violation, code violation, or occurrence of any zero string length greater than seven contiguous zeros. | |
| | HDB3 | Any noncode bipolar violation, code violation, or occurrence of any zero string length greater than three contiguous zeros. | |
| Framing Bit Errors (FERs) | SF:D4 | Any $F_T$ bit error. | 16 |
| | SF:*SLC*-96 | Any $F_T$ bit error. | |
| | SF:DDS | Any $F_T$, $F_S$, or time slot 24 FAS bit error. | |
| | ESF | Any $F_E$ bit error. | |
| | CEPT | Any FAS (0011011) or NOT FAS (bit 2) bit error. | |
| CRC Errors | ESF or CEPT with CRC | Any received checksum in error. | 16 |
| Received E Bits = 0 | CEPT with CRC | E bits = 0. | 16 |

For errored second and severely errored second processing, the error conditions to be monitored are programmable and can be selected by writing to registers Framer_PR4—Framer_PR7. Furthermore, the thresholds for errored seconds, bursty errored seconds, and severely errored seconds can also be made programmable by setting Framer_PR2, bit 3 (THR_ENABLE) high, and writing the desired threshold values in registers Framer_PR8—Framer_PR11. An optional mode where the threshold values are hardwired can be selected by setting THR_ENABLE = 0 (hardwired values are shown in the following tables).

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

Tables 44—47 summarize the errored second, bursty errored second, severely errored second, and unavailable second counter definitions.

**Table 44. T7698 Errored Second Counters Definition**

| Errored Event | T7698 Mode | Definition (Within a One-Second Period) | | Counter Size |
|---|---|---|---|---|
| | | Programmable | Hardwired Value | |
| Errored Second (ES) Events | DS1 (non-ESF) | ≥x FER events or any error conditions* | x = 1 | 16 |
| | DS1-ESF | ≥x CRC-6 errors or any error conditions | x = 1 | |
| | CEPT without CRC | ≥x FER events or any error conditions | x = 1 | |
| | CEPT with CRC-ET1 | ≥x CRC-4 errors or any error conditions | x = 1 | |
| | CEPT with CRC-ET1 Remote | ≥x E bit = 0 events or any error conditions | x = 1 | 16 |
| | CEPT with CRC-NT1 | ≥x Sa6 001X code events or any error conditions | x = 1 | 16 |
| | CEPT with CRC-NT1 Remote | ≥x Sa6 00X1 code events or any error conditions | x = 1 | 16 |

* Depending on the T7698 mode, the error conditions used to determine the errored and severely errored seconds can be: loss of frame alignment (LFA), severely errored frame (SEF), loss of multiframe alignment (LMFA), alarm indication signal (AIS), remote frame alarm (RFA), and the Sa6_8hex, Sa6_Ehex, Sa6_Fhex, an dSa6_Chex codes. The desired error condition can be enabled by setting the corresponding bit high in registers Framer_PR4—Framer_PR7.

## Frame Monitors (continued)

### Alarms and Performance Monitoring (continued)

**Table 45. T7698 Bursty Errored Second Counters Definition**

| Errored Event | T7698 Mode | Definition (Within a One-Second Period) | | Counter Size |
|---|---|---|---|---|
| | | Programmable | Hardwired Value | |
| Bursty Errored Second (BES) Events | DS1 (non-ESF) | x < FER < y | x = 1, y = 8 | 16 |
| | DS1-ESF | x < CRC-6 errors < y | x = 1, y = 320 | |
| | CEPT without CRC | x < FER < y | x = 1, y = 16 | |
| | CEPT with CRC-ET1 | x < CRC-4 errors < y | x = 1, y = 915 | |
| | CEPT with CRC-ET1 Remote | x < E bit = 0 events < y | x = 1, y = 915 | 16 |
| | CEPT with CRC-NT1 | x < Sa6 001X code events < y | x = 1, y = 915 | 16 |
| | CEPT with CRC-NT1 Remote | x < Sa6 00X1 code events < y | x = 1, y = 915 | 16 |

**Table 46. T7698 Severely Errored Second Counters Definition**

| Errored Event | T7698 Mode | Definition (Within a One-Second Period) | | Counter Size |
|---|---|---|---|---|
| | | Programmable | Hardwired Value | |
| Severely Errored Second (SES) Events | DS1 (non-ESF) | ≥y FER events or any error conditions | y = 8 | 16 |
| | DS1-ESF | ≥y CRC-6 errors or any error conditions | y = 320 | |
| | CEPT without CRC | ≥y FER events or any error conditions | y =16 | |
| | CEPT with CRC-ET1 | ≥y CRC-4 errors or any error conditions | y = 915 | |
| | CEPT with CRC-ET1 Remote | ≥y E bit = 0 events or any error conditions | y = 915 | 16 |
| | CEPT with CRC-NT1 | ≥y Sa6 001X code events or any error conditions | y = 915 | 16 |
| | CEPT with CRC-NT1 Remote | ≥y Sa6 00X1 code events or any error conditions | y = 915 | 16 |

**Table 47. T7698 Unavailable Second Counter Definition**

| Errored Event | T7698 Mode | Definition | Counter Size |
|---|---|---|---|
| Unavailable Second Events | All | A one-second period in the unavailable state*. | 16 |

* The unavailable state is asserted upon detection of ten consecutive severely errored second events, and is deasserted upon detection of ten consecutive seconds that were not severely errored.

## Frame Monitors (continued)

### Frame Monitor Register Structure

T7698 frame monitor registers are structured into two groups:

1. Parameter registers (Framer_PR0—Framer_PR12, Framer_PR14).
2. Status and counter registers (accessed through register 15).
   A. Clear-on-read status registers (Framer_SR0—Framer_SR7 and Framer_SR52).
   B. Clear-on-read counter registers (Framer_SR8—Framer_SR51).

All status and counter registers are clocked with the receive frame monitor corresponding line clock (TCLK1—TCLK4 and RCLK1—RCLK4 for the eight receive frame monitors).

All status registers are cleared on read. However, if the event or condition setting the status bit high is still present at the time of the read, the bit will remain in the high state for the duration of the alarm condition. If the event or condition is no longer present at the time of the read, then the bit is cleared on read. Moreover, only those bits in the 1 state at the time of the read are cleared.

All of the 16-bit counter registers are cleared on read only after reading both bytes. Once a read is initiated on the byte, the updating of the counter is disabled until both bytes are read.

Table 48 summarizes the frame monitor registers.

**Table 48. Frame Monitor Registers**

| Register Name | Function | Address | Type |
|---|---|---|---|
| Framer_PR0 | Parameter/Control | 0000 | Read/Write |
| Framer_PR1 | Parameter/Control | 0001 | Read/Write |
| Framer_PR2 | Parameter/Control | 0010 | Read/Write |
| Framer_PR3 | Parameter/Control | 0011 | Read/Write |
| Framer_PR4 | Parameter/Control | 0100 | Read/Write |
| Framer_PR5 | Parameter/Control | 0101 | Read/Write |
| Framer_PR6 | Parameter/Control | 0110 | Read/Write |
| Framer_PR7 | Parameter/Control | 0111 | Read/Write |
| Framer_PR8 | Parameter/Control | 1000 | Read/Write |
| Framer_PR9 | Parameter/Control | 1001 | Read/Write |
| Framer_PR10 | Parameter/Control | 1010 | Read/Write |
| Framer_PR11 | Parameter/Control | 1011 | Read/Write |
| Framer_PR12 | Parameter/Control | 1100 | Read/Write |
| Framer_PR14 | Parameter/Control | 1110 | Read/Write |
| Framer_SR | Status/Counter registers Framer_SR0—Framer_SR52 are read through this register | 1111 | Read only |

Note: Register 13 is the global index register.

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers

The following registers define the mode configuration of each frame monitor unit, and are all read/write registers.

#### Frame Monitor Mode Option Register (Framer_PR0)

**Table 49. Framer_PR0 Frame Monitor Mode Bits Decoding**

| Frame Format | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| ESF | (See Table 50.) | | | 0 | 0 | 0 | 0 | 0 |
| D4 | | | | 0 | 0 | 0 | 0 | 1 |
| DDS with FDL | | | | 0 | 0 | 0 | 1 | 0 |
| *SLC*-96 | | | | 0 | 0 | 0 | 1 | 1 |
| CEPT with no CRC-4 | | | | 0 | 0 | 1 | 0 | 0 |
| CEPT with CRC-4 | | | | 0 | 0 | 1 | 0 | 1 |

**Table 50. Framer_PR0 Line Code Option Bits Decoding**

| Line Code Format | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| B8ZS (DS1)/HDB3 (CEPT) | 0 | 0 | 0 | (See Table 49.) | | | | |
| Single Rail | 0 | 0 | 1 | | | | | |
| AMI | 0 | 1 | 1 | | | | | |

#### Frame Monitor CRC-4 Multiframe Control Option Register (Framer_PR1)

This register defines the CEPT CRC-4 options for the frame monitor unit. Frame monitor mode must be CEPT with CRC-4 to enable this register, otherwise these bits are ignored.

**Table 51. CEPT CRC-4 Option Bits Decoding**

| Framer_PR1 CRC-4 Options | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| CRC-4 with 915 Counter | 0 | X | X | X | X | X | 1 | 1 |
| CRC-4 with 100 ms Timer | 0 | X | X | X | 0 | 1 | X | 1 |
| CRC-4 Interworking Search with 400 ms Timer | 0 | X | X | X | 1 | 0 | X | 1 |
| CRC-4 with 990 REB Counter | 0 | X | X | 1 | X | X | X | 1 |
| CRC-4 with 990 REB Counter: A Bit = 1 Restart | 0 | X | 1 | 1 | X | X | X | 1 |
| CRC-4 with 990 REB Counter: Sa6-$F_{hex}$ or Sa6-$E_{hex}$ Restart | 0 | 1 | X | 1 | X | X | X | 1 |

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers (continued)

#### Frame Monitor Control Option Register (Framer_PR2)

These bits enable/disable various control/mode options.

**Table 52. Frame Monitor Control Option Register (Framer_PR2)**

| Bit | Description |
|---|---|
| 0 | **Receive A-Bit Filter (CEPT Only).** A 0 enables the A-bit alarm on any occurrence of an A bit = 1 event. A 1 forces the occurrence of three consecutive A bit = 1 events to assert and three consecutive A bit = 0 events to deassert the A-bit (RFA) alarm. |
| 1 | **Synchronous Sa6 Monitoring (CEPT Only).** A 0 enables the asynchronous monitoring of the Sa6 codes relative to the receive CRC-4 submultiframe. A 1 enables synchronous monitoring of the Sa6 pattern relative to the receive CRC-4 submultiframe. |
| 2 | **AIS Detection Mode (CEPT Only).** A 0 enables the detection of received line AIS as described in ETSI Draft prETS 300 233:1992. A 1 enables the detection of received line AIS as described in ITU Rec. G.775. |
| 3 | **THR_Enable (All Modes).** A 1 enables the thresholds for errored seconds, bursty errored seconds, and severely errored seconds to be programmed by writing the desired threshold to registers Framer_PR8—Framer_PR11. A 0 selects the hardwired threshold values shown in Tables 44—46. |
| 4 | **G.826 Mode.** A 0 forces the performance counters (errored second, severely errored second, and unavailable state) to count the current status. A 1 forces these counters to conform to the ITU G.826 standard. A delay of ten seconds is inherent in the G.826 mode. Transition from 0 to 1 in this bit will clear all performance counters. |
| 5 | **Receive Frame Monitor Reframe (All Modes).** This bit should normally be 0. A 0 to 1 transition of this bit generates a clock pulse that forces the loss of frame alignment (LFA) state and initiates a frame alignment search. Subsequent reframe commands must have this bit in the 0 state first. |
| 6 | **Factory Test.** This bit must always be set to 0. |
| 7 | **Software Restart (All Modes).** This bit should be set to 0 for normal operation. Setting this bit high forces reframe and clears internal counters, but keeps the parameter registers as programmed. This bit must be set to 0 to deassert this state. |

#### Frame Monitor CEPT Data Link Option Register (Framer_PR3)

This register controls the time slot used for CEPT data link.

**Table 53. Frame Monitor CEPT Data Link Option Register (Framer_PR3)**

| Bits | Description | | | |
|---|---|---|---|---|
| **0—2** | **Bit 2** | **Bit 1** | **Bit 0** | |
| | 0 | 0 | 0 | Sa4 time slot is used for data link. |
| | 0 | 0 | 1 | Sa5 time slot is used for data link. |
| | 0 | 1 | 0 | Sa6 time slot is used for data link. |
| | 0 | 1 | 1 | Sa7 time slot is used for data link. |
| | 1 | 0 | 0 | Sa8 time slot is used for data link. |
| **3—7** | **Reserved.** Must be set to the 0 state. | | | |

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers (continued)

#### ET1 Errored Event Enable Register* (Framer_PR4)

These bits enable the errored events used to determine errored and severely errored seconds at the local ET interface. A 1 in the bit position enables the errored event.

**Table 54. ET1 Errored Event Enable Register (Framer_PR4)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Framer_PR4 | 0 | 0 | 0 | 0 | 0 | AIS | LMFA | SEF (DS1)<br>LFA (CEPT) |

#### ET1 Remote End Errored Event Enable Register* (Framer_PR5)

These bits enable the errored events used to determine errored and severely errored seconds at the ET's remote end interface. A 1 in the bit position enables the errored event.

**Table 55. ET1 Remote End Errored Event Enable Register (Framer_PR5)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Framer_PR5 | 0 | Sa6-F$_{hex}$ | Sa6-E$_{hex}$ | Sa6-8$_{hex}$ | RFA | AIS | LMFA | SEF (DS1)<br>LFA (CEPT) |

#### NT1 Errored Event Enable Register* (Framer_PR6)

These bits enable the errored events used to determine errored and severely errored seconds at the network termination-1 interface. A 1 in the bit position enables the errored event.

**Table 56. NT1 Errored Event Enable Register (Framer_PR6)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Framer_PR6 | Sa6-C$_{hex}$ | 0 | 0 | Sa6-8$_{hex}$ | 0 | AIS | LMFA | SEF (DS1)<br>LFA (CEPT) |

#### NT1 Remote End Errored Event Enable Register* (Framer_PR7)

These bits enable the errored events used to determine errored and severely errored seconds at the network termination-1 remote end interface.

**Table 57. NT1 Remote End Errored Event Enable Register (Framer_PR7)**

| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Framer_PR7 | Sa6-C$_{hex}$ | Sa6-F$_{hex}$ | Sa6-E$_{hex}$ | Sa6-8$_{hex}$ | RFA | AIS | LMFA | SEF (DS1)<br>LFA (CEPT) |

* One occurrence of any one of these events causes an errored second and a severely errored second count increment.

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers (continued)

#### Errored Second Threshold Register (Framer_PR8)

This 8-bit register defines the errored event threshold for an errored second (ES). A one-second interval with errors less than the ES threshold value is not an errored second. Programming 00(hex) into this register disables the errored second threshold monitor circuitry.

**Table 58. Errored Second Threshold Register (Framer_PR8)**

| Register | Bits | Description |
|---|---|---|
| Framer_PR8 | 7—0 | ES Threshold Register (bit 7—bit 0) |

#### Severely Errored Second Threshold Register (Framer_PR9—Framer_PR10)

This 16-bit register defines the errored event threshold for a severely errored second (SES). A one-second interval with errors less than the SES threshold value is not a severely errored second. Programming 00(hex) into these two registers disables the severely errored second threshold monitor circuitry.

**Table 59. SES Threshold Register (Framer_PR9—Framer_PR10)**

| Register | Bits | Description |
|---|---|---|
| Framer_PR9 | 7—0 | SES MSB Threshold Register (bit 15—bit 8) |
| Framer_PR10 | 7—0 | SES LSB Threshold Register (bit 7—bit 0) |

#### Bursty Errored Second Threshold Register (Framer_PR11)

This 8-bit register defines the errored event threshold for a bursty errored second (BES). A one-second interval with errors less than the BES threshold value is not a BES. Programming 00(hex) in this register disables the BES threshold monitor circuitry.

**Table 60. BES Threshold Register (Framer_PR11)**

| Register | Bits | Description |
|---|---|---|
| Framer_PR11 | 7—0 | BES Threshold Register (bit 7—bit 0) |

#### Frame Monitor Exercise Register (Framer_PR12)

This register is for simulation purposes only. Set register to 00(hex) during normal operation.

**Table 61. Frame Monitor Exercise Register (Framer_PR12)**

| Bits | | Description |
|---|---|---|
| 5—0 | | See Table 62. |
| 6 | 7 | Second Pulse Interval |
| 0 | 0 | 1 s Pulse |
| 0 | 1 | 500 ms Pulse |
| 1 | 0 | 100 ms Pulse |
| 1 | 1 | Manufacturer's Test |

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers (continued)

**Table 62. Frame Monitor Exercise Register (Framer_PR12) Bits 5—0**

| Exercise Type | 5 | 4 | 3 | 2 | 1 | 0 | Exercise | Framing Format |
|---|---|---|---|---|---|---|---|---|
| Status Counters | 0 | 0 | 0 | 0 | 1 | 1 | CEPT 100 ms and 400 ms timers | CEPT with CRC-4 |
| | 0 | 0 | 0 | 1 | 0 | 0 | CEPT 915 CRC-4 error counter | CEPT with CRC-4 |
| | 0 | 0 | 0 | 1 | 1 | 1 | CEPT 990 E bit = 0 counter | CEPT with CRC-4 |
| Facility Status | 0 | 0 | 1 | 0 | 0 | 0 | Line format violation | All |
| | | | | | | | CRC checksum error | ESF or CEPT |
| | | | | | | | Receive remote frame alarm | D4 or ESF |
| | 0 | 0 | 1 | 0 | 0 | 1 | Alarm indication signal detection | All |
| | | | | | | | Loss of frame alignment | CEPT |
| | | | | | | | Receive remote frame alarm | Japanese D4 |
| | 0 | 0 | 1 | 0 | 1 | 1 | Frame-bit errors & loss of frame alignment | All |
| | | | | | | | Remote frame alarm | D4 and DDS |
| | | | | | | | CRC bit errors | ESF and CEPT |
| | 0 | 0 | 1 | 1 | 0 | 0 | Frame-bit errors | All |
| | 0 | 0 | 1 | 1 | 0 | 1 | Frame-bit errors & loss of frame alignment | All |
| | 0 | 0 | 1 | 1 | 1 | 0 | Frame-bit errors & loss of frame alignment | All |
| | | | | | | | Change of frame alignment | ESF, DDS, and CEPT |
| | 0 | 0 | 1 | 1 | 1 | 1 | Excessive CRC checksum errors | ESF and CEPT |
| Performance Status | 0 | 1 | 0 | 0 | 0 | 0 | Errored second | All |
| | 0 | 1 | 0 | 0 | 0 | 1 | Bursty errored second | |
| | 0 | 1 | 0 | 0 | 1 | 0 | Severely errored second | |
| | 0 | 1 | 0 | 0 | 1 | 1 | Severely errored second threshold | |
| | 0 | 1 | 0 | 1 | 0 | 0 | Unavailable state | |
| | 0 | 1 | 0 | 1 | 0 | 1 | Errored second threshold | |
| | 0 | 1 | 0 | 1 | 1 | 0 | All counters | |
| | 0 | 1 | 0 | 1 | 1 | 1 | Second pulse | |

## Frame Monitors (continued)

### Frame Monitor Parameter/Control Registers (continued)

**Table 62. Frame Monitor Exercise Register (Framer_PR12) Bits 5—0** (continued)

| Exercise Type | 5 | 4 | 3 | 2 | 1 | 0 | Exercise | Framing Format |
|---|---|---|---|---|---|---|---|---|
| Status Counters | 1 | 0 | 0 | 0 | 0 | 1 | CRC error counter | All |
| | 1 | 0 | 0 | 0 | 1 | 0 | Bursty errored second counter | |
| | 1 | 0 | 0 | 0 | 1 | 1 | Errored second counter | |
| | 1 | 0 | 0 | 1 | 0 | 0 | Severely errored second counter | |
| | 1 | 0 | 0 | 1 | 0 | 1 | Unavailable second counter | |
| | 1 | 0 | 0 | 1 | 1 | 0 | Line format violation counter | |
| | 1 | 0 | 0 | 1 | 1 | 1 | Frame-bit error counter | |
| Manufacturer's | 1 | 1 | 0 | 0 | 0 | 0 | Factory test | All |
| | All other combinations | | | | | | Reserved | All |

#### Frame Monitor CRC Option Register (Framer_PR14)

These bits enable/disable various CRC control options.

**Table 63. Frame Monitor CRC Option Register (Framer_PR14)**

| Bit | Description |
|---|---|
| 0 | A 0 forces loss of frame alignment due to excessive CRC errors for the ESF and CEPT with CRC-4 modes. Setting this bit to 1 prevents CRC errors from forcing loss of frame alignment. |
| 1 | This bit applies to ESF mode only. If bit 0 above is 0 (i.e., LFA due to CRC errors is enabled), then setting this bit to 0 forces LFA due to 32 CRC-6 errors out of 33 CRC checks, and setting this bit to 1 forces LFA due to greater than 320 CRC-6 errors in one second. |
| 2—7 | Reserved. |

#### Frame Monitor Status/Counter Register (Framer_SR)

Frame monitor status/counter register (register 15) is a read-only register and provides access to the status and counter registers Framer_SR0—Framer_SR52. Every new access to this register starts the read at register Framer_SR0. To read status registers Framer_SR1 to Framer_SR52, the first read must be followed by subsequent reads. The read address is incremented internally, so subsequent reads will access registers Framer_SR1—Framer_SR52. The chip select ($\overline{CS}$) must remain low for the entire time that register 15 is being read.

**Table 64. Frame Monitor Status/Counter Register (Framer_SR)**

| Bit | Description |
|---|---|
| 0—7 | Status registers Framer_SR0—Framer_SR52 are read through this register. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers

#### Frame Monitor Main Status Register (SR0)

This register reports on the alarm/event conditions in registers Framer_SR1—Framer_SR7. The bits in this register are cleared on read if the clear condition is satisfied.

**Table 65. Frame Monitor Main Status Register (Framer_SR0)**

| Bits | Description | Clear Condition |
|---|---|---|
| 0 | A 1 indicates one of the bits in register Framer_SR1 was set. Read register SR1 for additional information. | When all of the bits in register Framer_SR1 are cleared. |
| 1 | A 1 indicates one of the bits in register Framer_SR2 was set. Read register SR2 for additional information. | When all of the bits in register Framer_SR2 are cleared. |
| 2 | A 1 indicates one of the bits in register Framer_SR3 was set. Read register SR3 for additional information. | When all of the bits in register Framer_SR3 are cleared. |
| 3 | A 1 indicates one of the bits in register Framer_SR4 was set. Read register SR4 for additional information. | When all of the bits in register Framer_SR4 are cleared. |
| 4 | A 1 indicates one of the bits in register Framer_SR5 was set. Read register SR5 for additional information. | When all of the bits in register Framer_SR5 are cleared. |
| 5 | A 1 indicates one of the bits in register Framer_SR6 was set. Read register SR6 for additional information. | When all of the bits in register Framer_SR6 are cleared. |
| 6 | A 1 indicates one of the bits in register Framer_SR7 was set. Read register SR7 for additional information. | When all of the bits in register Framer_SR7 are cleared. |
| 7 | Reserved. | — |

#### Facility Alarm Condition Register (Framer_SR1)

A bit set to 1 indicates the frame monitor has recently detected the corresponding alarm condition. The alarm condition may or may not be present at the time of the read.

**Table 66. Facility Alarm Condition Register (Framer_SR1)**

| Bits | Description |
|---|---|
| 0 | **Loss of Frame Alignment (LFA).** A 1 indicates the frame monitor detected a loss of frame alignment. |
| 1 | **Loss of Superframe Alignment (LSFA).** A 1 indicates the frame monitor detected a loss of superframe alignment in the D4 and *SLC*-96 framing formats. This bit is 0 in all other framing modes. |
| 2 | **Alarm Indication Signal (AIS).** A 1 indicates the frame monitor detected an AIS pattern from its remote line end. |
| 3 | **Loss of Frame Alignment Since Last Read (LFALR).** A 1 indicates that the LFA state indicated in bit 0 of this register is the same LFA state from the previous read. |
| 4 | **Lack of Time Slot 0 CRC-4 Multiframe Alignment (LTS0MFA).** A 1 indicates the frame monitor has not detected time slot 0 CRC-4 multiframe alignment after basic frame alignment is found. This bit is 0 when receive CRC-4 checking is disabled or when the frame monitor is in the DS1 mode. |
| 5 | **Severely Errored Frame (SEF).** A 1 indicates the frame monitor detected a severely errored frame. |
| 6 | **Reserved.** |
| 7 | **Auxiliary Pattern Alarm (AUXP).** This bit is asserted when the frame monitor is in the LFA state and has detected a valid CEPT AUXP. This bit is 0 when the frame monitor is in the DS1 mode. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### Facility Remote Alarm Status Register (Framer_SR2)

A bit set to 1 indicates the frame monitor has recently detected the corresponding alarm condition. The alarm condition may or may not be present at the time of the read.

**Table 67. Facility Remote Alarm Status Register (Framer_SR2)**

| Bits | Description |
|---|---|
| 0 | **Remote Frame Alarm (RFA).** A 1 indicates the frame monitor detected a remote frame (yellow) alarm. |
| 1 | **Remote Japanese Frame Alarm (RJFA).** A 1 indicates the frame monitor detected the Japanese DS1 format frame alarm. This bit is 0 in the CEPT mode. |
| 2 | **Continuous Received E Bits (RCEBIT).** A 1 indicates the detection of a five-second interval containing ≥991 E bit = 0 events in each second. This bit is 0 when the frame monitor is in the DS1 mode. |
| 3 | **Received Sa6 = 8 (RSA8).** A 1 indicates the frame monitor detected a Sa6 code equal to 1000. This bit is 0 in the DS1 mode. |
| 4 | **Received Sa6 = A (hex) (RSAA).** A 1 indicates the frame monitor detected a Sa6 code equal to 1010. This bit is 0 in the DS1 mode. |
| 5 | **Received Sa6 = C (hex) (RSAC).** A 1 indicates the frame monitor detected a Sa6 code equal to 1100. This bit is 0 in the DS1 mode. |
| 6 | **Received Sa6 = E (hex) (RSAE).** A 1 indicates the frame monitor detected a Sa6 code equal to 1110. This bit is 0 in the DS1 mode. |
| 7 | **Received Sa6 = F (hex) (RSAF).** A 1 indicates the frame monitor detected a Sa6 code equal to 1111. This bit is 0 in the DS1 mode. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### Local and Remote ET Facility Event Register (Framer_SR3)

A bit set to 1 indicates the frame monitor has recently received the given errored event.

**Table 68. Local and Remote ET Facility Event Register (Framer_SR3)**

| Bits | Description |
|---|---|
| 0 | **Errored Second (ES).** A 1 indicates the frame monitor detected an errored event within a one-second interval at the local ET interface. |
| 1 | **Bursty Errored Second (BES).** A 1 indicates the frame monitor detected a bursty errored condition within a one-second interval at the local ET interface. |
| 2 | **Severely Errored Second (SES).** A 1 indicates the frame monitor detected a severely errored condition within a one-second interval at the local ET interface. |
| 3 | **Unavailable State (UASTATE).** A 1 indicates the frame monitor has detected at least 10 consecutive severely errored seconds at the local ET interface. If the G.826 mode is used (see register Framer_PR2, bit 4), it results in a 10 second delay in reporting of this condition. |
| 4 | **ET Remote Errored Second (ETRE_ES).** A 1 indicates the frame monitor detected an errored event within a one-second interval at the remote ET interface. This bit is 0 when the frame monitor is in the DS1 mode. |
| 5 | **ET Remote Bursty Errored Second (ETRE_BES).** A 1 indicates the frame monitor detected a bursty errored condition within a one-second interval at the remote ET interface. This bit is 0 when the frame monitor is in the DS1 mode. |
| 6 | **ET Remote Severely Errored Second (ETRE_SES).** A 1 indicates the frame monitor detected a severely errored condition within a one-second interval at the remote ET interface. This bit is 0 when the frame monitor is in the DS1 mode. |
| 7 | **ET Remote Unavailable State (ETRE_UASTAE).** A 1 indicates the frame monitor has detected at least 10 consecutive severely errored seconds at the remote ET interface. If the G.826 mode is used (see the parameter register), it results in a 10 second delay in reporting of this condition. This bit is 0 when the frame monitor is in the DS1 mode. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### Local and Remote Network Termination-1 Facility Event Register (Framer_SR4)

A bit set to 1 indicates the frame monitor has recently received the given errored event. All of the bits in this register are 0 in the DS1 mode.

**Table 69. Local and Remote Network Termination-1 Facility Event Register (Framer_SR4)**

| Bits | Description |
|---|---|
| 0 | **NT Errored Second (NT_ES).** A 1 indicates the frame monitor detected an errored event within a one-second interval at the network termination-1 interface. |
| 1 | **NT Bursty Errored Second (NT_BES).** A 1 indicates the frame monitor detected a bursty errored condition within a one-second interval at the network termination-1 interface. |
| 2 | **NT Severely Errored Second (NT_SES).** A 1 indicates the frame monitor detected a severely errored condition within a one-second interval at the network termination-1 interface. |
| 3 | **NT Unavailable State (NT_UASTATE).** A 1 indicates the frame monitor has detected at least ten consecutive severely errored seconds at the network termination-1 interface. If the G.826 mode is used (see register Framer_PR2, bit 4), it results in a 10 second delay in reporting of this condition. |
| 4 | **NT Remote Errored Second (NTRE_ES).** A 1 indicates the frame monitor detected an errored event within a one-second interval at the network termination-1 remote end interface. |
| 5 | **NT Remote Bursty Errored Second (NTRE_BES).** A 1 indicates the frame monitor detected a bursty errored condition within a one-second interval at the network termination-1 remote end interface. |
| 6 | **NT Remote Severely Errored Second (NTRE_SES).** A 1 indicates the frame monitor detected a severely errored condition within a one-second interval at the network termination-1 remote end interface. |
| 7 | **NT Remote Unavailable State (NTRE_UASTAE).** A 1 indicates the frame monitor has detected at least 10 consecutive severely errored seconds at the network termination-1 remote end interface. If the G.826 mode is used (see register Framer_PR2, bit 4), it results in a 10 second delay in reporting of this condition. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### Facility Event Register (Framer_SR5)

A bit set to 1 indicates the frame monitor has recently received the given condition.

**Table 70. Facility Event Register (Framer_SR5)**

| Bit | Description |
|---|---|
| 0 | **Change of Frame Alignment (CFA).** A 1 indicates the frame monitor established a new alignment which differs from the previous alignment. |
| 1 | **Change of Superframe Alignment (CSFA).** A 1 indicates the frame monitor has established superframe alignment in the D4 and *SLC*-96 modes. This alignment is established only after frame alignment is determined. This bit is zero in all other framing modes. |
| 2 | **CRC Monitor Reset (CRCRST).** A 1 indicates the CRC multiframe alignment in the frame monitor has been established. In ESF mode, this event coincides with the establishment of the frame alignment. In CEPT mode, this event will always follow the establishment of the primary basic frame. |
| 3—5 | **Reserved.** |
| 6 | **Indication of Excessive CRC Errors (CRC_EXC).** A 1 indicates that the frame monitor has detected excessive CRC errors. In ESF mode, 32 CRC errors out of 33 CRC checks set the CRC_EXC bit, if Framer_PR14, bit 1 = 0. And >320 CRC errors in one second set the CRC_EXC bit, if Framer_PR14, bit 1 = 1. In CEPT modes, >914 CRC submultiframe errors out of 1000 CRC submultiframe checks set the CRC_EXC bit. If Framer_PR14 bit 0 is set to 0, then excessive CRC errors force loss of frame alignment. |
| 7 | **CRC-4 Multiframe Alignment Timer Expire Indication.** A 1 indicates either the 100 ms or the 400 ms CRC-4 interworking timer expired (depending on the mode chosen through register Framer_PR1). This bit is 0 in the DS1, CEPT with no CRC-4, or CEPT with no timer modes. |

#### Facility Errored Event Register (Framer_SR6)

A bit set to 1 indicates the frame monitor has recently received the given condition.

**Table 71. Facility Errored Event Register (Framer_SR6)**

| Bits | Description |
|---|---|
| 0 | **Line Format Violation (LFV).** A 1 indicates that the frame monitor detected a line format violation. |
| 1 | **Frame-Bit Error (FBE).** A 1 indicates that the frame monitor detected a frame-bit or frame alignment pattern error. |
| 2 | **Received CRC Errors (RCRCEP).** A 1 indicates that the frame monitor has detected CRC errors. |
| 3 | **Receive E bit = 0 (REPITP).** A 1 indicates that the frame monitor has detected an E bit = 0 condition. This bit is 0 in the DS1 mode. |
| 4—5 | **Reserved.** |
| 6 | **Line Loopback On Code Detect (LLBON).** A 1 indicates that the frame monitor detected the line loopback enable code. This code is defined in the ANSI T1.403 as a framed 00001 pattern where the frame bit is inserted into the pattern. |
| 7 | **Line Loopback Off Code Detect (LLBOFF).** A 1 indicates that the frame monitor detected the line loopback disable code. This code is defined in the ANSI T1.403 as a framed 001 pattern where the frame bit is inserted into the pattern. |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### Facility Out of Unavailable State Register (Framer_SR7)

A bit set to 1 indicates that the frame monitor has recently received the given condition.

**Table 72. Facility Out of Unavailable State Register (Framer_SR7)**

| Bit | Description |
|---|---|
| 0 | **Out of Unavailable State (OUAS).** A 1 indicates that the frame monitor detected ten consecutive seconds that were not severely errored while in the unavailable state at the local ET interface. |
| 1 | **ET Remote Out of Unavailable State (ETRE_OUAS).** A 1 indicates that the frame monitor detected ten consecutive seconds that were not severely errored while in the unavailable state at the remote ET interface. |
| 2 | **NT Out of Unavailable State (NT_OUAS).** A 1 indicates that the frame monitor detected ten consecutive seconds that were not severely errored while in the unavailable state at the network termination-1. |
| 3 | **NT Remote Out of Unavailable State (NTRE_OUAS).** A 1 indicates that the frame monitor detected ten consecutive seconds that were not severely errored while in the unavailable state at the network termination-1 remote end. |
| 4—7 | **Reserved.** |

#### Bipolar Violation Counter Registers (Framer_SR8—Framer_SR9)

These registers contain the 16-bit count of received bipolar violations.

**Table 73. Bipolar Violation Counter Registers (Framer_SR8—Framer_SR9)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | BPVs counter (bit 15—bit 8). |
| LSB | 7—0 | BPVs counter (bit 7—bit 0). |

#### Framing Bit Error Counter Registers (Framer_SR10—Framer_SR11)

These registers contain the 16-bit count of framing bit errors. Framing bit errors are not counted during loss of frame alignment.

**Table 74. Framing Bit Error Counter Registers (Framer_SR10—Framer_SR11)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | FER counter (bit 15—bit 8). |
| LSB | 7—0 | FER counter (bit 7—bit 0). |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

#### CRC Error Counter Register (Framer_SR12—Framer_SR13)

These registers contain the 16-bit count of CRC errors. CRC errors are not counted during loss of frame alignment and loss of CEPT CRC multiframe alignment.

**Table 75. CRC-4 Error Counter Register (Framer_SR12—Framer_SR13)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | CRC error counter (bit 15—bit 8). |
| LSB | 7—0 | CRC error counter (bit 7—bit 0). |

#### E-Bit Counter Register (Framer_SR14—Framer_SR15)

These registers contain the 16-bit count of received E bit = 0 events. E bits are not counted during loss of frame alignment and loss of CRC-4 multiframe alignment.

**Table 76. E-Bit Counter Register (Framer_SR14—Framer_SR15)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | E-bit counter (bit 15—bit 8). |
| LSB | 7—0 | E-bit counter (bit 7—bit 0). |

#### CRC-4 Errors at NT1 from NT2 Counter Registers (Framer_SR16—Framer_SR17)

These registers contain the 16-bit count of each occurrence of Sa6 code 001X, detected synchronously to the CRC-4 multiframe.

**Table 77. CRC-4 Errors at NT1 from NT2 Counter Registers (Framer_SR16—Framer_SR17)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | CRC-4 errors at NT1 counter (bit 15—bit 8). |
| LSB | 7—0 | CRC-4 errors at NT1 counter (bit 7—bit 0). |

#### E Bit at NT1 from NT2 Counter Register (Framer_SR18—Framer_SR19)

These registers contain the 16-bit count of each occurrence of Sa6 code 00X1, detected synchronously to the CRC-4 multiframe.

**Table 78. E Bit at NT1 from NT2 Counter Registers (Framer_SR18—Framer_SR19)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | E bit at NT1 counter (bit 15—bit 8). |
| LSB | 7—0 | E bit at NT1 counter (bit 7—bit 0). |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

The following registers are dedicated to the exchange termination and its remote end interface. The alarm conditions to evaluate errored seconds and severely errored seconds are defined in the ET1 and ET1-remote enable registers (registers Framer_PR4 and Framer_PR5). The ET errored seconds and severely errored seconds counters monitor the occurrences of CRC errors or receive framing bit errors. The ET-RE errored seconds and severely errored seconds counters monitor the occurrences of received E bits = 0.

**Table 79. ET Errored Seconds Counter Register (Framer_SR20—Framer_SR21)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET errored seconds counter (bit 7—bit 0). |

**Table 80. ET Bursty Errored Seconds Counter Register (Framer_SR22—Framer_SR23)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET bursty errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET bursty errored seconds counter (bit 7—bit 0). |

**Table 81. ET Severely Errored Seconds Counter Register (Framer_SR24—Framer_SR25)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET severely errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET severely errored seconds counter (bit 7—bit 0). |

**Table 82. ET Unavailable Seconds Counter Register (Framer_SR26—Framer_SR27)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET unavailable seconds counter bits (bit 15—bit 8). |
| LSB | 7—0 | ET unavailable seconds counter bits (bit 7—bit 0). |

**Table 83. ET-RE Errored Seconds Counter Register (Framer_SR28—Framer_SR29)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET-RE errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET-RE errored seconds counter (bit 7—bit 0). |

**Table 84. ET-RE Bursty Errored Seconds Counter Register (Framer_SR30—Framer_SR31)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET-RE bursty errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET-RE bursty errored seconds counter (bit 7—bit 0). |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

**Table 85. ET-RE Severely Errored Seconds Counter Register (Framer_SR32—Framer_SR33)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET-RE severely errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | ET-RE severely errored seconds counter (bit 7—bit 0). |

**Table 86. ET-RE Unavailable Seconds Counter Register (Framer_SR34—Framer_SR35)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | ET-RE unavailable seconds counter bits (bit 15—bit 8). |
| LSB | 7—0 | ET-RE unavailable seconds counter bits (bit 7—bit 0). |

The following status registers are dedicated to the NT1 and the NT1 remote end (NT1-RE) interface. The alarm conditions to evaluate errored seconds and severely errored seconds are defined in the NT1 and NT1-RE enable registers (registers Framer_PR6 and Framer_PR7). The NT1 errored seconds and severely errored seconds monitor the occurrences of Sa6 = 001X. The NT1-RE errored seconds and severely errored seconds monitor the occurrences of Sa6 = 00X1.

**Table 87. NT1 Errored Seconds Counter Register (Framer_SR36—Framer_SR37)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1 errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1 errored seconds counter (bit 7—bit 0). |

**Table 88. NT1 Bursty Errored Seconds Counter Register (Framer_SR38—Framer_SR39)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1 bursty errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1 bursty errored seconds counter (bit 7—bit 0). |

**Table 89. NT1 Severely Errored Seconds Counter Register (Framer_SR40—Framer_SR41)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1 severely errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1 severely errored seconds counter (bit 7—bit 0). |

**Table 90. NT1 Unavailable Seconds Counter Register (Framer_SR42—Framer_SR43)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1 unavailable seconds counter bits (bit 15—bit 8). |
| LSB | 7—0 | NT1 unavailable seconds counter bits (bit 7—bit 0). |

## Frame Monitors (continued)

### Frame Monitor Status/Counter Registers (continued)

**Table 91. NT1-RE Errored Seconds Counter Register (Framer_SR44—Framer_SR45)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1-RE errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1-RE errored seconds counter (bit 7—bit 0). |

**Table 92. NT1-RE Bursty Errored Seconds Counter Register (Framer_SR46—Framer_SR47)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1-RE bursty errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1-RE bursty errored seconds counter (bit 7—bit 0). |

**Table 93. NT1-RE Severely Errored Seconds Counter Register (Framer_SR48—Framer_SR49)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1-RE severely errored seconds counter (bit 15—bit 8). |
| LSB | 7—0 | NT1-RE severely errored seconds counter (bit 7—bit 0). |

**Table 94. NT1-RE Unavailable Seconds Counter Register (Framer_SR50—Framer_SR51)**

| Byte | Bits | Description |
|---|---|---|
| MSB | 7—0 | NT1-RE unavailable seconds counter bits (bit 15—bit 8). |
| LSB | 7—0 | NT1-RE unavailable seconds counter bits (bit 7—bit 0). |

#### Received CEPT Time Slot 0 (TS0) Bits

Bits [0—4] in this register contain the last valid received NOT FAS, time slot 0, Sa4 to Sa8 bits while the frame monitor was in basic frame alignment. Bits 5 and 6 contain the Frame 13 and Frame 15 E bits, respectively, when the frame monitor is in the CEPT with CRC-4 mode, and the FAS and NOT FAS Si bits (TS0, bit 1), respectively, when the frame monitor is in the CEPT without CRC-4 mode.

**Table 95. Received NOT FAS TSO RSA and E Bits Framer_(SR52)**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 0 | Frame 15 E bit (CEPT with CRC-4) or NOT FAS bit 1 (CEPT without CRC-4) | Frame 13 E bit (CEPT with CRC-4) or FAS bit 1 (CEPT without CRC-4) | Sa8 | Sa7 | Sa6 | Sa5 | Sa4 |

## Facility Data Links

Figure 23 shows the block diagram of the receive facility data link and its interface with the receive frame monitor. The receive frame monitor extracts the data link bits (RFD) from the DS1 or CEPT data link and generates a data link clock (RFCK) to be used by the FDL section.

T7698 is capable of extracting the data from the facility data link in the *SLC*-96, DDS, ESF, and CEPT framing formats. In CEPT, any one of the Sa bits (Sa4—Sa8) can be declared as the facility data link. Access to the FDL can be through the 64-byte FIFO of the FDL block. Data passing through the FDL HDLC section may be HDLC framed or passed through transparently.

A brief summary of the facility data link functions is given below with more details to follow in the features section.

1. Bit-oriented message operation. The ANSI T1.403-1995 bit-oriented data link messages are recognized and stored in register FDL_SR2. The number of times that an ANSI code must be received for detection can be programmed from 1 to 10 by writing to register FDL_PR0, bits 4—7. When the code is detected, the RANSI bit (register FDL_SR0, bit 4) is set.
2. HDLC operation. This is the default mode of operation when the FDL receiver is enabled (register FDL_PR0, bit 1 = 1). The HDLC framer detects the HDLC flags, checks the CRC bytes, and stores the data in the receive FIFO.
3. HDLC operation with performance report messages (PRM). This mode can be enabled by setting register FDL_PR0, bits 1 and 2 high. In this case, the frame header, PRM message, and the frame check sequence are stored in the FIFO.
4. Transparent operation. Setting the HTRANS bit (register FDL_PR3, bit 6) disables the HDLC processing. Incoming data link bits are stored in the FIFO.
5. Transparent operation with pattern match. When the MATCH bit (register FDL_PR3, bit 5) is set high in addition to the HTRANS bit, the facility data link starts storing the data in the FIFO only after the programmable match character (register FDL_PR2, bits 0—7) has been detected.

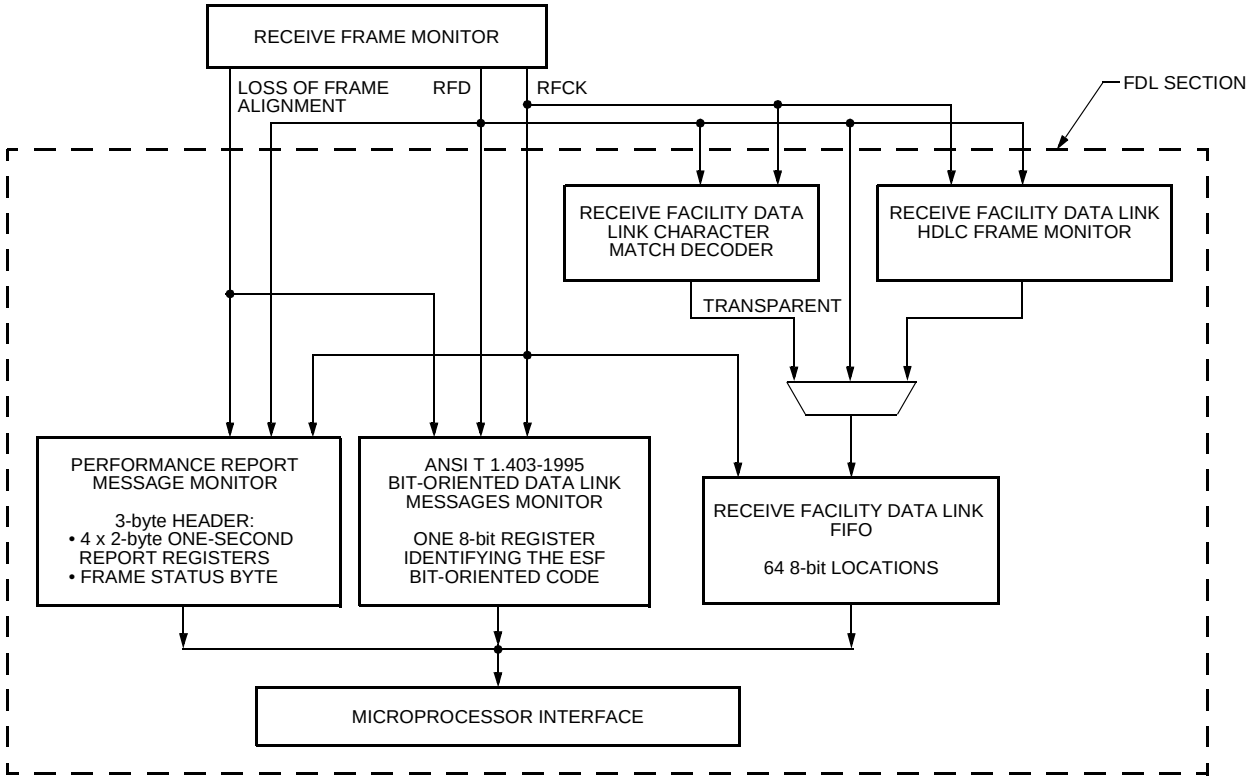



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**Figure 23. Block Diagram of the Receive Facility Data Link**

## Facility Data Links (continued)

### FDL Features

#### ANSI T1.403 Bit Codes

1. The receive FDL monitor will detect any of the ANSI T1.403 ESF bit-oriented messages.
2. The received ESF FDL bit messages are received in the form $0X_5X_4X_3X_2X_1X_0011111111$. The right-most bit is received first. The bits designated as X are the defined ANSI ESF FDL code bits. These code bits are written in the received FDL ANSI bit code status register (FDL_SR2) when the entire code is received.
3. The minimum number of times a valid code must be received before it is reported can be programmed from 1 to 10.

The FDL ANSI Bit Code Status Register has the following format.

**Table 96. FDL ANSI Bit Code Status Register (FDL_SR2)**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | $X_5$ | $X_4$ | $X_3$ | $X_2$ | $X_1$ | $X_0$ |

#### ANSI Performance Report Messages (PRM)

As defined in ANSI T1.403, the Performance Report Messages consist of four pairs of octets containing receive frame monitor status. The format of the PRM is shown in Table 97.

**Table 97. Performance Report Message Structure**

**Note:** Octet numbering is as given in Figure 6 of ANSI T1.403-1995.

| Octet No. | PRM B7 | PRM B6 | PRM B5 | PRM B4 | PRM B3 | PRM B2 | PRM B1 | PRM B0 | |
|---|---|---|---|---|---|---|---|---|---|
| 5 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 | t0 |
| 6 | FE | SE | LB | G1 | R | G2 | Nm | Nl | |
| 7 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 | t1 |
| 8 | FE | SE | LB | G1 | R | G2 | Nm | Nl | |
| 9 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 | t2 |
| 10 | FE | SE | LB | G1 | R | G2 | Nm | Nl | |
| 11 | G3 | LV | G4 | U1 | U2 | G5 | SL | G6 | t3 |
| 12 | FE | SE | LB | G1 | R | G2 | Nm | Nl | |

## Facility Data Links (continued)

### FDL Features (continued)

#### HDLC Mode

The receive queue manager forms a status of frame (SF) byte for each HDLC frame and stores the SF byte in the receive FDL FIFO after the last data byte of the associated frame. HDLC frames with n bytes will have (n + 1) bytes stored in the receive FIFO. The frame check sequence (CRC) bytes of the received HDLC frame are not stored into the receive FIFO, unless the HRPF bit (register FDL_PR0, bit 2) is set (i.e., HDLC mode with PRM is enabled).

The SF byte has the following format.

**Table 98. HDLC Status of Frame Byte**

| RSF B7 | RSF B6 | RSF B5 | RSF B4 | RSF B3 | RSF B2 | RSF B1 | RSF B0 |
|---|---|---|---|---|---|---|---|
| BAD CRC | ABORT | FIFO OVERRUN | BAD BYTE COUNT | 0 | 0 | 0 | 0 |

Whenever an SF byte is present in the FIFO, the end of frame (EOF) bit (register FDL_SR1, FDL bit 7) is set. The receiver queue status (RQS) bits (register FDL_SR1, bits 0—6) report the number of bytes up to and including the first SF byte. If no SF byte is present in the FIFO, the count directly reflects the number of data bytes available to be read. Depending on the FDL frame size, it is possible for multiple frames to be present in the FIFO. The receive fill level (RFL) indicator (register FDL_PR1, bits 0—5) can be programmed in the receive FDL control register to tailor the service time interval to the system environment. The FIFO full (RF) status bit (register FDL_SR0, bit 0) is set in the status register when the FIFO reaches the preprogrammed full position. In the HDLC mode, REOF status bit (register FDL_SR0, bit 1) is set high when the receiver has identified the end of frame and has written the SF byte for that frame. The FDL overrun status bit (register FDL_SR0, bit 2) is set high when the receiver needs to write either status or data to the FIFO when the FIFO is full. An overrun condition will cause the last byte of the FIFO to be overwritten with an SF byte indicating the overrun status. In the HDLC mode, the receive idle (RIDL) status bit (register FDL_SR0, bit 3) is set high whenever 15 or more continuous 1s have been detected.

#### Transparent Mode

The receive FIFO receives FDL data from the receive frame monitor and directly loads this FDL information bit for bit, least significant bit first. If the MATCH bit is set in the FDL control register, the receive FDL FIFO will load data only after the matched pattern has been detected. The match character and all subsequent bytes are placed into the receive FIFO.

## Facility Data Links (continued)

### FDL Features (continued)

#### Receive HDLC Operation

This section describes the standard HDLC functions performed by the T7698's receive HDLC block. HDLC operation is the default mode of operation after the FDL receiver is enabled. The FDL receives the data link data and clock from the frame monitor, identifies frames for proper format, reconstructs data bytes, provides bit destuffing as necessary, and loads parallel data into the receive FIFO. HDLC frames on the serial link have the following format.

**Table 99. HDLC Frame Format**

| Opening Flag | User Data Field | Frame Check Sequence (CRC) | Closing Flag |
|---|---|---|---|
| 01111110 | ≥8 bits | 16 bits | 01111110 |

All bits between the opening flag and the CRC are considered user data bits and are stored in the FIFO buffers. The 16 bits preceding the closing flag are the frame check sequence or cyclic redundancy check (CRC) bits.

**Zero-Bit Deletion (Bit Destuffing).** The HDLC protocol recognizes three special bit patterns: flags, aborts, and idles. These patterns have the common characteristic of containing at least six consecutive 1s. It is assumed that zero-bit stuffing is done on user data and CRC fields of the frame to avoid mimicking one of these special patterns; whenever five 1s occur between flags, a 0 bit is automatically inserted after the fifth 1, prior to transmission of the next bit. When the detector detects five successive 1s followed by a 0, the 0 is assumed to have been inserted and is deleted (bit destuffing).

**Flags.** The receiver recognizes the 01111110 pattern as a flag. Two successive flags may or may not share the intermediate 0 bit and are identified as two flags (i.e., both 011111101111110 and 0111111001111110 are recognized by the T7698's HDLC block). When another flag is identified, it is treated as the closing flag. As mentioned above, a flag sequence in the user data or FCS fields is prevented by zero-bit insertion. The HDLC receiver recognizes a single flag between frames as both a closing and opening flag.

**Aborts.** When receiving a frame, the receiver recognizes the abort sequence whenever it receives a 0 followed by seven consecutive 1s. This status results in the abort bit, and possibly the bad byte count bit and/or bad CRC bits, being set in the status of frame status byte which is appended to the receive data queue. The last two bytes of user data are assumed to be CRC bits and are not placed in the queue. All subsequent bytes are ignored until a valid opening flag is received.

**Idles.** In accordance with the HDLC protocol, the HDLC block recognizes 15 or more contiguous received 1s as idle. When the HDLC block receives 15 contiguous 1s, the receiver status idle bit (RIDL) is set.

**CRC.** For a given user data field, 16 additional bits that constitute an error-detecting code are added to the data field. As defined in the HDLC protocol, the frame check sequence bits are transmitted most significant bit first and are bit stuffed. CRC (or cyclic redundancy) is calculated as a function of the user data bits by using the ITU-T standard polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

The receiver performs the same calculation on the received bits after destuffing and compares the results to an expected result. An error occurs if, and only if, there is a mismatch. The result of the CRC check is reported in bit 7 of the status of frame byte, which is placed in the receive FIFO after the last data byte of the frame. The CRC is not stored in the FIFO unless the HRPF bit (register FDL_PR0, bit 2) is set.

**Status of Frame Byte Description.** The receiver status is available in two ways. First, the queue manager creates a status of frame (SF) byte for each HDLC frame and stores this status byte in the FIFO after the last data byte of the associated frame. Thus, a frame containing n user data bytes results in n + 1 bytes present in the receive FIFO. The SF byte has the format shown in Table 98.

Bit 7 of the SF byte is the CRC status bit. If an incorrect CRC was detected, this bit is set to 1. If the CRC was correct, the bit is 0.

## Facility Data Links (continued)

### FDL Features (continued)

Bit 6 of the SF byte is the abort status. A high (1) indicates the frame associated with this status byte was aborted (i.e., the abort sequence was detected after an opening flag and before a subsequent closing flag). An abort can also cause bits 7 and/or 4 to go high (1). An abort is not reported when a flag is followed by seven 1s.

If the FIFO overrun bit (bit 5) is high, it indicates that a FIFO overrun occurred (the 64-byte FIFO size was exceeded; see the Receiver Overrun section below).

The bad byte count bit (bit 4) indicates whether or not the bit count received was a multiple of eight (i.e., an integer number of bytes). A high (1) indicates that the bit count received after 0-bit deletion was not a multiple of eight, and a low indicates that the bit count was a multiple of eight. When a non-byte-aligned frame is received, all bits received are present in the receive FIFO, but the byte before the SF byte contains less than eight valid data bits. The nondata bits are the first bits of the received CRC. The HDLC block provides no indication of how many of the bits in the byte are valid. It is up to the user and the protocol to decide what to do with non-byte-aligned frames.

Bits 0 to 3 of the SF byte are not used and are guaranteed to be 0 when read. A good frame is implied when the SF byte is 00 hexadecimal.

The last byte of a completed frame in the receive FIFO is always the SF byte. As a frame is received, the 2 bytes preceding the closing flag are assumed to be the frame check sequence (CRC) bits and are not loaded into the FIFO, unless the HRPF bit (register FDL_PR0, bit 2) is set. Thus, the final 2 bytes received in an aborted frame are not placed in the queue, and an aborted frame of 2 bytes or less may cause only an SF status byte to appear in the FIFO. The writing of the SF byte is followed by setting the REOF status bit (register FDL_SR0, bit 1).

The receive queue status (RQS) bits (register FDL_SR1, bits 0—6) are updated as bytes are loaded into the receive FIFO. The SF byte is included in the byte count. When the first SF byte is placed in the FIFO, the EOF bit (register FDL_SR1, bit 7) is set, and the status freezes until the FIFO is read. As bytes are read from the FIFO, the RQS count decreases until it reads 1. The byte read when RQS is 0000001 and the EOF bit is high (1) is the SF byte describing the error status of the frame just read. Once the first SF byte is read from the FIFO, the FIFO status is updated to report the number of bytes to the next SF byte, if any, or the number of additional bytes present. When EOF is low, no SF byte is currently present in the FIFO, and the RQS bits report the number of bytes present. As bytes are read from the FIFO, RQS count decreases with each read until it reads 0 when the FIFO is totally empty. The EOF bit is also low when the FIFO is completely empty. Thus, the RQS and EOF bits provide a mechanism to recognize the end of one frame and the beginning of another. Reading the receiver status register does not affect the FIFO buffers. In the event of a receiver overrun (see below), an SF byte is written to the receive FIFO. Multiple SF bytes can be present in the FIFO. Note that the RQS reports only the number of bytes to the first SF status byte.

To allow users to tailor receiver FIFO service intervals to their systems, the receiver fill level (RFL) bits (register FDL_PR1, bits 0—5) are provided. These bits are coded in binary and determine when the receiver full (RF) status bit (register FDL_SR0, bit 1) is set. The value programmed in the RFL bits represents the total number of bytes necessary in the FIFO to set the RF status bit. The RF bit alone is not sufficient to determine the number of bytes to read, as some of the bytes may be SF bytes. The RQS and EOF bits allow the user to determine the number of bytes to read.

**Programming Note:** Since the receiver writing to the receive FIFO and the host reading from the receive FIFO are asynchronous events, it is possible for a host read to put the number of bytes in the receive FIFO just below the programmed RFL level and a receiver write to put it back above the RFL level. This causes the receiver full (RF) status bit to be set again.

**Receiver Overrun.** A receiver overrun occurs if the 64-byte limit of the receiver FIFO is exceeded, i.e., data has been received faster than it has been read out of the receive FIFO and written to the system memory. Upon overrun, an SF byte with the overrun bit (bit 5) set replaces the last byte in the FIFO. The SF byte can have other error conditions present. For example, it is unlikely that the CRC is correct. Thus, care should be taken to prioritize the possible frame errors in the software service routine. The last byte in the FIFO is overwritten with the SF byte regardless of the type of byte (data or SF status) being overwritten. The overrun condition is reported by setting the ROVERUN (register FDL_SR0, bit 2) status bit. Data is ignored until the condition is cleared and a new frame begins. The overrun condition is cleared by reading register FDL_SR0 and reading at least one byte from the receive FIFO. Because multiple frames can be present in the FIFO, good frames as well as the overrun frame can be present. The host can determine the overrun frame by looking at the SF status byte.

## Facility Data Links (continued)

### Facility Data Link Parameter/Status Registers

The facility data link (FDL) has eight registers summarized in the following table.

**Table 100. Facility Data Link Registers**

| Register Name | Function | Address | Type |
|---|---|---|---|
| FDL_PR0 | Parameter | 0000 | R/W |
| FDL_PR1 | Parameter | 0001 | R/W |
| FDL_PR2 | Parameter | 0010 | R/W |
| FDL_PR3 | Parameter | 0011 | R/W |
| FDL_SR0 | Status | 0100 | R |
| FDL_SR1 | Status | 0101 | R |
| FDL_SR2 | Status | 0110 | R |
| FDL_SR3 | Status | 0111 | R |

Access to the 64-bit FIFO is through register 07 (FDL_SR3).

The following registers define the mode configuration of each FDL, and are all read/write registers.

**Table 101. FDL Configuration Control Register (FDL_PR0)**

| Bits | Description |
|---|---|
| 0 | **FDL Receiver Reset (HRR).** HRR = 1 generates an internal pulse that resets the FDL receiver. The FDL receiver FIFO and related circuitry are cleared. The REOF, RF, RIDLE, and OVERRUN status bits are cleared. This bit resets to 0. |
| 1 | **FDL Receiver Enable (HRE).** HRE = 1 activates the FDL receiver. HDLC is the default mode of operation. HRE = 0 forces the receiver into an inactive state. This bit resets to 0. |
| 2 | **FDL Receive PRM Frames (HRPF).** HRPF = 1 allows the receive FDL unit to write the entire received performance report message into the receive FIFO. This bit resets to 0. |
| 3 | **Test FIFO (TR FIFO).** This bit is reserved for testing purposes and should be set to 0. |
| 4—7 | **Number of ANSI Code Detect CNCD[0:3].** These bits define the number of times an ANSI code must be received before the code is recognized and stored. Resets to the value 0101(10). A value of 1000(1) is set when 0000 is inadvertently written for these bits. |

## Facility Data Links (continued)

### Facility Data Link Parameter/Status Registers (continued)

**Table 102. FDL Receiver Fill Level Control Register (FDL_PR1)**

| Bits | Description |
|---|---|
| 0—5 | **Receive Fill Level (RFL[0:5]).** Bits 0—5 define the receive FIFO full threshold value that will cause the receive FIFO fill (RF) status bit to be set. RFL = 00000 forces the receive FIFO to set the RF bit when the receive FIFO is completely full. RFL = 01111 will force the receive FIFO to set the RF bit when the receive FIFO contains 15 or more bytes. |
| 6—7 | **Reserved.** |

**Table 103. FDL Receiver Match Character Register (FDL_PR2)**

| Bits | Description |
|---|---|
| 0—7 | **Receiver Match Character (RHMC0—RHMC7).** This character is used only in the transparent mode (register FDL_PR3, bit 6 = 1). When the pattern match bit (register FDL_PR3, bit 5) is set to 1, the receiver searches the incoming bit stream for the receiver match character. Data is loaded into the receive FIFO only after this character has been identified. The byte identified as matching the receiver match character is the first byte loaded into the FIFO. The default is to search for an HDLC flag, but any character can be programmed by the user. The search for the receive match character is in a sliding window fashion. |

**Table 104. FDL Transparent Mode Control Register (FDL_PR3)**

| Bits | Description |
|---|---|
| 0—2 | **Reserved.** |
| 3 | **Match Status (MSTAT).** Read only. When this bit is set to 1, the receiver match character has been recognized. If no match is being performed (register FDL_PR3, bit 5 = 0), the MSTAT bit is set to 1 automatically when the first bit is received. |
| 4 | **Reserved.** Should be set to 0. |
| 5 | **Pattern Match (MATCH).** When this bit is set to 1, the FDL receiver does not load the data into the receive FIFO until the receive match character has been detected. When this bit is 0, the receiver loads the data into the receive FIFO without searching for a match character. |
| 6 | **FDL Transparent Mode (HTRANS).** When this bit is set to 1, the FDL receiver performs no HDLC processing on incoming data. |
| 7 | **FDL Test.** This bit is reserved for manufacturing test purposes only and should be set to 0. |

## Facility Data Links (continued)

### Facility Data Link Parameter/Status Registers (continued)

The following registers report the status of the FDL/HDLC and are read only.

**Table 105. FDL Fill Status Register (FDL_SR0)**

| Bits | Description |
|---|---|
| 0 | **Receiver Full (RF).** This bit is set to 1 when the receive FIFO is at or above the programmed full level (see register FDL_PR1). This status bit is cleared to 0 by a read of register FDL_SR3 (register 07). |
| 1 | **Receive End of Frame (REOF).** This bit is set to 1 when the receiver has finished receiving a frame. It becomes 1 upon reception of the last bit of the closing flag of a frame or the last bit of an abort sequence. This status bit is cleared to 0 by a read of this register. This bit is not generated in the transparent mode. |
| 2 | **Receiver Overrun (ROVERUN).** This bit is set to 1 when the receive FIFO has overrun its capacity. This status bit is cleared to 0 by a read of this register. |
| 3 | **Receiver Idle (RIDL).** This bit is set to 1 when the receiver is idle (i.e., 15 or more consecutive 1s have been received). This status bit is cleared to 0 by a read of this register. |
| 4 | **Receive ANSI Bit Codes (RANSI).** This bit is set to 1 when the FDL receiver recognizes a valid T1.403 ESF FDL bit code. The receive ANSI bit code is stored in register FDL_SR2. This status bit is cleared to 0 by a read of this register. |
| 5—7 | **Reserved.** Must be set to 0. |

**Table 106. FDL Receiver Status Register (FDL_SR1)**

| Bits | Description |
|---|---|
| 0—6 | **Receive Queue Status (RQS[0:6]).** Bits 0—6 indicate how many bytes are in the receive FIFO, including the first status of frame (SF) byte. The bits are encoded in binary where bit 0 is the least significant bit. |
| 7 | **End of Frame (EOF).** When EOF = 1 the receive queue status indicates the number of bytes up to and including the first SF byte. |

**Table 107. FDL Receiver ANSI ESF Bit Codes (FDL_SR2)**

| Bits | Description |
|---|---|
| 0—5 | **RANSI[0:5].** This register contains bits X0X1X2X3X4X5 of the ESF FDL bit messages of the following form: $0X_5X_4X_3X_2X_1X_0$0 11111111. These bits are cleared to 3F when a clear-on-read occurs. |
| 6—7 | **Reserved.** |

**Table 108. Receiver FDL FIFO Access Register (FDL_SR3)**

| Bits | Description |
|---|---|
| 0—7 | **DATA0—DATA7.** The user data received via the FDL receiver are read through this register. |

## XCLK Reference Clock

The device requires an externally applied clock, XCLK (pin 83), for the clock and data recovery function and the jitter attenuation option. XCLK must be a continuously active (i.e., ungapped, unjittered, and unswitched) and an independent reference clock such as from an external system oscillator or system clock for proper operation. It must not be derived from any recovered line clock (i.e., from RLCK or any synthesized frequency of RLCK).

XCLK may be supplied in one of four formats; 16 x DS1, DS1, 16 x CEPT, or CEPT. The format is selected globally for the device by CLKS (pin 1) and CLKM (pin 51).

CLKS determines the relationship between the primary line data rate and the clock signal applied to XCLK. For CLKS = 0, a clock at 16x the primary line data rate clock (24.704 MHz for DS1 and 32.768 MHz for CEPT) must be applied to XCLK. For CLKS = 1, a primary line data rate clock (1.544 MHz for DS1 and 2.048 MHz for CEPT) must be applied to XCLK.

The CLKS pin has an internal pull-down resistor allowing the pin to be left open, i.e., a no connect, in applications using a 16x reference clock. The CLKS pin must be pulled up to $V_{DD}$ for applications using a primary line data rate clock.

CLKM determines whether the clock synthesizer is operating in CEPT or DS1 mode when XCLK is a primary line data rate clock. For CLKM = 0, the clock synthesizer operates in DS1 mode (1.544 MHz). For CLKM = 1, the clock synthesizer operates in CEPT mode (2.048 MHz). The CLKM pin is ignored when CLKS = 0.

The CLKM pin has an internal pull-down resistor allowing the pin to be left open, i.e., a no connect, in applications using a DS1 line rate reference clock. The CLKM pin must be pulled up to $V_{DD}$ for applications using a CEPT line data rate clock.

### 16x XCLK Reference Clock

The specifications for XCLK using a 16x reference clock are defined in Table 109. The 16x reference clock is selected when CLKS = 0.

**Table 109. XCLK (16x, CLKS = 0) Timing Specifications**

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Frequency:<br>DS1<br>CEPT | <br>—<br>— | <br>24.704<br>32.768 | <br>—<br>— | <br>MHz<br>MHz |
| Range*,† | –100 | — | 100 | ppm |
| Duty Cycle | 40 | — | 60 | % |

* When JABW0 = 1 and the jitter attenuator is used in the receive data path, the tolerance on XCLK should be tightened to ±20 ppm in order to meet the jitter accommodation requirements of TBR12/13 as given in G.823 for line data rates of ±50 ppm.

† If XCLK is used as the source for AIS (see Alarm Indication Signal Generator (XAIS) on page 31), it must meet the nominal transmission specifications of 1.544 MHz ± 32 ppm for DS1 (T1), or 2.048 MHz ± 50 ppm for CEPT (E1).

## XCLK Reference Clock (continued)

### Primary Line Rate XCLK Reference Clock and Internal Reference Clock Synthesizer

In some applications, it is more desirable to provide a reference clock at the primary data rate. In such cases, the LIU can utilize an internal 16x clock synthesizer allowing the XCLK pin to accept a primary data rate clock. The specifications for XCLK using a primary rate reference clock are defined in Table 110.

**Table 110. XCLK (1x, CLKS = 1) Timing Specifications**

| Parameter | Value | | | Unit |
|---|---|---|---|---|
| | Min | Typ | Max | |
| Frequency:<br>DS1<br>CEPT | <br>—<br>— | <br>1.544<br>2.048 | <br>—<br>— | <br>MHz<br>MHz |
| Range*,† | –100 | — | 100 | ppm |
| Duty Cycle | 40 | — | 60 | % |
| Rise and Fall Times (10%—90%) | — | — | 5 | ns |

* When JABW0 = 1 and the jitter attenuator is used in the receive data path, the tolerance on XCLK should be tightened to ±20 ppm in order to meet the jitter accommodation requirements of TBR12/13 as given in G.823 for line data rates of ±50 ppm.

† If XCLK is used as the source for AIS (see Alarm Indication Signal Generator (XAIS) on page 31), it must meet the nominal transmission specifications of 1.544 MHz ± 32 ppm for DS1 (T1), or 2.048 MHz ± 50 ppm for CEPT (E1).

The data rate reference clock and the internal clock synthesizer is selected when CLKS = 1. In this mode, a valid and stable data rate reference clock must be applied to the XCLK pin before and during the time a hardware reset is activated ($\overline{\text{RESET}}$ = 0). The reset must be held active for a minimum of two data rate clock periods to ensure proper resetting of the clock synthesizer circuit. Upon the deactivation of the reset pin ($\overline{\text{RESET}}$ = 1), the LIU will extend the reset condition internally for approximately $1/2(2^{12} - 1)$ line clock periods, or 1.3 ms for DS1 and 1 ms for CEPT after the hardware reset pin has become inactive, allowing the clock synthesizer additional time to settle. No activity such as microprocessor read/write should be performed during this period. The device will be operational 2.7 ms after the deactivation of the hardware reset pin. Issuing an LIU software restart (LIU_REG2 bit 5 (RESTART) = 1) does not impact the clock synthesizer circuit.

## Power Supply Bypassing

External bypassing is required for all channels. A 1.0 µF capacitor must be connected between $V_{DD}X$ and GNDX. In addition, a 0.1 µF capacitor must be connected between $V_{DDD}$ and $GND_D$, and a 0.1 µF capacitor must be connected between $V_{DDA}$ and $GND_A$. Ground plane connections are required for GNDX, $GND_D$, and $GND_A$. Power plane connections are also required for $V_{DD}X$ and $V_{DDD}$. The need to reduce high-frequency coupling into the analog supply ($V_{DDA}$) may require an inductive bead to be inserted between the power plane and the $V_{DDA}$ pin of every channel.

Capacitors used for power supply bypassing should be placed as close as possible to the device pins for maximum effectiveness.

## Line Circuitry

The transmit and receive tip/ring connections provide a matched interface to the cable (i.e., terminating impedance matches the characteristic impedance of the cable). The diagram in Figure 24 shows the appropriate external components to interface to the cable for a single transmit/receive channel. The component values are summarized in Table 111, based on the specific application.

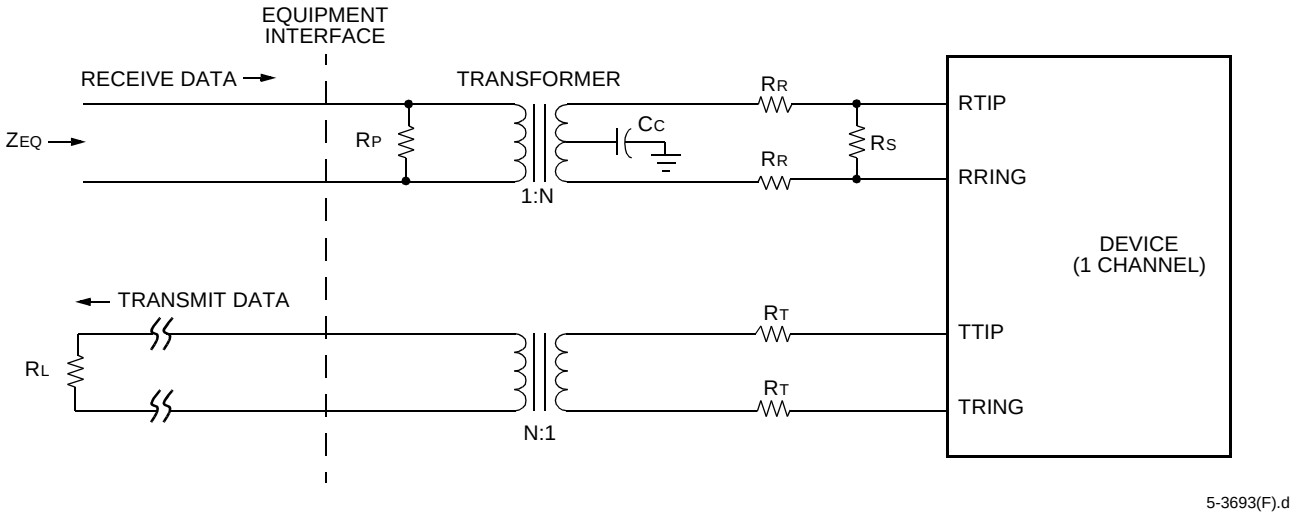


**Figure 24. Line Termination Circuitry**

**Table 111. Termination Components by Application**

Resistor tolerances are ±1%. Transformer turns ratio tolerances are ±2%.

| Symbol | Name | Cable Type | | | | Unit |
|---|---|---|---|---|---|---|
| | | DS1[1] Twisted Pair | CEPT 75 Ω[2] Coaxial | | CEPT 120 Ω[4] Twisted Pair | |
| | | | Option 1[3] | Option 2[4] | | |
| $C_C$ | Center Tap Capacitor | 0.1 | 0.1 | 0.1 | 0.1 | µF |
| $R_P$ | Receive Primary Impedance | 200 | 200 | 200 | 200 | Ω |
| $R_R$ | Receive Series Impedance | 71.5 | 28.7 | 59 | 174 | |
| $R_S$ | Receive Secondary Impedance | 113 | 82.5 | 102 | 205 | |
| $Z_{EQ}$ | Equivalent Line Termination | 100 | 75 | 75 | 120 | |
| | Tolerance | ±4 | ±4 | ±4 | ±4 | % |
| $R_T$ | Transmit Series Impedance | 0 | 26.1 | 15.4 | 26.1 | Ω |
| $R_L$ | Transmit Load Termination[5] | 100 | 75 | 75 | 120 | |
| N | Transformer Turns Ratio | 1.14 | 1.08 | 1.36 | 1.36 | — |

1. Use Lucent 2795B transformer.
2. For CEPT 75 Ω applications, Option 1 is recommended over Option 2 for lower device power dissipation. Option 2 increases power dissipation by 13 mW per channel when driving 50% ones data. Option 2 allows for the use of the same transformer as in CEPT 120 Ω applications.
3. Use Lucent 2795D transformer.
4. Use Lucent 2795C transformer.
5. A ±5% tolerance is allowed for the transmit load termination, $R_L$.

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

**Table 112. Absolute Maximum Ratings**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| dc Supply Voltage | –0.5 | 6.5 | V |
| Storage Temperature | –65 | 125 | °C |
| Maximum Voltage (digital pins) with Respect to $V_{DDD}$ | — | 0.5 | V |
| Minimum Voltage (digital pins) with Respect to $GND_D$ | –0.5 | — | V |
| Maximum Allowable Voltages (RTIP[1—4], RRING[1—4]) with Respect to $V_{DD}$ | — | 0.5 | V |
| Minimum Allowable Voltages (RTIP[1—4], RRING[1—4]) with Respect to GND | –0.5 | — | V |

## Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

**Table 113. ESD Threshold Voltage**

| Device | Model | Voltage |
|---|---|---|
| T7698 | HBM | 2000 V |
| | CDM (corner pins) | 1000 V |
| | CDM (non-corner pins) | 500 V |

## Operating Conditions

**Table 114. Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient Temperature | $T_A$ | –40 | — | 85 | °C |
| Power Supply | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V |

## Power Requirements

The majority of the power used by the T7698 device is used by the line drivers. Therefore, the power is very dependent on data pattern and signal amplitude. The signal amplitude is a function of the transmit equalization in DS1 mode. When configured for greater cable loss, the signal amplitude is greater at the output drivers, and thus uses more power. For this reason, the power specification of Table 115 are given for various conditions. The typical specification is for a quasi-random signal and the maximum specification is for a mark (all 1s) pattern. The power also varies somewhat for DS1 versus CEPT, so figures are given for both.

**Table 115. Power Consumption**

| Parameter | Power | | Unit |
|---|---|---|---|
| | Typ | Max | |
| CEPT | 570 | 815 | mW |
| DS1 | 530 | 850 | mW |
| DS1 w/ Max Eq. | 665 | 1110 | mW |

Power dissipation is the amount of power dissipated in the device. It is equal to the power drawn by the device minus the power dissipated in the line.

**Table 116. Power Dissipation**

| Parameter | Power | | Unit |
|---|---|---|---|
| | Typ | Max | |
| CEPT | 505 | 685 | mW |
| DS1 | 435 | 660 | mW |
| DS1 w/ Max Eq. | 485 | 750 | mW |

## Electrical Characteristics

**Table 117. Logic Interface Characteristics**

**Note:** The following internal resistors are provided: 50 kΩ pull-up on the $\overline{ICT}$ and $\overline{RESET}$ pins, 50 kΩ pull-down on the CLKS and CLKM pins, and 100 kΩ pull-up on the $\overline{CS}$, XCLK, and BCLK pins. This requires these input pins to sink no more than 20 µA. The device uses TTL input and output buffers; all buffers are CMOS-compatible.

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage:<br>Low<br>High | <br>$V_{IL}$<br>$V_{IH}$ | — | <br>$GND_D$<br>2.1 | <br>0.8<br>$V_{DDD}$ | <br>V<br>V |
| Input Leakage | $I_L$ | — | — | 10 | µA |
| Output Voltage:<br>Low<br>High | <br>$V_{OL}$<br>$V_{OH}$ | <br>$I_{OL}$ = –5.0 mA<br>$I_{OH}$ = 5.0 mA | <br>$GND_D$<br>$V_{DDD}$ – 0.5 | <br>0.4<br>$V_{DDD}$ | <br>V<br>V |
| Input Capacitance | $C_I$ | — | — | 3.0 | pF |
| Load Capacitance* | $C_L$ | — | — | 50 | pF |

* 100 pF allowed for AD[7:0] (pins 69 to 76).

# Timing Characteristics

## Microprocessor Interface Timing

The I/O timing specifications for the microprocessor interface are given in Table 118 and shown in Figures 25—32. The microprocessor interface pins use CMOS I/O levels. All outputs, except the address/data bus AD[7:0], are rated for a capacitive load of 50 pF. The AD[7:0] outputs are rated for a 100 pF load. The minimum read and write cycle time is 200 ns for all device configurations.

**Table 118. Microprocessor Interface I/O Timing Specifications**

| Symbol | Configuration | Parameter | Setup (ns) (Min) | Hold (ns) (Min) | Delay (ns) (Max) |
|---|---|---|---|---|---|
| t1 | Modes 1 & 2 | $\overline{AS}$ Asserted Width | — | 10 | — |
| t2 | | Address Valid to $\overline{AS}$ Asserted (deMUX) | 10 | — | — |
| t3 | | $\overline{AS}$ Asserted to Address Invalid (deMUX) | — | 10 | — |
| t4 | | $\overline{CS}$ Asserted to $\overline{AS}$ Asserted | 10 | — | — |
| t5 | | R/$\overline{W}$ Valid to $\overline{DS}$ Asserted (read) | 5 | — | — |
| t6 | | $\overline{AS}$ Asserted to $\overline{DS}$ Asserted | 30 | — | — |
| t7 | | $\overline{CS}$ Asserted to $\overline{DTACK}$ High | — | — | 25 |
| t8 | | $\overline{DS}$ Asserted to $\overline{DTACK}$ Asserted (read) | — | — | 20 |
| t9 | | $\overline{DS}$ Asserted to Data Valid | — | — | 50 |
| t10 | | $\overline{DS}$ Deasserted to $\overline{CS}$ Deasserted | — | 15 | — |
| t11 | | $\overline{DS}$ Deasserted to R/$\overline{W}$ Invalid | — | 5 | — |
| t12 | | $\overline{DS}$ Deasserted to $\overline{DTACK}$ Deasserted | — | — | 20 |
| t13 | | $\overline{CS}$ Deasserted to $\overline{DTACK}$ High Impedance | — | — | 10 |
| t14 | | $\overline{DS}$ Deasserted to Data Invalid (read) | — | 5 | — |
| t15 | | R/$\overline{W}$ Valid to $\overline{DS}$ Asserted (write) | 5 | — | — |
| t16 | | $\overline{AS}$ Asserted to $\overline{DS}$ Asserted (write) | 10 | — | — |
| t17 | | $\overline{DS}$ Asserted Width (write) | — | 5 | — |
| t18 | | Data Valid to $\overline{DS}$ Asserted (write) | 5 | — | — |
| t19 | | $\overline{DS}$ Deasserted to Data Invalid (write) | — | 10 | — |
| t20 | | $\overline{DS}$ Asserted to $\overline{DTACK}$ Asserted (write) | — | — | 20 |
| t21 | | Address Valid to $\overline{AS}$ Asserted (MUX) | 10 | — | — |
| t22 | | $\overline{AS}$ Asserted to Address Invalid (MUX) | — | 10 | — |

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 25—32.

## Timing Characteristics (continued)

### Microprocessor Interface Timing (continued)

**Table 118. Microprocessor Interface I/O Timing Specifications** (continued)

| Symbol | Configuration | Parameter | Setup (ns) (Min) | Hold (ns) (Min) | Delay (ns) (Max) |
|---|---|---|---|---|---|
| t23 | Modes 3 & 4 | ALE Asserted Width | — | 10 | — |
| t24 | | Address Valid to ALE Asserted (deMUX) | 10 | — | — |
| t25 | | ALE Asserted to Address Invalid (deMUX) | — | 10 | — |
| t26 | | $\overline{CS}$ Asserted to ALE Asserted | 10 | — | — |
| t27 | | ALE Asserted to $\overline{RD}$ Asserted | 30 | — | — |
| t28 | | $\overline{CS}$ Asserted to RDY Low | — | — | 20 |
| t29 | | Falling Edge of MPCLK to RDY Asserted (read) | — | — | 25 |
| t30 | | $\overline{RD}$ Asserted (read) to Data Valid | — | — | 50 |
| t31 | | $\overline{RD}$ Deasserted to Data Invalid (read) | — | 5 | — |
| t32 | | $\overline{RD}$ Deasserted to RDY Deasserted | — | — | 20 |
| t33 | | $\overline{RD}$ Deasserted to $\overline{CS}$ Deasserted | — | 15 | — |
| t34 | | $\overline{CS}$ Deasserted to RDY High Impedance | — | — | 10 |
| t35 | | ALE Asserted to $\overline{WR}$ Asserted (write) | 10 | — | — |
| t36 | | $\overline{WR}$ Asserted Width (write) | — | 5 | — |
| t37 | | Data Valid to $\overline{WR}$ Asserted (write) | 5 | — | — |
| t38 | | $\overline{WR}$ Deasserted to Data Invalid (write) | — | 10 | — |
| t39 | | $\overline{WR}$ Deasserted to RDY Deasserted | — | — | 20 |
| t40 | | $\overline{WR}$ Deasserted to $\overline{CS}$ Deasserted | — | 15 | — |
| t41 | | Rising Edge of MPCLK to RDY Asserted (write) | — | — | 25 |
| t42 | | Address Valid to ALE Asserted (MUX) | 10 | — | — |
| t43 | | ALE Asserted to Address Invalid (MUX) | — | 10 | — |

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 25—32.

## Timing Characteristics (continued)

### Microprocessor Interface Timing (continued)

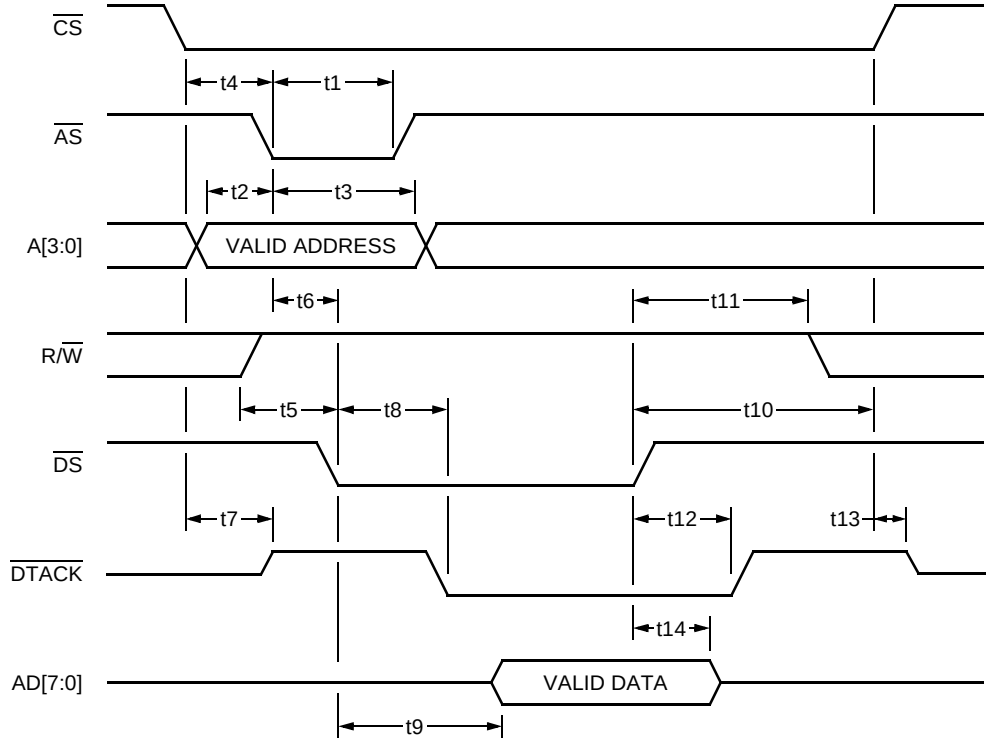


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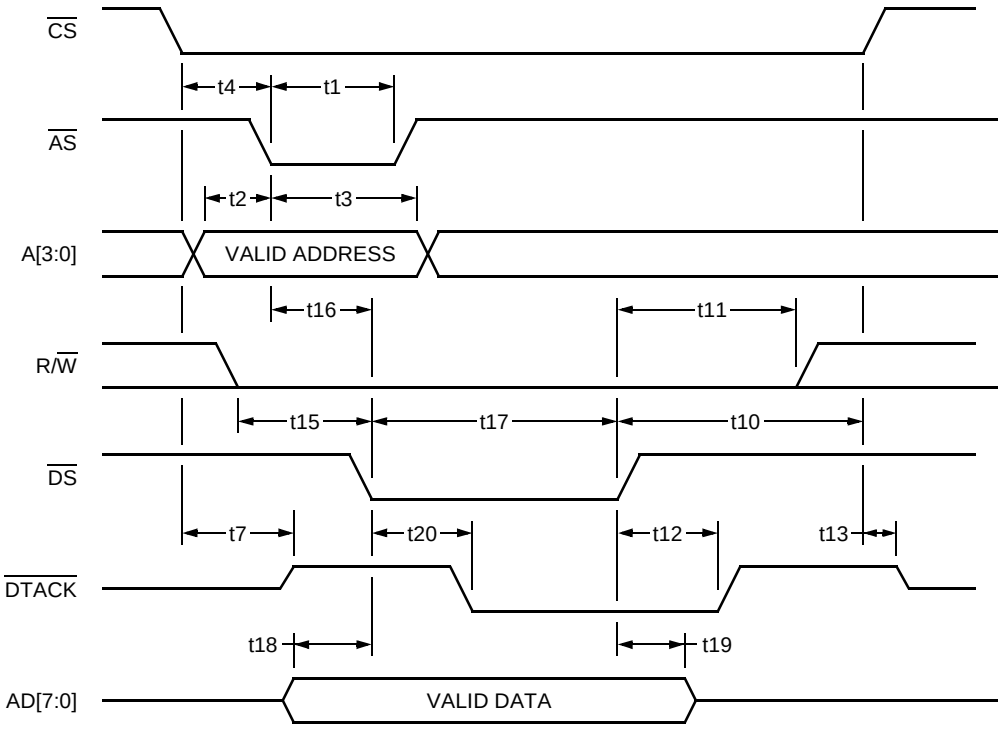
**Figure 25. Mode 1—Read Cycle Timing (MPMODE = 0, MPMUX = 0 )**




5-7193(F)r.3

**Figure 26. Mode 1—Write Cycle Timing (MPMODE = 0, MPMUX = 0)**

## Timing Characteristics (continued)

### Microprocessor Interface Timing (continued)

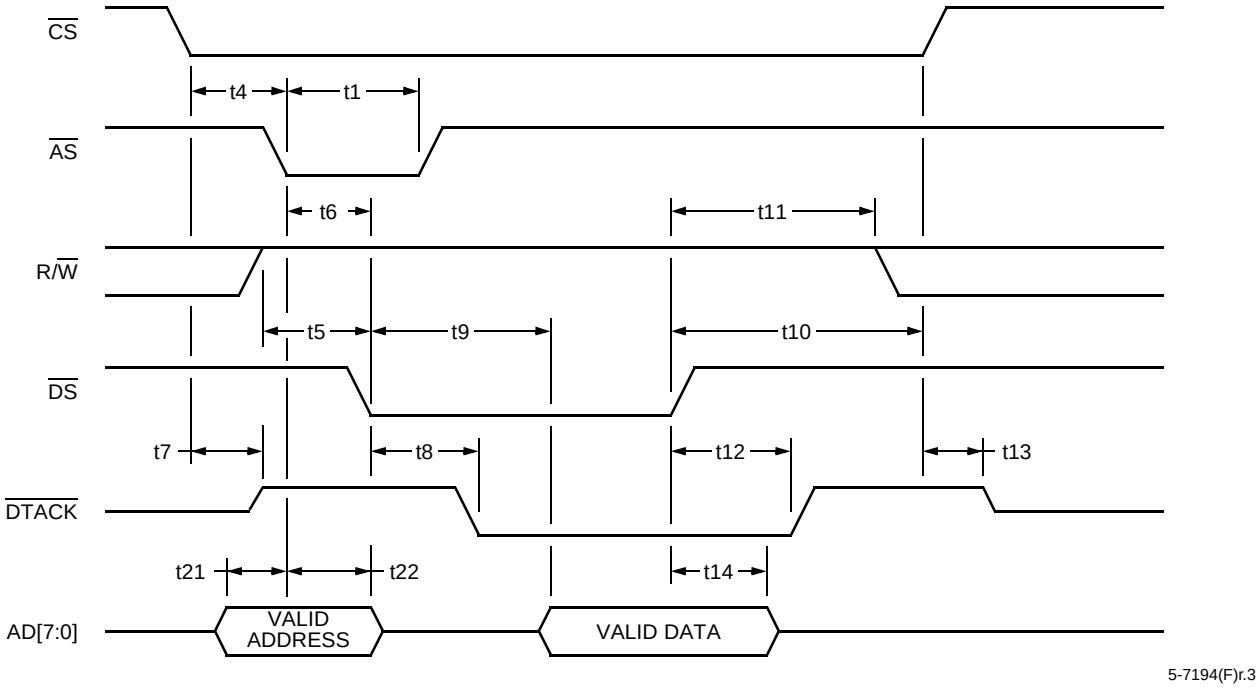



**Figure 27. Mode 2—Read Cycle Timing (MPMODE = 0, MPMUX = 1)**

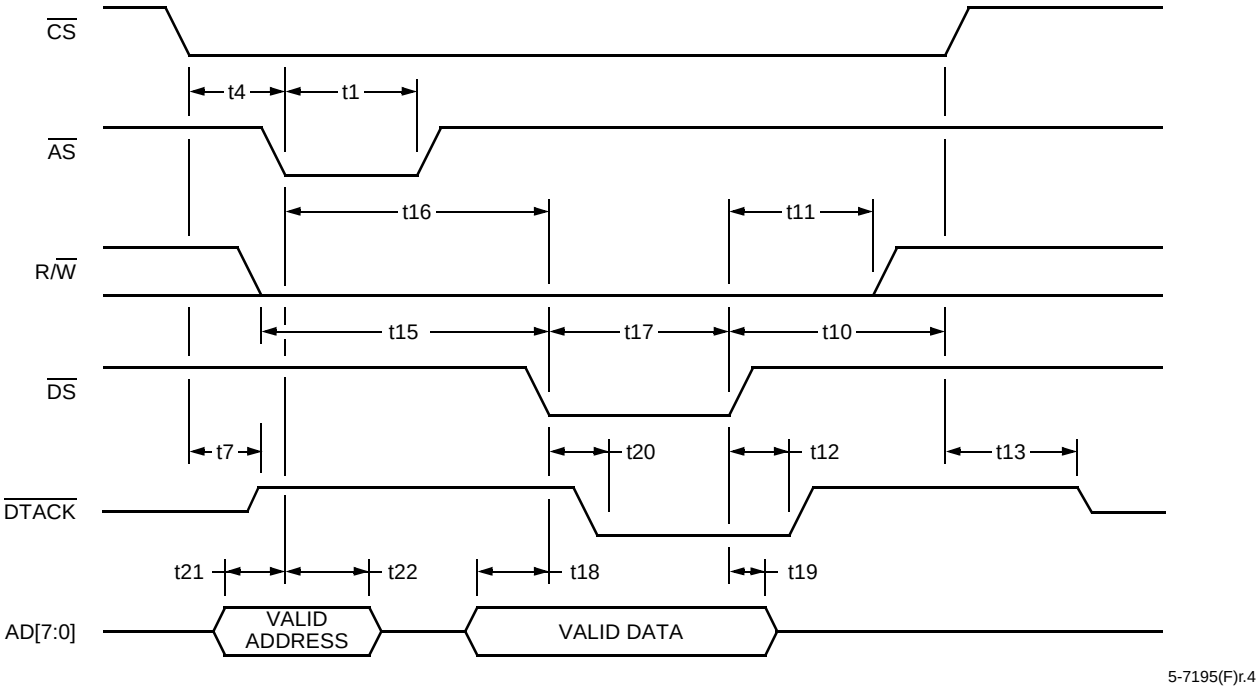
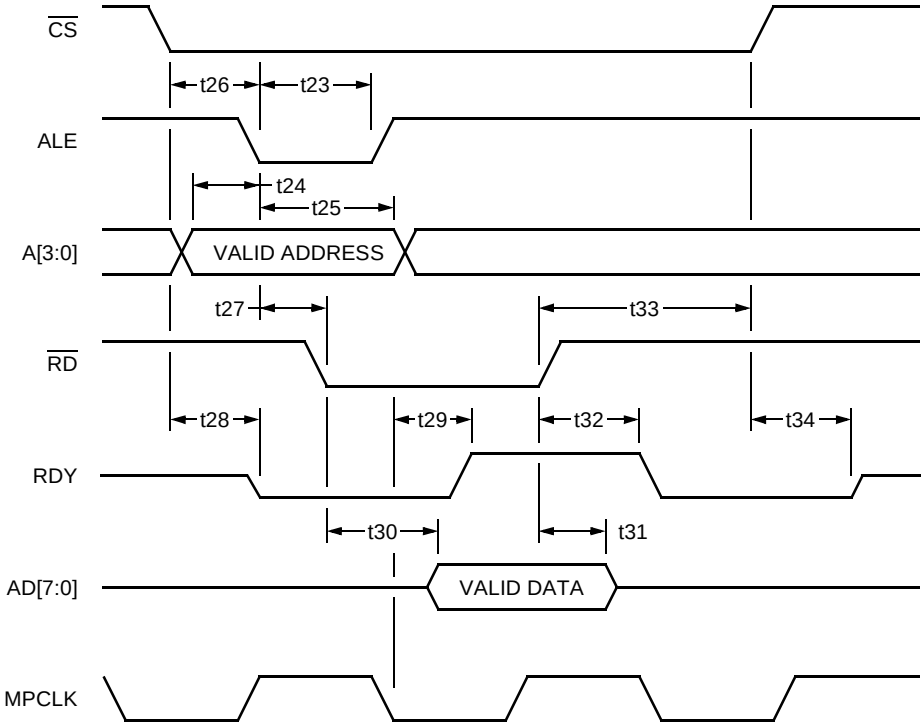



**Figure 28. Mode 2—Write Cycle Timing (MPMODE = 0, MPMUX = 1)**

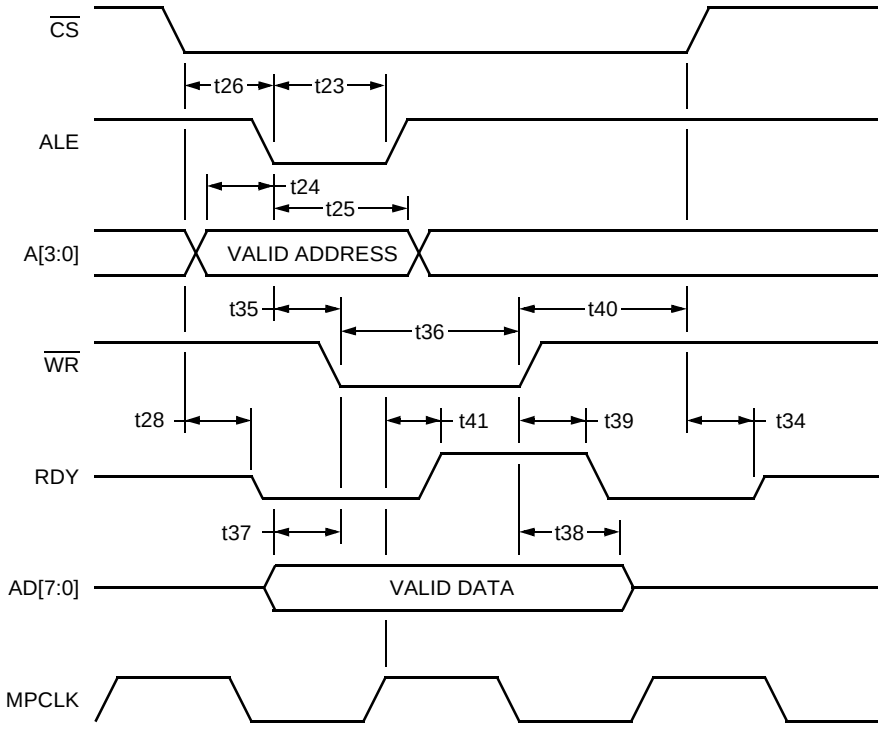
## Timing Characteristics (continued)

### Microprocessor Interface Timing (continued)




5-7196(F)r.3

**Figure 29. Mode 3—Read Cycle Timing (MPMODE = 1, MPMUX = 0)**




5-7197(F)r.3

**Figure 30. Mode 3—Write Cycle Timing (MPMODE = 1, MPMUX = 0)**

## Timing Characteristics (continued)

### Microprocessor Interface Timing (continued)

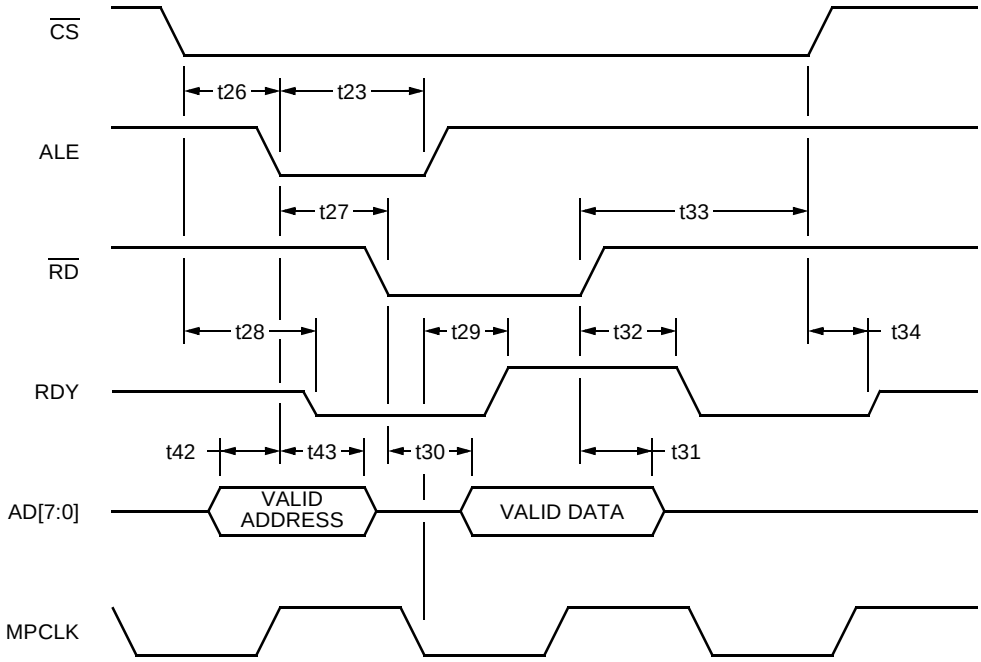



**Figure 31. Mode 4—Read Cycle Timing (MPMODE = 1, MPMUX = 1)**

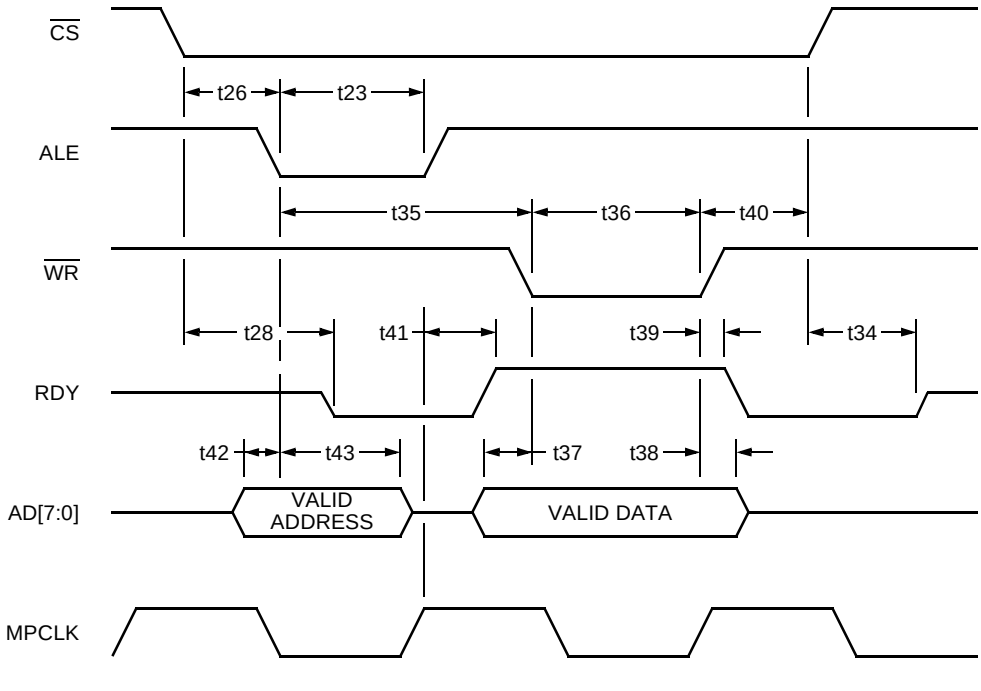



**Figure 32. Mode 4—Write Cycle Timing (MPMODE = 1, MPMUX = 1)**

## Timing Characteristics (continued)

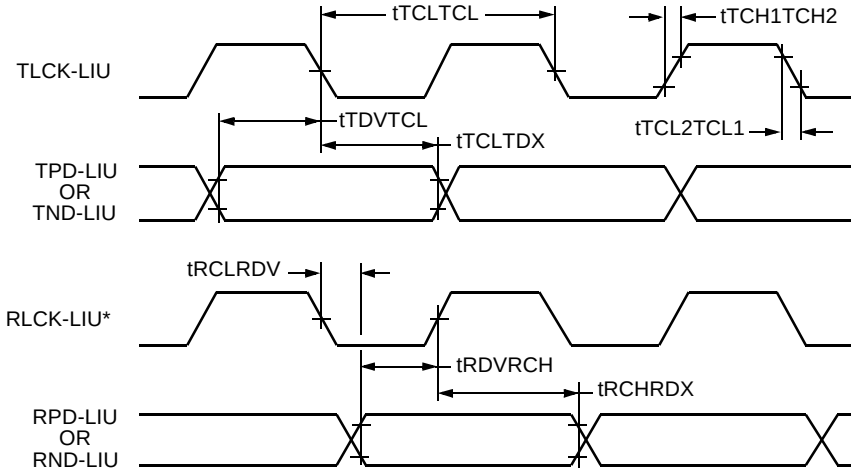
### Data Interface Timing

**Table 119. Data Interface Timing**

**Note:** The digital system interface timing is shown in Figure 33 for ACM = 0. If ACM = 1, then the RCLK signal in Figure 33 will be inverted.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| tTCLTCL | Average TCLK Clock Period:<br>DS1<br>CEPT | <br>—<br>— | <br>647.7<br>488.0 | <br>—<br>— | <br>ns<br>ns |
| tTDC | TCLK Duty Cycle*<br>TCLK Minimum High/Low Time† | 30<br>100 | —<br>— | 70<br>— | %<br>ns |
| tTDVTCL | Transmit Data Setup Time | 50 | — | — | ns |
| tTCLTDX | Transmit Data Hold Time | 40 | — | — | ns |
| tTCH1TCH2 | Clock Rise Time (10%/90%) | — | — | 40 | ns |
| tTCL2TCL1 | Clock Fall Time (90%/10%) | — | — | 40 | ns |
| tRCHRCL | RCLK Duty Cycle | 45 | 50 | 55 | % |
| tRDVRCH | Receive Data Setup Time | 140 | — | — | ns |
| tRCHRDX | Receive Data Hold Time | 180 | — | — | ns |
| tRCLRDV | Receive Propagation Delay | — | — | 40 | ns |

* Refers to each individual bit period for JAT = 0 applications.
† Refers to each individual bit period for JAT = 1 applications using a gapped TCLK.




5-1156(F).br.2

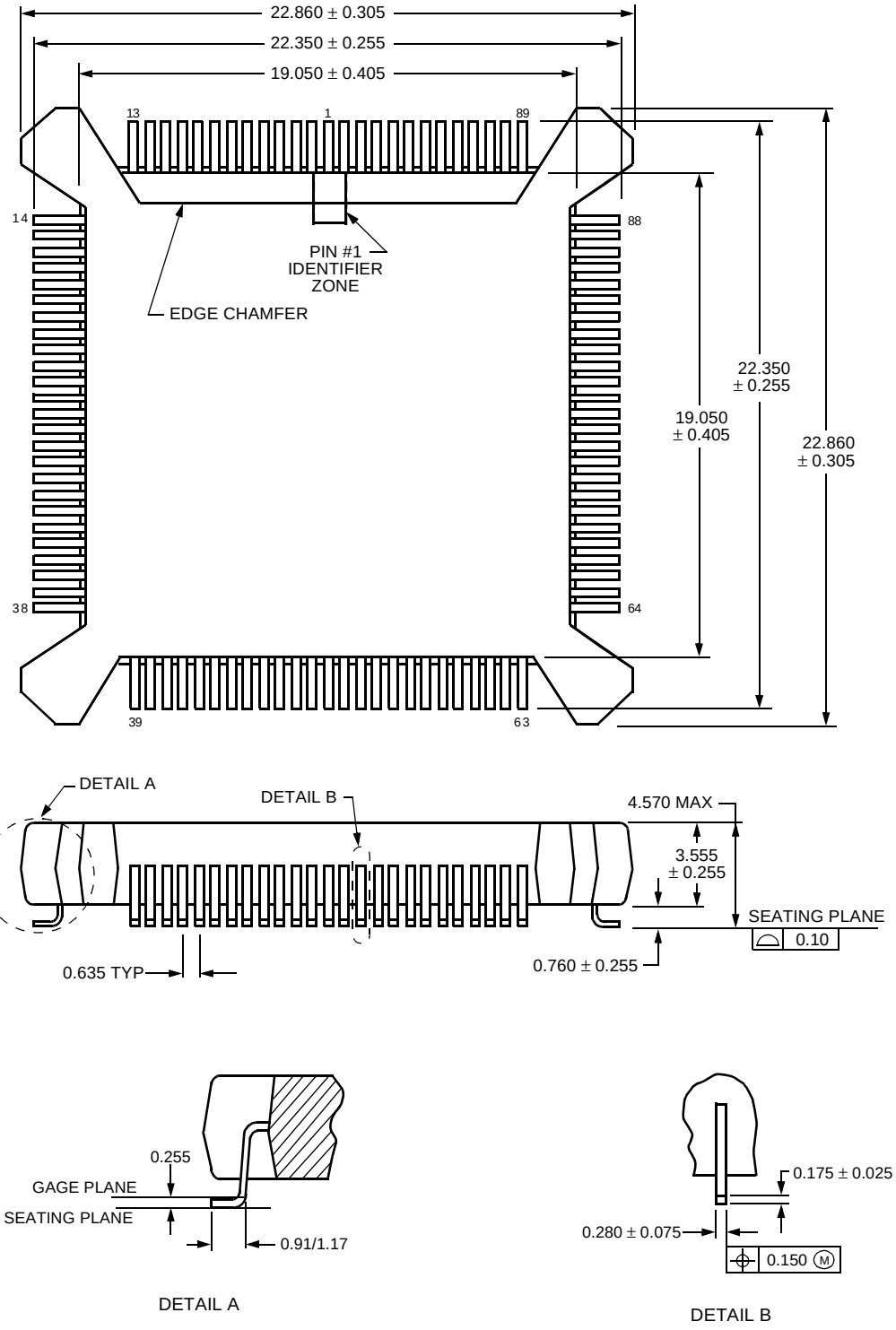
* Invert RCLK for ACM = 1.

**Figure 33. Interface Data Timing (ACM = 0)**

## Outline Diagram

### 100-Pin BQFP

Dimensions are in millimeters.




5-1970(F).r11

## Ordering Information

| Device Code | Package | Temperature | Comcode (Ordering Number) |
|---|---|---|---|
| T-7698---FL3-DB | 100-Pin BQFP | –40 °C to +85 °C | 108347188 |

## DS98-297T1E1 Replaces DS98-228TIC to Incorporate the Following Updates

1. Pages 103—108, Microprocessor Interface Timing section clarified.
2. Pages 45—46, Channel Configuration and Control Registers (0110—1001, 1011, 1100) section updated.
3. Pages 23 and 31, Table 7 and Table 13, Register Map for CODE Bits added in the Line Interface section.
4. Page 99, Primary Line Rate XCLK Reference Clock and Internal Reference Clock Synthesizer section added.

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