CT2500
MIL-STD-1397 Type D & E Low Level Serial Interface Protocol Chip

Features

- **Performs Source and Sink functions**
- **Implements Type D & E protocols**
- **Burst Mode Capability**
- **Built in System Integrity Features**
- **Double Buffered Communications**
- **Low power CMOS**
- **Available in a PGA Package**
- **Operates over full Military temperature range -55°C to +125°C**

AEROFLEX CIRCUIT TECHNOLOGY
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General Description

The CT2500 provides a complete interface between the MIL-STD-1397 transceiver chip set (CT1698) and most microprocessor based systems. The unit is monolithic and fabricated in CMOS technology, thereby having very low power requirements. The unit handles all protocols of Type D & E interfaces including Burst Mode Data and forced EF functions. Screened per individual test methods of MIL-STD-883. Aeroflex Circuit Technology is an 80,000ft^2 MIL-PRF-38534 certified facility in Plainview, N.Y.

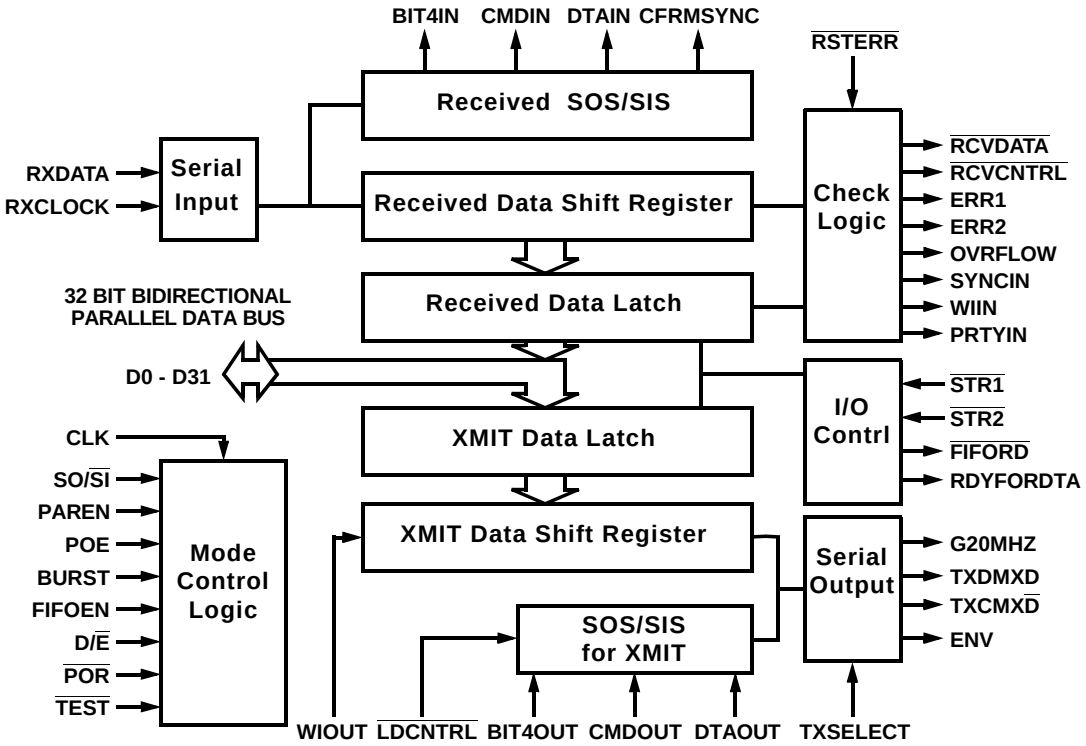


Figure 1 – Block Diagram

I/O CONTROL

The CT2500 is very flexible in it's I/O architecture. The unit can handle 16 bit and 32 bit data and command word loading. In addition, data words can be preloaded into an external FIFO and the unit will load data words from the FIFO directly without subsystem intervention. Similarly, data can be received and automatically loaded into a FIFO. This frees up the subsystem until the data transfer is complete. These options are desirable especially when operating under burst mode transmissions. Control frames are sent by strobing LDCNTRL and data is sent by strobing STR2.

DATA TRANSFERS

The CT2500 is built to send and receive Type D and E Control frames. It can transmit and receive 32-bit command and data word. All 32-bit communications are double buffered for maximum flexibility. This allows the subsystem to respond with less critical timing constraints. Burst mode data transmission can be initiated by setting the "Burst Mode" pin high. Automatic FIFO operation is enabled by setting "FIFOEN" pin high. The serial data out is automatically formatted for the CT1698 to send out along the cable.

SOURCE AND SINK MODES

Both Source and Sink Mode operations are available in the CT2500. Selection of modes is accomplished through the Source/Sink pin. In the Source Mode, the unit will transmit control frames, 32 bit command and data words including burst mode data. It will receive control frames only. In Sink Mode, the unit will transmit control frames only and receive control frames, 32 bit command and data words, and burst mode data.

SYSTEM INTEGRITY FEATURES

The CT2500 has built in system integrity features. The unit can generate and send parity with all 32 bit transmissions. For reception of 32 bit words, the unit can check for parity, frame, overrun, sync, and bit count errors.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±10%, T_C = -55 °C to +125°C, unless otherwise specified)

SYMBOL	PARAMETER	LIMIT
I_{DD}	Quiescent current	100uA max
P_{DS}	Power Dissipation	200mW max
Iin	Input leakage	10uA max
Ioz	Tri-state leakage	10uA max
V_{IH}	Input high level	2.0V min
V_{IL}	Input low level	0.8V max
V_{OH}	Output high level	2.4V min @ I_{OH} = -4mA
V_{OL}	Output low level	0.4V max @ I_{OL} = 4mA

I/O FUNCTION LISTING

NAME	I/O	DESCRIPTION
SO/$\overline{SI}$	**I**	**Source / Sink Mode Select** Determines the overall Functioning Mode of the Device. "1"= Source emulation. This mode enables the chip to send control frames, single command and data words and burst data. It is able to receive control frames. "0" = Sink emulation. In this mode, the chip can only send control frames. It can receive control frames, command words, single data words and burst data.
DO-D31	**I/O**	**Parallel Bi-directional Data Bus (Internal Pullups)** *Source Mode*: Input to 32 bit transmit data latch *Sink Mode*: Tri-state output from 32 bit received data latch
D/$\overline{E}$	**I**	**Type D / Type E Control Frame Length Select (Internal Pulldown)** "1" = Three bit control frames are transmitted and the received control frame is checked for a proper three bit length. "0" = Four bit control frames are transmitted and the received control frame is checked for a proper four bit length.
PAREN	**I**	**Parity Enable (Internal Pullup)** "1" = Parity bit is generated in Source mode and checked for in Sink mode. "0" = No parity is generated or checked for.
POE	**I**	**Parity Odd or Even Select (Internal Pullup)** "1" = Odd parity "0" = Even parity
CLK	**I**	**System Clock** 20 megahertz with 50% duty cycle
BURST	**I**	**Burst Mode Select** "1" = Data transmission and Reception can be done in Burst mode "0" = Normal operation *Source Mode*: Data words loaded during the transmission of another will be concatenated to the transmission without addition of SYNC or WI bits. The first word will have a SYNC bit of "1" and and a WI bit, which must be set to "0". The Burst line must remain stable for the entire duration of the loading and transmission of the data. *Sink Mode*: During a Burst data reception, after the SYNC and WI bits, data words are picked off at bit count multiples of 32, or 33 with parity enabled, and loaded into the output latch. The transmission is considered ended when a gap is detected. The line must be stable during the entire reception.
$\overline{STR1}$ and $\overline{STR2}$	**I**	**Strobe One Bar and Strobe Two Bar** Control Strobes for Reading and Writing the Parallel I/O data Latches *Source Mode*: $\overline{STR1}$ loads data present on DO-D15 into the lower 16 bit input latch and $\overline{STR2}$ loads data on D16-D31 into the upper 16 bit input latch. Upon completion of $\overline{STR2}$, a sequence is initiated to load the entire 32 bits into a shift register and start a transmission. The lower 16 bits must be loaded prior to or during the load of the upper 16 bits. For a 32 bit load, $\overline{STR1}$ and $\overline{STR2}$ can be tied together. *Sink Mode*: $\overline{STR1}$ enables the lower 16 bits of a received word to be output on D0-D15. $\overline{STR2}$ enables the upper 16 bits of a received word to be output on D16-D31. The entire 32 bits of data must be read before another data reception or it will be overwritten. If this occurs, the overflow flag, OVRFLOW, will go high. The data is considered completely read upon the completion of $\overline{STR2}$.
CMDIN	**O**	**Command In** Third bit of the Received Control Frame. Valid during $\overline{RCVCNTRL}$.
DTAIN	**O**	**Data In** Second bit of the Received Control Frame. Valid during $\overline{RCVCNTRL}$.

I/O FUNCTION LISTING (Continued)

NAME	I/O	DESCRIPTION
$\overline{\text{RCVCNTRL}}$	**O**	**Received Control Bar** Pulses low upon reception of a Control Frame in both Sink and Source modes.
$\overline{\text{RCVDTA}}$	**O**	**Received Data/Command Word Bar** Pulses low upon reception of a Data or Command word
ERR1, ERR2	**O**	**Error Bit One and Error Bit Two** ERR1 ERR2 0 0 No Error 0 1 Bit Count Error in Received Data/Command word or Control Frame 1 0 Parity Error in Received Data 1 1 Sync Error in Received Data/Command word or Control Frame
OVRFLOW	**O**	**Overflow Error** "1" = Overflow occurred in the Received Data Latch. Data not read in time.
$\overline{\text{RSTERR}}$	**I**	**Reset Error Flags Bar (Internal Pullup)** A low pulse on this line resets the ERR1, ERR2 and OVRFLOW error flags.
$\overline{\text{POR}}$	**I**	**Power on Reset Bar** A Master reset. A low pulse on this line resets the internal sequences and error flags. It does not reset the I/O Data latches.
WIOUT	**I**	**Word Identifier Bit Out** The value on this line is latched during $\overline{\text{STR2}}$ for the WI bit position in the word to be transmitted. A "0" indicates a Data word and a "1" indicates a Command/Interrupt word.
WIIN	**O**	**Word Identifier Bit In** The WI bit of the received word is present on this line during $\overline{\text{RCVDTA}}$ and indicates whether the word is a Data word or a Command/Interrupt word. The value is latched at the first $\overline{\text{RCVDTA}}$ for an entire Burst Mode reception.
CMDOUT	**I**	**Command Out** Third bit of the transmitted Control Frame.
DTAOUT	**I**	**Data Out** Second bit of the transmitted Control Frame.
$\overline{\text{LDCNTRL}}$	**I**	**Load Control Frame Bar** This loads the status of CMDOUT, DTAOUT and BIT4OUT into the Control Frame to be transmitted. Transmission will commence when the loading is completed. This applies to both Sink and Source modes.
FIFOEN	**I**	**FIFO Enable** *Source Mode*: When FIFOEN is held high ("1"), $\overline{\text{FIFORD}}$'s (FIFO Read Bars) will be generated when the input data latch is empty (RDYFORDTA = 1). During the $\overline{\text{FIFORD}}$, data presented to the parallel bus will be loaded into the input data latch and transmitted when ready. In a non-burst (single word) condition, FIFOEN must be removed before RDYFORDTA comes back. A positive pulse of 100 ns duration satisfies this requirement. *Sink Mode*: The parallel data bus goes active during $\overline{\text{RCVDTA}}$ and will hold for approximately 25 ns after its rising edge. With a FIFO directly connected to the data bus, $\overline{\text{RCVDTA}}$ can be used to load all received words into the FIFO. Gating $\overline{\text{RCVDTA}}$ with WIIN selects only the data words for loading.

I/O FUNCTION LISTING (Continued)

NAME	I/O	DESCRIPTION
$\overline{\text{FIFORD}}$	**O**	**FIFO Read Bar** When the device is configured as a Source, this output pulses low during FIFOEN mode enabling data from a FIFO to be loaded into the input data latch for transmission.
RDYFORDTA	**O**	**Ready For Data** This signal is high when the input data latch is available for new data to be loaded in. When the data is loaded, RDYFORDTA goes low until the word is dumped into the output shift register.
ENV	**O**	**Envelope** This output envelopes the serial output data by being high during transmission.
TXDMXD	**O**	**Transmit Data / Manchester Data** Serial NRZ data out or Manchester Data out depending on the TXSELECT mode.
TXCMX$\overline{\text{D}}$	**O**	**Transmit Clock / Manchester Data Bar** Output shift clock or Manchester Data Bar depending on the TXSELECT mode.
G20MHZ	**O**	**Gated 20 Mhz** A gated 20 Mhz clock used in conjunction with Transmit Data, Transmit Clock and Envelope to generate Manchester data using other Aeroflex encoders such as the CT1698.
TXSELECT	**I**	**Transmit Mode Select. (Internal Pulldown)** "1" = Serial output format is Manchester Data and Data Bar. "0" = Output will be NRZ Data and Shift Clock.
RXDATA	**I**	**Received Data** Received serial NRZ Data in.
RXCLOCK	**I**	**Received Clock** Received Shift Clock In.
$\overline{\text{TEST}}$	**I**	**Test Mode Bar (Internal Pullup)** A low on this pin puts the device into an internal wrap-around test mode. Transmit Data and Transmit Clock are internally connected to Received Data and Received Clock. The circuit must be in Source mode and only 32 bit data loads and reads are allowed. In this mode, STR2 loads the full 32 bits for transmission. When this word is wrapped back, RCVDTA will pulse low indicating reception of a data or command word. STR1 enables the received data latch to be read out. Transmission of control frames can also be tested in this mode using the regular LDCNTRL and RCVCNTRL signals.
BIT4IN	**O**	**Bit Four In** Fourth bit of received Type E control frame.
BIT4OUT	**I**	**Bit Four Out (Internal Pullup)** Fourth bit of Type E control frame to be transmitted.
SYNCIN	**O**	**Sync In** Sync position of the Received Data Latch.
CFRMSYNC	**O**	**Control Frame Sync In** Sync position of the Received Control Frame Latch
PRTYIN	**O**	**Parity In** Parity bit position of the Received Data Latch.

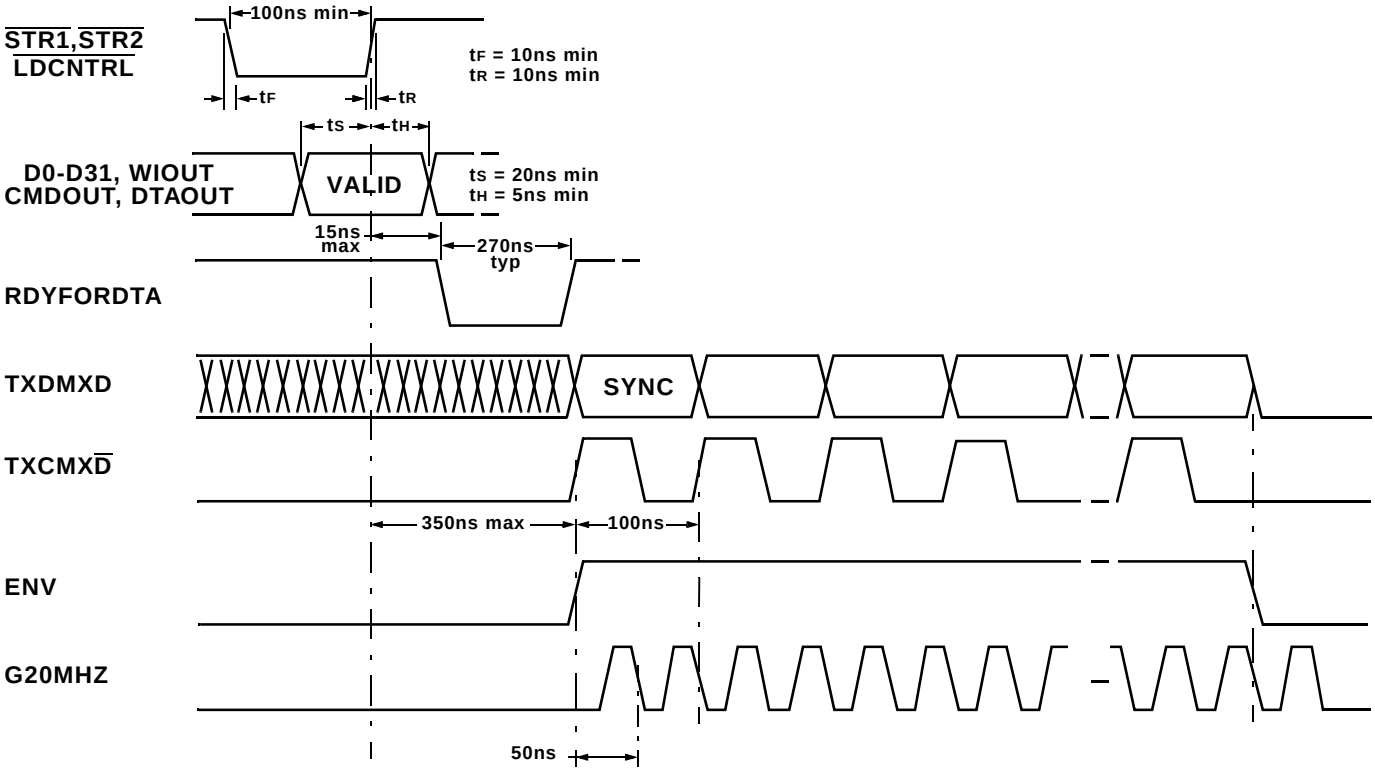


Figure 2 – Transmit Timing Diagram

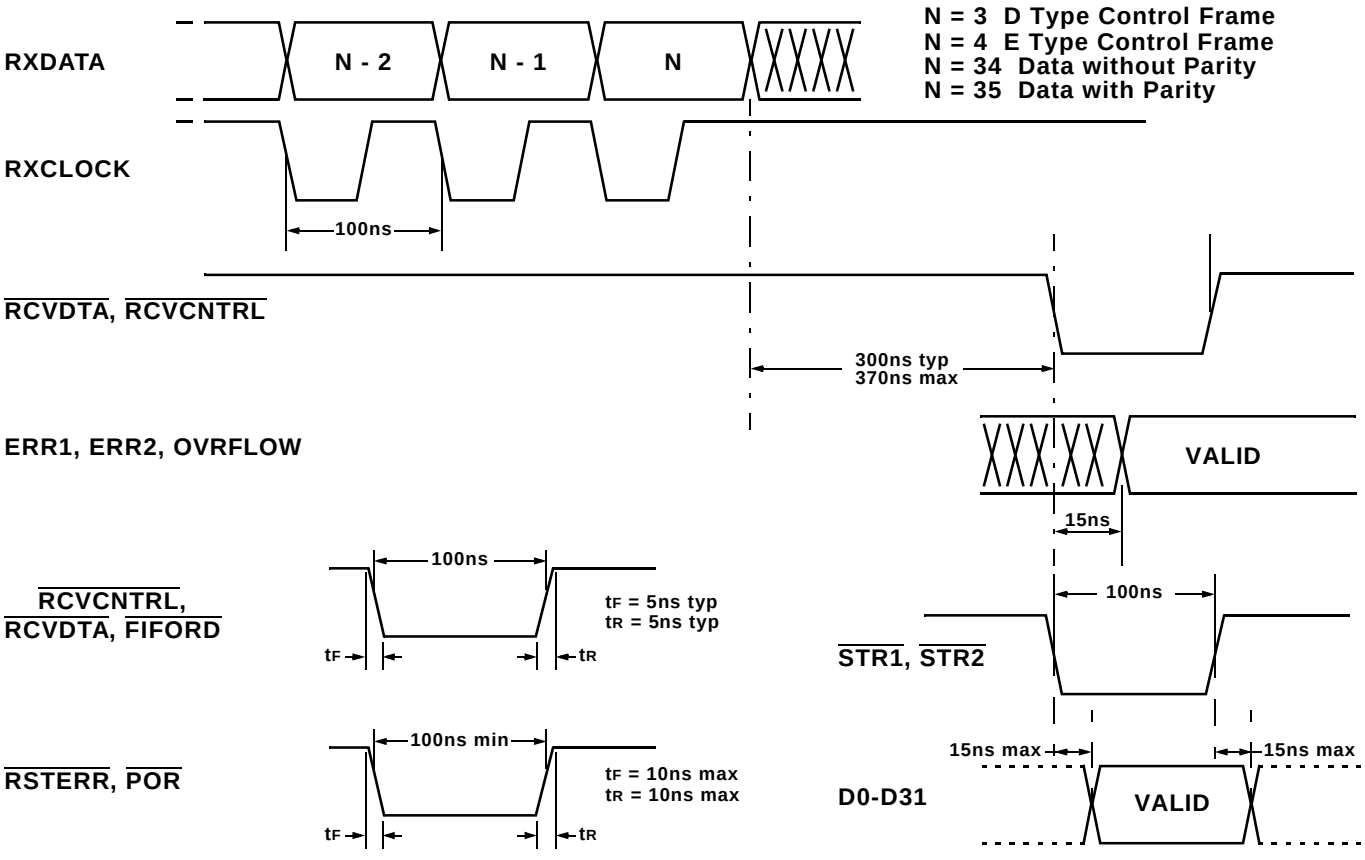


Figure 3 – Receive Timing Diagram

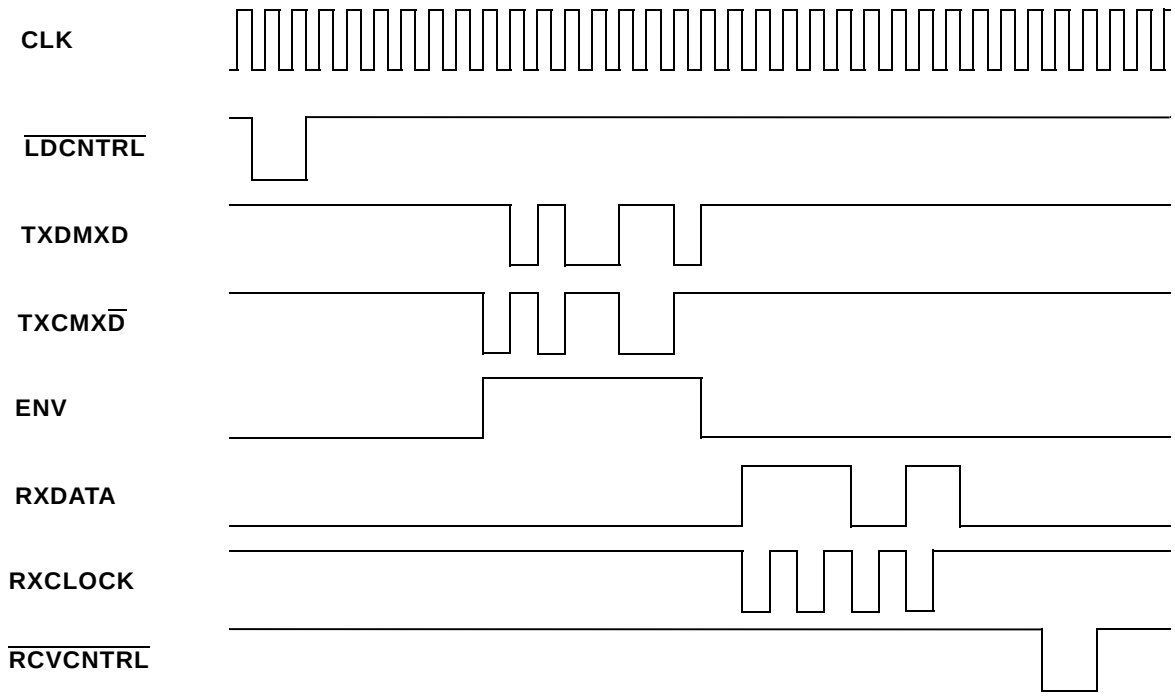


Figure 4 – Control Frame Transfer Diagram

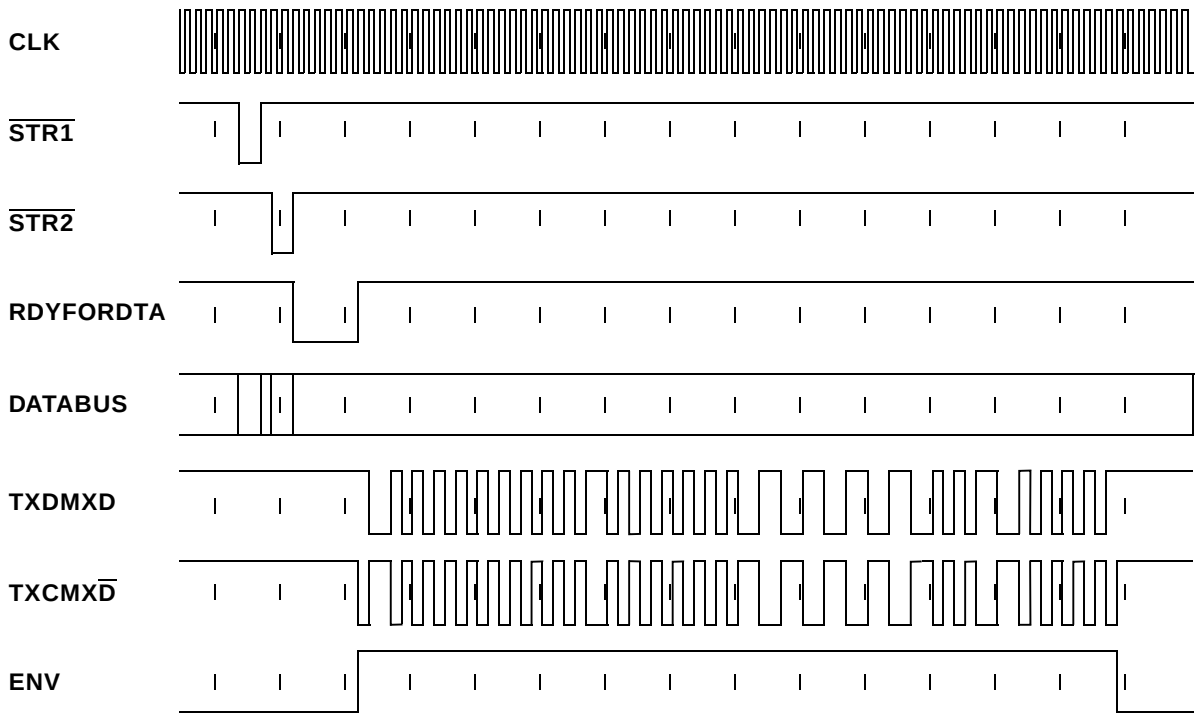


Figure 5 – Source Data Frame Example Diagram

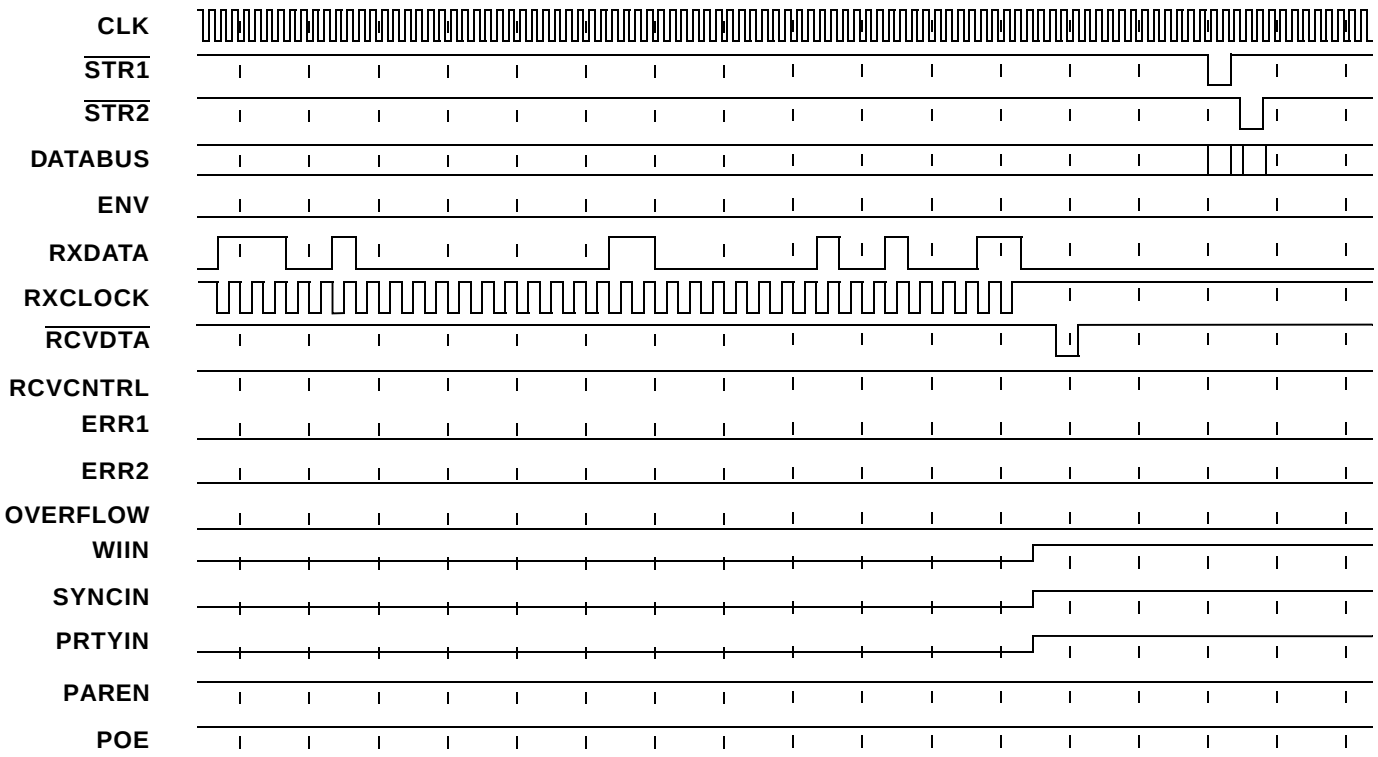


Figure 6 – Sink Data Frame Example Diagram

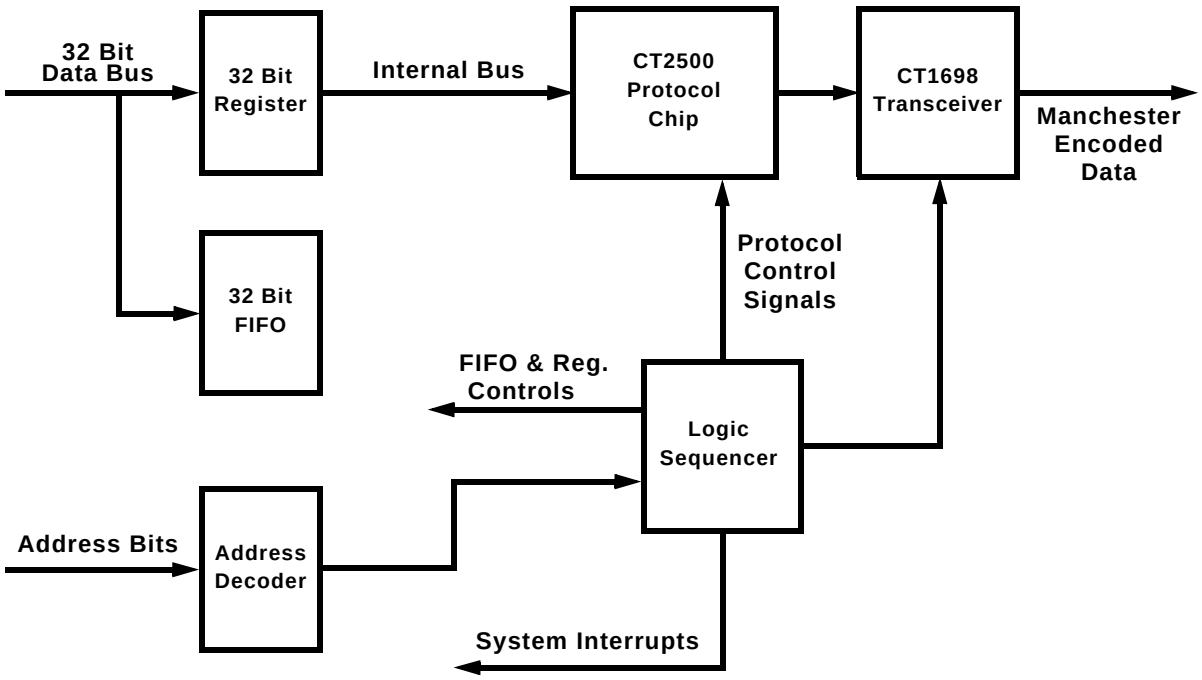


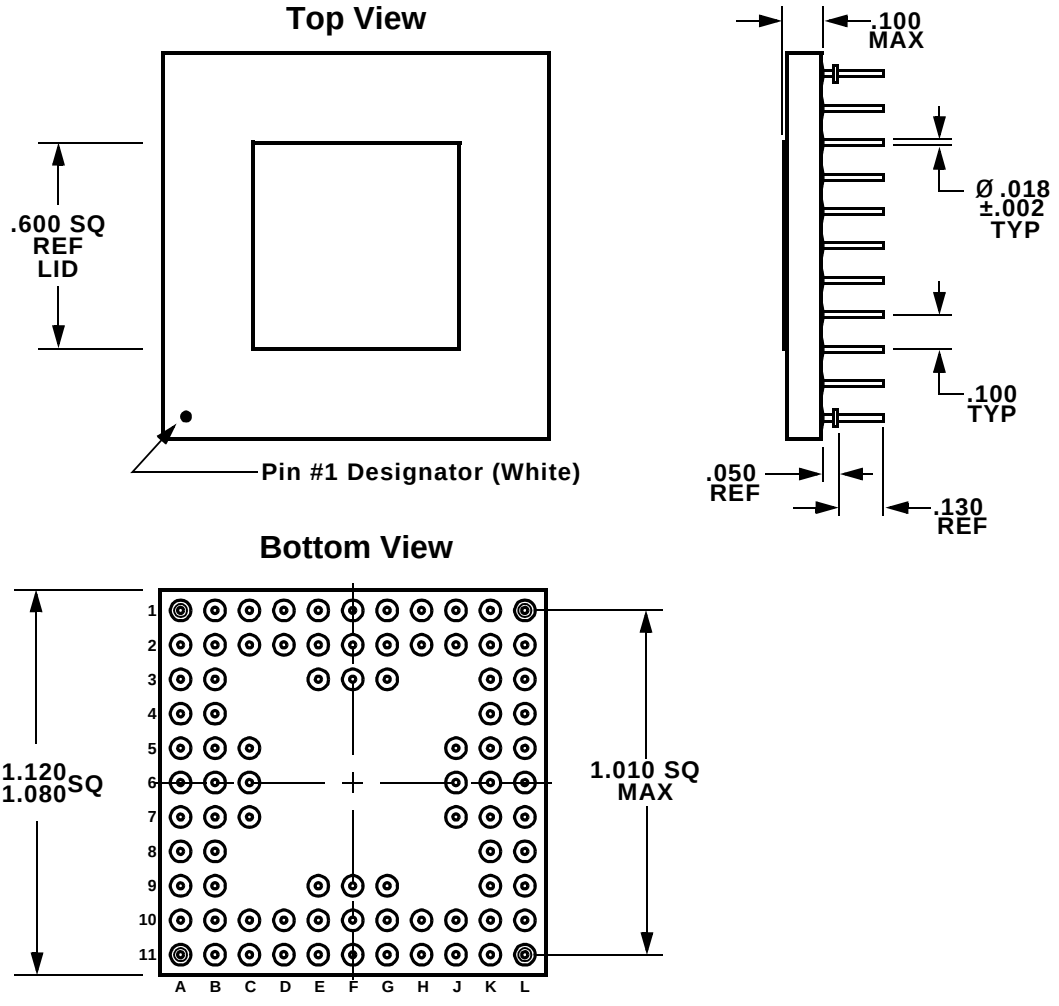
Figure 7 – Typical I/O Board Configuration (Source and Sink Mode)

PIN OUTS – 84 PIN PGA (CT2500)			
Pin	**Signal**	**Pin**	**Signal**
B2	BURST	K10	GND
C2	CLK	J10	POE
B1	CMDOUT	K11	D15
C1	DTAOUT	J11	D14
D2	BIT4OUT	H10	D13
D1	$\overline{\text{RSTERR}}$	H11	D12
E3	FIFOEN	F10	D11
E2	$\overline{\text{LDCNTRL}}$	G10	D10
E1	$\overline{\text{POR}}$	G11	D9
F2	GND	G9	GND
F3	GND	F9	GND
G3	SYNCIN	F11	D8
G1	RXCLOCK	E11	D7
G2	RXDATA	E10	D6
F1	SO/$\overline{\text{SI}}$	E9	D5
H1	$\overline{\text{STR1}}$	D11	D4
H2	$\overline{\text{STR2}}$	D10	D3
J1	$\overline{\text{TEST}}$	C11	D2
K1	WIOUT	B11	D1
J2	D31	C10	PRTYIN
L1	CFRMSYNC	A11	V_{DD}
K2	V_{DD}	B10	V_{DD}
K3	PAREN	B9	D/$\overline{\text{E}}$
L2	D30	A10	D0
L3	D29	A9	CMDIN
K4	D28	B8	DTAIN
L4	D27	A8	ENV
J5	D26	B6	ERR1
K5	D25	B7	ERR2
L5	D24	A7	$\overline{\text{FIFORD}}$
K6	BIT4IN	C7	V_{DD}
J6	V_{DD}	C6	V_{DD}
J7	V_{DD}	A6	TXSELECT
L7	D23	A5	OVRFLOW
K7	D22	B5	$\overline{\text{RCVCNTRL}}$
L6	D21	C5	$\overline{\text{RCVDTA}}$
L8	D20	A4	RDYFORDTA
K8	D19	B4	TXCMX$\overline{\text{D}}$
L9	D18	A3	TXDMXD
L10	D17	A2	WIIN
K9	D16	B3	G20MHZ
L11	GND	A1	GND

Ordering Information

Model Number	Package
CT2500	PGA Package

Package Outline – 84 Pin PGA



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