Continuous Rate 12.3 Mb/s to 1.25 Gb/s Clock and Data Recovery IC

Preliminary Technical Data

ADN2815

FEATURES

Serial data input: 12.3 Mb/s to 1.25 Gb/s
Exceeds SONET requirements for jitter transfer/ generation/tolerance
Patented clock recovery architecture
No reference clock required
Loss of lock indicator
I²C™ interface to access optional features
Single-supply operation: 3.3 V
Low power: 300 mW typical
5 mm × 5 mm 32-lead LFCSP

APPLICATIONS

SONET OC-1/3/12 and all associated FEC rates
Fibre Channel, GbE, HDTV, etc.
WDM transponders
Regenerators/repeaters
Test equipment
Broadband cross-connects and routers

PRODUCT DESCRIPTION

The ADN2815 provides the receiver functions of quantization and clock and data recovery for continuous data rates from 12.3 Mb/s to 1.25 Gb/s. The ADN2815 automatically locks to all data rates without the need for an external reference clock or programming. All SONET jitter requirements are met, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for −40°C to +85°C ambient temperature, unless otherwise noted.

The ADN2815 is available in a compact 5 mm × 5 mm 32-lead chip scale package.

FUNCTIONAL BLOCK DIAGRAM

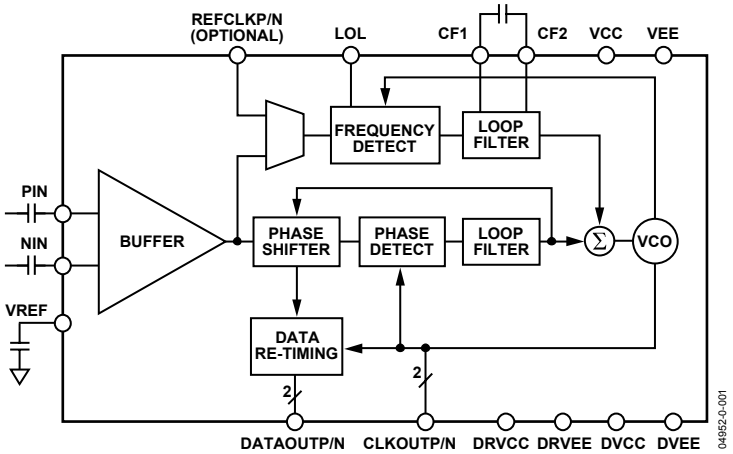

Figure 1.

Rev. PrA

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REVISION HISTORY

6/04—Revision PrA: Initial Version

SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, Input Data Pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
QUANTIZER—DC CHARACTERISTICS					
Input Voltage Range	@ PIN or NIN, dc-coupled	1.8		2.8	V
Peak-to-Peak Differential Input	PIN – NIN	0.2		2.0	V
Input Common Mode Level	DC-coupled	2.3	2.5	2.8	V
QUANTIZER—AC CHARACTERISTICS					
Data Rate		12.3		1250	Mb/s
S11	@ 2.5 GHz		−15		dB
Input Resistance	Differential		100		Ω
Input Capacitance			0.65		pF
LOSS OF LOCK DETECT (LOL)					
VCO Frequency Error for LOL Assert	With respect to nominal		1000		ppm
VCO Frequency Error for LOL De-Assert	With respect to nominal		250		ppm
LOL Response Time	12.3 Mb/s		4		ms
	OC-12		1.0		µs
	GbE		1.0		µs
ACQUISITION TIME					
Lock to Data Mode	1GbE		1.5		ms
	OC-12		2.0		ms
	OC-3		3.4		ms
	OC-1		9.8		ms
	12.3 Mb/s		40.0		ms
Optional Lock to REFCLK Mode			10.0		ms
DATA RATE READBACK ACCURACY					
Coarse Readback	(See Table 13)		10		%
Fine Readback	In addition to REFCLK accuracy				
	Data rate ≤ 20 Mb/s			200	ppm
	Data rate > 20 Mb/s			100	ppm
POWER SUPPLY VOLTAGE		3.0	3.3	3.6	V
POWER SUPPLY CURRENT			90		mA
OPERATING TEMPERATURE RANGE		−40		+85	°C

JITTER SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 uF, SLICEP = SLICEN = VEE, Input Data Pattern: PRBS $2^{23} - 1$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
PHASE-LOCKED LOOP CHARACTERISTICS					
Jitter Transfer BW	OC-12		71	108	kHz
	OC-3		23	35	kHz
Jitter Peaking	OC-12		0	0.03	dB
	OC-3		0	0.03	dB
Jitter Generation	OC-12, 12 kHz to 5 MHz		0.001	0.002	UI rms
			0.01	0.019	UI p-p
	OC-3, 12 kHz to 1.3 MHz		0.001	0.002	UI rms
			0.01	0.011	UI p-p
Jitter Tolerance	1GbE, IEEE802.3				
	637kHz	0.749			UI p-p
	OC-12, $2^{23} - 1$ PRBS				
	30 Hz[1]	100			UI p-p
	300 Hz[1]	44			UI p-p
	25 kHz	2.5			UI p-p
	250 kHz[1]	1.0			UI p-p
	OC-3, $2^{23} - 1$ PRBS				
	30 Hz[1]	50			UI p-p
	300 Hz[1]	24			UI p-p
	6500 Hz	3.5			UI p-p
	65 kHz	1.0			UI p-p

[1] Jitter tolerance of the ADN2815 at these jitter frequencies is better than what the test equipment is able to measure.

OUTPUT AND TIMING SPECIFICATIONS

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
LVDS OUPUT CHARACTERISTICS					
(CLKOUTP/N, DATAOUTP/N)					
Single-Ended Output Swing	V_{SE} (see Figure 3)	250		400	mV
Differential Output Swing	V_{DIFF} (see Figure 3)	500		800	mV
Output Offset Voltage		1125	1200	1275	mV
Output Impedance	Differential		100		Ω
LVDS Ouputs Timing					
Rise Time	20% to 80%		TBD		ps
Fall Time	80% to 20%		TBD		ps
Setup Time	T_S (see Figure 2), GbE		400		ps
Hold Time	T_H (see Figure 2), GbE		400		ps
I^2C INTERFACE DC CHARACTERISTICS	LVCMOS				
Input High Voltage	V_{IH}	0.7 VCC			V
Input Low Voltage	V_{IL}			0.3 VCC	V
Input Current	V_{IN} = 0.1 VCC or V_{IN} = 0.9 VCC	−10.0		+10.0	µA
Output Low Voltage	V_{OL}, I_{OL} = 3.0 mA			0.4	V
I^2C INTERFACE TIMING	(See Figure 9)				
SCK Clock Frequency				400	kHz
SCK Pulse Width High	t_{HIGH}	600			ns
SCK Pulse Width Low	t_{LOW}	1300			ns
Start Condition Hold Time	$t_{HD;STA}$	600			ns
Start Condition Setup Time	$t_{SU;STA}$	600			ns
Data Setup Time	$t_{SU;DAT}$	100			ns
Data Hold Time	$t_{HD;DAT}$	300			ns
SCK/SDA Rise/Fall Time	T_R/T_F	20 + 0.1 Cb[1]		300	ns
Stop Condition Setup Time	$t_{SU;STO}$	600			ns
Bus Free Time between a Stop and a Start	t_{BUF}	1300			ns
REFCLK CHARACTERISTICS	Optional lock to REFCLK mode				
Input Voltage Range	@ REFCLKP or REFCLKN				
	V_{IL}		0		V
	V_{IH}		VCC		V
Minimum Differential Input Drive			100		mV p-p
Reference Frequency		12.3		200	MHz
Required Accuracy			100		ppm
LVTTL DC INPUT CHARACTERISTICS					
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
Input High Current	I_{IH}, V_{IN} = 2.4 V			5	µA
Input Low Current	I_{IL}, V_{IN} = 0.4 V	−5			µA
LVTTL DC OUTPUT CHARACTERISTICS					
Output High Voltage	V_{OH}, I_{OH} = −2.0 mA	2.4			V
Output Low Voltage	V_{OL}, I_{OL} = 2.0 mA			0.4	V

[1] Cb = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.

ABSOLUTE MAXIMUM RATINGS

$T_A = T_{MIN}$ to T_{MAX}, VCC = V_{MIN} to V_{MAX}, VEE = 0 V, C_F = 0.47 µF, SLICEP = SLICEN = VEE, unless otherwise noted.

Table 4.

Parameter	Rating
Supply Voltage (VCC)	4.2 V
Minimum Input Voltage (All Inputs)	VEE – 0.4 V
Maximum Input Voltage (All Inputs)	VCC + 0.4 V
Maximum Junction Temperature	125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering 10 s)	300°C

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance

32-LFCSP, 4-layer board with exposed paddle soldered to VEE θ_{JA} = 28°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING CHARACTERISTICS

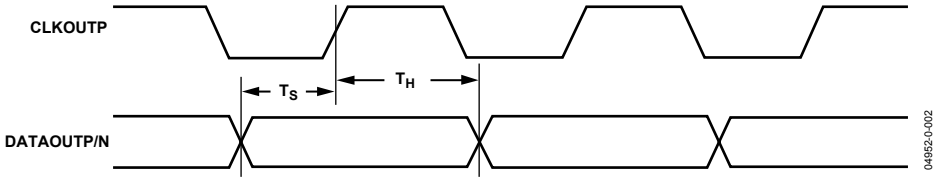


Figure 2. Output Timing

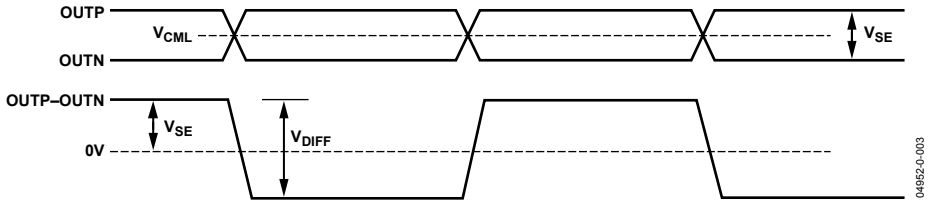


Figure 3. Single-Ended vs. Differential Output Specifications

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

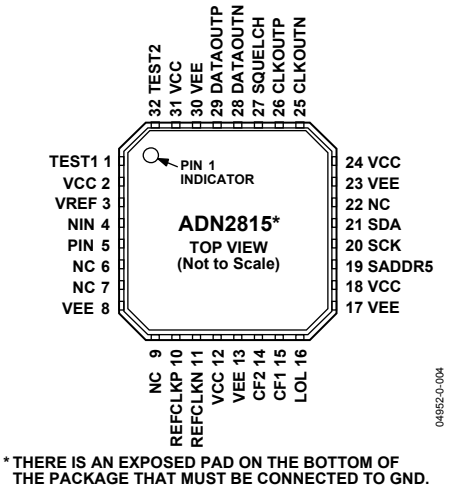


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	TEST1		Connect to VCC.
2	VCC	P	Power for Limamp, LOS.
3	VREF	AO	Internal VREF Voltage. Decouple to GND with a 0.1 µF capacitor.
4	NIN	AI	Differential Data Input. CML.
5	PIN	AI	Differential Data Input. CML.
6 ,7	NC		No Connect
8	VEE	P	GND for Limamp, LOS.
9	NC		No Connect
10	REFCLKP	DI	Differential REFCLK Input. 12.3 MHz to 200 MHz.
11	REFCLKN	DI	Differential REFCLK Input. 12.3 MHz to 200 MHz.
12	VCC	P	VCO Power.
13	VEE	P	VCO GND.
14	CF2	AO	Frequency Loop Capacitor.
15	CF1	AO	Frequency Loop Capacitor.
16	LOL	DO	Loss of Lock Indicator. LVTTL active high.
17	VEE	P	FLL Detector GND.
18	VCC	P	FLL Detector Power.
19	SADDR5	DI	Slave Address Bit 5.
20	SCK	DI	I^2C Clock Input.
21	SDA	DI	I^2C Data Input.
22	NC		No Connect
23	VEE	P	Output Buffer, I^2C GND.
24	VCC	P	Output Buffer, I^2C Power.
25	CLKOUTN	DO	Differential Recovered Clock Output. LVDS.
26	CLKOUTP	DO	Differential Recovered Clock Output. LVDS.
27	SQUELCH	DI	Disable Clock and Data Outputs. Active high. LVTLL.
28	DATAOUTN	DO	Differential Recovered Data Output. LVDS.
29	DATAOUTP	DO	Differential Recovered Data Output. LVDS.
30	VEE	P	Phase Detector, Phase Shifter GND.
31	VCC	P	Phase Detector, Phase Shifter Power.
32	TEST2		Connect to VCC.
Exposed Pad	Pad	P	Connect to GND

[1]Type: P = power, AI = analog input, AO = analog output, DI = digital input, DO = digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

I²C INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

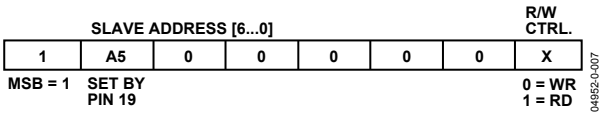


Figure 5. Slave Address Configuration

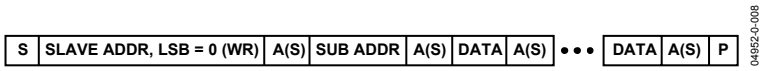


Figure 6. I²C Write Data Transfer

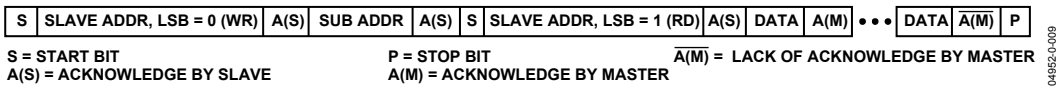


Figure 7. I²C Read Data Transfer

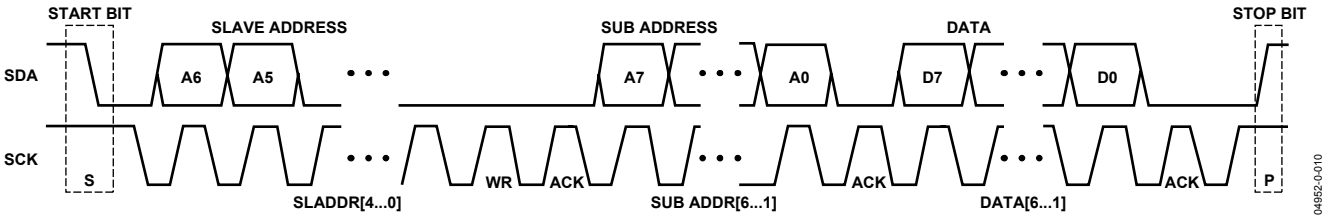


Figure 8. I²C Data Transfer Timing

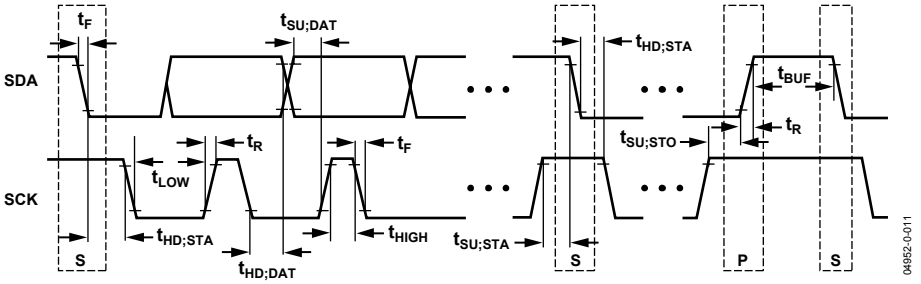


Figure 9. I²C Port Timing Diagram

Table 6. Internal Register Map[1]

Reg Name	R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0
FREQ0	R	0x0	MSB							LSB
FREQ1	R	0x1	MSB							LSB
FREQ2	R	0x2	0	MSB						LSB
RATE	R	0x3	COARSE_RD[8] MSB			Coarse datarate readback				COARSE_RD[1]
MISC	R	0x4	x	x	x	Static LOL	LOL status	Datarate measure complete	x	COARSE_ RD[0] LSB
CTRLA	W	0x8	F_{REF} range			Datarate/DIV_F_{REF} ratio			Measure datarate	Lock to reference
CTRLB	W	0x9	Config LOL	Reset MISC[4]	System reset	0	Reset MISC[2]	0	0	0
CTRLC	W	0x11	0	0	0	0	0	0	Squelch mode	0

[1] All writeable registers default to 0x00.

Table 7. Miscellaneous Register, MISC

			Static LOL	LOL Status	Datarate Measurement Complete		Coarse Rate Readback LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
x	x	x	0 = Waiting for next LOL 1 = Static LOL until reset	0 = Locked 1 = Acquiring	0 = Measuring datarate 1 = Measurement complete	x	COARSE_RD[0]

Table 8. Control Register, CTRLA[1]

F_{REF} Range			Datarate/Div_F_{REF} Ratio					Measure Datarate	Lock to Reference
D7	**D6**		**D5**	**D4**	**D3**	**D2**		**D1**	**D0**
0	0	12.3 MHz to 25 MHz	0	0	0	0	1	Set to 1 to measure datarate	0 = Lock to input data
0	1	25 MHz to 50 MHz	0	0	0	1	2		1 = Lock to reference clock
1	0	50 MHz to 100 MHz	0	0	1	0	4		
1	1	100 MHz to 200 MHz			n		2^n		
			1	0	0	0	256		

[1] Where DIV_F_{REF} is the divided down reference referred to the 12.3 MHz to 25 MHz band (see the Reference Clock (Optional) section).

Table 9. Control Register, CTRLB

Config LOL	Reset MISC[4]	System Reset		Reset MISC[2]			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0 = LOL pin normal operation 1 = LOL pin is static LOL	Write a 1 followed by 0 to reset MISC[4]	Write a 1 followed by 0 to reset ADN2815	Set to 0	Write a 1 followed by 0 to reset MISC[2]	Set to 0	Set to 0	Set to 0

Table 10. Control Register, CTRLC

						Squelch Mode	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	0 = Squelch CLK and DATA 1 = Squelch CLK or DATA	Set to 0

JITTER SPECIFICATIONS

The ADN2815 CDR is designed to achieve the best bit-error-rate (BER) performance and exceeds the jitter transfer, generation, and tolerance specifications proposed for SONET/SDH equipment defined in the Telcordia Technologies specification.

Jitter is the dynamic displacement of digital signal edges from their long-term average positions, measured in unit intervals (UI), where 1 UI = 1 bit period. Jitter on the input data can cause dynamic phase errors on the recovered clock sampling edge. Jitter on the recovered clock causes jitter on the retimed data.

The following sections briefly summarize the specifications of jitter generation, transfer, and tolerance in accordance with the Telcordia document (GR-253-CORE, Issue 3, September 2000) for the optical interface at the equipment level and the ADN2815 performance with respect to those specifications.

JITTER GENERATION

The jitter generation specification limits the amount of jitter that can be generated by the device with no jitter and wander applied at the input. For SONET devices, the jitter generated must be less than 0.01 UI rms, and must be less than 0.1 UIp-p.

JITTER TRANSFER

The jitter transfer function is the ratio of the jitter on the output signal to the jitter applied on the input signal versus the frequency. This parameter measures the limited amount of the jitter on an input signal that can be transferred to the output signal (see Figure 10).

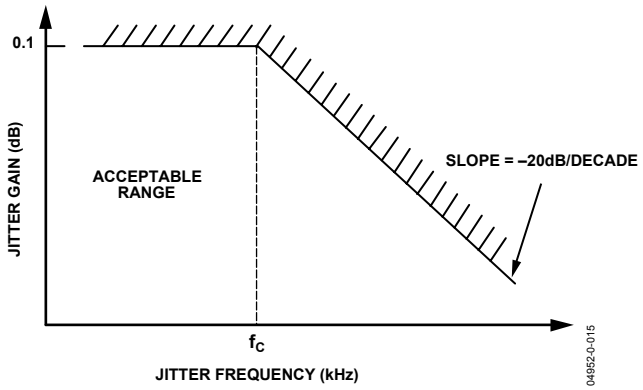


Figure 10. Jitter Transfer Curve

JITTER TOLERANCE

The jitter tolerance is defined as the peak-to-peak amplitude of the sinusoidal jitter applied on the input signal, which causes a 1 dB power penalty. This is a stress test intended to ensure that no additional penalty is incurred under the operating conditions (see Figure 11).

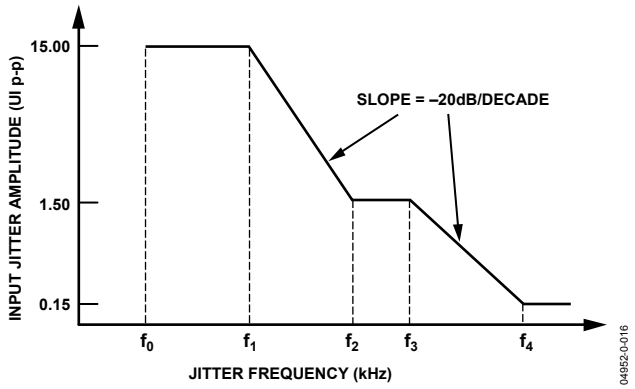


Figure 11. SONET Jitter Tolerance Mask

THEORY OF OPERATION

The ADN2815 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops, which share a common control voltage. A high speed delay-locked loop path uses a voltage controlled phase shifter to track the high frequency components of input jitter. A separate phase control loop, comprised of the VCO, tracks the low frequency components of input jitter. The initial frequency of the VCO is set by yet a third loop, which compares the VCO frequency with the input data frequency and sets the coarse tuning voltage. The jitter tracking phase-locked loop controls the VCO by the fine-tuning control.

The delay- and phase-loops together track the phase of the input data signal. For example, when the clock lags input data, the phase detector drives the VCO to higher frequency, and also increases the delay through the phase shifter; both these actions serve to reduce the phase error between the clock and data. The faster clock picks up phase, while the delayed data loses phase. Because the loop filter is an integrator, the static phase error is driven to zero.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

The delay- and phase-loops together simultaneously provide wide-band jitter accommodation and narrow-band jitter filtering. The linearized block diagram in Figure 12 shows that the jitter transfer function, Z(s)/X(s), is a second-order low-pass providing excellent filtering. Note that the jitter transfer has no zero, unlike an ordinary second-order phase-locked loop. This means that the main PLL loop has virtually zero jitter peaking (see Figure 13). This makes this circuit ideal for signal regenerator applications, where jitter peaking in a cascade of regenerators can contribute to hazardous jitter accumulation.

The error transfer, e(s)/X(s), has the same high-pass form as an ordinary phase-locked loop. This transfer function is free to be optimized to give excellent wide-band jitter accommodation, because the jitter transfer function, Z(s)/X(s), provides the narrow-band jitter filtering.

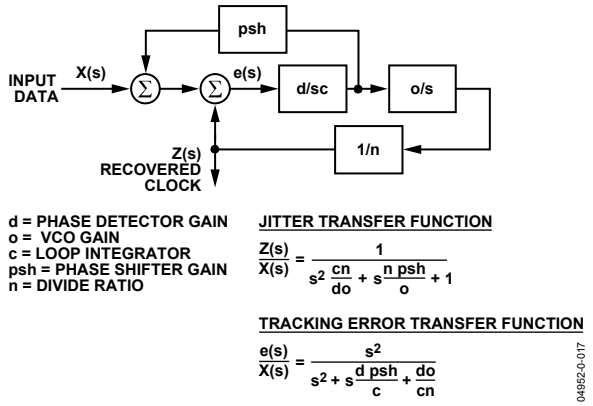


Figure 12. ADN2815 PLL/DLL Architecture

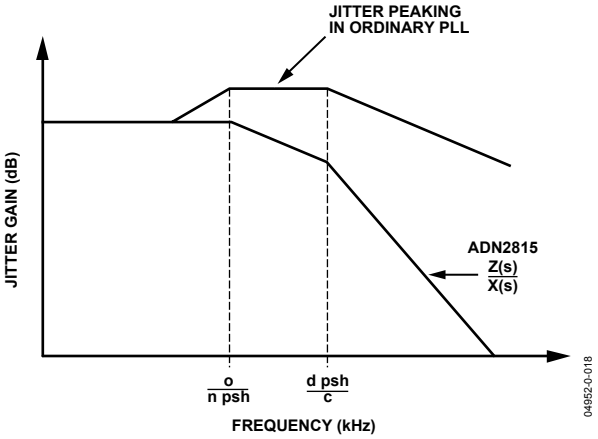


Figure 13. ADN2815 Jitter Response vs. Conventional PLL

The delay- and phase-loops contribute to overall jitter accommodation. At low frequencies of input jitter on the data signal, the integrator in the loop filter provides high gain to track large jitter amplitudes with small phase error. In this case, the VCO is frequency modulated and jitter is tracked as in an ordinary phase-locked loop. The amount of low frequency jitter that can be tracked is a function of the VCO tuning range. A wider tuning range gives larger accommodation of low frequency jitter. The internal loop control voltage remains small for small phase errors, so the phase shifter remains close to the center of its range and thus contributes little to the low frequency jitter accommodation.

At medium jitter frequencies, the gain and tuning range of the VCO are not large enough to track input jitter. In this case, the VCO control voltage becomes large and saturates, and the VCO frequency dwells at one extreme of its tuning range or the other. The size of the VCO tuning range, therefore, has only a small effect on the jitter accommodation. The delay-locked loop control voltage is now larger, and so the phase shifter takes on the burden of tracking the input jitter. The phase shifter range, in UI, can be seen as a broad plateau on the jitter tolerance curve. The phase shifter has a minimum range of 2 UI at all data rates.

The gain of the loop integrator is small for high jitter frequencies, so that larger phase differences are needed to make the loop control voltage big enough to tune the range of the phase shifter. Large phase errors at high jitter frequencies cannot be tolerated. In this region, the gain of the integrator determines the jitter accommodation. Because the gain of the loop integrator declines linearly with frequency, jitter accommodation is lower with higher jitter frequency. At the highest frequencies, the loop gain is very small, and little tuning of the phase shifter can be expected. In this case, jitter accommodation is determined by the eye opening of the input data, the static phase error, and the residual loop jitter generation. The jitter accommodation is roughly 0.5 UI in this region. The corner frequency between the declining slope and the flat region is the closed loop bandwidth of the delay-locked loop, which is roughly 1.5 MHz at 1.25Gb/s.

FUNCTIONAL DESCRIPTION

FREQUENCY ACQUISITION

The ADN2815 acquires frequency from the data over a range of data frequencies from 12.3 Mb/s to 1.25 Gb/s. The lock detector circuit compares the frequency of the VCO and the frequency of the incoming data. When these frequencies differ by more than 1000 ppm, LOL is asserted. This initiates a frequency acquisition cycle. The VCO frequency is reset to the bottom of its range, which is 12.3 MHz. The frequency detector then compares this VCO frequency and the incoming data frequency and increments the VCO frequency, if necessary. Initially, the VCO frequency is incremented in large steps to aid fast acquisition. As the VCO frequency approaches the data frequency, the step size is reduced until the VCO frequency is within 250 ppm of the data frequency, at which point LOL is de-asserted.

Once LOL is de-asserted, the frequency-locked loop is turned off. The PLL/DLL pulls in the VCO frequency the rest of the way until the VCO frequency equals the data frequency.

The frequency loop requires a single external capacitor between CF1 and CF2, Pins 14 and 15. A 0.47 µF ± 20%, X7R ceramic chip capacitor with < 10 nA leakage current is recommended. Leakage current of the capacitor can be calculated by dividing the maximum voltage across the 0.47 µF capacitor, ~3 V, by the insulation resistance of the capacitor. The insulation resistance of the 0.47 uF capacitor should be greater than 300 MΩ.

INPUT BUFFER

The input buffer has differential inputs (PIN/NIN), which are internally terminated with 50 Ω to an on-chip voltage reference (VREF = 2.5 V typically). The minimum differential input level required to achieve a BER of 10e-10 is 200mVpp.

LOCK DETECTOR OPERATION

The lock detector on the ADN2815 has three modes of operation: normal mode, REFCLK mode, and static LOL mode.

Normal Mode

In normal mode, the ADN2815 is a continuous rate CDR that locks onto any data rate from 12.3 Mb/s to 1.25 Gb/s without the use of a reference clock as an acquisition aid. In this mode, the lock detector monitors the frequency difference between the VCO and the input data frequency, and de-asserts the loss of lock signal, which appears on LOL Pin 16, when the VCO is within 250 ppm of the data frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount and also acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is re-asserted and control returns to the frequency loop, which begins a new frequency acquisition starting at the lowest point in the VCO operating range, 12.3 MHz. The LOL pin remains asserted until the VCO locks onto a valid input data stream to within 250 ppm frequency error. This hysteresis is shown in Figure 14.

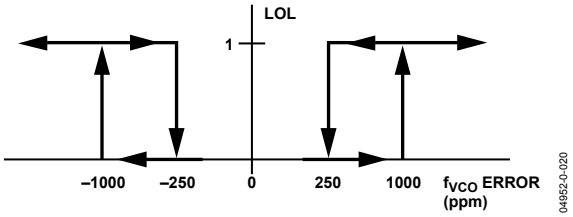


Figure 14. Transfer Function of LOL

LOL Detector Operation Using a Reference Clock

In this mode, a reference clock is used as an acquisition aid to lock the ADN2815 VCO. Lock to reference mode is enabled by setting CTRLA[0] to 1. The user also needs to write to the CTRLA[7:6] and CTRLA[5:2] bits in order to set the reference frequency range and the divide ratio of the data rate with respect to the reference frequency. For more details, see the Reference Clock (Optional) section. In this mode, the lock detector monitors the difference in frequency between the divided down VCO and the divided down reference clock. The loss of lock signal, which appears on the LOL Pin 16, is de-asserted when the VCO is within 250 ppm of the desired frequency. This enables the D/PLL, which pulls the VCO frequency in the remaining amount with respect to the input data and also acquires phase lock. Once locked, if the input frequency error exceeds 1000 ppm (0.1%), the loss of lock signal is re-asserted and control returns to the frequency loop, which re-acquires with respect to the reference clock. The LOL pin remains asserted until the VCO frequency is within 250 ppm of the desired frequency. This hysteresis is shown in Figure 14.

Static LOL Mode

The ADN2815 implements a static LOL feature, which indicates if a loss of lock condition has ever occurred and remains asserted, even if the ADN2815 regains lock, until the static LOL bit is manually reset. The I^2C register bit, MISC[4], is the static LOL bit. If there is ever an occurrence of a loss of lock condition, this bit is internally asserted to logic high. The MISC[4] bit remains high even after the ADN2815 has re-acquired lock to a new data rate. This bit can be reset by writing a 1 followed by 0 to I^2C Register Bit CTRLB[6]. Once reset, the MISC[4] bit remains de-asserted until another loss of lock condition occurs.

Writing a 1 to I^2C Register Bit CTRLB[7] causes the LOL pin, Pin 16, to become a static LOL indicator. In this mode, the LOL pin mirrors the contents of the MISC[4] bit and has the functionality described in the previous paragraph. The CTRLB[7] bit defaults to 0. In this mode, the LOL pin operates in the normal operating mode, that is, it is asserted only when

the ADN2815 is in acquisition mode and de-asserts when the ADN2815 has re-acquired lock.

HARMONIC DETECTOR

The ADN2815 provides a harmonic detector, which detects whether or not the input data has changed to a lower harmonic of the data rate that the VCO is currently locked onto. For example, if the input data *instantaneously* changes from OC-12, 622.08Mb/s, to an OC-3, 155.52 Mb/s bit stream, this could be perceived as a valid OC-12 bit stream, because the OC-3 data pattern is exactly 4× slower than the OC-12 pattern. So, if the change in data rate is instantaneous, a 101 pattern at OC-3 would be perceived by the ADN2815 as a 111100001111 pattern at OC-12. If the change to a lower harmonic is instantaneous, a typical CDR could remain locked at the higher data rate.

The ADN2815 implements a harmonic detector that automatically identifies whether or not the input data has switched to a lower harmonic of the data rate that the VCO is currently locked onto. When a harmonic is identified, the LOL pin is asserted and a new frequency acquisition is initiated. The ADN2815 automatically locks onto the new data rate, and the LOL pin is de-asserted.

However, the harmonic detector does not detect higher harmonics of the data rate. If the input data rate switches to a higher harmonic of the data rate the VCO is currently locked onto, the VCO loses lock, the LOL pin is asserted, and a new frequency acquisition is initiated. The ADN2815 automatically locks onto the new data rate.

The time to detect lock to harmonic is

$$16{,}384 \times (T_d/\rho)$$

where:

$1/T_d$ is the new data rate. For example, if the data rate is switched from OC-12 to OC-3, then T_d = 1/155.52 MHz.

ρ is the data transition density. Most coding schemes seek to ensure that ρ = 0.5, for example, PRBS, 8B/10B.

When the ADN2815 is placed in lock to reference mode, the harmonic detector is disabled.

SQUELCH MODE

Two squelch modes are available with the ADN2815. Squelch DATAOUT *AND* CLKOUT mode is selected when CTRLC[1] = 0 (default mode). In this mode, when the squelch input, Pin 27, is driven to a TTL high state, both the clock and data outputs are set to the zero state to suppress downstream processing. If the squelch function is not required, Pin 27 should be tied to VEE.

Squelch DATAOUT *OR* CLKOUT mode is selected when CTRLC[1] is 1. In this mode, when the squelch input is driven to a high state, the DATAOUT pins are squelched. When the squelch input is driven to a low state, the CLKOUT pins are squelched. This is especially useful in repeater applications, where the recovered clock may not be needed.

I²C INTERFACE

The ADN2815 supports a 2-wire, I²C compatible, serial bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCK), carry information between any devices connected to the bus. Each slave device is recognized by a unique address. The ADN2815 has two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is factory programmed to 1. B5 of the slave address is set by Pin 19, SADDR5. Slave address bits [4:0] are defaulted to all 0s. The slave address consists of the 7 MSBs of an 8-bit word. The LSB of the word sets either a read or write operation (see Figure 5). Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCK lines waiting for the start condition and correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADN2815 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-bit addresses plus the R/W bit. The ADN2815 has 8 subaddresses to enable the user-accessible internal registers (see **Error! Reference source not found.** through Table 7). It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. Autoincrement mode is supported, allowing data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then they cause an immediate jump to the idle condition. During a given SCK high period, the user should issue one start condition, one stop

condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADN2815 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while reading back in autoincrement mode, then the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. In a no-acknowledge condition, the SDATA line is not pulled low on the ninth pulse. See Figure 6 and Figure 7 for sample read and write data transfers and Figure 8 for a more detailed timing diagram.

REFERENCE CLOCK (OPTIONAL)

A reference clock is not required to perform clock and data recovery with the ADN2815. However, support for an optional reference clock is provided. The reference clock can be driven differentially or single-ended. If the reference clock is not being used, then REFCLKP should be tied to VCC, and REFCLKN can be left floating or tied to VEE (the inputs are internally terminated to VCC/2). See Figure 15 through Figure 17 for sample configurations.

The REFCLK input buffer accepts any differential signal with a peak-to-peak differential amplitude of greater than 100 mV (for example, LVPECL or LVDS) or a standard single-ended low voltage TTL input, providing maximum system flexibility. Phase noise and duty cycle of the reference clock are not critical and 100 ppm accuracy is sufficient.

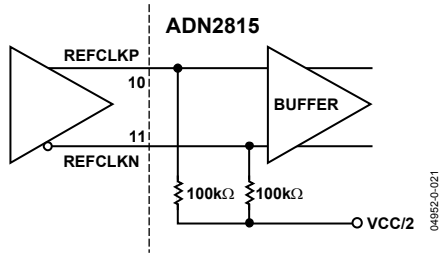


Figure 15. Differential REFCLK Configuration

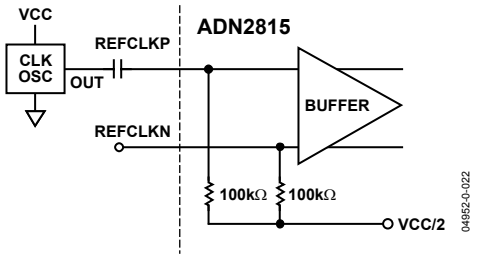


Figure 16. Single-Ended REFCLK Configuration

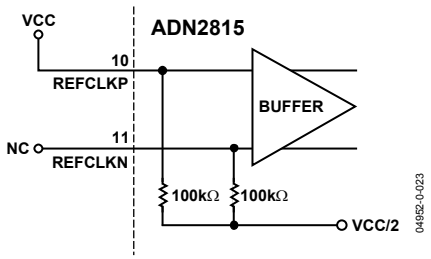


Figure 17. No REFCLK Configuration

The two uses of the reference clock are mutually exclusive. The reference clock can be used either as an acquisition aid for the ADN2815 to lock onto data, or to measure the frequency of the incoming data to within 0.01%. (There is the capability to measure the data rate to approximately ±10% without the use of a reference clock.) The modes are mutually exclusive, because, in the first use, the user knows exactly what the data rate is and wants to force the part to lock onto only that data rate; in the second use, the user does not know what the data rate is and wants to measure it.

Lock to reference mode is enabled by writing a 1 to I²C Register Bit CTRLA[0]. Fine data rate readback mode is enabled by writing a 1 to I²C Register Bit CTRLA[1]. Writing a 1 to both of these bits at the same time causes an indeterminate state and is not supported.

Using the Reference Clock to Lock onto Data

In this mode, the ADN2815 locks onto a frequency derived from the reference clock according to the following equation:

$$Data\ Rate/2^{CTRLA[5:2]} = REFCLK/2^{CTRLA[7:6]}$$

The user must know exactly what the data rate is, and provide a reference clock that is a function of this rate. The ADN2815 can still be used as a continuous rate device in this configuration, provided that the user has the ability to provide a reference clock that has a variable frequency (see Application Note AN-632).

The reference clock can be anywhere between 12.3 MHz and 200 MHz. By default, the ADN2815 expects a reference clock of between 12.3 MHz and 25 MHz. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2815 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6].

Table 11. CTRLA Settings

CTRLA[7:6]	Range (MHz)
00	12.3 to 25
01	25 to 50
10	50 to 100
11	100 to 200

CTRLA[5:2]	Ratio
0000	1
0001	2
n	2^n
1000	256

The user can specify a fixed integer multiple of the reference clock to lock onto using CTRLA[5:2], where CTRLA should be set to the data rate/DIV_F_{REF}, where DIV_F_{REF} represents the divided-down reference referred to the 12.3 MHz to 25 MHz band. For example, if the reference clock frequency was 38.88 MHz and the input data rate was 622.08 Mb/s, then CTRLA[7:6] would be set to [01] to give a divided-down reference clock of 19.44 MHz. CTRLA[5:2] would be set to [0101], that is, 5, because

622.08 Mb/s/19.44 MHz = 2^5

In this mode, if the ADN2815 loses lock for any reason, it relocks onto the reference clock and continues to output a stable clock.

While the ADN2815 is operating in lock to reference mode, if the user ever changes the reference frequency, the F_{REF} range (CTRLA[7:6]), or the F_{REF} ratio (CTRLA[5:2]), this must be followed by writing a 0 to 1 transition into the CTRLA[0] bit to initiate a new lock to reference command.

Using the Reference Clock to Measure Data Frequency

The user can also provide a reference clock to measure the recovered data frequency. In this case, the user provides a reference clock, and the ADN2815 compares the frequency of the incoming data to the incoming reference clock and returns a ratio of the two frequencies to 0.01% (100 ppm). The accuracy error of the reference clock is added to the accuracy of the ADN2815 data rate measurement. For example, if a 100-ppm accuracy reference clock is used, the total accuracy of the measurement is within 200 ppm.

The reference clock can range from 12.3 MHz and 200 MHz. The ADN2815 expects a reference clock between 12.3 MHz and 25 MHz by default. If it is between 25 MHz and 50 MHz, 50 MHz and 100 MHz, or 100 MHz and 200 MHz, the user needs to configure the ADN2815 to use the correct reference frequency range by setting two bits of the CTRLA register, CTRLA[7:6]. Using the reference clock to determine the frequency of the incoming data does not affect the manner in which the part locks onto data. In this mode, the reference clock is used only to determine the frequency of the data. For this reason, the user does not need to know the data rate to use the reference clock in this manner.

Prior to reading back the data rate using the reference clock, the CTRLA[7:6] bits must be set to the appropriate frequency range with respect to the reference clock being used. A fine data rate readback is then executed as follows:

Step 1: Write a 1 to CTRLA[1]. This enables the fine data rate measurement capability of the ADN2815. This bit is level sensitive and does not need to be reset to perform subsequent frequency measurements.

Step 2: Reset MISC[2] by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement.

Step 3: Read back MISC[2]. If it is 0, then the measurement is not complete. If it is 1, then the measurement is complete and the data rate can be read back on FREQ[22:0]. The time for a data rate measurement is typically 80 ms.

Step 4: Read back the data rate from registers FREQ2[6:0], FREQ1[7:0], and FREQ0[7:0].

Use the following equation to determine the data rate:

$$f_{DATARATE} = \left(FREQ[22..0] \times f_{REFCLK}\right) / 2^{(14+SEL\_RATE)}$$

where:

FREQ[22:0] is the reading from FREQ2[6:0] (MSByte), FREQ1[7:0], and FREQ0[7:0] (LSByte).

Table 12.

D22	D21...D17	D16	D15	D14...D9	D8	D7	D6...D1	D0
FREQ2[6:0]			FREQ1[7:0]			FREQ0[7:0]		

$f_{DATARATE}$ is the data rate (Mb/s).

f_{REFCLK} is the REFCLK frequency (MHz).

SEL_RATE is the setting from CTRLA[7:6].

For example, if the reference clock frequency is 32 MHz, SEL_RATE = 1, since the CTRLA[7:6] setting would be [01], because the reference frequency would fall into the 25 MHz to 50 MHz range. Assume for this example that the input data rate is 1.25 Gb/s (GbE). After following Steps 1 through 4, the value that is read back on FREQ[22:0] = 0x138800, which is equal to 1.28×10^6. Plugging this value into the equation yields

$$\left(1.28e6 \times 32e6\right) / \left(2^{(14+1)}\right) = 1.25\,\text{Gb/s}$$

If subsequent frequency measurements are required, CTRLA[1] should remain set to 1. It does not need to be reset. The measurement process is reset by writing a 1 followed by a 0 to CTRLB[3]. This initiates a new data rate measurement. Follow Steps 2 through 4 to read back the new data rate.

Note: A data rate readback is valid only if LOL is low. If LOL is high, the data rate readback is invalid.

Additional Features Available via the I²C Interface

Coarse Data Rate Readback

The data rate can be read back over the I²C interface to approximately ±10% without the need of an external reference clock. A 9-bit register, COARSE_RD[8:0], can be read back when LOL is de-asserted. The 8 MSBs of this register are the contents of the RATE[7:0] register. The LSB of the COARSE_RD register is Bit MISC[0].

Table 13 provides coarse data rate readback to within ±10%.

System Reset

A frequency acquisition can be initiated by writing a 1 followed by a 0 to the I²C Register Bit CTRLB[5]. This initiates a new frequency acquisition while keeping the ADN2815 in the operating mode that it was previously programmed to in registers CTRL[A], CTRL[B], and CTRL[C].

APPLICATIONS INFORMATION

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

Power Supply Connections and Ground Planes

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance, especially on Pin 23, which is the ground return for the output buffers. The exposed pad should be connected to the GND plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 22 µF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the PCB. When using 0.1 µF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply VCC and VEE, as close as possible to the ADN2815 VCC pins.

If connections to the supply and ground are made through vias, the use of multiple vias in parallel helps to reduce series inductance, especially on Pin 24, which supplies power to the high speed CLKOUTP/CLKOUTN and DATAOUTP/DATAOUTN output buffers. Refer to the schematic in Figure 18 for recommended connections.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{plane} = 0.88\varepsilon_r A/d\,(\text{pF})$$

where:

ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and GND planes (cm^2).
d is the separation between planes (mm).

For FR-4, ε_r = 4.4 mm and 0.25 mm spacing, C ~15 pF/cm^2.

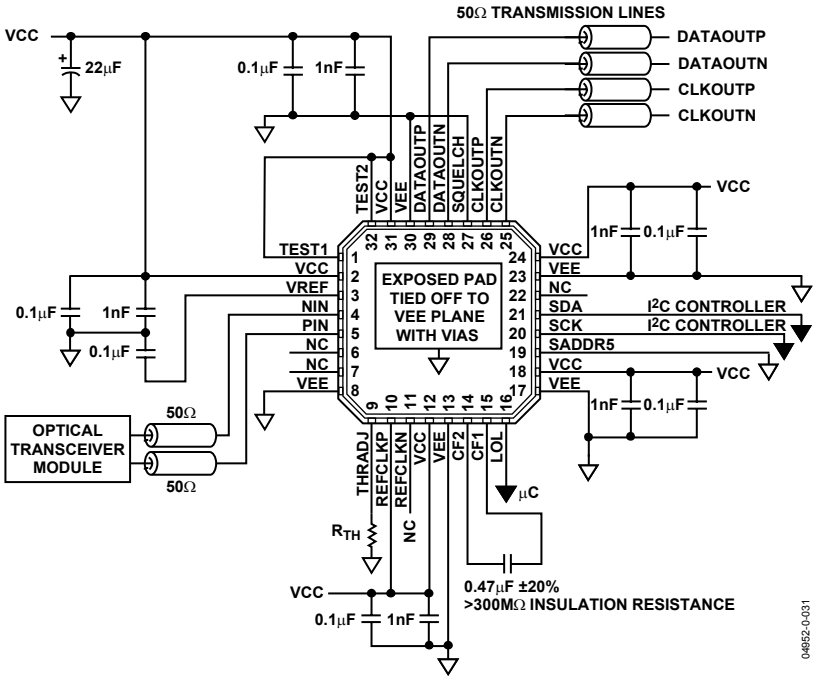


Figure 18. Typical ADN2815 Applications Circuit

Transmission Lines

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections: PIN, NIN, CLKOUTP, CLKOUTN, DATAOUTP, DATAOUTN (also REFCLKP, REFCLKN, if a high frequency reference clock is used, such as 155 MHz). It is also necessary for the PIN/NIN input traces to be matched in length, and the CLKOUTP/N and DATAOUTP/N output traces to be matched in length to avoid skew between the differential traces. The high speed inputs, PIN and NIN, are internally terminated with 50 Ω to an internal reference voltage (see Figure 19). A 0.1 µF is recommended between VREF, Pin 3, and GND to provide an ac ground for the inputs.

As with any high speed mixed-signal design, take care to keep all high speed digital traces away from sensitive analog nodes.

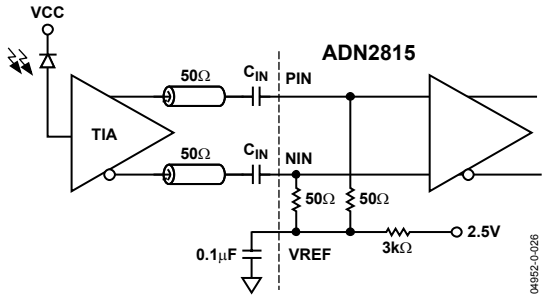


Figure 19. ADN2815 AC-Coupled Input Configuration

Soldering Guidelines for Chip Scale Package

The lands on the 32 LFCSP are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the printed circuit board should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

Choosing AC Coupling Capacitors

AC coupling capacitors at the input (PIN, NIN) and output (DATAOUTP, DATAOUTN) of the ADN2815 must be chosen such that the device works properly over the full range of data rates used in the application. When choosing the capacitors, the time constant formed with the two 50 Ω resistors in the signal path must be considered. When a large number of consecutive identical digits (CIDs) are applied, the capacitor voltage can droop due to baseline wander (see Figure 20), causing pattern-dependent jitter (PDJ).

The user must determine how much droop is tolerable and choose an ac coupling capacitor based on that amount of droop. The amount of PDJ can then be approximated based on the capacitor selection. The actual capacitor value selection may require some trade-offs between droop and PDJ.

Example: Assuming that 2% droop can be tolerated, then the maximum differential droop is 4%. Normalizing to V_{pp}:

$$Droop = \Delta V = 0.04\ V = 0.5\ V_{pp}(1 - e^{-t/\tau})\ ;\ \text{therefore, } \tau = 12t$$

where:

τ is the RC time constant (C is the ac coupling capacitor, R = 100 Ω seen by C).

t is the total discharge time, which is equal to *n T*.

n is the number of CIDs.

T is the bit period.

The capacitor value can then be calculated by combining the equations for τ and t:

$$C = 12nT/R$$

Once the capacitor value is selected, the PDJ can be approximated as

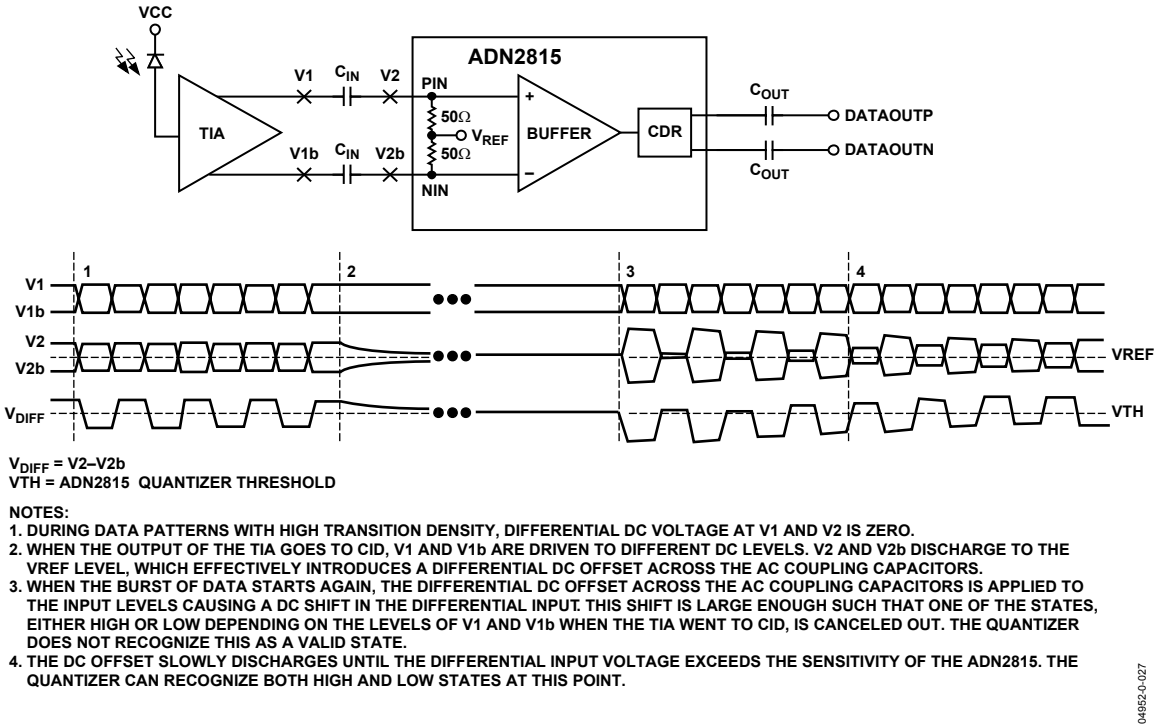
$$PDJ_{pspp} = 0.5t_r\left(1 - e^{(-nT/RC)}\right)/0.6$$

where:

PDJ_{pspp} is the amount of pattern-dependent jitter allowed; < 0.01 UI p-p typical.

t_r is the rise time, which is equal to 0.22/*BW*, where *BW* ~ 0.7 (bit rate).

Note that this expression for t_r is accurate only for the inputs. The output rise time for the ADN2815 is ~100 ps regardless of data rate.



V_{DIFF} = V2–V2b
VTH = ADN2815 QUANTIZER THRESHOLD

NOTES:
1. DURING DATA PATTERNS WITH HIGH TRANSITION DENSITY, DIFFERENTIAL DC VOLTAGE AT V1 AND V2 IS ZERO.
2. WHEN THE OUTPUT OF THE TIA GOES TO CID, V1 AND V1b ARE DRIVEN TO DIFFERENT DC LEVELS. V2 AND V2b DISCHARGE TO THE VREF LEVEL, WHICH EFFECTIVELY INTRODUCES A DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS.
3. WHEN THE BURST OF DATA STARTS AGAIN, THE DIFFERENTIAL DC OFFSET ACROSS THE AC COUPLING CAPACITORS IS APPLIED TO THE INPUT LEVELS CAUSING A DC SHIFT IN THE DIFFERENTIAL INPUT. THIS SHIFT IS LARGE ENOUGH SUCH THAT ONE OF THE STATES, EITHER HIGH OR LOW DEPENDING ON THE LEVELS OF V1 AND V1b WHEN THE TIA WENT TO CID, IS CANCELED OUT. THE QUANTIZER DOES NOT RECOGNIZE THIS AS A VALID STATE.
4. THE DC OFFSET SLOWLY DISCHARGES UNTIL THE DIFFERENTIAL INPUT VOLTAGE EXCEEDS THE SENSITIVITY OF THE ADN2815. THE QUANTIZER CAN RECOGNIZE BOTH HIGH AND LOW STATES AT THIS POINT.

Figure 20. Example of Baseline Wander

COARSE DATA RATE READBACK LOOK-UP TABLE

Code is the 9-bit value read back from COARSE_RD[8:0].

Table 13. Look-Up Table

Code	F_{MID}	Code	F_{MID}	Code	F_{MID}	Code	F_{MID}
0	5.1934e+06	48	1.4828e+07	96	4.1547e+07	144	1.1862e+08
1	5.1930e+06	49	1.4827e+07	97	4.1544e+07	145	1.1862e+08
2	5.2930e+06	50	1.5121e+07	98	4.2344e+07	146	1.2097e+08
3	5.3989e+06	51	1.5435e+07	99	4.3191e+07	147	1.2348e+08
4	5.5124e+06	52	1.5770e+07	100	4.4099e+07	148	1.2616e+08
5	5.6325e+06	53	1.6127e+07	101	4.5060e+07	149	1.2901e+08
6	5.7612e+06	54	1.6510e+07	102	4.6090e+07	150	1.3208e+08
7	5.8995e+06	55	1.6917e+07	103	4.7196e+07	151	1.3534e+08
8	6.0473e+06	56	1.7357e+07	104	4.8378e+07	152	1.3885e+08
9	6.2097e+06	57	1.7836e+07	105	4.9678e+07	153	1.4269e+08
10	6.3819e+06	58	1.8347e+07	106	5.1055e+07	154	1.4678e+08
11	6.5675e+06	59	1.8896e+07	107	5.2540e+07	155	1.5117e+08
12	6.7688e+06	60	1.9493e+07	108	5.4150e+07	156	1.5594e+08
13	6.9874e+06	61	2.0136e+07	109	5.5899e+07	157	1.6109e+08
14	7.2262e+06	62	2.0833e+07	110	5.7810e+07	158	1.6667e+08
15	7.4863e+06	63	2.1582e+07	111	5.9890e+07	159	1.7266e+08
16	7.4139e+06	64	2.0774e+07	112	5.9311e+07	160	1.6619e+08
17	7.4135e+06	65	2.0772e+07	113	5.9308e+07	161	1.6617e+08
18	7.5606e+06	66	2.1172e+07	114	6.0485e+07	162	1.6938e+08
19	7.7173e+06	67	2.1596e+07	115	6.1739e+07	163	1.7277e+08
20	7.8852e+06	68	2.2049e+07	116	6.3081e+07	164	1.7640e+08
21	8.0633e+06	69	2.2530e+07	117	6.4506e+07	165	1.8024e+08
22	8.2548e+06	70	2.3045e+07	118	6.6038e+07	166	1.8436e+08
23	8.4586e+06	71	2.3598e+07	119	6.7669e+07	167	1.8878e+08
24	8.6784e+06	72	2.4189e+07	120	6.9427e+07	168	1.9351e+08
25	8.9180e+06	73	2.4839e+07	121	7.1344e+07	169	1.9871e+08
26	9.1736e+06	74	2.5527e+07	122	7.3388e+07	170	2.0422e+08
27	9.4481e+06	75	2.6270e+07	123	7.5585e+07	171	2.1016e+08
28	9.7464e+06	76	2.7075e+07	124	7.7971e+07	172	2.1660e+08
29	1.0068e+07	77	2.7950e+07	125	8.0546e+07	173	2.2360e+08
30	1.0417e+07	78	2.8905e+07	126	8.3333e+07	174	2.3124e+08
31	1.0791e+07	79	2.9945e+07	127	8.6328e+07	175	2.3956e+08
32	1.0387e+07	80	2.9655e+07	128	8.3095e+07	176	2.3724e+08
33	1.0386e+07	81	2.9654e+07	129	8.3087e+07	177	2.3723e+08
34	1.0586e+07	82	3.0242e+07	130	8.4689e+07	178	2.4194e+08
35	1.0798e+07	83	3.0869e+07	131	8.6383e+07	179	2.4695e+08
36	1.1025e+07	84	3.1541e+07	132	8.8198e+07	180	2.5233e+08
37	1.1265e+07	85	3.2253e+07	133	9.0120e+07	181	2.5802e+08
38	1.1522e+07	86	3.3019e+07	134	9.2179e+07	182	2.6415e+08
39	1.1799e+07	87	3.3834e+07	135	9.4392e+07	183	2.7067e+08
40	1.2095e+07	88	3.4714e+07	136	9.6757e+07	184	2.7771e+08
41	1.2419e+07	89	3.5672e+07	137	9.9356e+07	185	2.8538e+08
42	1.2764e+07	90	3.6694e+07	138	1.0211e+08	186	2.9355e+08
43	1.3135e+07	91	3.7792e+07	139	1.0508e+08	187	3.0234e+08
44	1.3538e+07	92	3.8985e+07	140	1.0830e+08	188	3.1188e+08
45	1.3975e+07	93	4.0273e+07	141	1.1180e+08	189	3.2218e+08
46	1.4452e+07	94	4.1666e+07	142	1.1562e+08	190	3.3333e+08
47	1.4973e+07	95	4.3164e+07	143	1.1978e+08	191	3.4531e+08

Code	F_{MID}
192	3.3238e+08
193	3.3235e+08
194	3.3876e+08
195	3.4553e+08
196	3.5279e+08
197	3.6048e+08
198	3.6872e+08
199	3.7757e+08
200	3.8703e+08
201	3.9742e+08
202	4.0844e+08
203	4.2032e+08
204	4.3320e+08
205	4.4719e+08
206	4.6248e+08
207	4.7912e+08

Code	F_{MID}
208	4.7449e+08
209	4.7447e+08
210	4.8388e+08
211	4.9391e+08
212	5.0465e+08
213	5.1605e+08
214	5.2831e+08
215	5.4135e+08
216	5.5542e+08
217	5.7075e+08
218	5.8711e+08
219	6.0468e+08
220	6.2377e+08
221	6.4437e+08
222	6.6666e+08
223	6.9062e+08

Code	F_{MID}
224	6.6476e+08
225	6.6470e+08
226	6.7751e+08
227	6.9106e+08
228	7.0558e+08
229	7.2096e+08
230	7.3743e+08
231	7.5514e+08
232	7.7405e+08
233	7.9485e+08
234	8.1688e+08
235	8.4064e+08
236	8.6640e+08
237	8.9438e+08
238	9.2496e+08
239	9.5825e+08

Code	F_{MID}
240	9.4898e+08
241	9.4893e+08
242	9.6776e+08
243	9.8782e+08
244	1.0093e+09
245	1.0321e+09
246	1.0566e+09
247	1.0827e+09
248	1.1108e+09
249	1.1415e+09
250	1.1742e+09
251	1.2094e+09
252	1.2475e+09
253	1.2887e+09
254	1.3333e+09
255	1.3812e+09

OUTLINE DIMENSIONS

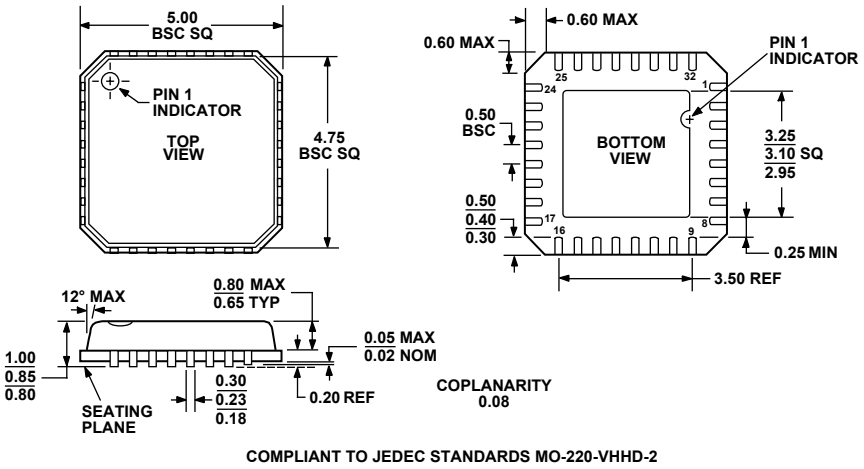


Figure 21. 32-Lead Frame Chip Scale Package [LFCSP]
(CP-32)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN2815ACP	–40°C to 85°C	32-LFCSP	CP-32
ADN2815ACP-RL	–40°C to 85°C	32-LFCSP, tape-reel, 2500 pcs	CP-32
ADN2815ACP-RL7	–40°C to 85°C	32-LFCSP, tape-reel, 1500 pcs	CP-32

NOTES

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PR04952-0-8/04(PrA)