0.4 Ω CMOS, Dual DPDT Switch in WLCSP/LFCSP/TSSOP Packages

ADG888

FEATURES

1.8 V to 5.5 V operation
Ultralow on resistance
  0.4 Ω typical
  0.6 Ω maximum at 5 V supply
Excellent audio performance, ultralow distortion
  0.07 Ω typical
  0.14 Ω maximum R_{ON} flatness
High current carrying capability
  400 mA continuous
  600 mA peak current at 5 V
Automotive temperature range: –40°C to +125°C
Rail-to-rail switching operation
Typical power consumption (<0.1 μW)

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communication systems
Data switching

FUNCTIONAL BLOCK DIAGRAM

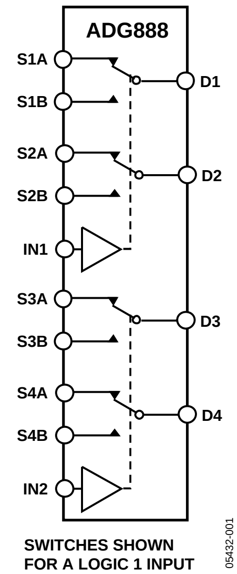

Figure 1.

GENERAL DESCRIPTION

The ADG888 is a low voltage, dual DPDT (double pole double throw) CMOS device optimized for high performance audio switching. With its low power and small physical size, it is ideal for portable devices.

This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range making it an ideal solution for applications requiring minimal distortion through the switch. The ADG888 also has the capability of carrying large amounts of current, typically 400 mA at 5 V operation.

When on, each switch conducts equally well in both directions and has an input signal range that extends to the supplies. The ADG888 exhibits break-before-make switching action.

The ADG888 is available in a 4 × 4 bump, 2.0 mm × 2.0 mm WLCSP; a 4 mm × 4 mm, 16-lead LFCSP; and a 16-lead TSSOP. These packages make the ADG888 the ideal solution for space-constrained applications.

PRODUCT HIGHLIGHTS

1. <0.6 Ω over full temperature range of –40°C to +125°C.
2. High current handling capability (400 mA continuous current at 5 V).
3. Low THD + N (0.008% typical).
4. Tiny 2 mm × 2 mm, 16-ball WLCSP package, and 16-lead LFCSP and TSSOP packages.

Rev. 0

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REVISION HISTORY

7/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.2 V to 5.5 V, GND = 0 V, unless otherwise noted.[1]

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.4			Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA;
	0.48	0.55	0.6	Ω max	See Figure 16
On Resistance Match Between	0.04			Ω typ	V_{DD} = 4.2 V, V_S = 2.2 V, I_{DS} = 100 mA
Channels (ΔR_{ON})	0.06	0.07	0.075	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	0.07			Ω typ	V_{DD} = 4.2 V, V_S = 0 V to V_{DD},
	0.11	0.13	0.14	Ω max	I_{DS} = 100 mA
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 17
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	22			ns typ	R_L = 50 Ω, C_L = 35 pF
	30	33	35	ns max	V_S = 3 V/0 V; see Figure 19
t_{OFF}	13			ns typ	R_L = 50 Ω, C_L = 35 pF
	17	18	19	ns max	V_S = 3 V/0 V; see Figure 19
Break-Before-Make Time Delay (t_{BBM})	9			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 3 V; see Figure 20
Charge Injection	70			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 21
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 22
Channel-to-Channel Crosstalk	−99			dB typ	Adjacent channel; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 25
	−67			dB typ	Adjacent switch; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 23
Total Harmonic Distortion (THD + N)	0.008			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 3 V p-p
Insertion Loss	−0.03			dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
−3 dB Bandwidth	29			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
C_S (OFF)	58			pF typ	
C_D, C_S (ON)	110			pF typ	
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 5.5 V
		1	4	μA max	

[1] Temperature range, Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted[1].

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD},
	0.7	0.75	0.8	Ω max	I_S = 100 mA; see Figure 16
On Resistance Match Between	0.045			Ω typ	V_{DD} = 2.7 V, V_S = 1 V,
Channels (ΔR_{ON})	0.065	0.07	0.075	Ω max	I_S = 100 mA
On Resistance Flatness ($R_{FLAT(ON)}$)	0.16			Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD},
			0.25	Ω max	I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage I_S (OFF)	±0.2			nA typ	V_S = 1 V/2.6 V, V_D = 2.6 V/1 V; see Figure 17
Channel On Leakage I_D, I_S (ON)	±0.2			nA typ	V_S = V_D = 1 V or 2.6 V; see Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
C_{IN}, Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	28			ns typ	R_L = 50 Ω, C_L = 35 pF; see Figure 19
	43	47	50	ns max	V_S = 1.5 V/0 V
t_{OFF}	13			ns typ	R_L = 50 Ω, C_L = 35 pF; see Figure 19
	20	21	22	ns max	V_S = 1.5 V/0 V
Break-Before-Make Time Delay (t_{BBM})	14			ns typ	R_L = 50 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 20
Charge Injection	50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 21
Off Isolation	−67			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 22
Channel-to-Channel Crosstalk	−99			dB typ	Adjacent channel; R_L = 50 V, C_L = 5 pF, f = 100 kHz; see Figure 25
	−67			dB typ	Adjacent switch; R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 23
Total Harmonic Distortion (THD + N)	0.01			%	R_L = 32 Ω, f = 20 Hz to 20 kHz, V_S = 1 V p-p
Insertion Loss	−0.04			dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
−3 dB Bandwidth	29			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
C_S (OFF)	60			pF typ	
C_D, C_S (ON)	115			pF typ	
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 3.6 V
		1	2	μA max	

[1] Temperature range, Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +6 V
Analog Inputs[1], Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 10 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	400 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP Package	
θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
θ_{JC} Thermal Impedance	27.6°C/W
16-Lead WLCSP Package	
θ_{JA} Thermal Impedance (4-Layer Board)	130°C/W
16-Lead LFCSP Package	
θ_{JA} Thermal Impedance (4-Layer Board)	30.4°C/W
IR Reflow, Peak Temperature <20 sec	235°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

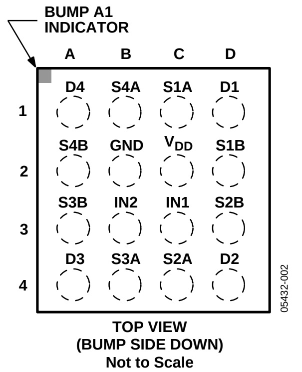
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



TOP VIEW
(Solder Bumps on Opposite Side)
Figure 2. 16-Lead WLCSP (CB-16)

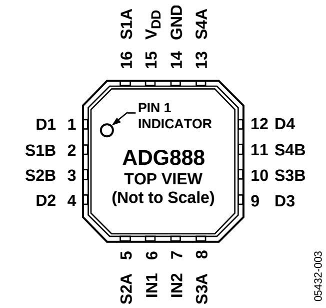


Figure 3. 16-Lead LFCSP_VQ (CP-16-4)

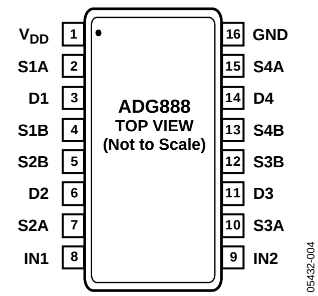


Figure 4. 16-Lead TSSOP (RU-16)

Table 4. Pin Function Descriptions

Bump No. WL CSP	Pin No. LFCSP_VQ	Pin No. TSSOP	Mnemonic	Description
2c	15	1	V_{DD}	Most Positive Power Supply Potential.
2b	14	16	GND	Ground (0 V) Reference.
1b, 1c, 2a, 2d, 3a, 3d, 4b, 4c	2, 3, 5, 8, 10, 11, 13, 16	2, 4, 5, 7, 10, 12, 13, 15	S	Source Terminal. May be an input or output.
1a, 1d, 4a, 4d	1, 4, 9, 12	3, 6, 11, 14	D	Drain Terminal. May be an input or output.
3b, 3c	6, 7	8, 9	IN	Logic Control Input.

TRUTH TABLE

Table 5.

Logic (IN1/IN2)	Switch 1A/2A/3A/4A	Switch 1B/2B/3B/4B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

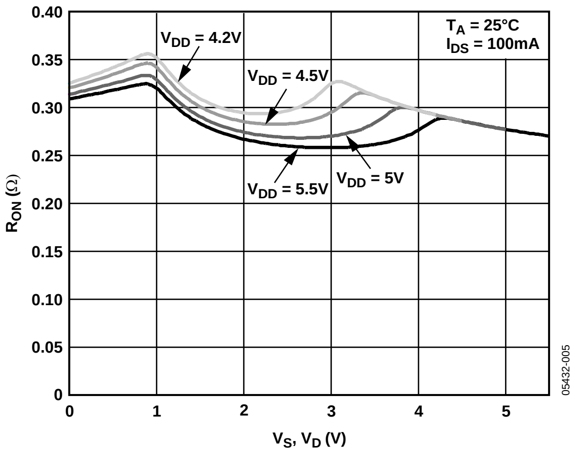


Figure 5. On Resistance vs. V_D (V_S) V_{DD} = 4.2 V to 5.5 V

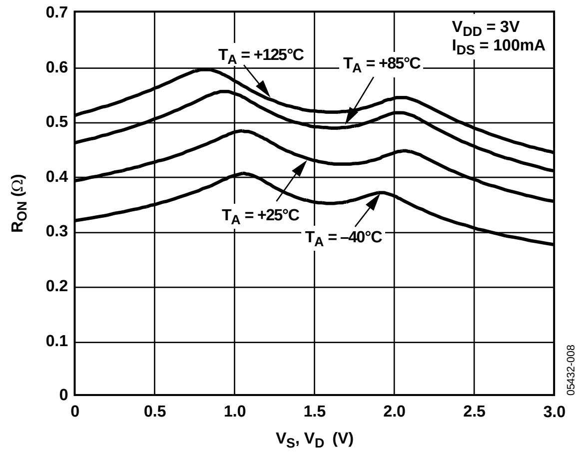


Figure 8. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 3 V

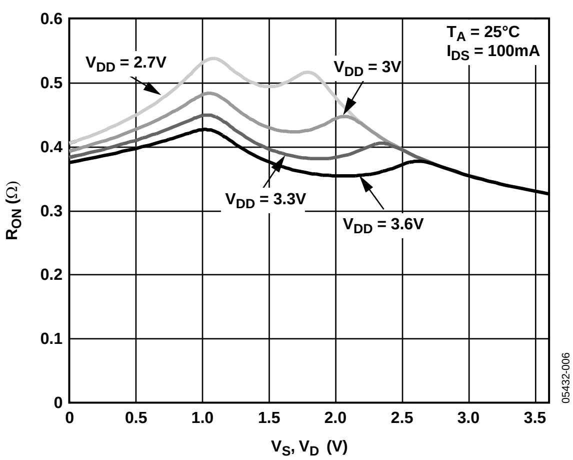


Figure 6. On Resistance vs. V_D (V_S) V_{DD} = 2.7 V to 3.6 V

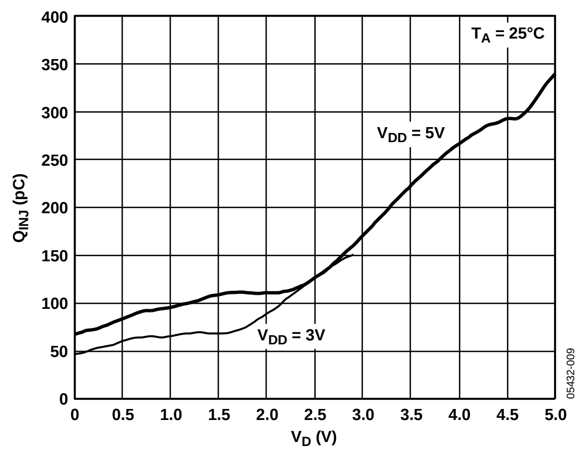


Figure 9. Charge Injection vs. Source Voltage

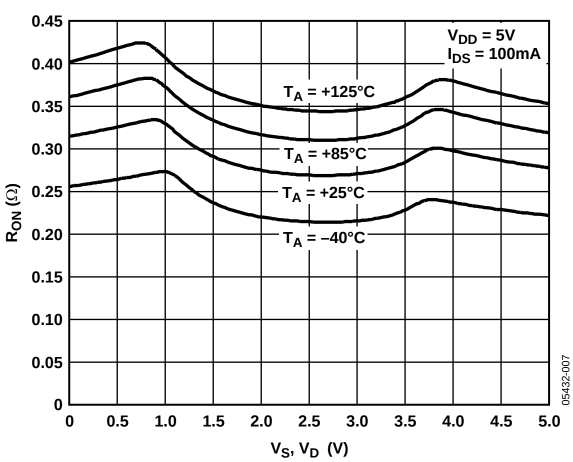


Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, V_{DD} = 5 V

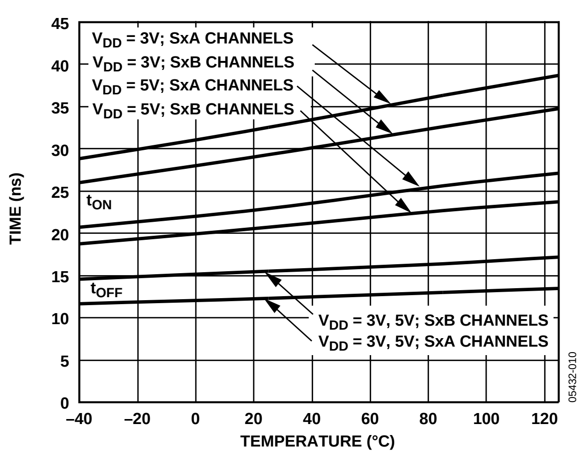


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

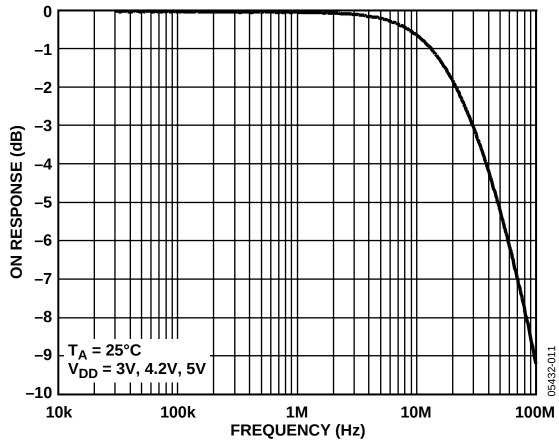


Figure 11. Bandwidth

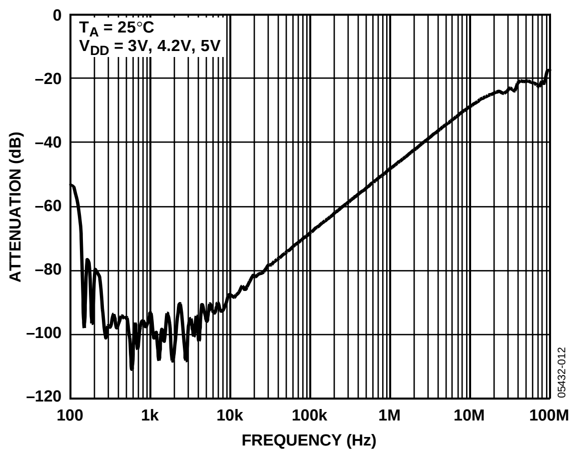


Figure 12. Off Isolation vs. Frequency

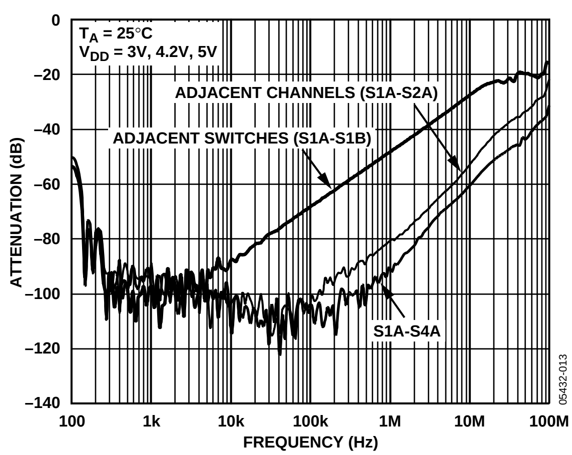


Figure 13. Crosstalk vs. Frequency

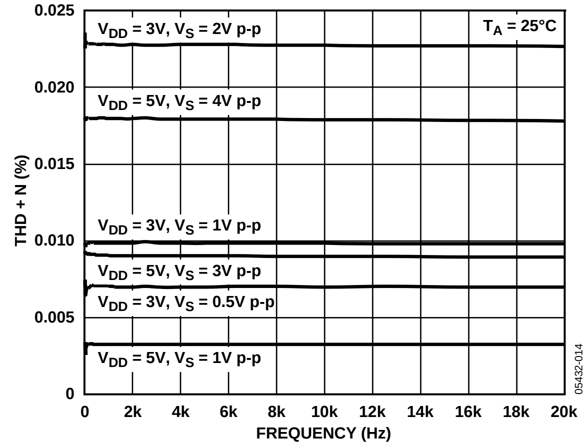


Figure 14. Total Harmonic Distortion + Noise (THD + N)

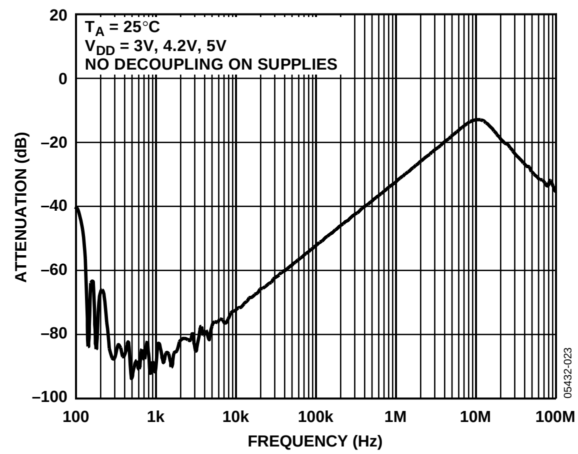


Figure 15. AC PSRR

TEST CIRCUITS

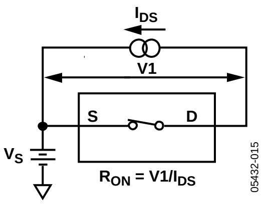


Figure 16. On Resistance

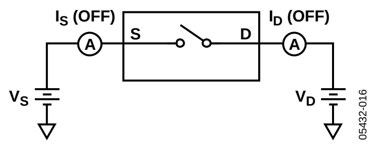


Figure 17. Off Leakage

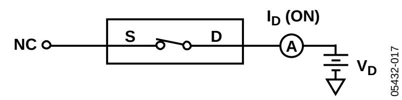


Figure 18. On Leakage

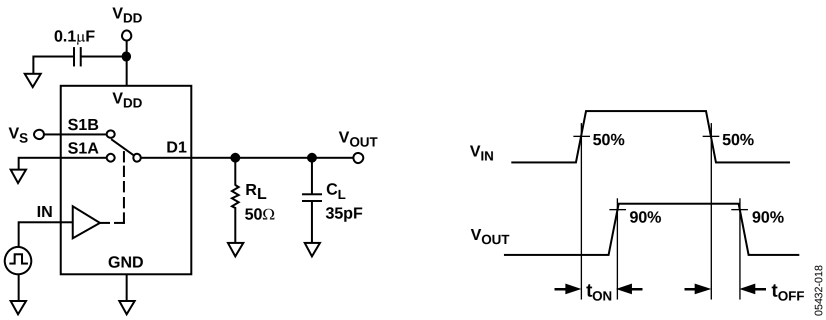


Figure 19. Switching Times, t_{ON}, t_{OFF}

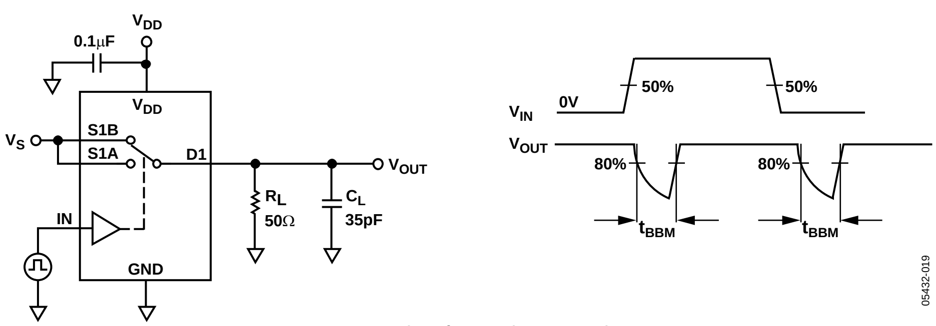


Figure 20. Break-Before-Make Time Delay, t_{BBM}

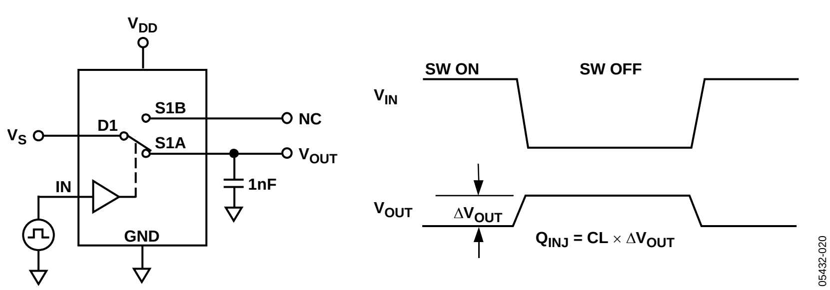
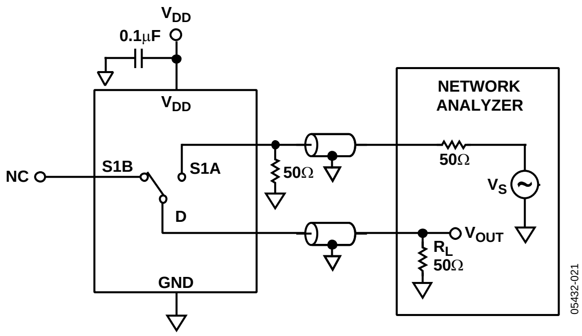
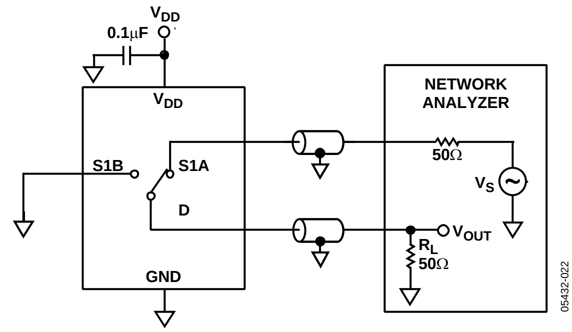


Figure 21. Charge Injection



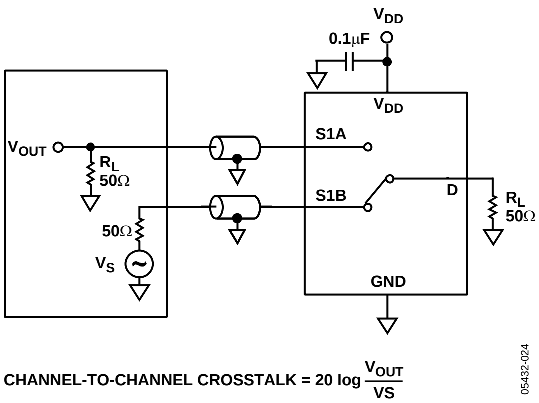
$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 22. Off Isolation



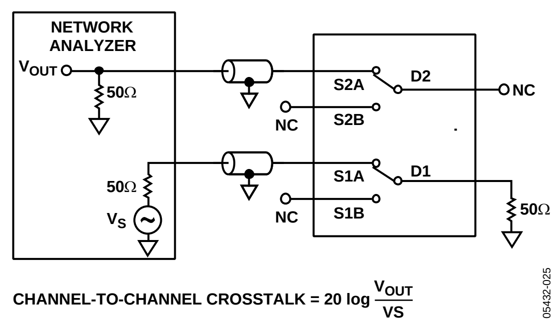
$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT}\ \text{WITH SWITCH}}{V_{OUT}\ \text{WITHOUT SWITCH}}$$

Figure 24. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 23. Channel-to-Channel Crosstalk (S1A to S1B)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{VS}$$

Figure 25. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}
Positive supply current.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On resistance match between any two channels.

I_S (OFF)
Source leakage current with the switch off.

I_D, I_S (ON)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (OFF)
Off switch source capacitance. Measured with reference to ground.

C_D, C_S (ON)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. This is specified for two conditions:

> Adjacent channel, that is, S1A to S2A, S1B to S2B, S3A to S4A, or S3B to S4B.
>
> Adjacent switch, that is, S1A to S1B, S2A to S2B, S3A to S3B, or S4A to S4B.

−3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitudes plus signal noise to the fundamental.

OUTLINE DIMENSIONS

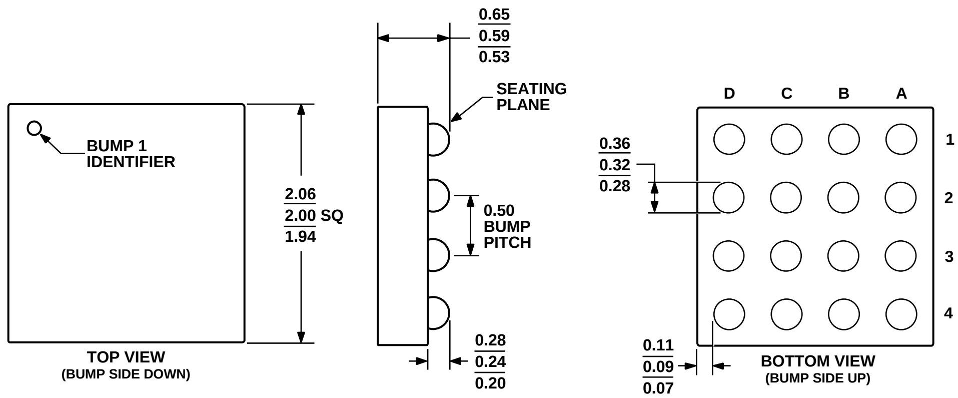
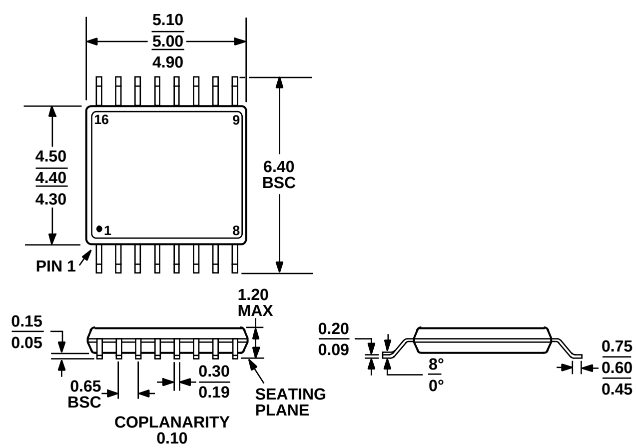
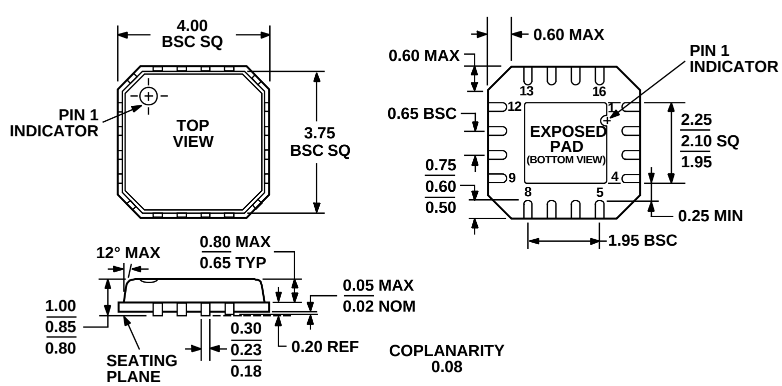


Figure 26. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 27. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 28. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG888YRUZ[2]	−40°C to +125°C	16 Lead Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG888YRUZ-REEL[2]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG888YRUZ-REEL7[2]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG888YCPZ-REEL[2]	−40°C to +125°C	16- Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-4	S0D
ADG888YCPZ-REEL7[2]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-4	S0D
ADG888YCBZ-REEL[2]	−40°C to +125°C	16-Ball Wafer Level Chip Scale Package (WLCSP)	CB-16	S0D
ADG888YCBZ-REEL7[2]	−40°C to +125°C	16-Ball Wafer Level Chip Scale Package (WLCSP)	CB-16	S0D

[1] Branding on these packages is limited to three characters due to space constraints.
[2] Z = Pb-free part.

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