

# Axcelerator Family FPGAs



## Leading-Edge Performance

- 350+ MHz System Performance
- 500+ MHz Internal Performance
- High-Performance Embedded FIFOs
- 700Mb/s LVDS Capable I/Os

## Specifications

- Up to 2 Million Equivalent System Gates
- Up to 684 I/Os
- Up to 10,752 Dedicated Flip-Flops
- Up to 339kbits Embedded SRAM/FIFO
- Manufactured on Advanced 0.15µm CMOS Antifuse Process Technology, 7 Layers of Metal

## Features

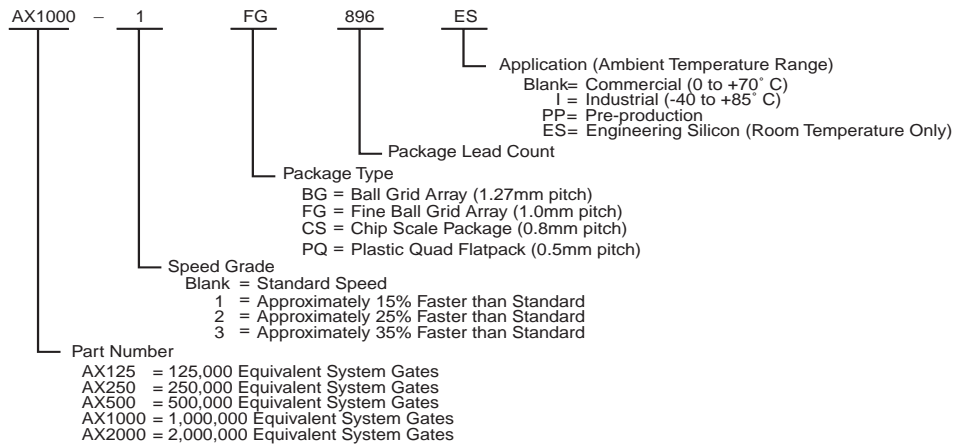
- Single-Chip, Nonvolatile Solution
- Up to 100% Resource Utilization with 100% Pin Locking
- 1.5V Core Voltage for Low Power
- Footprint Compatible Packaging
- Flexible, Multi-Standard I/Os:
  - 1.5V, 1.8V, 2.5V, 3.3V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTTL, LVCMOS, 3.3V PCI, and 3.3V PCI-X
  - Differential I/O Standards: LVPECL and LVDS

- Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
- Registered I/Os with 64-bit Deep FIFO on Each Pin ("PerPin FIFO")
- Hot-Swap Compliant I/Os (Except PCI)
- Programmable Slew Rate and Drive Strength on Outputs
- Programmable Delay and Weak Pull-Up/Pull-Down Circuits on Inputs
- Embedded Memory:
  - Variable-Aspect 4,608-bit RAM Blocks (x1, x2, x4, x9, x18, x36 Organizations Available)
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
  - ROM Emulation Capability
- Segmentable Clock Resources
- Embedded Phase-Locked Loop:
  - 14-200 MHz Input Range
  - Frequency Synthesis Capabilities up to 1 GHz
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability with Actel Silicon Explorer II
- Boundary-Scan Testing Compliant with IEEE Standard 1149.1 (JTAG)
- FuseLock™ Secure Programming Technology Prevents Reverse Engineering and Design Theft

## Axcelerator Family Product Profile

Device	AX125	AX250	AX500	AX1000	AX2000
<b>Capacity (in Equivalent System Gates)</b>	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
<b>Modules</b>					
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
<b>Embedded RAM/FIFO</b>					
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Number of PerPin FIFOs	168	248	336	516	684
Total PerPin FIFO Bits	10,752	15,872	21,504	33,024	43,776
Total Embedded RAM Bits	29,184	71,168	95,232	198,912	338,688
<b>Clocks (Segmentable)</b>					
Hardwired	4	4	4	4	4
Routed	4	4	4	4	4
<b>PLLs</b>	8	8	8	8	8
<b>I/Os</b>					
I/O Banks	8	8	8	8	8
I/O Blocks	8	8	16	24	32
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1008	1548	2052
<b>Package</b>					
CSP	180				
PQFP		208	208		
BGA				729	
FBGA	256, 324	256, 484	484, 676	484, 676, 896	896, 1152

## Ordering Information



## Product Plan

	Speed Grade				Application	
	Std	-1	-2	-3	C	I
<b>AX125 Device</b>						
180-Pin Chip Scale Package (CSP)	P	P	P	P	P	P
256-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
324-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
<b>AX250 Device</b>						
208-Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	P
256-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
484-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
<b>AX500 Device</b>						
208-Plastic Quad Flat Pack (PQFP)	P	P	P	P	P	P
484-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
676-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
<b>AX1000 Device</b>						
484-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
676-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
729-Pin Ball Grid Array (BGA)	P	P	P	P	P	P
896-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
<b>AX2000 Device</b>						
896-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P
1152-Pin Fine Pitch Ball Grid Array (FBGA)	P	P	P	P	P	P

Contact your Actel sales representative for package availability.

Applications: C = Commercial    Availability: ✓ = Limited Availability. Contact your Actel Sales representative for the latest availability information.  
 I = Industrial  
 P = Planned

## Device Resources

Device	User I/Os (including clock buffers)				
	AX125	AX250	AX500	AX1000	AX2000
CS180	98				
PQ208		115	115		
FG256	138	138			
FG324	168				
FG484		248	317	317	
FG676			336	418	
BG729				516	
FG896				516	586
FG1152					684

**Package Definitions:** FBGA = Fine Ball Grid Array, CSP = Chip-Scale Package, BGA = Ball Grid Array  
 The FG256, FG324 and FG484 are footprint compatible with each other. The FG676, FG896 and FG1152 are also footprint compatible with each other.

## General Description

Actel's newest FPGA family, Accelerator, offers high performance at densities of up to two million equivalent system gates. Based upon Actel's new AX architecture, Accelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, PerPin FIFOs, and carry logic.

### Device Architecture

Actel's AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1). The entire floor of the AX device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing, unlike SRAM FPGAs where chip area is lost to routing.

### Programmable Interconnect Element

The Accelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 2 on page 4). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs), and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry.

The extremely small size of these interconnect elements gives the Accelerator family abundant routing resources and provides excellent protection against design piracy and cloning (FuseLock technology). Reverse engineering is virtually impossible because it is extremely difficult to distinguish between programmed and unprogrammed antifuses, and since Accelerator devices are nonvolatile, single-chip solutions, there is no configuration bitstream to intercept or read out (see Security in the "Special Fuses" section on page 108).

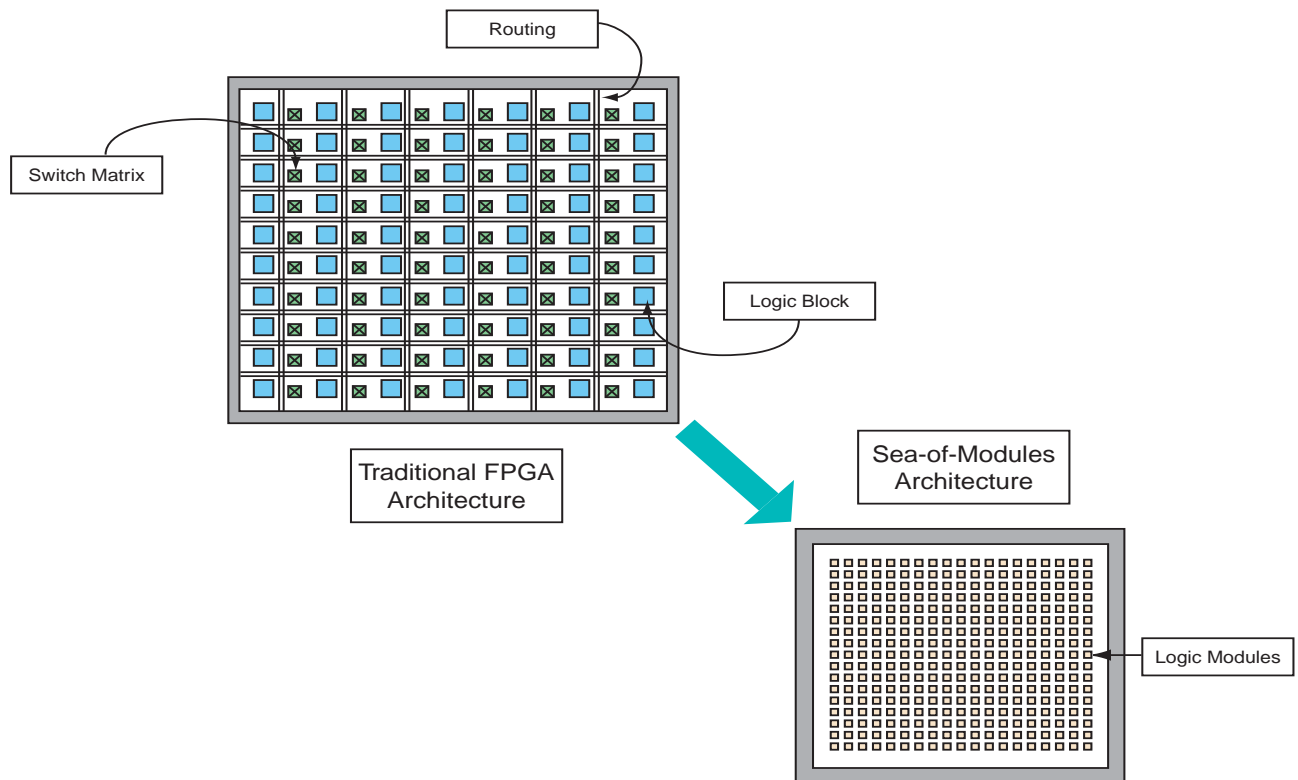
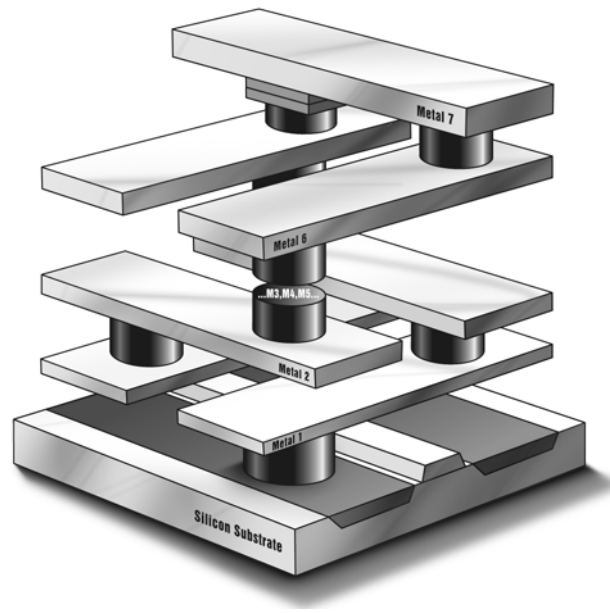


Figure 1 • Sea-of-Modules Comparison



**Figure 2 • Accelerator Family Interconnect Elements**

## Logic Modules

Actel's Accelerator family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell). The AX C-cell can implement more than 4,000 combinatorial functions of up to 5 inputs (Figure 3 on page 5). The C-cell contains carry logic for even more efficient implementation of arithmetic functions. With its small size, the C-cell structure is extremely synthesis-friendly, simplifying the overall design as well as reducing design time.

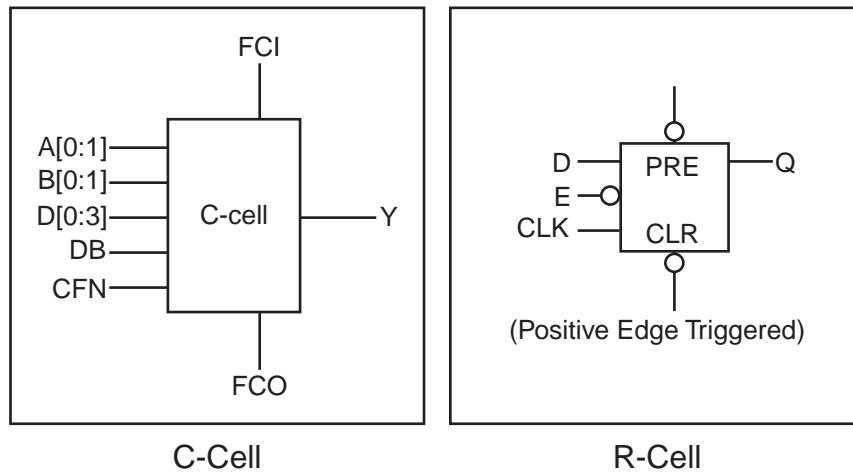
The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 3 on page 5). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hard-wired clocks, the routed clocks, or the internal logic.

Two C-cells, a single R-cell, and two Transmit (TX) and two Receive (RX) routing buffers form a Cluster, and two Clusters comprise a SuperCluster (Figure 4 on page 5). Each SuperCluster contains an independent Buffer module, which supports automatic buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

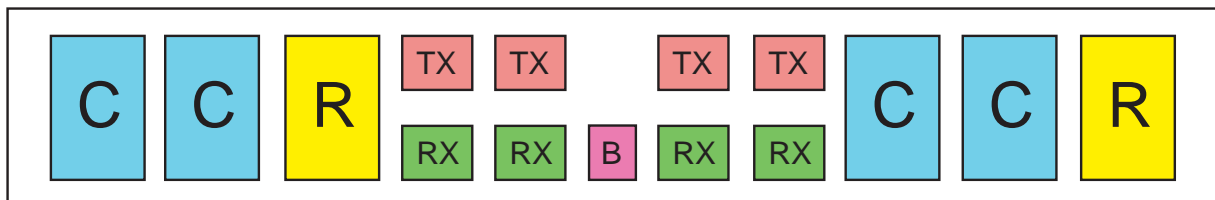
The logic modules within the SuperCluster are arranged so that two combinatorial modules are side by side, giving a C-C-R - C-C-R pattern to the SuperCluster. This C-C-R pattern enables efficient implementation (minimum delay) of 2-bit carry logic for improved arithmetic performance (Figure 5 on page 5).

The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

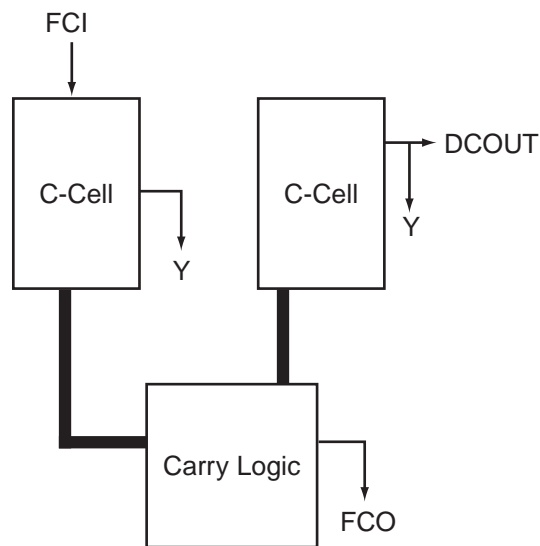
At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and 3 SRAM blocks for the AX250). The SRAM blocks are arranged in a column on the west side of the tile (Figure 6 on page 6). For example, the AX1000 is composed of a 3x3 array of 9 core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1 on page 6).



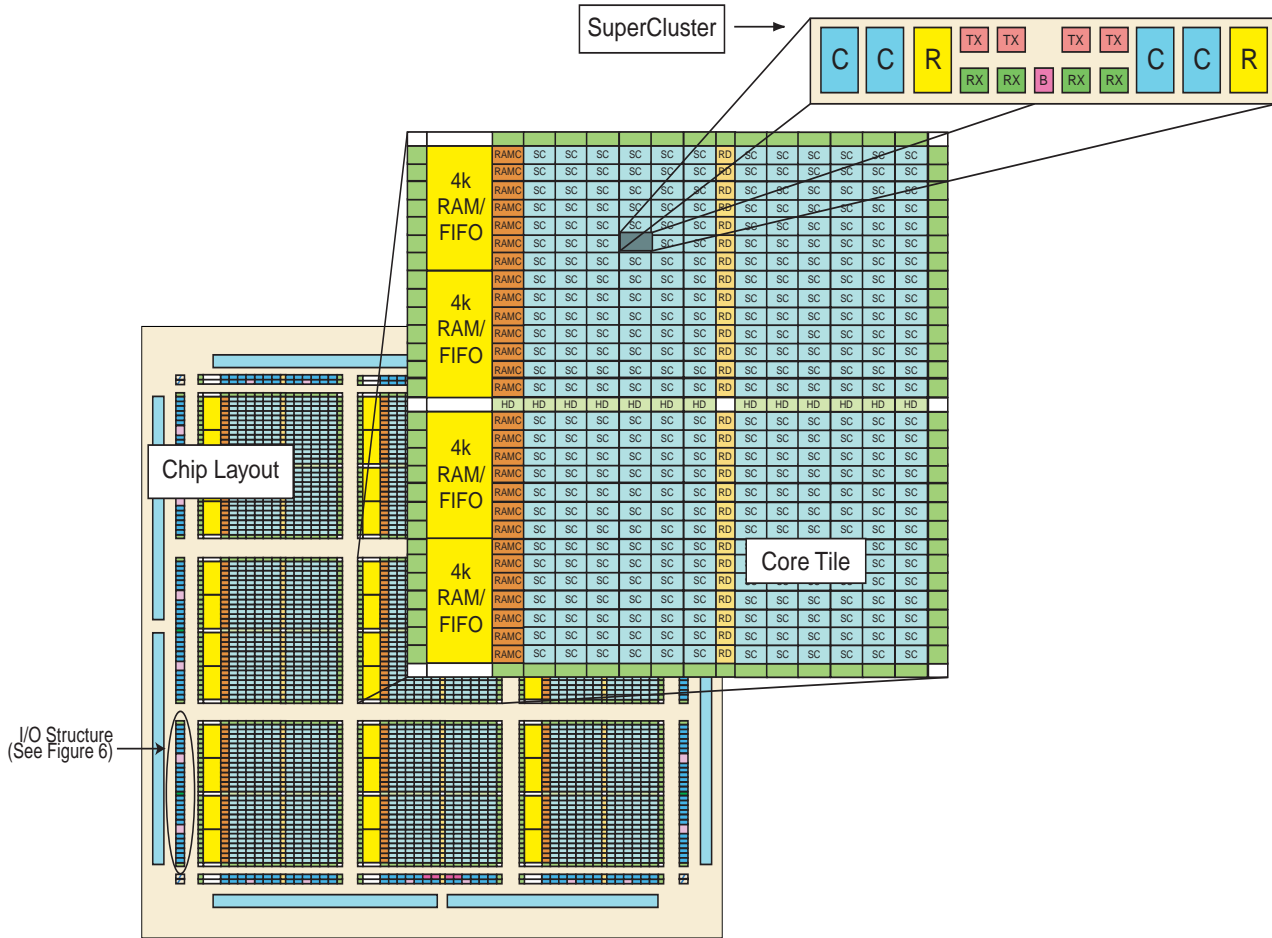
**Figure 3 • AX C-Cell and R-Cell**



**Figure 4 • AX SuperCluster**



**Figure 5 • AX 2-bit Carry Logic**



**Figure 6 • AX Device Architecture (AX1000 shown)**

**Table 1 • Number of Core Tiles per Device**

Device	Number of Core Tiles
AX125	1 regular tile
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

## Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by 8 and read out by 1. The embedded SRAM blocks can be initialized at power up via the device JTAG port (ROM emulation mode).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

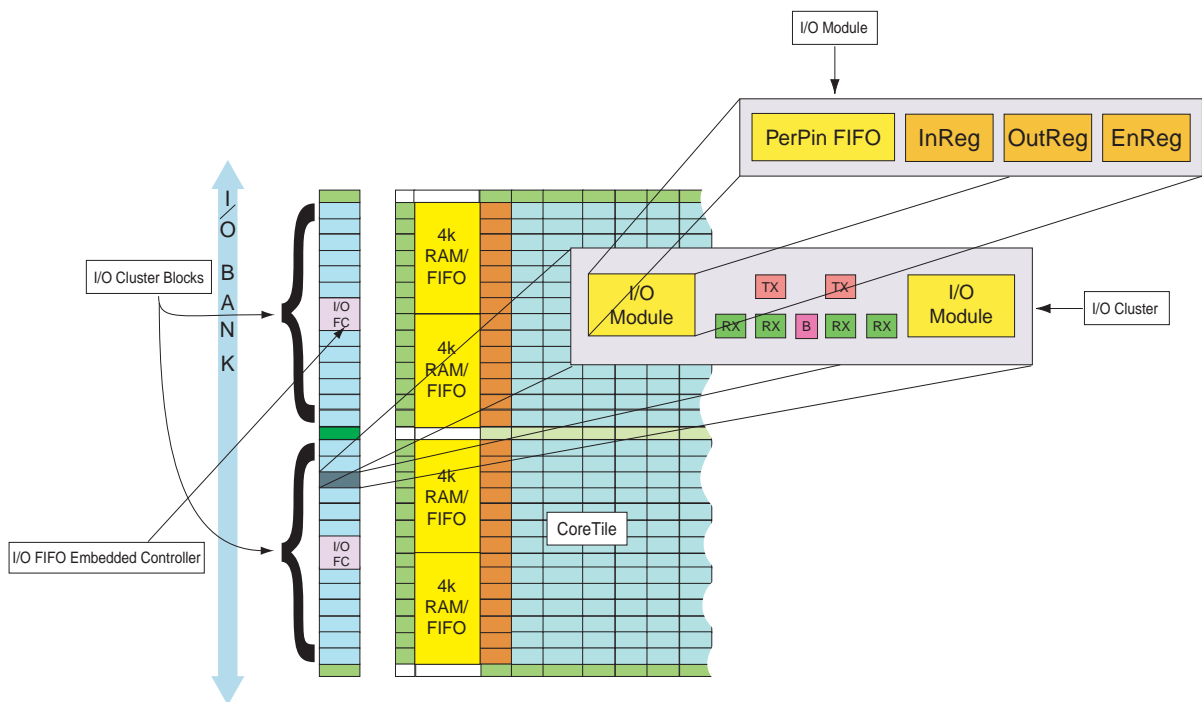
## I/O Logic

The Accelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Accelerator FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (2 per side). The configuration of these banks determines the I/O standards supported (see the “User I/Os” section on page 19 for more information).

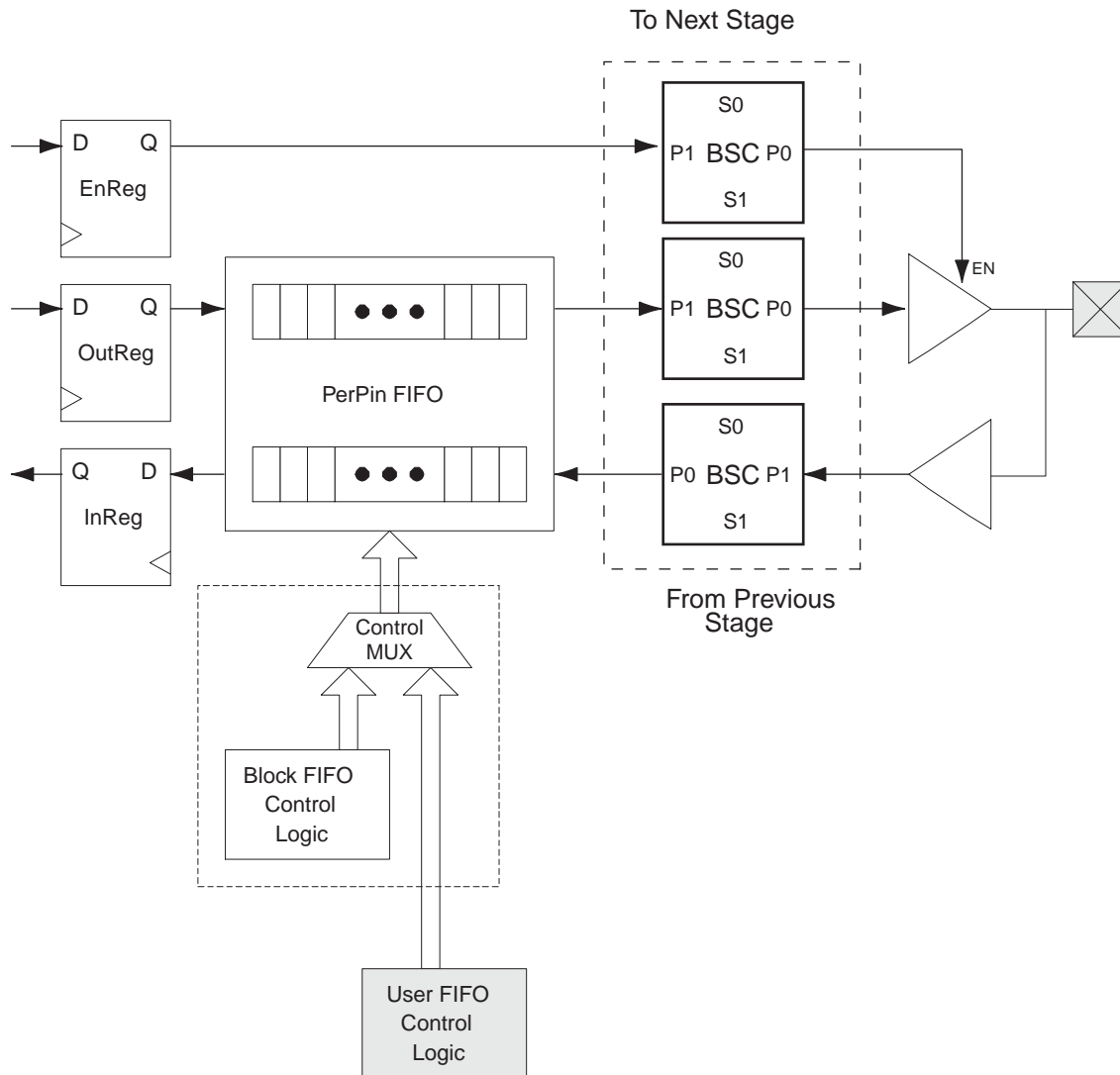
Each I/O module has an input register (InReg), an output register (OutReg), an enable register (EnReg), and a PerPin FIFO (Figure 7). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module. While I/O pads are organized into banks (for configuring I/O standards), the I/O Clusters are organized into blocks for control of the PerPin FIFOs. This is also illustrated in Figure 7.

Unique to the AX architecture is a 64-bit, bidirectional PerPin (I/O) FIFO, enabling buffering of either input or output data, as illustrated in Figure 8 on page 8. Note that the boundary-scan cells (BSC) associated with the I/O are also shown in Figure 8 on page 8. The PerPin FIFO can be bypassed if desired. This allows the designer to build input or output FIFOs directly adjacent to the pins without using any of the internal FPGA resources.

PerPin FIFOs are organized into blocks of up to 26 pins (up to 34 in the AX250) (Figure 8 on page 8). This means that they can be controlled by the built-in I/O FIFO Embedded Controller. Refer to the “PerPin FIFO” section on page 81 for more information. Each PerPin FIFO can be exempted from the I/O FIFO Embedded Controller and can be individually controlled from internal logic. Like its RAM FIFO counterpart, the I/O FIFO Embedded Controller provides FULL and EMPTY flags as well as programmable AFULL and AEMPTY flags.



**Figure 7 • I/O Cluster Arrangement**



**Figure 8 • PerPin FIFO Structure**



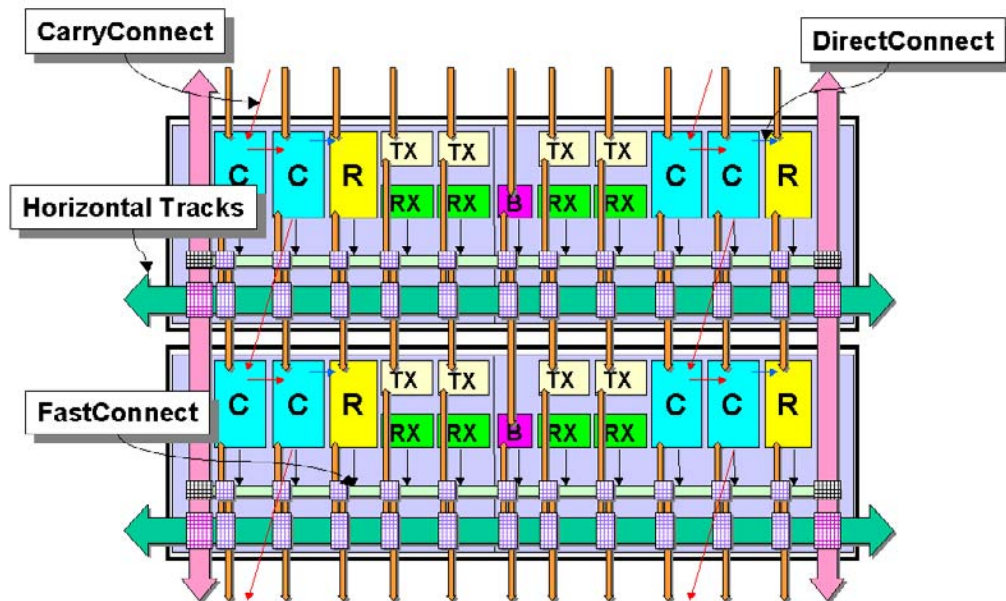
## Routing

The AX hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together. For the I/O routing structures (Figure 9). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the FCO output of one 2-bit, C-cell carry logic to the FCI input of the 2-bit, C-cell carry logic of the SuperCluster below it. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. In SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the track as well as segmented routing of varying lengths.



**Figure 9 • AX Routing Structures**

## Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 3 on page 5).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power up.

Each HCLK and CLK have an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency between 20 MHz and 1 GHz. Different PLLs can be cascaded to create complex frequency combinations.

In addition, the PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250ps increments. The reference clock needed to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

## Low Power (LP) Mode

The AX architecture was created for high performance designs, and includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled, outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source ( $V_{PUMP}$ ) to the device to bypass the internal charge pump (See the “[Low Power Mode](#)” section on [page 107](#) for more information).

## Design Environment

The Axcelerator family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment ([Figure 10 on page 11](#)). Libero IDE includes Synplify® for Actel from Synplify®, ViewDraw for Actel from Mentor Graphics, ModelSim™ HDL Simulator from Model Technology™, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Actel.

Actel's Designer software provides a comprehensive suite of backend development tools for FPGA development. The Designer software includes timing-driven place-and-route, a world-class integrated static timing analyzer and constraints editor, a design netlist schematic viewer, and SmartPower, a tool that allows the user to quickly estimate

the power consumption in a design. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, our back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplify, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and Unix operating systems.

## Programming

Programming support is provided through Actel's Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. Factory programming is available for high-volume production needs.

## In-System Diagnostic and Debug Capabilities

The Axcelerator FPGA series includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation. Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled by Silicon Explorer II ([Figure 11 on page 11](#)), Actel's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See the “[Silicon Explorer II Probe](#)” section on [page 108](#)).

## Summary

Actel's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, high-speed I/Os, and PerPin FIFOs. The Axcelerator family also provides the designer with high performance and efficient device utilization at high gate counts – even with fixed pins.

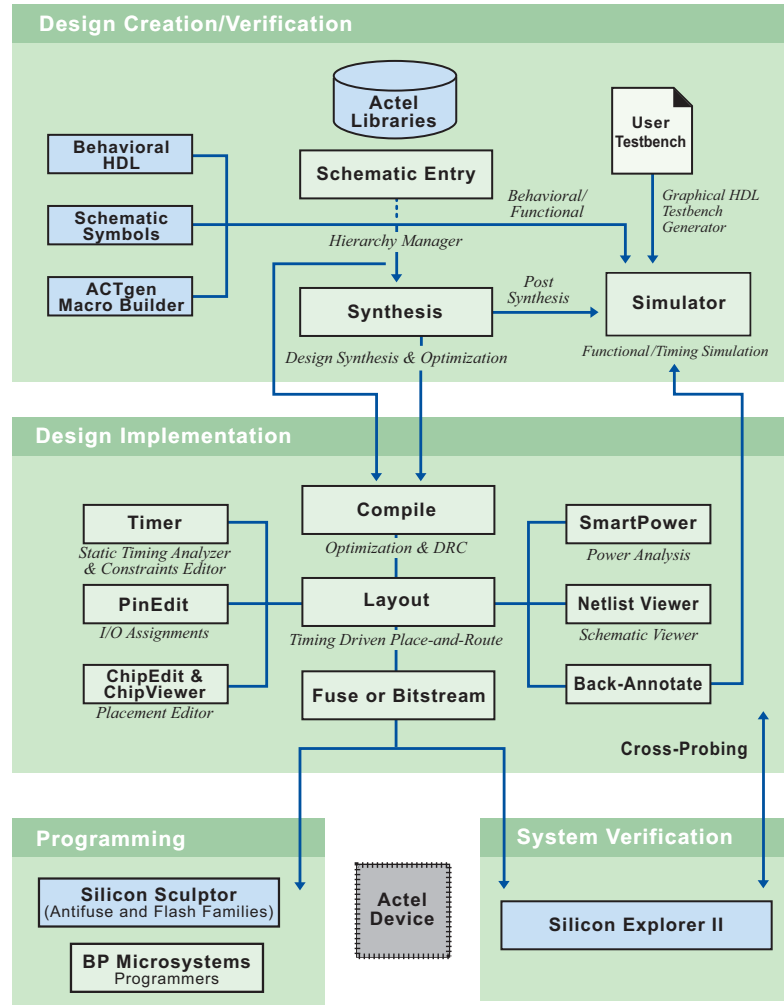


Figure 10 • Design Flow

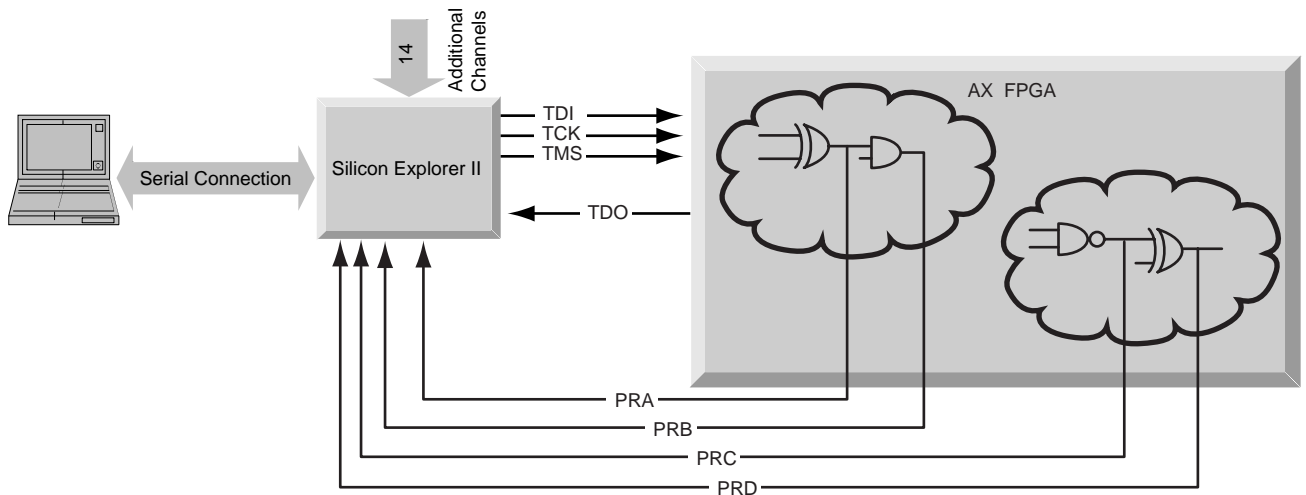


Figure 11 • Probe Setup

# General Specifications

## Supply Voltages

V <sub>CCA</sub>	V <sub>CCI</sub>	Input Tolerance	Output Drive Level
1.5V	1.5V	3.3V	1.5V
1.5V	1.8V	3.3V	1.8V
1.5V	2.5V	3.3V	2.5V
1.5V	3.3V	3.3V	3.3V

## I/O Features Comparison

I/O Assignment	Clamp Diode	Hot Insertion/ 3.3V Tolerance <sup>1</sup>	5V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes <sup>2</sup>	Enabled/Disabled	
3.3V PCI, 3.3V PCI-X	Yes	No	Yes <sup>3</sup>	Enabled/Disabled	
LVC MOS2.5V	No	Yes	No	Enabled/Disabled	
LVC MOS1.8V	No	Yes	No	Enabled/Disabled	
LVC MOS1.5V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled <sup>4</sup>
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled <sup>5</sup>
I/O used as V <sub>REF</sub> pin	No	No	No	Disabled	Disabled

### Notes:

1. All the I/O standards except 3.3V PCI and 3.3V PCI-X are capable of both hot insertion and 3.3V tolerance.
2. Can be implemented with an IDT bus switch.
3. Can be implemented with an external resistor.
4. The OE input of the output buffer must be de-asserted permanently (handled by software).
5. The OE input of the output buffer must be asserted permanently (handled by software).

## 5V Tolerance

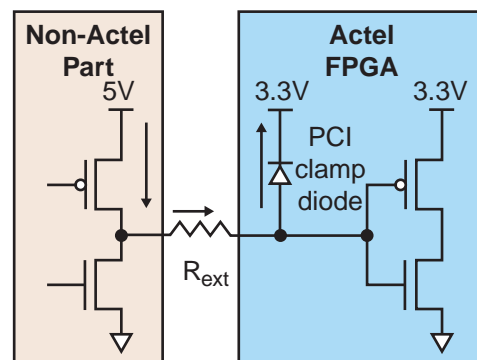
There are two schemes to achieve 5V tolerance:

1. 3.3V PCI and 3.3V PCI-X are the only I/O standards that allow 5V tolerance. To implement this, an internal clamp diode between the input pad and the V<sub>CCI</sub> pad is enabled so that the voltage at the input pin is clamped in Equation 1:

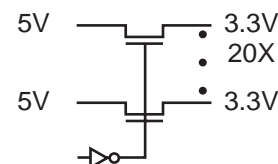
$$V_{\text{input}} = V_{\text{CCI}} + V_{\text{diode}} = 3.3\text{V} + 0.8\text{V} = 4.1\text{V} \quad (1)$$

An external series resistor (~100Ω) is required between the input pin and the 5V signal source to limit the current (Figure 12).

2. 5V tolerance can also be achieved with 3.3V I/O standards (3.3V PCI, 3.3V PCI-X, and LVTTL) using a bus-switch product (e.g. IDTQS32X2384). This will convert the 5V signal to a 3.3V signal with minimum delay (Figure 13).



**Figure 12 • Use of an External Resistor for 5V Tolerance**



**Figure 13 • Bus Switch IDTQS32X2384**

## Operating Conditions

### Absolute Maximum Conditions

Stresses beyond those listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for

extended periods may affect device reliability. Devices should not be operated outside the "Recommended Operating Conditions" table.

### Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
$V_{CCA}$	DC Core Supply Voltage	TBD	V
$V_{CCI}$	DC I/O Supply Voltage	TBD	V
$V_{REF}$	DC I/O Reference Voltage	TBD	V
$V_I$	Input Voltage	TBD	V
$V_O$	Output Voltage	TBD	V
$T_{STG}$	Storage Temperature	-60 to +150	°C
$V_{CCDA}^*$	Supply Voltage for Differential I/Os	TBD	V

**Note:** \* Should be the maximum of all  $V_I$ .

### Recommended Operating Conditions

Parameter Range	Commercial	Industrial	Units
Ambient Temperature ( $T_A$ ) <sup>1</sup>	0 to +70	-40 to +85	°C
1.5V Core Supply Voltage	1.4 to 1.6	1.4 to 1.6	V
1.5V I/O Supply Voltage	1.4 to 1.6	1.4 to 1.6	V
1.8V I/O Supply Voltage	1.7 to 1.9	1.7 to 1.9	V
2.5V I/O Supply Voltage <sup>2</sup>	2.3 to 2.7	2.3 to 2.7	V
3.3V I/O Supply Voltage	3.0 to 3.6	3.0 to 3.6	V
2.5V $V_{CCDA}$ I/O Supply Voltage (no differential I/O used)	2.3 to 2.7	2.3 to 2.7	V
3.3V $V_{CCDA}$ I/O Supply Voltage (differential or voltage-referenced I/O used)	3.0 to 3.6	3.0 to 3.6	V
3.3V $V_{PUMP}$ Supply Voltage	3.0 to 3.6	3.0 to 3.6	V

**Notes:**

1. Ambient temperature ( $T_A$ ) is used for commercial and industrial; case temperature ( $T_C$ ) is used for military.
2. 2.375V to 2.65V for LVDS operation.

## Calculating Power Dissipation

### Standby Power

Device		AX125		AX250		AX500		AX1000		AX2000	
Symbol	Parameter	25°C	85°C	25°C	85°C	25°C	85°C	25°C	85°C	25°C	85°C
$I_{CC}$	Standby Current (Core)	3mA		6mA		10mA		20mA		40mA	
$I_{CCBANK}$	Standby Current per I/O Bank <ul style="list-style-type: none"> <li>Active</li> <li>Low Power mode</li> </ul>										
$I_{CCPLL}$	Standby Current per PLL <ul style="list-style-type: none"> <li>Active</li> <li>Low Power mode</li> </ul>										
$I_{CCCP}$	Standby Current, Charge Pump <ul style="list-style-type: none"> <li>Active</li> <li>Low Power mode</li> </ul>										

**Note:** Values shown for 25°C are typical; 85°C values represent worst-case operation conditions.

### Default $C_{load}/V_{CCI}$

	$C_{load}$	$V_{CCI}$	$P(\mu W/MHz)^*$
<b>Single-Ended without <math>V_{REF}</math></b>			
LVTTL	35 pF	3.3V	381.15
LVC MOS – 25	35 pF	2.5V	218.75
LVC MOS – 18	35 pF	1.8V	113.40
LVC MOS – 15 (JESD8-11)	35 pF	1.8V	TBD
PCI	10 pF	3.3V	108.9
PCI-X	10 pF	3.3V	108.9
<b>Single-Ended with <math>V_{REF}</math></b>			
HSTLI	20 pF	1.5V	45.0
SSTL – 2I	30 pF	2.5V	187.5
SSTL – 2II	30 pF	2.5V	187.5
SSTL – 3I	30 pF	3.3V	326.7
SSTL – 3II	30 pF	3.3V	326.7
<b>Voltage-Referenced</b>			
GTLP – 25	N/A	2.5V	TBD
GTLP – 33	N/A	3.3V	TBD
<b>Differential</b>			
LVPECL – 33	N/A	3.3V	TBD
LVDS – 25	N/A	2.5V	TBD

**Note:** \*  $P_{load}$  is the dynamic power due to the charging/discharging of an output load. Typical formula is  $P_{load} = C_{load} * V_{CCI}^2$ .

## Different Components Contributing to the Total Power Consumption in Axcelerator Devices

Component	Definition	Device Specific Value (in $\mu\text{W}/\text{MHz}$ )				
		AX125	AX250	AX500	AX1000	AX2000
P1	Core tile HCLK power component	33	TBD	71	130	216
P2	R-cell power component	0.2	TBD	0.2	0.2	0.2
P3	HCLK signal power dissipation	4.5	TBD	9	13.5	18
P4	Core tile RCLK power component	33	TBD	71	130	216
P5	R-cell power component	0.3	TBD	0.3	0.3	0.3
P6	RCLK signal power dissipation	6.5	TBD	13	19.5	26
P7	Power dissipation due to the switching activity on the R-cell	1.6	TBD	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	TBD	1.4	1.4	1.4
P9	Power component associated with the input voltage	10	TBD	10	10	10
P10	Power component associated with the output voltage	90	TBD	90	90	90
P11	Power component associated with the read operation in the RAM block	25	TBD	25	25	25
P12	Power component associated with the write operation in the RAM block	30	TBD	30	30	30
P13	Core PLL power component	TBD	TBD	TBD	TBD	TBD
P14	Power dissipation due to the clock output of the PLL	TBD	TBD	TBD	TBD	TBD
P15	Power dissipation due to the clock output of the PLL	TBD	TBD	TBD	TBD	TBD

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}}$$

$$P_{\text{dc}} = \text{TBD}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}}$$

$$P_{\text{HCLK}} = (P1 + P2 * s + P3 * \text{sqrt}[s]) * F_s$$

$s$  = is the number of R-cells clocked by this clock

$F_s$  = the clock frequency

$$P_{\text{CLK}} = (P4 + P5 * s + P6 * \text{sqrt}[s]) * F_s$$

$s$  = the number of R-cells clocked by this clock

$F_s$  = is the clock frequency

$$P_{\text{R-cells}} = P7 * ms * F_s$$

$ms$  = is the number of R-cells switching at each  $F_s$  cycle

$F_s$  = is the clock frequency

$$P_{\text{C-cells}} = P8 * mc * F_s$$

$mc$  = is the number of C-cells switching at each  $F_s$  cycle

$F_s$  = is the clock frequency

$$P_{\text{inputs}} = P9 * pi * F_{pi}$$

$pi$  = is the number of inputs

$F_{pi}$  = is the average input frequency

$$P_{\text{outputs}} = (P10 + C_{\text{load}} * V_{\text{CCI}}^2) * po * F_{po}$$

$C_{\text{load}}$  = the output load (technology dependent)

$V_{\text{CCI}}$  = the output voltage (technology dependent)

$po$  = the number of outputs

$F_{po}$  = the average output frequency

$$P_{\text{memory}} = P11 * N_{\text{block}} * F_{\text{RCLK}} + P12 * N_{\text{block}} * F_{\text{WCLK}}$$

$N_{\text{block}}$  = the number of RAM/FIFO blocks (1 block = 4k)

$F_{\text{RCLK}}$  = the read-clock frequency of the memory

$F_{\text{WCLK}}$  = the write-clock frequency of the memory

$$P_{\text{PLL}} = P13 * F_{\text{RefCLK}} + P14 * F_{\text{CLK1}} + P15 * F_{\text{CLK2}}$$

P13 = TBD

P14 = TBD

P15 = TBD

$F_{\text{RefCLK}}$  = the clock frequency of the clock input of the PLL

$F_{\text{CLK1}}$  = the clock frequency of the first clock output of the PLL

$F_{\text{CLK2}}$  = the clock frequency of the second clock output of the PLL

### Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, 1 C-cell, 1 reset input, and 1 output.

This design uses one HCLK at 100 MHz.

$ms = 1,080$  (in a shift register 100% of R-cells are toggling at each clock cycle)

$F_s = 100$  MHz

$s = 1080$

$$\Rightarrow P_{\text{HCLK}} = (P1 + P2 * s + P3 * \text{sqrt}[s]) * F_s = 79 \text{ mW}$$

and  $F_s = 100$  MHz

$$\Rightarrow P_{\text{R-cells}} = P7 * ms * F_s = 173 \text{ mW}$$

$mc = 1$  (1 C-cell in this shift-register)

and  $F_s = 100$  MHz

$$\Rightarrow P_{\text{C-cells}} = P8 * mc * F_s = 0.14 \text{ mW}$$

$F_{\text{pi}} \sim 0$  MHz

and  $pi = 1$  (1 reset input  $\Rightarrow$  this is why  $F_{\text{pi}}=0$ )

$$\Rightarrow P_{\text{inputs}} = P9 * pi * F_{\text{pi}} = 0 \text{ mW}$$

$F_{\text{po}} = 50$  MHz

$C_{\text{load}} = 35$  pF

$V_{\text{CCI}} = 3.3$  V

and  $po = 1$

$$\Rightarrow P_{\text{outputs}} = (P10 + C_{\text{load}} * V_{\text{CCI}}^2) * po * F_{\text{po}} = 24 \text{ mW}$$

No RAM/FIFO in this shift-register

$$\Rightarrow P_{\text{memory}} = 0 \text{ mW}$$

No PLL in this shift-register

$$\Rightarrow P_{\text{PLL}} = 0 \text{ mW}$$

$$P_{\text{ac}} = P_{\text{HCLK}} + P_{\text{CLK}} + P_{\text{R-cells}} + P_{\text{C-cells}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{PLL}} = 276 \text{ mW}$$

$P_{\text{dc}} = \text{TBD}$

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}} = \text{TBD}$$



## Thermal Characteristics

### Introduction

The temperature variable in Actel's Designer Series software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature. Equation 2 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_a \quad (2)$$

Where:

$T_a$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient

$$\Delta T = \theta_{ja} * P \quad (3)$$

$\theta_{ja}$  = Junction to ambient of package.  $\theta_{ja}$  numbers are located in the "Package Thermal Characteristics" table.

### Package Thermal Characteristics

The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates.

The absolute maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja}(\text{}^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{14^\circ\text{C/W}} = 5.71\text{W}$$

### Package Thermal Characteristics

Package Type	Pin Count	$\theta_{jc}$	Still Air	$\theta_{ja}$ 1.0m/s	$\theta_{ja}$ 2.5m/s	Units
Chip Scale Package (CSP)	180	TBD	57.8	51.0	TBD	C/W
Plastic Quad Flat Pack (PQFP)	208	TBD	26	23.5	20.9	C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	C/W
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	C/W
Fine Pitch Ball Grid Array (FBGA)	324	TBD	25.8	22.1	20.9	C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	C/W

### Temperature and Voltage Timing Derating Factors

(Normalized to Worst-Case Commercial,  $T_J = 70^\circ\text{C}$ ,  $V_{CCA} = 1.425\text{V}$ )

$V_{CCA}$	Junction Temperature						
	$-55^\circ\text{C}$	$-40^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$125^\circ\text{C}$
1.4V	0.77	0.80	0.88	0.93	1.02	1.05	1.13
1.425V	0.75	0.78	0.86	0.91	1.00	1.03	1.11
1.5V	0.7	0.73	0.80	0.84	0.93	0.95	1.03
1.525V	0.68	0.71	0.78	0.82	0.91	0.93	1.01
1.6V	0.66	0.68	0.75	0.79	0.87	0.89	0.97

#### Notes:

- The user can set the junction temperature in Designer software to be any integer value in the range of  $-55^\circ\text{C}$  to  $175^\circ\text{C}$ .
- The user can set the core voltage in Designer software to be any value between 1.4V to 1.6V.

# I/O Specifications

## Pin Description

### Supply Pins

GND Ground

Low supply voltage.

$V_{CCA}$  Supply Voltage

Supply voltage for array (1.5V). See the “Supply Voltages” section on page 12 for more information.

$V_{CCIBx}$  Supply Voltage

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See the “Supply Voltages” section on page 12 and the “User I/Os” section on page 19 for more information.

$V_{CCDA}$  Supply Voltage

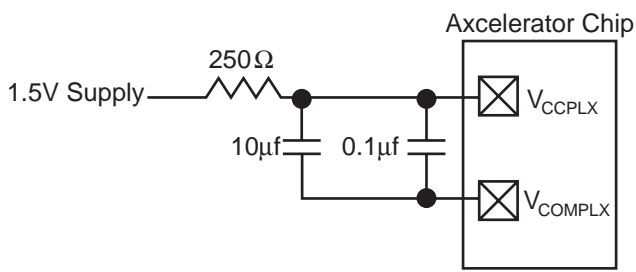
Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. See the “Supply Voltages” section on page 12 for more information.  $V_{CCDA}$  is either 3.3V or 2.5V.  $V_{CCDA}$  must use 3.3V when voltage referenced and/or differential is used. Additionally,  $V_{CCDA}$  must be greater than or equal to any  $V_{CCI}$  voltages (i.e.  $V_{CCDA} \geq V_{CCIBx}$ ).

$V_{CCPLA/B/C/D/E/F/G/H}$  Supply Voltage

PLL analog power supply (1.5V) for internal PLL. There are eight in each device.  $V_{CCPLA}$  supports the PLL associated with global resource HCLKA,  $V_{CCPLB}$  supports the PLL associated with global resource HCLKB, etc.

$V_{COMPLA/B/C/D/E/F/G/H}$  Supply Voltage

Compensation reference signals for internal PLL. There are eight in each device.  $V_{COMPLA}$  supports the PLL associated with global resource HCLKA,  $V_{COMPLE}$  supports the PLL associated with global resource CLKE, etc.



$V_{PUMP}$  Supply Voltage  
(External Pump)

In the low power mode,  $V_{PUMP}$  will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on  $V_{PUMP}$  reaches 3.3V.<sup>1</sup> In normal device operation, when using the internal charge pump,  $V_{PUMP}$  should be tied to GND.

### User-Defined Supply Pins

$V_{REF}$  Supply Voltage

Reference voltage for I/O banks.  $V_{REF}$  pins are configured by the user from regular I/O pins;  $V_{REF}$  are not in fixed locations. There can be one or more  $V_{REF}$  pins in an I/O bank.

$V_{TT}$  Board Termination Voltage

Refer to Table 1 on page 19 for more information.

### Global Pins

HCLKA/B/C/D Dedicated (Hard-wired)  
Clocks A, B, C and D

These pins are the clock input for sequential modules or north PLLs. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven.

CLKE/F/G/H Global Clocks  
E, F, G, and H

These pins are clock inputs for clock distribution networks or south PLLs. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). The clock input is buffered prior to clocking the R-cells.

### JTAG/Probe Pins

PRA/B/C/D Probe A/B/C/D

The Probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins’ probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK Test Clock

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

TDI Test Data Input

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal 10kΩ pull-up resistor.

<sup>1</sup>When  $V_{PUMP}=3.3V$ , it shuts off the internal charge pump. See the “Low Power Mode” section on page 107.

**TDO** Test Data Output  
Serial output for JTAG boundary-scan testing.

**TMS** Test Mode Select  
The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal 10k $\Omega$  pull-up resistor.

**TRST** Boundary Scan Reset Pin  
The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a programmable 10k $\Omega$  pull-up resistor (i.e. with or without the pull-up resistor).

## Special Functions

**LP** Low Power Pin  
The LP pin controls the low power mode of Axcelerator devices. The device is placed in the low power mode by connecting the LP pin to logic high. To exit the low power mode, the LP pin must be set LOW. Additionally, the LP pin must be set LOW during chip powering-up or chip powering-down operations. See the “Low Power Mode” section on page 107 for more details.

**NC** No Connection  
This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

## User I/Os<sup>2</sup>

### Introduction

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5V, 1.8V, 2.5V, and 3.3V) with its bank-selectable I/Os. Table 1 contains the I/O standards supported by the Axcelerator family.

*2Do not use an external resistor to pull the I/O above  $V_{CCI}$  for a higher logic “1” voltage level. The desired higher logic “1” voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above  $V_{CCI}$ .*

**Table 1 • I/O Standards Supported by the Axcelerator Family**

I/O Standard	Input/Output Supply Voltage ( $V_{CCI}$ )	Input Reference Voltage ( $V_{REF}$ )	Board Termination Voltage ( $V_{TT}$ )
LVTTTL	3.3	N/A	N/A
LVC MOS 2.5V	2.5	N/A	N/A
LVC MOS 1.8V	1.8	N/A	N/A
LVC MOS 1.5V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI, 3.3V PCI-X	3.3	N/A	N/A
GTL+ 3.3V	3.3	1.0	1.2
GTL+ 2.5V	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits.

All I/O standards are 3.3V tolerant, and I/O standards except 3.3V PCI and 3.3V PCI-X are capable of hot insertion. 3.3V PCI and 3.3V PCI-X are 5V tolerant with the aid of an external resistor (please see the “I/O Features Comparison” section on page 12).

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate the hold time requirement for input signals registered within the I/O cell. Note that the delay WILL be a function of process variations as well as temperature and voltage changes.

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). Each I/O also includes a dedicated FIFO with a fixed depth of 64. Every PerPin FIFO can buffer input data, output data, or be bypassed (See the “PerPin FIFO” section on page 81).

I/Os are organized into banks, and there are 8 banks per device – 2 per side (Figure 3 on page 26). Each I/O bank has a common  $V_{CCI}$ , the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus,  $V_{REF}$ . While  $V_{REF}$  must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a  $V_{REF}$ . Please note that output pins should not be located next to  $V_{REF}$  pins.

If voltage-referenced I/Os and/or differential I/Os are used, the differential amplifier supply voltage  $V_{CCDA}$  needs to be connected to 3.3V; otherwise  $V_{CCDA}$  must be tied to 3.3V (recommended) or 2.5V.

The required values of  $V_{CCDA}$ , the differential amplifier supply voltage, are given in Table 2 on page 20. Note that if differential amplifiers are used,  $V_{CCDA}$  is always 3.3V.

**Table 2 • Differential Amplifier Supply Voltage Requirements**

V <sub>CCDA</sub>	Using Differential I/O?	Using Voltage-Referenced I/O?	Maximum Value of V <sub>CCI</sub> in any Bank
3.3V	Yes		
3.3V	No	Yes	
2.5V	No	No	2.5V or less
3.3V	No	No	3.3V

The user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard.
- Use generic I/O macros and then use Actel's Designer PinEdit to specify the desired I/O standards. (Please note that this is not applicable to differential standards.)
- A combination of the first two methods.

Please refer to the *Using Accelerator I/O Resources* application note and *Macro Library Guide* for more details.

Simultaneous Switching Outputs (SSO)

Standard	BGA Package – Maximum # SSO
LVTTTL Slow Slew: 1, 8 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Slow Slew: 2, 12 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Slow Slew: 3, 16 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Slow Slew: 4, 24 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Fast Slew: 1, 8 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Fast Slew: 2, 12 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Fast Slew: 3, 16 mA drive	8 per V <sub>CCI</sub> or GND pair
LVTTTL Fast Slew: 4, 24 mA drive	8 per V <sub>CCI</sub> or GND pair
LVC MOS15 (JDEC8-11)	8 per V <sub>CCI</sub> or GND pair
LVC MOS18	8 per V <sub>CCI</sub> or GND pair
LVC MOS25	8 per V <sub>CCI</sub> or GND pair
PCI	8 per V <sub>CCI</sub> or GND pair
PCI-X	8 per V <sub>CCI</sub> or GND pair
GTL+	8 per V <sub>CCI</sub> or GND pair
HSTL Class I	8 per V <sub>CCI</sub> or GND pair
SSTL2 Class I	8 per V <sub>CCI</sub> or GND pair
SSTL2 Class II	8 per V <sub>CCI</sub> or GND pair
SSTL3 Class I	8 per V <sub>CCI</sub> or GND pair
SSTL3 Class II	8 per V <sub>CCI</sub> or GND pair

## I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (V<sub>REF</sub>) and an input/output supply voltage (V<sub>CCI</sub>), only I/Os with compatible standards can be assigned to the same bank.

Table 3 shows the compatible I/O standards for a common V<sub>REF</sub> (for voltage-referenced standards). Similarly, Table 4 shows compatible standards for a common V<sub>CCI</sub>.

**Table 3 • Compatible I/O Standards for Different V<sub>REF</sub> Values**

V <sub>REF</sub>	Compatible Standards
1.5V	SSTL 3 (Class I and II)
1.25V	SSTL 2 (Class I and II)
1.0V	GTL+ (2.5V and 3.3V Outputs)
0.75V	HSTL (Class I)

**Table 4 • Compatible I/O Standards for Different V<sub>CCI</sub> Values**

V <sub>CCI</sub> <sup>1</sup>	Compatible Standards	V <sub>REF</sub>
3.3V	LVTTTL/ PCI/ PCI-X/ LVPECL/ GTL+ 3.3V	1.0
3.3V	SSTL 3 (Class I and II)/ LVTTTL/ PCI/ PCI-X/ LVPECL	1.5
2.5V	LVC MOS 2.5V, GTL+ 2.5V, LVDS <sup>2</sup>	1.0
2.5V	LVC MOS 2.5V/ SSTL 2 (Classes I and II), LVDS <sup>2</sup>	1.25
1.8V	LVC MOS 1.8V	N/A
1.5V	LVC MOS 1.5V, HSTL Class I	0.75

**Notes:**

1. V<sub>CCI</sub> is used for both inputs and outputs.
2. V<sub>CCI</sub> = ±5%.

Table 5 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank. Note that two I/O standards are compatible if:

- Their  $V_{CCI}$  values are identical.
- Their  $V_{REF}$  standards are identical (if applicable).

For example, if LVTTTL 3.3V ( $V_{REF}=1.0V$ ) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTTL 3.3V PCI/PCI-X, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank. For instance, when using LVC MOS2.5 (+/-8%  $V_{CCI}$  tolerance) and LVDS (+/-5%  $V_{CCI}$  tolerance) within an I/O bank, the maximum voltage tolerance of the bank will be +/-5%  $V_{CCI}$ .

**Table 5 • Legal I/O Usage Matrix**

I/O Standard	LVTTTL 3.3V	LVC MOS 2.5V	LVC MOS 1.8V	LVC MOS 1.5V (JESD8-11)	3.3V PCI 3.3V PCI-X	GTL + (3.3V)	GTL + (2.5V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS (2.5V ±5%)	LVPECL (3.3V)
LVTTTL 3.3V ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
LVTTTL 3.3V( $V_{REF}=1.5V$ )	✓				✓					✓		✓
LVC MOS 2.5V ( $V_{REF}=1.0V$ )		✓					✓				✓	
LVC MOS 2.5V ( $V_{REF}=1.25V$ )		✓							✓		✓	
LVC MOS 1.8V			✓									
LVC MOS 1.5V ( $V_{REF}=1.75V$ ) (JESD8-11)				✓				✓				
3.3V PCI 3.3V PCI-X ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
3.3V PCI 3.3V PCI-X ( $V_{REF}=1.5V$ )	✓				✓					✓		✓
GTL + (3.3V)	✓				✓	✓						✓
GTL + (2.5V)		✓					✓					
HSTL Class I				✓				✓				
SSTL2 Class I & II		✓							✓		✓	
SSTL3 Class I & II	✓				✓					✓		✓
LVDS ( $V_{REF}=1.0V$ )		✓					✓				✓	
LVDS ( $V_{REF}=1.25V$ )		✓							✓		✓	
LVPECL ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
LVPECL ( $V_{REF}=1.5V$ )	✓				✓					✓		✓

Notes: A "✓" indicates whether standards can be used within a bank at the same time.

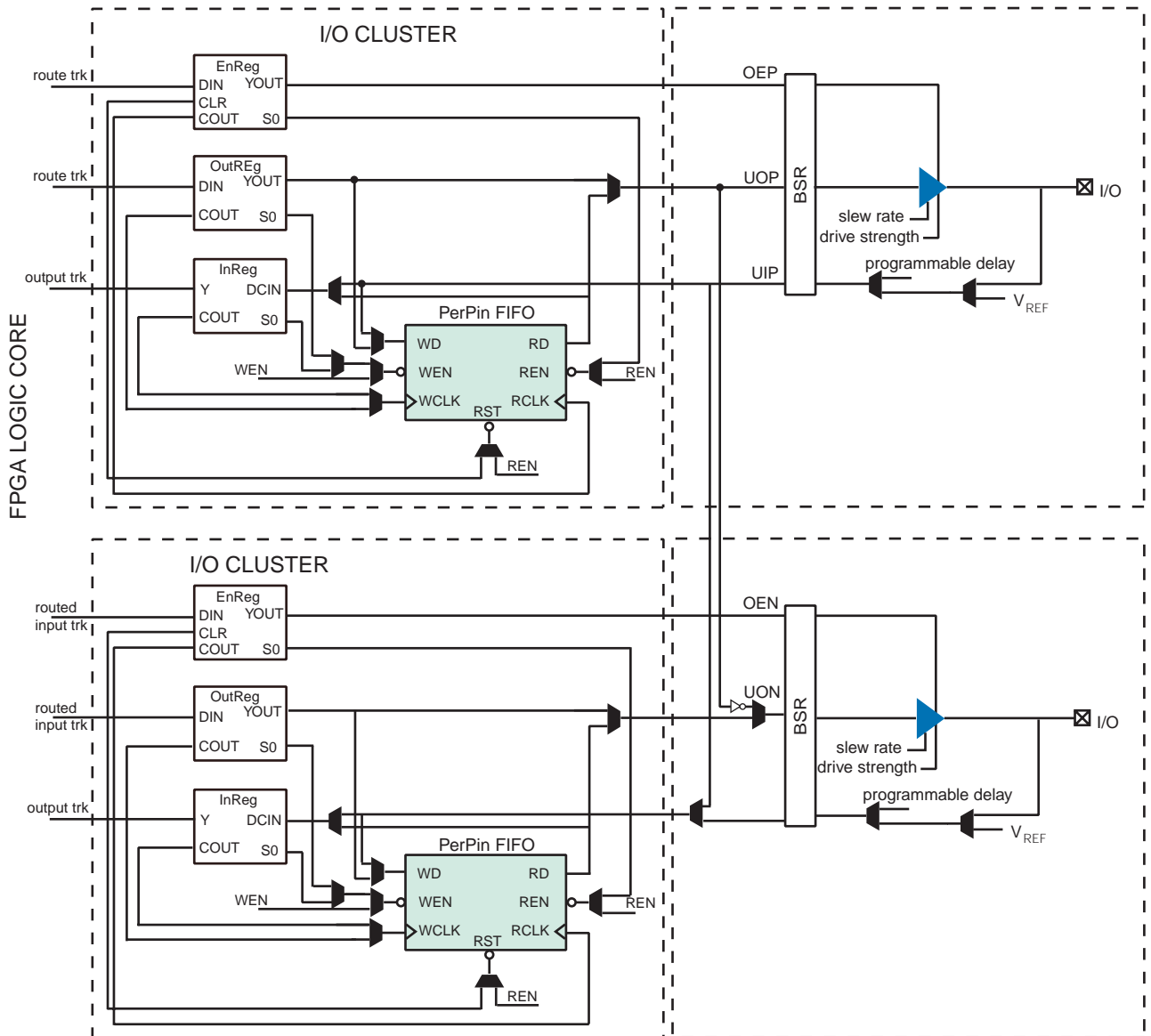
Examples:

- LVTTTL can be used with 3.3V PCI/PCI-X, and GTL+ (3.3V), when  $V_{REF}=1.0V$  (GTL+ requirement).
- LVTTTL can be used with 3.3V PCI/PCI-X, and SSTL3 Class I and II, when  $V_{REF}=1.5V$  (SSTL3 requirement).
- LVDS  $V_{CCI}=2.5V \pm 5\%$ .

## I/O Clusters

While I/O pads are organized into banks, the I/O Clusters are organized into blocks. There are two I/O Cluster Blocks per core tile side (Figure 7 on page 7). Each I/O cluster incorporates two I/O modules, four RX modules and two TX

modules, and a buffer module. Each I/O module incorporates one Input Register (InReg), one Output Register (OutReg), one Enable Register (EnReg), and a PerPin FIFO (Figure 1).



**Figure 1 • I/O Cluster Interface**

### Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. The I/O register usage can be either enabled/disabled by toggling the PerPin property in Actel's Designer software. Please note, this option must be turned off by default. It should be turned on if I/O-register usage is required.<sup>3</sup>

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design specific. The setting for each individual I/O overrides this global option.

### Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit. I/O Macros are provided for combinations of pull up/down for LVTTTL, LVCMOS (2.5V, 1.8V, and 1.5V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

### Customizing the I/O

- A 5-bit programmable input delay element is associated with each I/O bank (Table 6). It is optional for each input buffer within the bank (i.e. the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer.

**Table 6 • Timing for the Input Delay Element Associated with Each I/O**

Bits Used	Delay (ns)	Bits Used	Delay (ns)
0	0.54	16	2.01
1	0.65	17	2.13
2	0.71	18	2.19
3	0.83	19	2.3
4	0.9	20	2.38
5	1.01	21	2.49
6	1.08	22	2.55
7	1.19	23	2.67
8	1.27	24	2.75
9	1.39	25	2.87
10	1.45	26	2.93
11	1.56	27	3.04
12	1.64	28	3.12
13	1.75	29	3.23
14	1.81	30	3.29
15	1.93	31	3.41

<sup>3</sup>Please note that register combining for multi fanout nets is not supported.

- When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.
- The slew-rate value for the LVTTTL output buffer can be programmed. It can be set to either slow or fast.
- The drive strength value for LVTTTL output buffers can be programmed as well. There are four different drive strength values – 8mA, 12mA, 16mA, or 24mA – that can be specified in Designer.<sup>4</sup>

Using the Differential I/O Standards  
 Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Please note that there are no tristated or bidirectional I/O buffers for differential standards.

### Using the Voltage-Referenced I/O Standards

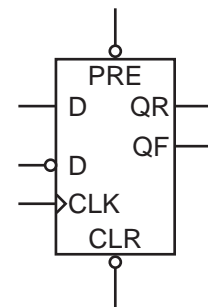
Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

### Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal (Figure 2). Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To use a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard)
2. Instantiate one of the DDR macros (DDR\_REG or DDR\_FIFO)
3. Connect the output from the Input buffer to the input of the DDR macro



**Figure 2 • DDR Register**

<sup>4</sup>These values are minimum drive strengths.



### Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the  $V_{CCI}$  and  $V_{REF}$  voltages for an I/O. The generic buffer macros assume the LVTTTL standard with slow slew rate and 24mA-drive strength. LVTTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hard-wired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs

(e.g. INBUF\_LVDS) or a pair of differential outputs (e.g. OUTBUF\_LVPECL).

- The pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR macros: DDR\_REG and DDR\_FIFO. They can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register and FIFO functionality. Designer software will map them to the I/O module in the same way it maps the other registers to the I/O module.

Table 7, Table 8, and Table 9 on page 25 list all the available macro names differentiated by their type, I/O standard, slew rate, and drive-strength.

**Table 7 • Macros for Single-Ended I/O Standards**

Standard	$V_{CCI}$	Macro Names
LVTTTL	3.3V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24,
3.3V PCI	3.3V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
3.3V PCI-X	3.3V	CLKBUF_PCI-X, HCLKBUF_PCI-X, INBUF_PCI-X, OUTBUF_PCI-X, TRIBUF_PCI-X, BIBUF_PCI-X
LVCMOS25	2.5V	CLKBUF_LVCMOS25, HCLKBUF_LVCMOS25, INBUF_LVCMOS25, OUTBUF_LVCMOS25, TRIBUF_LVCMOS25, BIBUF_LVCMOS25



**Table 7 • Macros for Single-Ended I/O Standards (Continued)**

Standard	V <sub>CCI</sub>	Macro Names
LVC MOS18	1.8V	CLKBUF_LVCMOS18, HCLKBUF_LVCMOS18, INBUF_LVCMOS18, OUTBUF_LVCMOS18, TRIBUF_LVCMOS18, BIBUF_LVCMOS18
LVC MOS15 (JESD8-11)	1.5V	CLKBUF_LVCMOS15, HCLKBUF_LVCMOS15, INBUF_LVCMOS15, OUTBUF_LVCMOS15, TRIBUF_LVCMOS15, BIBUF_LVCMOS15

**Table 8 • I/O Macros for Differential I/O Standards**

Standard	V <sub>CCI</sub>	Macro Names
LVPECL	3.3V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL, TRIBUF_LVPECL, BIBUF_LVPECL
LVDS	2.5V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS, TRIBUF_LVDS, BIBUF_LVDS

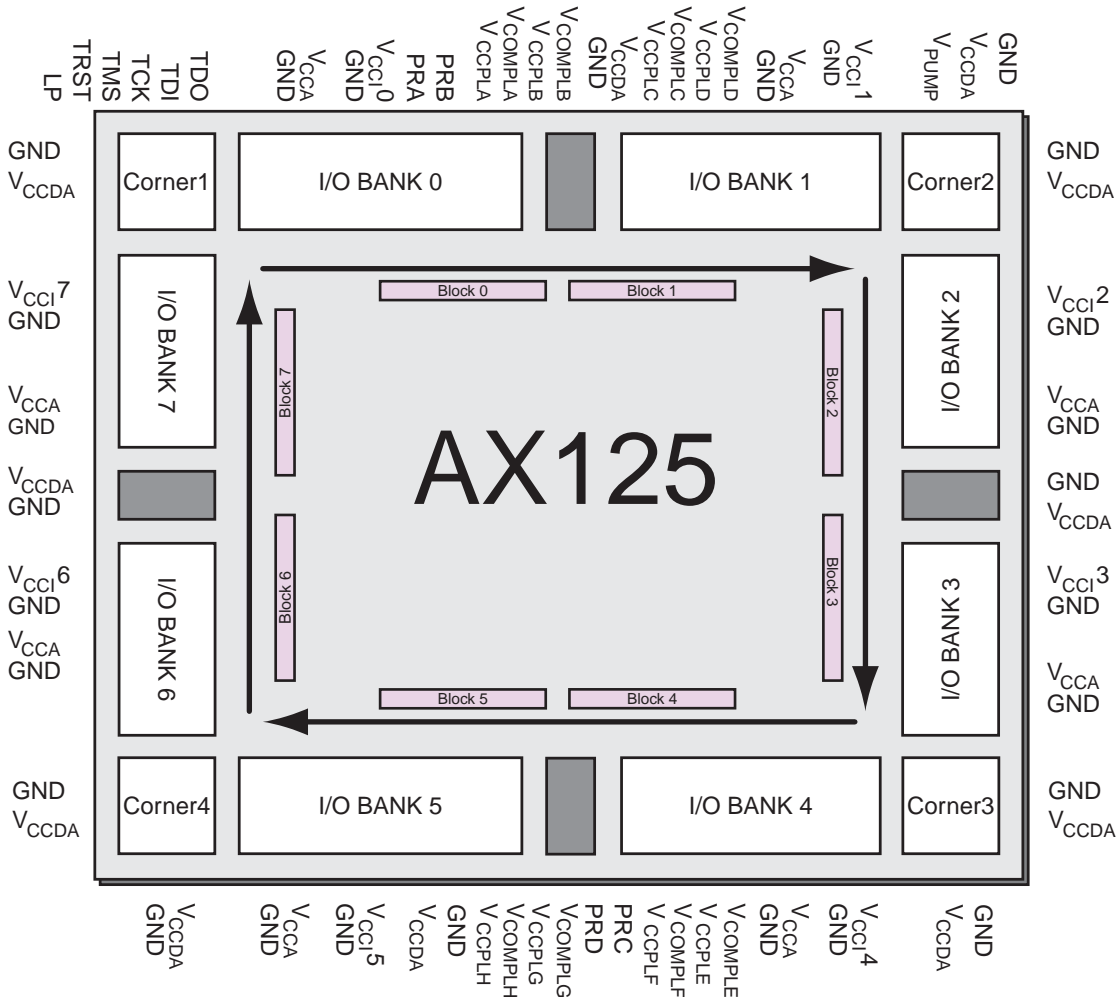
**Table 9 • I/O Macros for Voltage-Referenced I/O Standards**

Standard	V <sub>CCI</sub>	V <sub>REF</sub>	Macro Names
GTL+	3.3V	1.0V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5V	1.0V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25

## User I/O Naming Convention

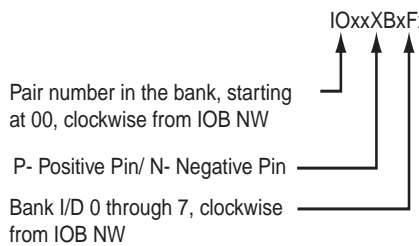
Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. This tells the user to which I/O bank and

which PerPin FIFO block it belongs, as well as the pairing and pin polarity for differential I/Os (Figure 3).



**Figure 3 • I/O Bank and Block Layout**

### General Naming Schemes



IOxxXBxFx ← FIFO Block Number, starting from 0, clockwise from IOB NW

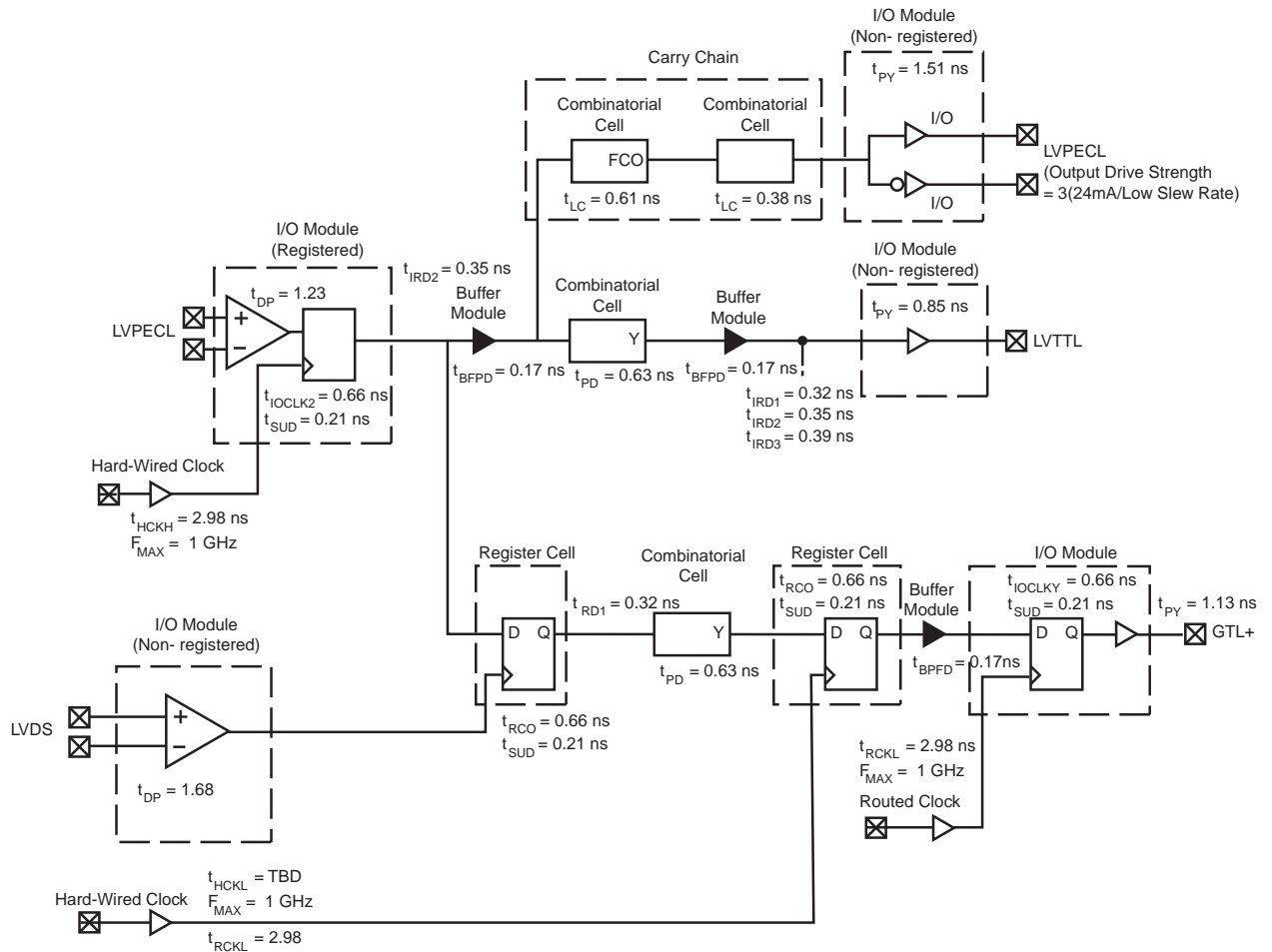
#### Examples:

**IO12PB1F1** is the positive pin of the thirteenth pair of the first I/O Bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair. This pin belongs to the second I/O FIFO Embedded Controller. For those I/Os that can be used either as a user I/O or as a special function, use the following nomenclature:

**IOxxXBxFx/special\_function\_name**

**IOxxPB1Fx/CLKA** this pin can be configured as a clock input or as a user I/O.

## Timing Model



**Note:** Timing data is for the AX500, -3 speed.

Hard-Wired Clock

$$\begin{aligned} \text{External Setup} &= (t_{DP} + t_{IRD2} + t_{SUD}) - t_{HCKL} \\ &= TBD \end{aligned}$$

Clock-to-Out (Pad-to-Pad)

$$= t_{HCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

Routed Clock

$$\begin{aligned} \text{External Setup} &= (t_{DP} + t_{IRD2} + t_{SUD}) - t_{RCKH} \\ &= TBD \end{aligned}$$

Clock-to-Out (Pad-to-Pad)

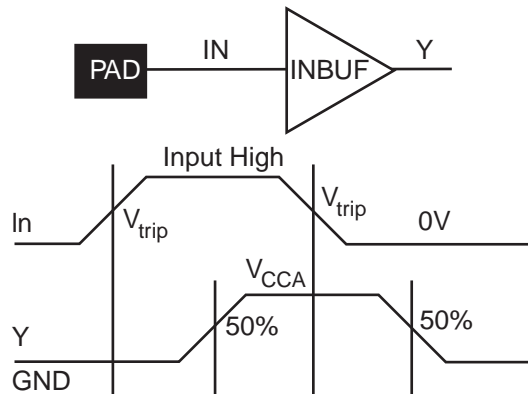
$$= t_{RCKH} + t_{RCO} + t_{RD1} + t_{DHL}$$

## I/O Standard Electrical Specifications

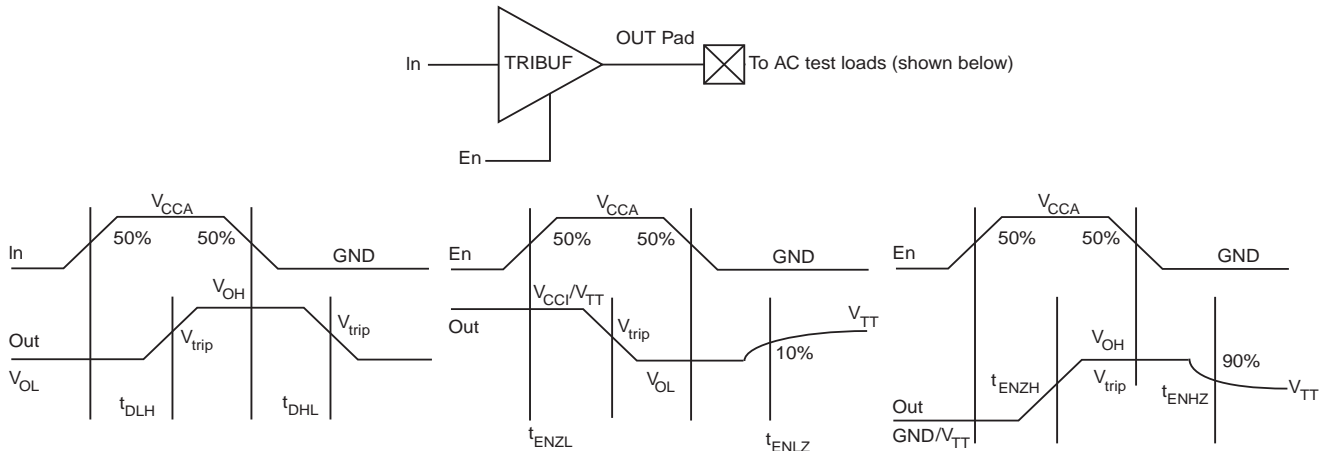
### Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
$C_{IN}$	Input Capacitance	$V_{IN}=0, f=1.0\text{ MHz}$			pF
$C_{INCLK}$	Input Capacitance on Clock Pin	$V_{IN}=0, f=1.0\text{ MHz}$			pF

### Input Buffer Delays

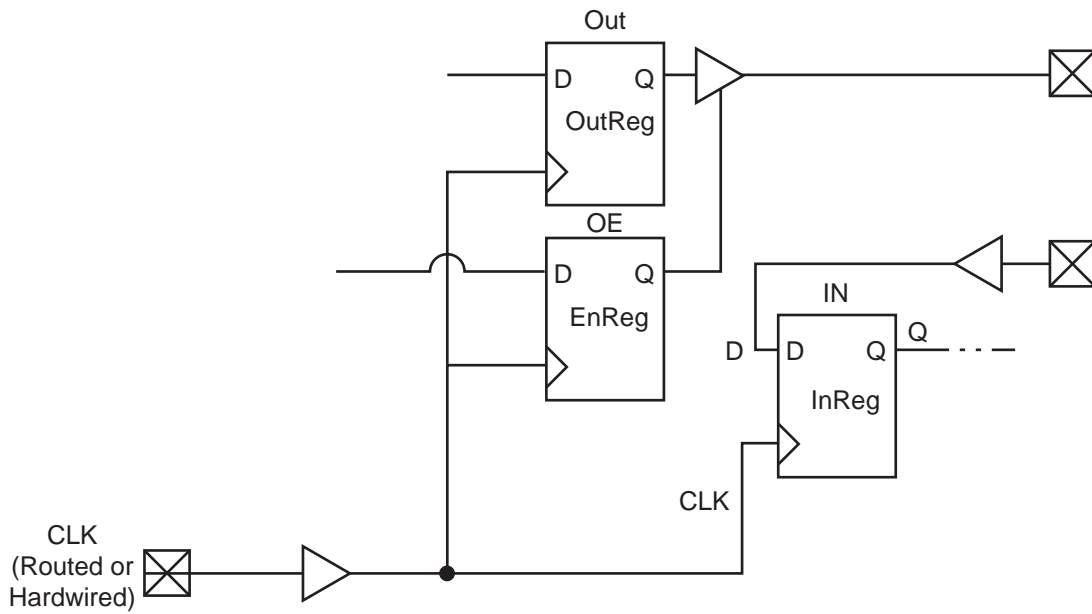


### Output Buffer Delays

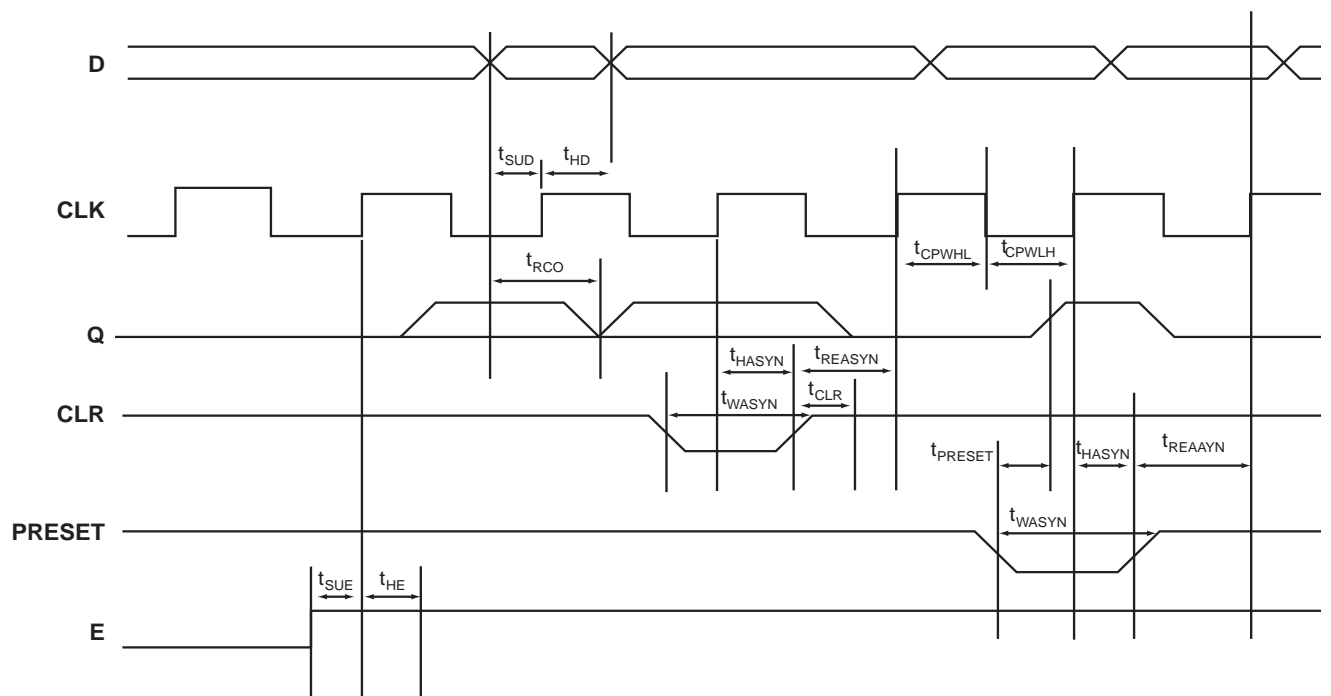


## I/O Module Timing Characteristics

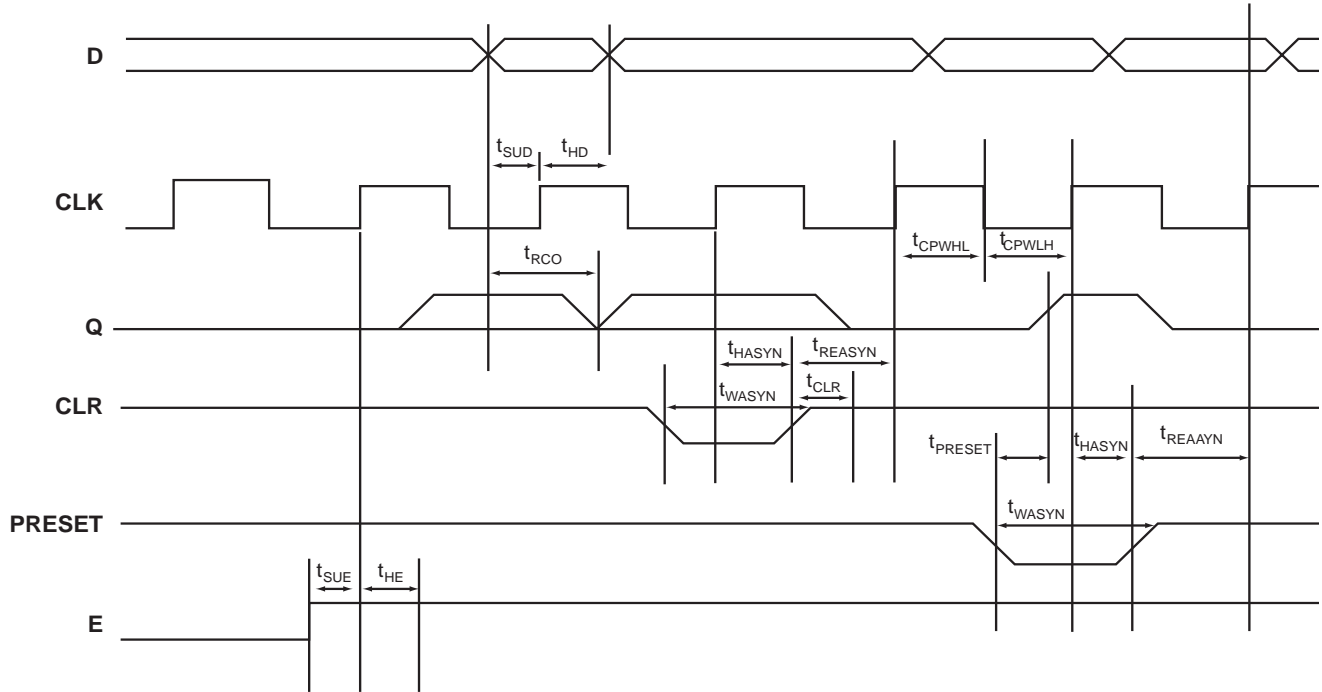
### Timing Model



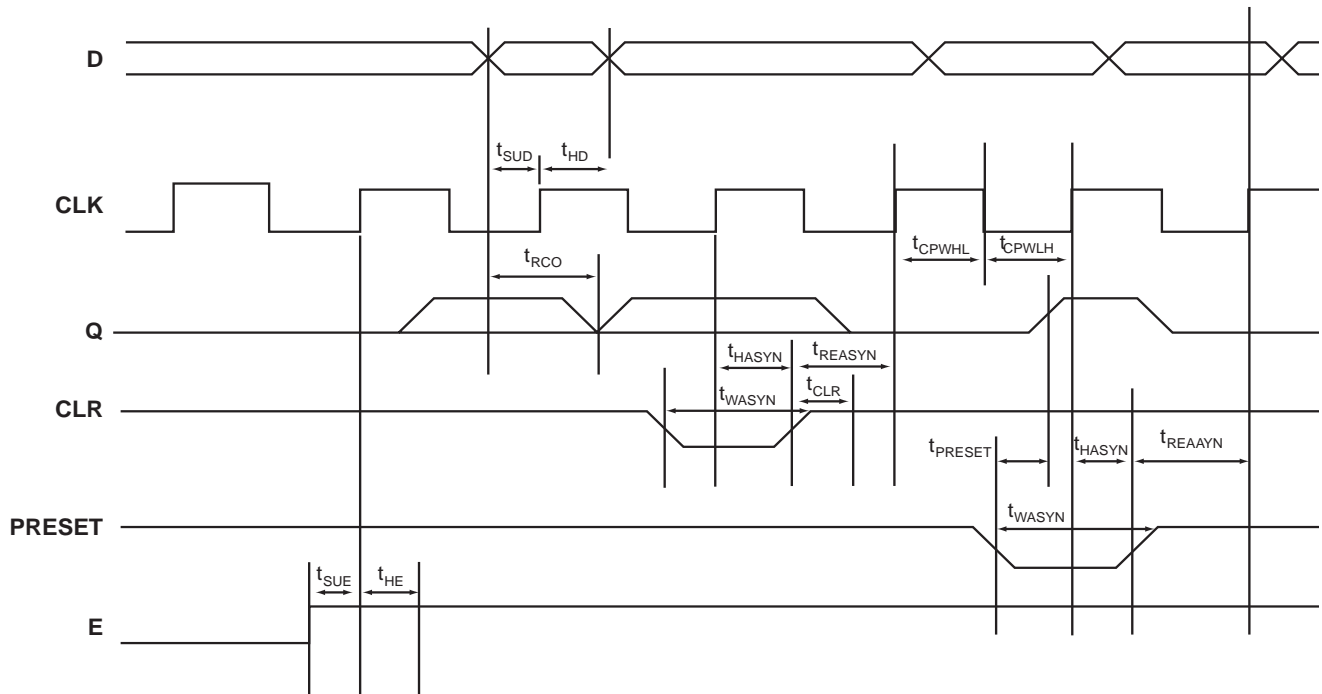
### Input Register Timing Characteristics



## Output Register Timing Characteristics



## Output Enable Register Timing Characteristics



## 3.3V LVTTTL

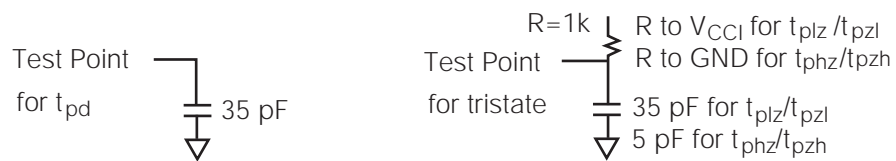
Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTTL input buffer and push-pull output buffer.

## DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	0.8	2.0	3.6	0.4	2.4	24	-24			

## AC Loadings

## AC Test Loads



## AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Cloud (pF)
0	3.0	1.40	N/A	35

## Timing Characteristics

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>LVTTTL Output Drive Strength = 1 (8mA) / Low Slew Rate</b>										
t <sub>DP</sub>	Input Buffer	1.50		1.73		1.96		2.34		ns
t <sub>PY</sub>	Output Buffer	10.16		10.15		13.29		15.63		ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register	0.66		0.76		0.86		1.02		ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register	8.80		10.15		11.51		13.54		ns
t <sub>SUD</sub>	Data Input Set-Up	0.20		0.23		0.27		0.31		ns
t <sub>SUE</sub>	Enable Input Set-Up	0.22		0.25		0.29		0.34		ns
t <sub>HD</sub>	Data Input Hold	0.00		0.00		0.00		0.00		ns
t <sub>HE</sub>	Enable Input Hold	0.00		0.00		0.00		0.00		ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time	0.21		0.24		0.28		0.32		ns
t <sub>HASYN</sub>	Asynchronous Removal Time	0.21		0.24		0.28		0.32		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.23		0.27		0.30		0.35		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.23		0.27		0.30		0.35		ns
<b>LVTTTL Output Drive Strength = 2 (12mA) / Low Slew Rate</b>										
t <sub>DP</sub>	Input Buffer	1.50		1.73		1.96		2.31		ns
t <sub>PY</sub>	Output Buffer	9.09		10.49		11.89		13.98		ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register	0.65		0.75		0.85		1.00		ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register	6.92		7.98		9.05		10.65		ns
t <sub>SUD</sub>	Data Input Set-Up	0.20		0.23		0.26		0.31		ns
t <sub>SUE</sub>	Enable Input Set-Up	0.22		0.25		0.29		0.34		ns
t <sub>HD</sub>	Data Input Hold	0.00		0.00		0.00		0.00		ns
t <sub>HE</sub>	Enable Input Hold	0.00		0.00		0.00		0.00		ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time	0.21		0.24		0.28		0.33		ns
t <sub>HASYN</sub>	Asynchronous Removal Time	0.21		0.24		0.28		0.33		ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q	0.23		0.27		0.30		0.36		ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q	0.23		0.27		0.30		0.36		ns
<b>LVTTTL Output Drive Strength =3 (16mA) / Low Slew Rate</b>										
t <sub>DP</sub>	Input Buffer	1.50		1.73		1.96		2.31		ns
t <sub>PY</sub>	Output Buffer	8.40		9.96		10.98		12.92		ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register	0.66		0.77		0.87		1.02		ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register	0.66		0.77		0.87		1.02		ns
t <sub>SUD</sub>	Data Input Set-Up	0.20		0.23		0.26		0.31		ns
t <sub>SUE</sub>	Enable Input Set-Up	0.22		0.25		0.29		0.34		ns
t <sub>HD</sub>	Data Input Hold	0.00		0.00		0.00		0.00		ns
t <sub>HE</sub>	Enable Input Hold	0.00		0.00		0.00		0.00		ns



Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
t <sub>HASYN</sub>	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns
<b>LVTTL Output Drive Strength = 4 (24mA) / Low Slew Rate</b>										
t <sub>DP</sub>	Input Buffer		1.50		1.73		1.96		2.31	ns
t <sub>PY</sub>	Output Buffer		8.07		9.31		10.55		12.42	ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		6.64		7.67		8.69		10.22	ns
t <sub>SUD</sub>	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
t <sub>SUE</sub>	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
t <sub>HD</sub>	Data Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>HE</sub>	Enable Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
t <sub>HASYN</sub>	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns
<b>LVTTL Output Drive Strength = 1 (8mA) / High Slew Rate</b>										
t <sub>DP</sub>	Input Buffer		1.50		1.73		1.96		2.31	ns
t <sub>PY</sub>	Output Buffer		2.41		2.78		3.15		3.71	ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
t <sub>SUD</sub>	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
t <sub>SUE</sub>	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
t <sub>HD</sub>	Data Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>HE</sub>	Enable Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
t <sub>HASYN</sub>	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns
<b>LVTTL Output Drive Strength = 2 (12mA) / High Slew Rate</b>										
t <sub>DP</sub>	Input Buffer		1.50		1.73		1.96		2.31	ns
t <sub>PY</sub>	Output Buffer		2.25		2.60		2.94		3.46	ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns
<b>LVTTTL Output Drive Strength =3 (16mA) / High Slew Rate</b>										
$t_{DP}$	Input Buffer		1.50		1.73		1.96		2.31	ns
$t_{PY}$	Output Buffer		2.24		2.58		2.93		3.45	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns
<b>LVTTTL Output Drive Strength = 4 (24mA) / High Slew Rate</b>										
$t_{DP}$	Input Buffer		1.50		1.73		1.96		4.35	ns
$t_{PY}$	Output Buffer		2.83		3.27		3.70		3.40	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns

## 2.5V LVCMOS

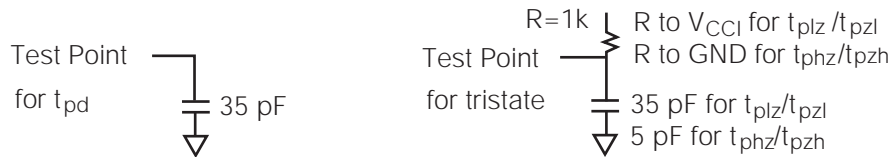
Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

### DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	0.7	1.7	3.6	0.4	2.0	12	-12			

### AC Loadings

#### AC Test Loads



### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
0	2.5	1.25	N/A	35

### Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CC1} = 2.3V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>LVC MOS25 Output Module Timing</b>										
$t_{DP}$	Input Buffer		1.44		1.66		1.88		2.225	ns
$t_{PY}$	Output Buffer		2.41		2.78		3.15		3.71	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns

### 1.8V LVCMOS

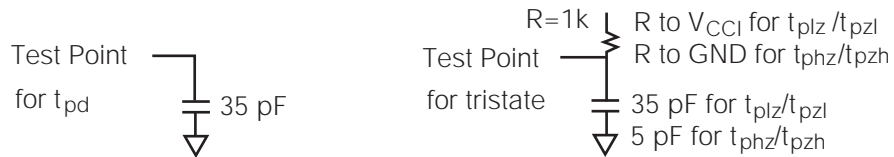
Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

#### DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	$0.2V_{CCI}$	$0.7V_{CCI}$	2.1	0.2	$V_{CCI}-0.2$	8mA	-8mA			

#### AC Loadings

#### AC Test Loads



#### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
0	1.8	$0.5V_{CCI}$	N/A	35

#### Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 1.7V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>LVC MOS18 Output Module Timing</b>										
$t_{DP}$	Input Buffer		2.42		2.79		3.16		4.35	ns
$t_{PY}$	Output Buffer		2.83		3.27		3.70		2.20	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns

1.5V LVCMOS (JESD8-11)

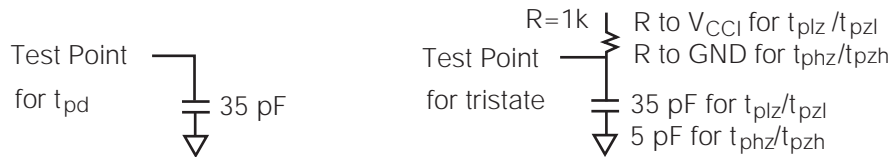
Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.5	$0.35V_{CCI}$	$0.65V_{CCI}$	1.95	0.4	$V_{CCI}-0.4$	8mA	-8mA			

AC Loadings

AC Test Loads



AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
0	1.8	$0.5V_{CCI}$	N/A	35

Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 1.4V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>LVCMOS15 (JESD8-11) I/O Module Timing</b>										
$t_{DP}$	Input Buffer		3.65		4.22		4.78		5.62	ns
$t_{PY}$	Output Buffer		2.35		2.71		3.07		3.61	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.21		0.25		0.28		0.33	ns
$t_{SUE}$	Enable Input Set-Up		0.24		0.27		0.31		0.37	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns

### 3.3V PCI, 3.3V PCI-X

Peripheral Component Interface for 3.3V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTTL input buffer and a push-pull output buffer. The input and output buffers are 5V tolerant with the aid of external components. Accelerator 3.3V PCI and 3.3V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

#### DC Input and Output Levels

	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
	Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
PCI	-0.5	$0.3V_{CCI}$	$0.5V_{CCI}$	$V_{CCI}+0.5$	(per PCI curves)						
PCI-X	-0.5	$0.35V_{CCI}$	$0.5V_{CCI}$	$V_{CCI}+0.5$	(per PCI curves)						

#### AC Loadings

AC Test Loads

TBD

#### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

#### Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>3.3V PCI/PCI-X Output Module Timing</b>										
$t_{DP}$	Input Buffer		1.16		1.34		1.52		1.78	ns
$t_{PY}$	Output Buffer		1.51		1.74		1.97		2.32	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.66		0.77		0.87		1.02	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.66		0.77		0.87		1.02	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.33	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.27		0.31		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.27		0.31		0.37	ns

3.3V PCI, 3.3V PCI-X V/I curve and the minimum and maximum PCI drive characteristics of the AX family will be done.

TBD

## Voltage Reference I/O Standards

GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an Open Drain output buffer. The  $V_{CCI}$  pin should be connected to 2.5V or 3.3V.

### DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
N/A	$V_{REF}-0.5$	$V_{REF}+0.1$	N/A	0.6	NA	NA	NA			

### AC Loadings

AC Test Loads

TBD

### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Clod (pF)
$V_{REF}-0.2$	$V_{REF}+0.2$	$V_{REF}$	1.0	0

### Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>2.5V GTL+ I/O Module Timing</b>										
$t_{DP}$	Input Buffer		1.37		1.58		1.79		2.11	ns
$t_{PY}$	Output Buffer		0.79		0.91		1.03		1.22	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>2.5V GTL+ I/O Module Timing</b>										
$t_{DP}$	Input Buffer		1.37		1.58		1.79		2.11	ns
$t_{PY}$	Output Buffer		0.79		0.91		1.03		1.22	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns



## HSTL Class I

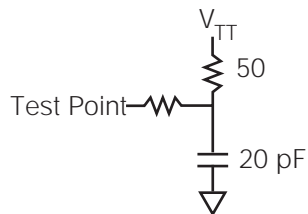
High-Speed Transceiver Logic is a general-purpose high-speed 1.5V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

## DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	$V_{REF}-0.1$	$V_{REF}+0.1$	3.6	0.4	$V_{CC}-0.4$	8	-8			

## AC Loadings

## AC Test Loads



## AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Cloud (pF)
$V_{REF}-0.5$	$V_{REF}+0.5$	$V_{REF}$	0.75	20

## Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 1.425V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>1.5V HSTL Class I I/O Module Timing</b>										
$t_{DP}$	Input Buffer		1.46		1.68		1.91		2.25	ns
$t_{PY}$	Output Buffer		3.58		4.13		4.68		5.51	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

**SSTL2**

Stub Series Terminated Logic for 2.5V is a general-purpose 2.5V memory bus standard (JESD8-9). The Accelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

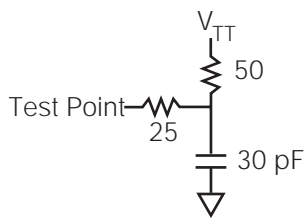
## Class I

## DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	$V_{REF}-0.2$	$V_{REF}+0.2$	3.6	$V_{REF}-0.57$	$V_{REF}+0.57$	7.6	-7.6			

## AC Loadings

## AC Test Loads



## AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
$V_{REF}-0.75$	$V_{REF}+0.75$	$V_{REF}$	1.25	30

## Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 2.3V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>2.5V SSTL2 Class I I/O Module Timing</b>										
$t_{DP}$	Input Buffer		1.53		1.77		2.00		2.35	ns
$t_{PY}$	Output Buffer		1.68		1.94		2.20		2.58	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

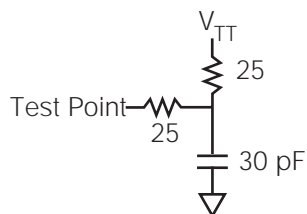
Class II

DC Input and Output Levels

V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OS</sub>	I <sub>IL</sub>	I <sub>IH</sub>
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	μA	μA
-0.3	V <sub>REF</sub> -0.2	V <sub>REF</sub> +0.2	3.6	V <sub>REF</sub> -0.8	V <sub>REF</sub> +0.8	15.2	-15.2			

AC Loadings

AC Test Loads



AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	V <sub>REF</sub> (typ) (V)	Load (pF)
V <sub>REF</sub> -0.75	V <sub>REF</sub> +0.75	V <sub>REF</sub>	1.25	30

Timing Characteristics

Worst-Case Commercial Conditions V<sub>CCA</sub> = 1.425V, V<sub>CCI</sub> = 2.3V, T<sub>J</sub> = 70°C

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>2.5V SSTL2 Class II I/O Module Timing</b>										
t <sub>DP</sub>	Input Buffer		1.00		1.16		1.31		1.55	ns
t <sub>PY</sub>	Output Buffer		1.05		1.21		1.38		1.62	ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
t <sub>SUD</sub>	Data Input Set-Up		0.22		0.25		0.28		0.34	ns
t <sub>SUE</sub>	Enable Input Set-Up		0.24		0.28		0.32		0.37	ns
t <sub>HD</sub>	Data Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>HE</sub>	Enable Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
t <sub>HASYN</sub>	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

**SSTL3**

Stub Series Terminated Logic for 3.3V is a general-purpose 3.3V memory bus standard (JESD8-8). The Accelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

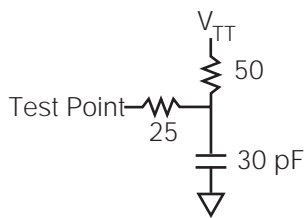
## Class I

## DC Input and Output Levels

$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$	$I_{OS}$	$I_{IL}$	$I_{IH}$
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	$\mu$ A	$\mu$ A
-0.3	$V_{REF}-0.2$	$V_{REF}+0.2$	3.6	$V_{REF}-0.6$	$V_{REF}+0.6$	8	-8			

## AC Loadings

## AC Test Loads



## AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	$V_{REF}$ (typ) (V)	Load (pF)
$V_{REF}-1.0$	$V_{REF}+1.0$	$V_{REF}$	1.50	30

## Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>2.5V SSTL3 Class I I/O Module Timing</b>										
$t_{DP}$	Input Buffer		1.23		1.42		1.61		1.89	ns
$t_{PY}$	Output Buffer		1.75		2.02		2.29		1.69	ns
$t_{IOCIKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

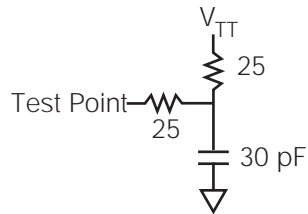
Class II

DC Input and Output Levels

V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OS</sub>	I <sub>IL</sub>	I <sub>IH</sub>
Min,V	Max,V	Min,V	Max,V	Max,V	Min,V	mA	mA	mA	μA	μA
-0.3	V <sub>REF</sub> -0.2	V <sub>REF</sub> +0.2	3.6	V <sub>REF</sub> -0.8	V <sub>REF</sub> +0.8	16	-16			

AC Loadings

AC Test Loads



AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	V <sub>REF</sub> (typ) (V)	Load (pF)
V <sub>REF</sub> -1.0	V <sub>REF</sub> +1.0	V <sub>REF</sub>	1.50	30

Timing Characteristics

Worst-Case Commercial Conditions V<sub>CCA</sub> = 1.425V, V<sub>CCI</sub> = 3.0V, T<sub>J</sub> = 70°C

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>3.3V SSTL3 Class II I/O Module Timing</b>										
t <sub>DP</sub>	Input Buffer		0.83		0.96		1.09		1.28	ns
t <sub>PY</sub>	Output Buffer		1.11		1.28		1.46		1.71	ns
t <sub>IOCIKQ</sub>	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
t <sub>IOCLKY</sub>	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
t <sub>SUD</sub>	Data Input Set-Up		0.22		0.25		0.28		0.34	ns
t <sub>SUE</sub>	Enable Input Set-Up		0.24		0.28		0.32		0.37	ns
t <sub>HD</sub>	Data Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>HE</sub>	Enable Input Hold		0.00		0.00		0.00		0.00	ns
t <sub>CPWHL</sub>	Clock Pulse Width High to Low									ns
t <sub>CPWLH</sub>	Clock Pulse Width Low to High									ns
t <sub>WASYN</sub>	Asynchronous Pulse Width									ns
t <sub>REASYN</sub>	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
t <sub>HASYN</sub>	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
t <sub>CLR</sub>	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
t <sub>PRESET</sub>	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

## Differential Standards

### Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O Cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Actel's Designer software when the user instantiates a differential I/O macro in the design.

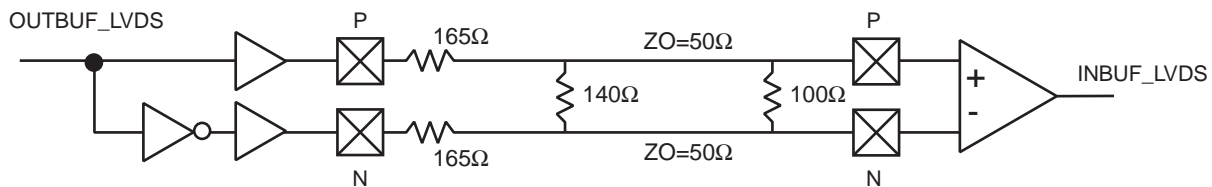
Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register

(OutReg), Enable Register (EnReg), Double Data Rate (DDR), and PerPin FIFO. However, there is no support for bidirectional I/Os or tristates with these standards.

### LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high speed differential I/O standard. It requires that one data bit is carried through two signal lines; so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350mV.

### LVDS Circuit



The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2V to 2.2V for a differential input with 400mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (Note that the driver is not a current-mode driver).

This driver provides a nominal constant current of 3.5mA. When this current flows through a 100Ω termination resistor on the receiver side, a voltage swing of 350mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

### DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
$V_{CCI}^1$	Supply Voltage	2.375	2.5	2.625	V
$V_{OH}$	Output High Voltage	1.25	1.425	1.6	V
$V_{OL}$	Output Low Voltage	0.9	1.075	1.25	V
$V_{ODIFF}$	Differential Output Voltage	250	350	450	mV
$V_{OCM}$	Output Common Mode Voltage	1.125	1.25	1.375	V
$V_{ICM}^2$	Input Common Mode Voltage	0.2	1.25	2.2	V

#### Notes:

1. +/- 5%
2. Differential input voltage = +/- 350mV.

### AC Loadings

#### AC Test Loads

TBD

#### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	Clload (pF)
1.2-0.125	1.2+0.125	1.2	TBD

## Timing Characteristics

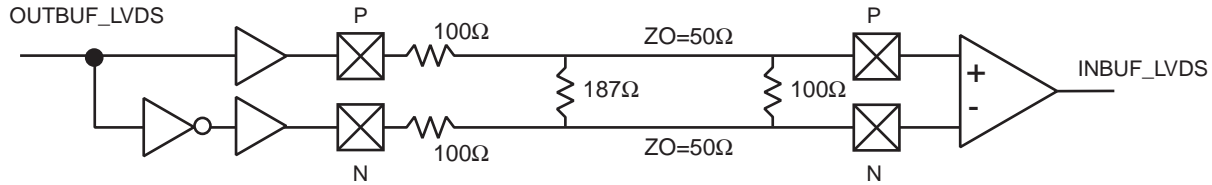
Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 2.3V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>LVDS Output Module Timing</b>										
$t_{DP}$	Input Buffer		1.66		1.92		2.17		2.55	ns
$t_{PY}$	Output Buffer		1.79		2.07		2.34		2.75	ns
$t_{IOCLKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850mV.

### LVPECL Circuit



The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. Please note that the  $V_{OH}$  levels are 200 mV below the standard LVPECL levels.

### DC Input and Output Levels

DC Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
$V_{CCI}$	3.0		3.3		3.6		V
$V_{OH}$	1.8	2.11	1.92	2.28	2.13	2.41	V
$V_{OL}$	0.96	1.27	1.06	1.43	1.30	1.57	V
$V_{IH}$	1.49	2.72	1.49	2.72	1.49	2.72	V
$V_{IL}$	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3		0.3		0.3		V

### AC Loadings

#### AC Test Loads

TBD

### AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point (V)	Load (pF)
1.6-0.3	1.6+0.3	1.6	TBD



## Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>LVPECL Output Module Timing</b>										
$t_{DP}$	Input Buffer		1.66		1.92		2.17		2.55	ns
$t_{PY}$	Output Buffer		1.70		1.96		2.22		2.62	ns
$t_{IOCLKQ}$	Sequential Clock-to-Q (External setup) for the input register		0.68		0.78		0.89		1.04	ns
$t_{IOCLKY}$	Clock-to-Output Y (FPGA setup) for the IO output register and the enable register		0.68		0.78		0.89		1.04	ns
$t_{SUD}$	Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{CPWHL}$	Clock Pulse Width High to Low									ns
$t_{CPWLH}$	Clock Pulse Width Low to High									ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.29		0.34	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.29		0.34	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.24		0.28		0.32		0.37	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.24		0.28		0.32		0.37	ns

# Module Specifications

## C-Cell

### Introduction

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Accelerator device. The AX architecture implements a new Combinatorial Cell that is an extension of the C-cell implemented in the SX-A family. One of the main highlights of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode. If carry-chain logic is not required, it can be disabled.

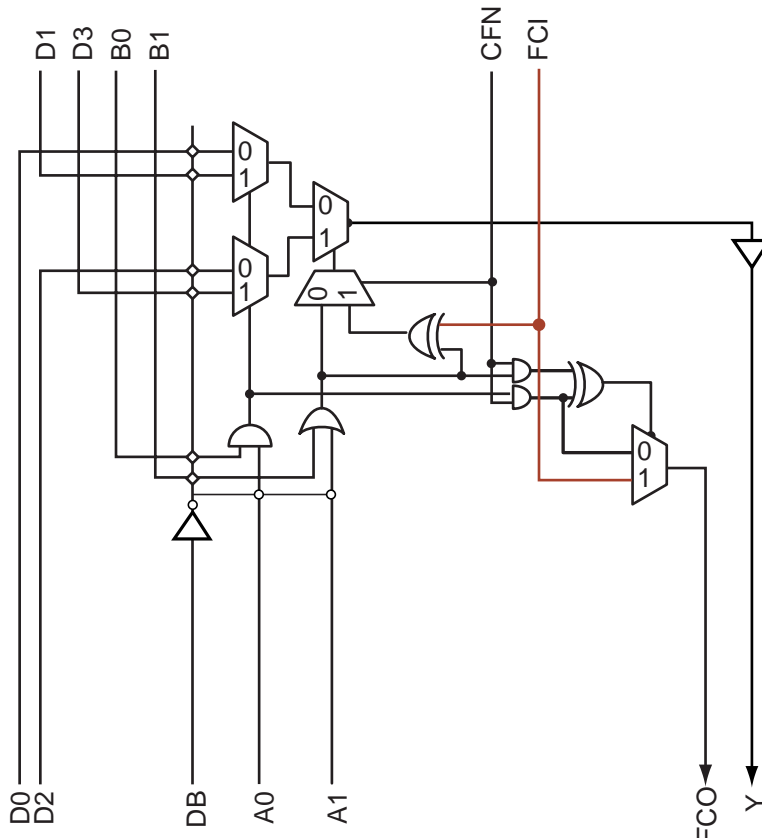
The C-cell features the following (Figure 4):

- 8-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four global clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.

- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1ns.
- A hard-wired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1ns.

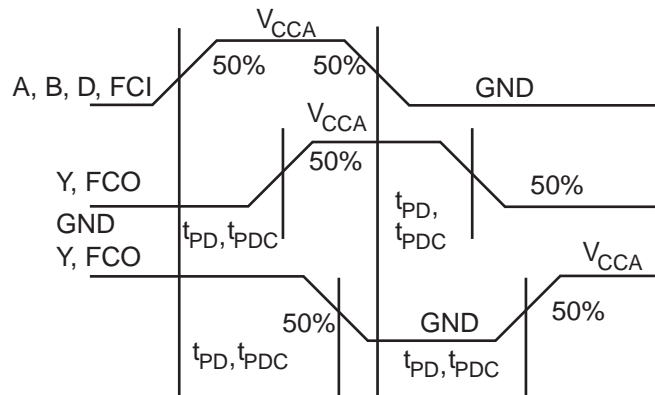
This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a 4-input XOR function in a single cell delay.

This configuration is handled automatically for the user with Actel's extensive macro library (please see Actel's *Macro Library Guide* for a complete listing of available Accelerator macros).



**Figure 4 • C-Cell**

Timing Model and Waveforms



Timing Characteristics

Worst-Case Commercial Conditions V<sub>CCA</sub> = 1.425V, V<sub>CCI</sub> = 3.0V, T<sub>J</sub> = 70°C

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>C-Cell Propagation Delays</b>										
t <sub>PD</sub>	Any input to output Y		0.65		0.75		0.85		1.00	ns
t <sub>PDC</sub>	Any input to carry chain output (FCO)		0.61		0.70		0.80		0.94	ns
t <sub>PDB</sub>	Any input through DB when one input is used		0.79		0.91		1.03		1.22	ns
t <sub>CCY</sub>	Input to carry chain (FCI) to Y		0.54		0.62		0.71		0.83	ns
t <sub>CC</sub>	Input to carry chain (FCI) to carry chain output (FCO)		0.07		0.08		0.09		0.11	ns

## Carry-Chain Logic

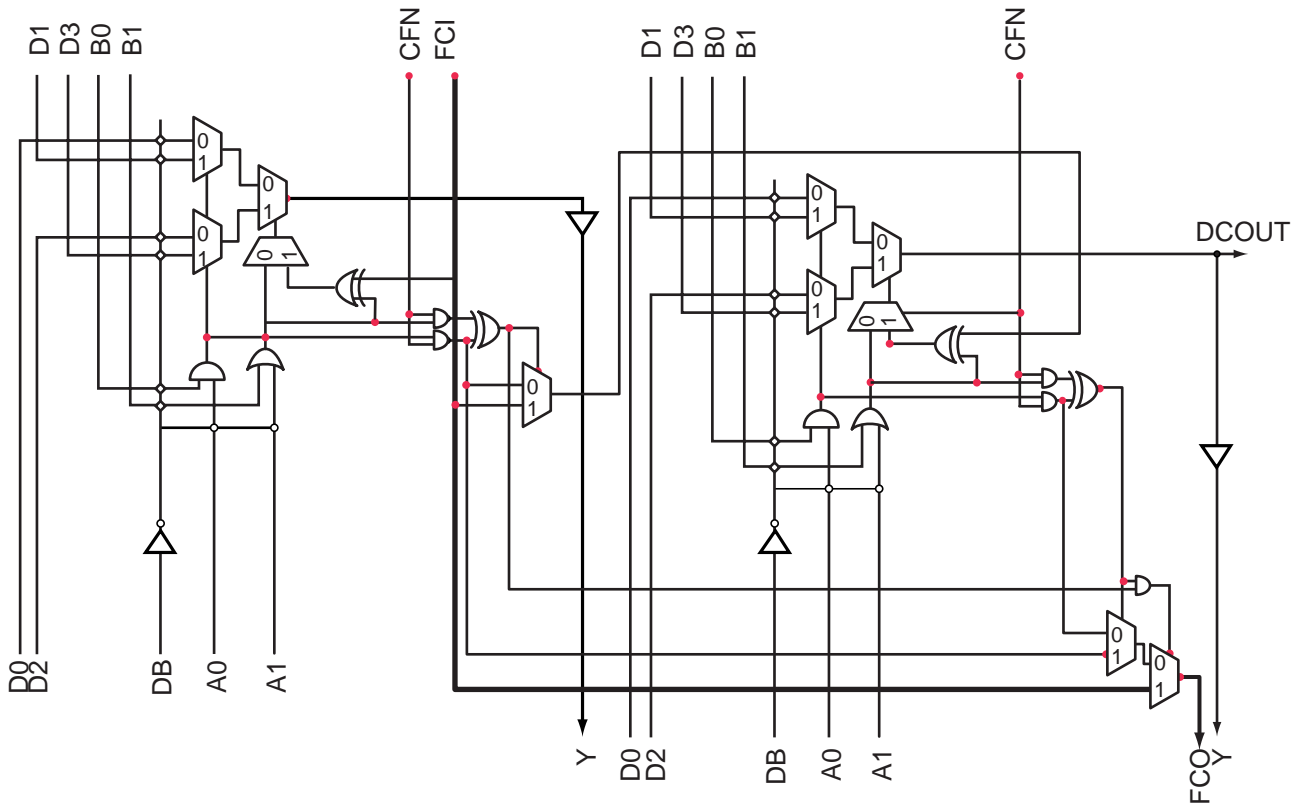
The Accelerator dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (i.e. carry out) for the two bits is generated in a Carry Look-ahead scheme to achieve minimum propagation delay from the FCI (i.e. carry in) into the two-bit Cluster. The two-bit carry logic is shown in Figure 5.

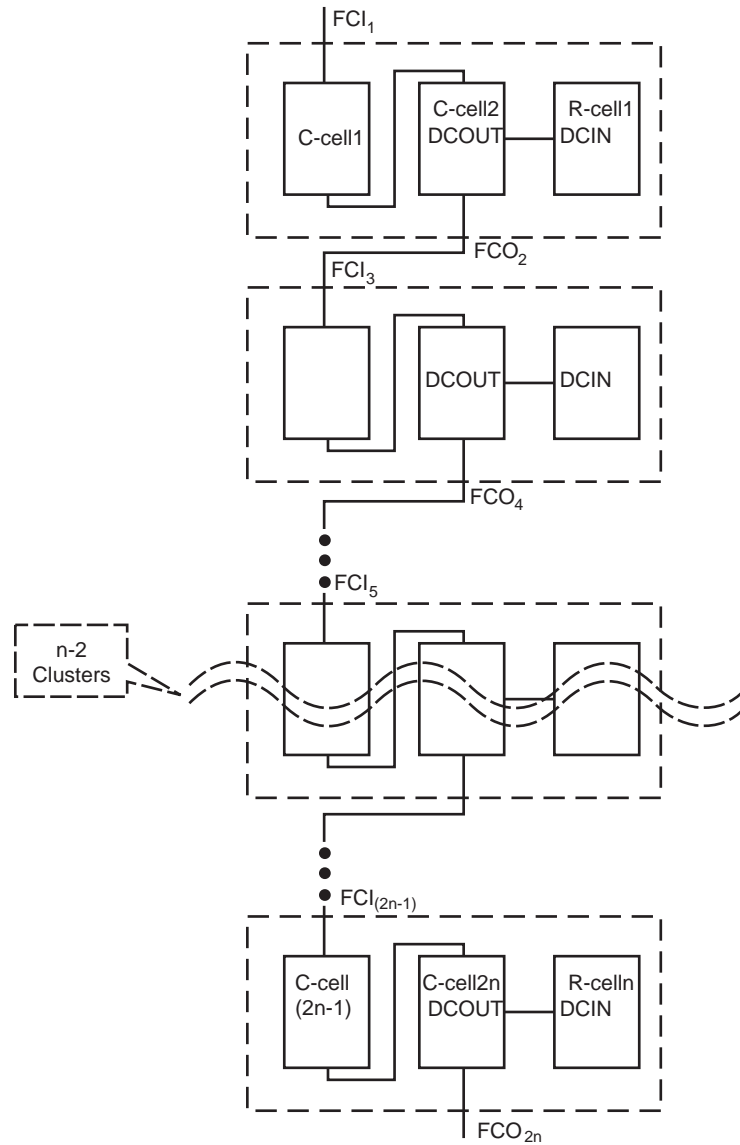
The FCI of one, two-C-cell cluster, is driven by the FCO of the two-C-cell Cluster immediately above it. Similarly, the FCO of one, two-C-cell cluster, drives the FCI input of the two-C-cell Cluster immediately below it (Figure 6 on page 53).

The carry-chain logic is selected via the CFN input. When carry logic is not needed, this signal is deasserted to save power.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.



**Figure 5 • AX 2-bit Carry Logic**



**Note:** The carry-chain sequence can end on either C-cell.

**Figure 6 • Carry-Chain Sequencing of C-cells**

### Timing Characteristics

Refer to the C-cell [“Timing Characteristics”](#) section on page 55 for more information on carry-chain timing.

## R-Cell

### Introduction

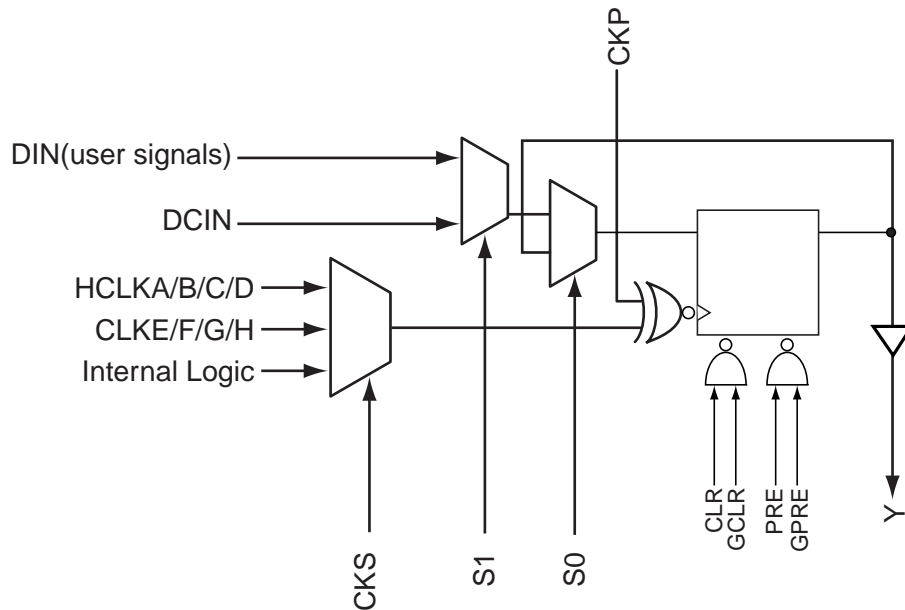
The R-cell, the sequential logic resource of the Accelerator devices, is the second logic module type in the AX family architecture. The Accelerator R-cell is an enhanced version of the SX-A R-cell. It includes additional clock inputs for all eight global resources of the Accelerator architecture as well as global presets and clears (Figure 7).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1ns of routing delay.
- The R-cell can be used as a stand-alone flip-flop. It can be driven by any other C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using it as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).

- Independent active low asynchronous clear (CLR).
- Independent active low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
  - One of the four high performance hardwired fast clocks (HCLKs)
  - One of the four routed clocks (CLKs)
  - User signals
- S0, S1, PSET, and CLR can be driven by CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

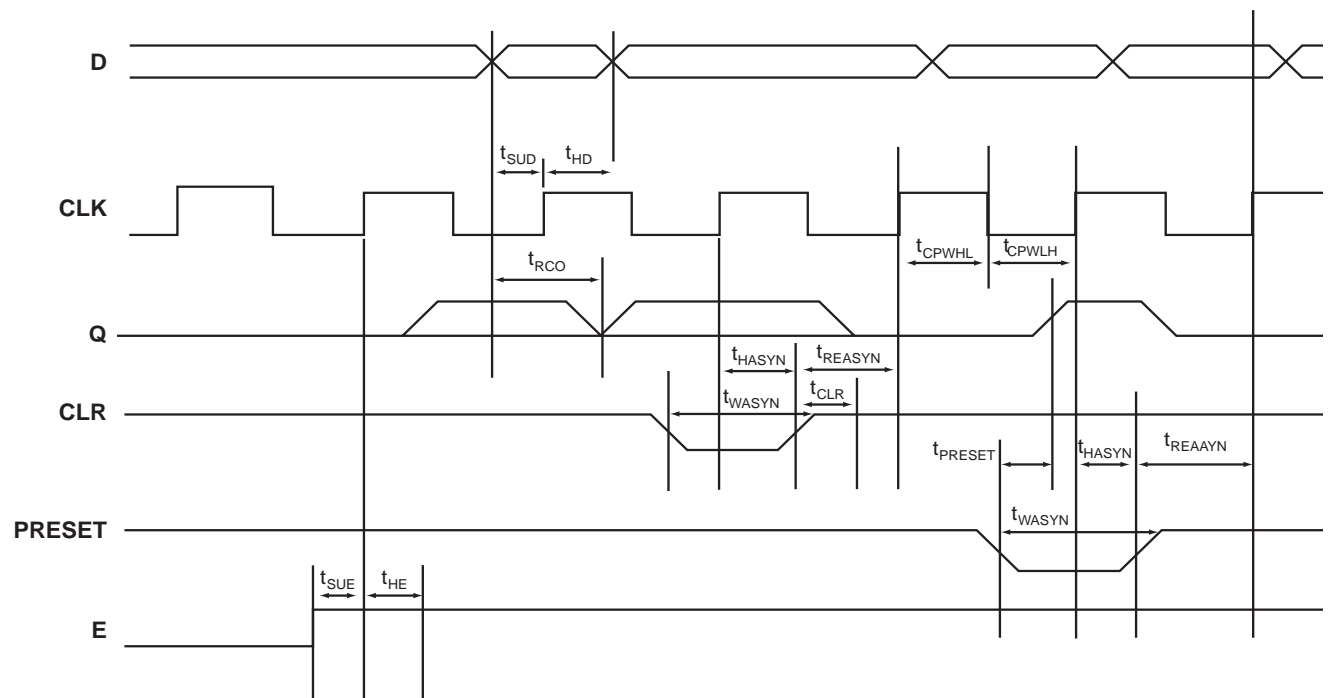
As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Actel's extensive macro library (please see Actel's *Macro Library Guide* for a complete listing of available AX macros).



**Figure 7 • R-Cell**

## Timing Models and Waveforms

## R-Cell Delays



## Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>R-Cell Propagation Delays</b>										
$t_{RCO}$	Sequential Clock-to-Q		0.58		0.67		0.76		0.89	ns
$t_{CLR}$	Asynchronous Clear-to-Q		0.21		0.24		0.27		0.32	ns
$t_{PRESET}$	Asynchronous Preset-to-Q		0.23		0.27		0.30		0.35	ns
$t_{SUD}$	Flip-Flop Data Input Set-Up		0.20		0.23		0.26		0.31	ns
$t_{SUE}$	Flip-Flop Enable Input Set-Up		0.22		0.25		0.29		0.34	ns
$t_{HD}$	Flip-Flop Data Input Hold		0.00		0.00		0.00		0.00	ns
$t_{HE}$	Flip-Flop Enable Input Hold		0.00		0.00		0.00		0.00	ns
$t_{WASYN}$	Asynchronous Pulse Width									ns
$t_{REASYN}$	Asynchronous Recovery Time		0.22		0.25		0.28		0.33	ns
$t_{HASYN}$	Asynchronous Removal Time		0.22		0.25		0.28		0.33	ns
$t_{CPWHL}$	Clock Pulse Width High to Low		0.05		0.06		0.07		0.08	ns
$t_{CPWLH}$	Clock Pulse Width Low to High		0.05		0.06		0.07		0.08	ns

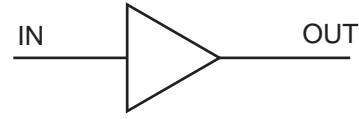
## Buffer Module

### Introduction

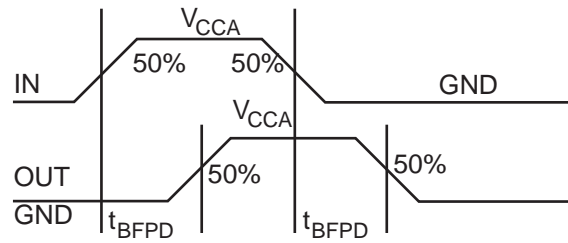
Each SuperCluster includes one buffer module (Figure 4 on page 5).

When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the AX architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

### Buffer Module Timing Model



### Buffer Module Waveform



### Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Buffer Module Propagation Delays</b>										
$t_{BFPD}$	Any input to output Y		0.17		0.20		0.22		0.26	ns



# Routing Specifications

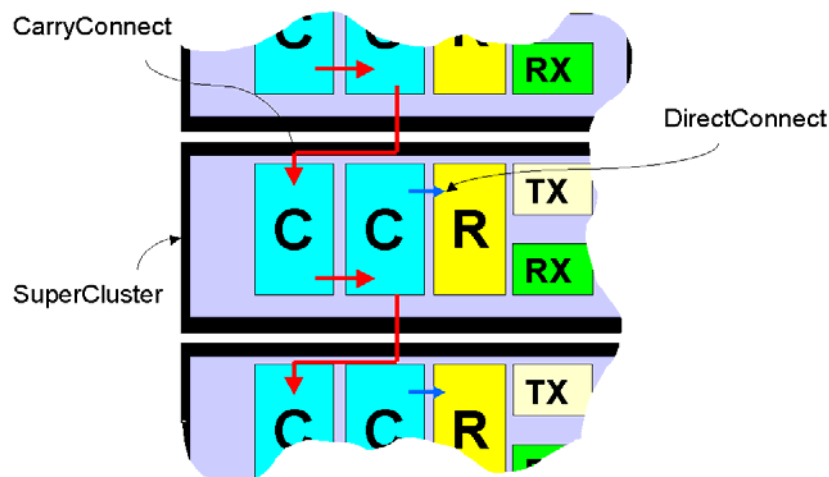
## Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect and Vertical and Horizontal Routing.

### DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 21). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.



**Figure 21 • DirectConnect and CarryConnect**

### CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 21). The FCO output of the right C-cell of a 2-C-cell Cluster drives the FCI input of the left C-cell in the 2-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Like the DirectConnects, this connection can be built without an antifuse connection. This connection has a delay of less than 0.1ns from the FCO of one 2-C-cell Cluster to the FCI of the 2-C-cell Cluster immediately below it (see the “Carry-Chain Logic” section on page 52 for more information).

### FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 22 on page 58). FastConnects provide a maximum delay of 0.3ns. The outputs of each logic module connect directly to the Output Tracks within a

SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

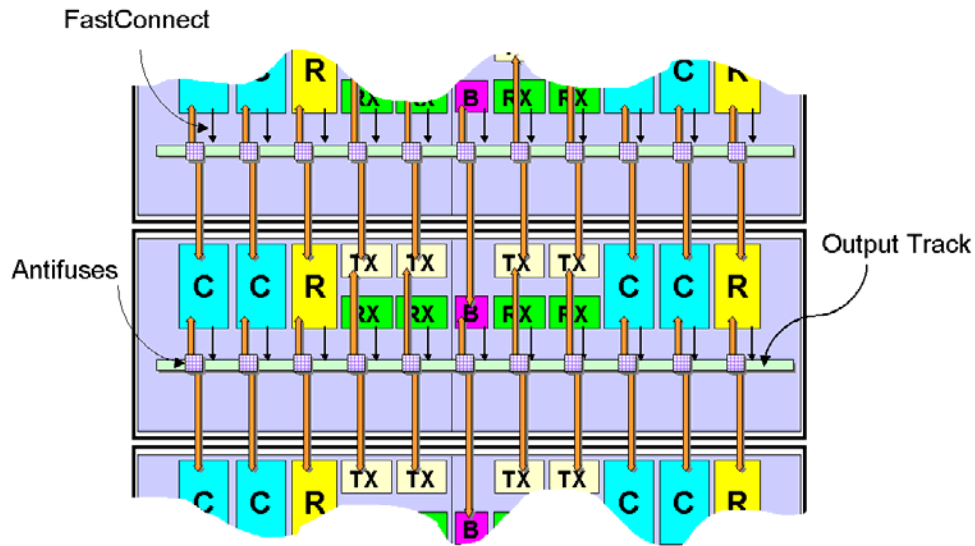
### Vertical and Horizontal Routing

Providing both local and long distance routing are the Vertical and Horizontal Tracks (Figure 23 on page 58). These tracks are composed of both short-distance, segmented routing and cross-chip routing tracks. The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

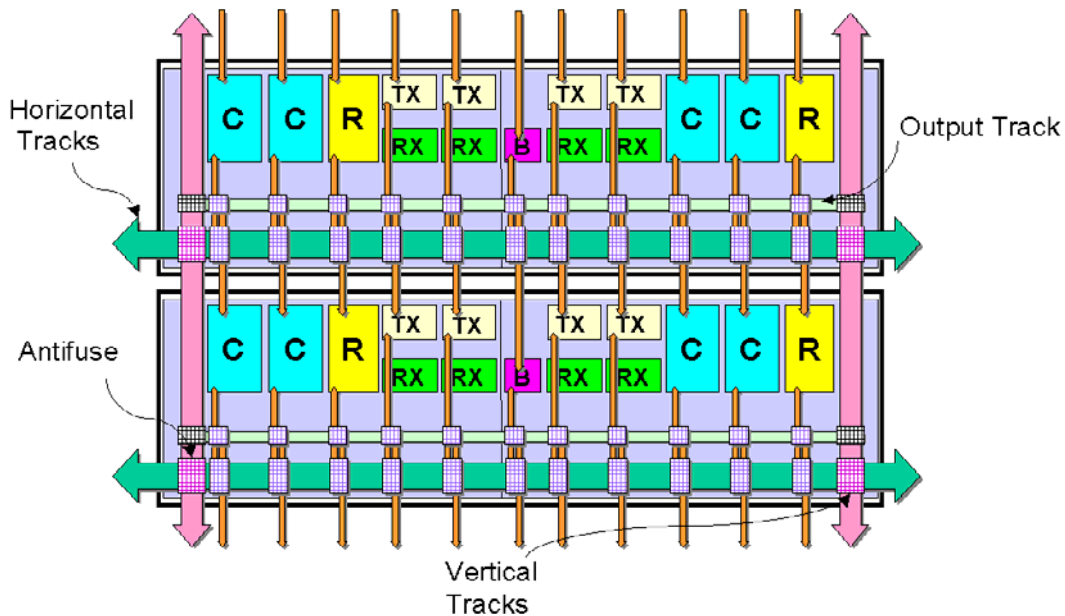
These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connect to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (Figure 23). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip

routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.



**Figure 22 • FastConnect Routing**



**Figure 23 • Horizontal and Vertical Tracks**

## Timing Characteristics

## AX125

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Predicted Routing Delays</b>										
t <sub>DC</sub>	Direct Connect Routing Delay, FO1		0.10		0.11		0.12		0.15	ns
t <sub>FC</sub>	Fast Connect Routing Delay, FO1		0.30		0.35		0.39		0.46	ns
t <sub>RD1</sub>	Routing delay for FO1		0.30		0.35		0.40		0.47	ns
t <sub>RD2</sub>	Routing delay for FO2		0.33		0.38		0.43		0.51	ns
t <sub>RD3</sub>	Routing delay for FO3		0.37		0.43		0.48		0.57	ns
t <sub>RD4</sub>	Routing delay for FO4		0.42		0.48		0.55		0.64	ns
t <sub>RD5</sub>	Routing delay for FO5		0.48		0.55		0.62		0.73	ns
t <sub>RD6</sub>	Routing delay for FO6		0.55		0.64		0.72		0.85	ns
t <sub>RD7</sub>	Routing delay for FO7		0.68		0.79		0.89		1.05	ns
t <sub>RD8</sub>	Routing delay for FO8		0.76		0.88		0.99		1.17	ns
t <sub>RD16</sub>	Routing delay for FO16		1.29		1.49		1.69		1.99	ns
t <sub>RD32</sub>	Routing delay for FO32		2.01		2.32		2.63		3.10	ns
t <sub>RD64</sub>	Routing delay for FO64									ns
t <sub>RD128</sub>	Routing delay for FO128									ns

## AX250 –TBD

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Predicted Routing Delays</b>										
t <sub>DC</sub>	DirectConnect Routing Delay, FO1									ns
t <sub>FC</sub>	Fast Connect Routing Delay, FO1									ns
t <sub>RD1</sub>	Routing delay for FO1									ns
t <sub>RD2</sub>	Routing delay for FO2									ns
t <sub>RD3</sub>	Routing delay for FO3									ns
t <sub>RD4</sub>	Routing delay for FO4									ns
t <sub>RD5</sub>	Routing delay for FO5									ns
t <sub>RD6</sub>	Routing delay for FO6									ns
t <sub>RD7</sub>	Routing delay for FO7									ns
t <sub>RD8</sub>	Routing delay for FO8									ns
t <sub>RD16</sub>	Routing delay for FO16									ns
t <sub>RD32</sub>	Routing delay for FO32									ns
t <sub>RD64</sub>	Routing delay for FO64									ns
t <sub>RD128</sub>	Routing delay for FO128									ns

## AX500

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Predicted Routing Delays</b>										
t <sub>DC</sub>	Direct Connect Routing Delay, FO1		0.10		0.11		0.12		0.15	ns
t <sub>FC</sub>	Fast Connect Routing Delay, FO1		0.30		0.35		0.39		0.46	ns
t <sub>RD1</sub>	Routing delay for FO1		0.34		0.39		0.45		0.53	ns
t <sub>RD2</sub>	Routing delay for FO2		0.35		0.41		0.46		0.54	ns
t <sub>RD3</sub>	Routing delay for FO3		0.42		0.48		0.55		0.64	ns
t <sub>RD4</sub>	Routing delay for FO4		0.48		0.56		0.63		0.75	ns
t <sub>RD5</sub>	Routing delay for FO5		0.52		0.60		0.68		0.80	ns
t <sub>RD6</sub>	Routing delay for FO6		0.73		0.84		0.96		1.13	ns
t <sub>RD7</sub>	Routing delay for FO7		0.78		0.90		1.02		1.20	ns
t <sub>RD8</sub>	Routing delay for FO8		0.86		1.00		1.13		1.33	ns
t <sub>RD16</sub>	Routing delay for FO16		1.88		2.17		2.46		2.89	ns
t <sub>RD32</sub>	Routing delay for FO32		3.08		3.55		4.03		4.74	ns
t <sub>RD64</sub>	Routing delay for FO64									ns
t <sub>RD128</sub>	Routing delay for FO128									ns

## AX1000

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Predicted Routing Delays</b>										
t <sub>DC</sub>	Direct Connect Routing Delay, FO1		0.10		0.12		0.13		0.15	ns
t <sub>FC</sub>	Fast Connect Routing Delay, FO1		0.30		0.35		0.39		0.46	ns
t <sub>RD1</sub>	Routing delay for FO1		0.39		0.45		0.51		0.60	ns
t <sub>RD2</sub>	Routing delay for FO2		0.46		0.53		0.60		0.71	ns
t <sub>RD3</sub>	Routing delay for FO3		0.48		0.56		0.63		0.74	ns
t <sub>RD4</sub>	Routing delay for FO4		0.55		0.63		0.71		0.84	ns
t <sub>RD5</sub>	Routing delay for FO5		0.63		0.73		0.82		0.97	ns
t <sub>RD6</sub>	Routing delay for FO6		0.86		0.99		1.13		1.32	ns
t <sub>RD7</sub>	Routing delay for FO7		0.88		1.02		1.15		1.36	ns
t <sub>RD8</sub>	Routing delay for FO8		1.28		1.48		1.68		1.97	ns
t <sub>RD16</sub>	Routing delay for FO16		2.23		2.57		2.91		3.42	ns
t <sub>RD32</sub>	Routing delay for FO32		3.68		4.24		4.81		5.65	ns
t <sub>RD64</sub>	Routing delay for FO64									ns
t <sub>RD128</sub>	Routing delay for FO128									ns

## AX2000

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Predicted Routing Delays</b>										
t <sub>DC</sub>	Direct Connect Routing Delay, FO1		0.10		0.12		0.13		0.15	ns
t <sub>FC</sub>	Fast Connect Routing Delay, FO1		0.30		0.35		0.39		0.46	ns
tRD1	Routing delay for FO1		0.43		0.50		0.56		0.66	ns
tRD2	Routing delay for FO2		0.51		0.59		0.67		0.79	ns
tRD3	Routing delay for FO3		0.61		0.70		0.80		0.94	ns
tRD4	Routing delay for FO4		0.66		0.76		0.87		1.02	ns
tRD5	Routing delay for FO5		0.85		0.98		1.11		1.31	ns
tRD6	Routing delay for FO6		1.28		1.48		1.68		1.97	ns
tRD7	Routing delay for FO7		1.43		1.65		1.87		2.20	ns
tRD8	Routing delay for FO8		1.50		1.73		1.96		2.31	ns
tRD16	Routing delay for FO16		2.24		2.58		2.92		3.44	ns
tRD32	Routing delay for FO32		3.68		4.24		4.81		5.65	ns
tRD64	Routing delay for FO64									ns
tRD128	Routing delay for FO128									ns

## Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Accelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the HCLK (hard-wired clock) and CLK (routed clock). Every Accelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

### Timing Characteristics

#### AX125

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Dedicated (Hard-Wired) Array Clock Networks</b>										
t <sub>HCKL</sub>	Input Low to High		2.18		2.52		2.85		3.35	ns
t <sub>HCKH</sub>	Input High to Low		2.81		3.24		3.67		4.32	ns
t <sub>HPWH</sub>	Minimum Pulse Width High									ns
t <sub>HPWL</sub>	Minimum Pulse Width Low									ns
t <sub>HCKSW</sub>	Maximum Skew		0.05		0.06		0.07		0.08	ns
t <sub>HP</sub>	Minimum Period									ns
t <sub>HMAX</sub>	Maximum Frequency									ns

#### AX250 – TBD

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Dedicated (Hard-Wired) Array Clock Networks</b>										
t <sub>HCKL</sub>	Input Low to High									ns
t <sub>HCKH</sub>	Input High to Low									ns
t <sub>HPWH</sub>	Minimum Pulse Width High									ns
t <sub>HPWL</sub>	Minimum Pulse Width Low									ns
t <sub>HCKSW</sub>	Maximum Skew									ns
t <sub>HP</sub>	Minimum Period									ns
t <sub>HMAX</sub>	Maximum Frequency									ns

## AX500

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Dedicated (Hard-Wired) Array Clock Networks</b>										
$t_{HCKL}$	Input Low to High		2.18		2.52		2.85		3.35	ns
$t_{HCKH}$	Input High to Low		2.81		3.24		3.67		4.32	ns
$t_{HPWH}$	Minimum Pulse Width High									ns
$t_{HPWL}$	Minimum Pulse Width Low									ns
$t_{HCKSW}$	Maximum Skew		0.10		0.12		0.13		0.15	ns
$t_{HP}$	Minimum Period									ns
$t_{HMAX}$	Maximum Frequency									ns

## AX1000

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Dedicated (Hard-Wired) Array Clock Networks</b>										
$t_{HCKL}$	Input Low to High		2.50		2.88		3.27		3.85	ns
$t_{HCKH}$	Input High to Low		3.10		3.58		4.05		4.77	ns
$t_{HPWH}$	Minimum Pulse Width High									ns
$t_{HPWL}$	Minimum Pulse Width Low									ns
$t_{HCKSW}$	Maximum Skew		0.20		0.23		0.26		0.31	ns
$t_{HP}$	Minimum Period									ns
$t_{HMAX}$	Maximum Frequency									ns

## AX2000

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Dedicated (Hard-Wired) Array Clock Networks</b>										
$t_{HCKL}$	Input Low to High		2.80		3.23		3.66		4.31	ns
$t_{HCKH}$	Input High to Low		3.30		3.81		4.32		5.08	ns
$t_{HPWH}$	Minimum Pulse Width High									ns
$t_{HPWL}$	Minimum Pulse Width Low									ns
$t_{HCKSW}$	Maximum Skew		0.40		0.46		0.52		0.62	ns
$t_{HP}$	Minimum Period									ns
$t_{HMAX}$	Maximum Frequency									ns

## Routed Clocks

The CLK is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register into the device (R-cells and I/O registers) as

well as any of the inputs of any of the C-cells in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fan-out nets. All four CLKs are available anywhere on the chip.

### Timing Characteristics

AX125

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Routed Array Clock Networks</b>										
$t_{RCKL}$	Input Low to High		2.50		2.88		3.27		3.85	ns
$t_{RCKH}$	Input High to Low		2.50		2.88		3.27		3.85	ns
$t_{RPWH}$	Minimum Pulse Width High									ns
$t_{RPWL}$	Minimum Pulse Width Low									ns
$t_{RCKSW}$	Maximum Skew		0.30		0.35		0.39		0.46	ns
$t_{RP}$	Minimum Period									ns
$t_{RMAX}$	Maximum Frequency									ns

AX250 – TBD

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Routed Array Clock Networks</b>										
$t_{RCKL}$	Input Low to High									ns
$t_{RCKH}$	Input High to Low									ns
$t_{RPWH}$	Minimum Pulse Width High									ns
$t_{RPWL}$	Minimum Pulse Width Low									ns
$t_{RCKSW}$	Maximum Skew									ns
$t_{RP}$	Minimum Period									ns
$t_{RMAX}$	Maximum Frequency									ns



## AX500

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Routed Array Clock Networks</b>										
$t_{RCKL}$	Input Low to High		2.86		3.30		3.74		4.40	ns
$t_{RCKH}$	Input High to Low		2.86		3.30		3.74		4.40	ns
$t_{RPWH}$	Minimum Pulse Width High									ns
$t_{RPWL}$	Minimum Pulse Width Low									ns
$t_{RCKSW}$	Maximum Skew		0.64		0.74		0.84		0.98	ns
$t_{RP}$	Minimum Period									ns
$t_{RMAX}$	Maximum Frequency									ns

## AX1000

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Routed Array Clock Networks</b>										
$t_{RCKL}$	Input Low to High		3.90		4.50		5.10		6.00	ns
$t_{RCKH}$	Input High to Low		3.90		4.50		5.10		6.00	ns
$t_{RPWH}$	Minimum Pulse Width High									ns
$t_{RPWL}$	Minimum Pulse Width Low									ns
$t_{RCKSW}$	Maximum Skew		1.40		1.62		1.83		2.15	ns
$t_{RP}$	Minimum Period									ns
$t_{RMAX}$	Maximum Frequency									ns

## AX2000

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>Routed Array Clock Networks</b>										
$t_{RCKL}$	Input Low to High		4.90		5.65		6.41		7.54	ns
$t_{RCKH}$	Input High to Low		4.90		5.65		6.41		7.54	ns
$t_{RPWH}$	Minimum Pulse Width High									ns
$t_{RPWL}$	Minimum Pulse Width Low									ns
$t_{RCKSW}$	Maximum Skew		2.60		3.00		3.40		4.00	ns
$t_{RP}$	Minimum Period									ns
$t_{RMAX}$	Maximum Frequency									ns

## Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group is located at the center of the north edge (in the I/O ring) of the chip and sources the four HCLKs. The second group is located at the center of the south edge (again in the I/O ring) and sources the four CLKs (Figure 24).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 25).

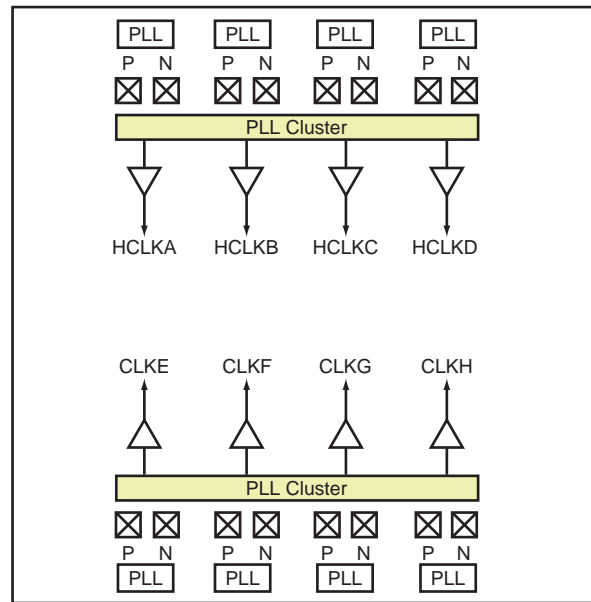


Figure 24 • PLL Group

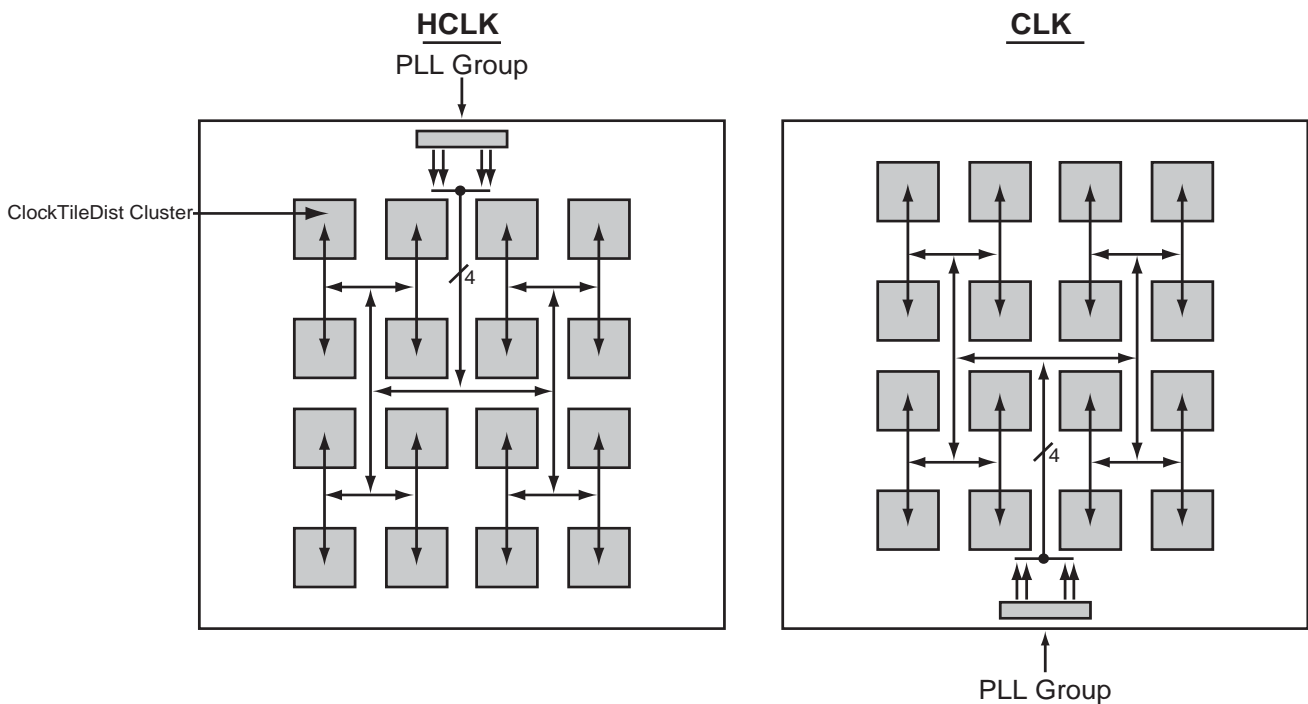


Figure 25 • Example of HCLK and CLK Distributions on the AX2000

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column.

The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row, providing for a low-skew global fanout within the core tile (Figure 26 and Figure 27).

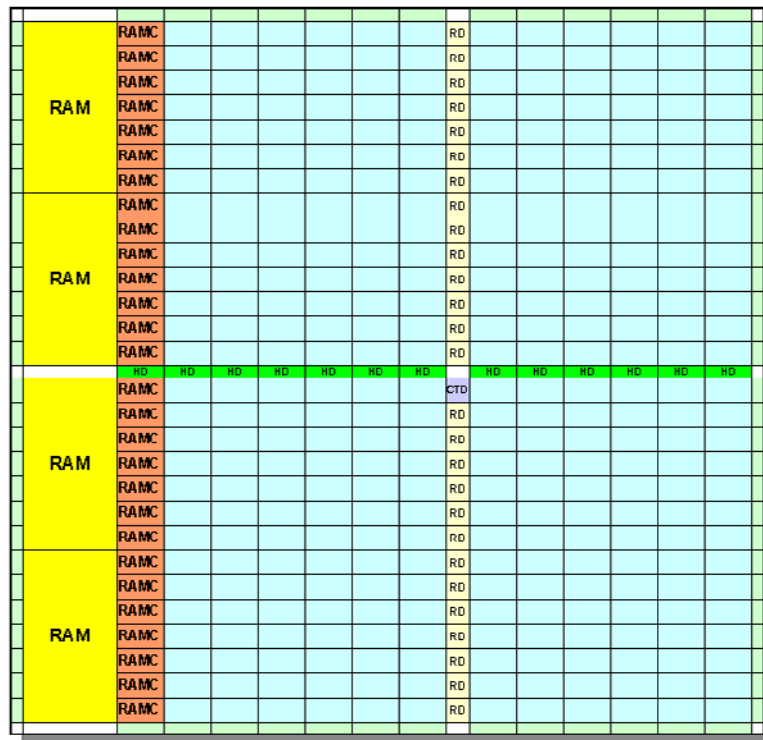


Figure 26 • CTD, CD, and HD Module Layout

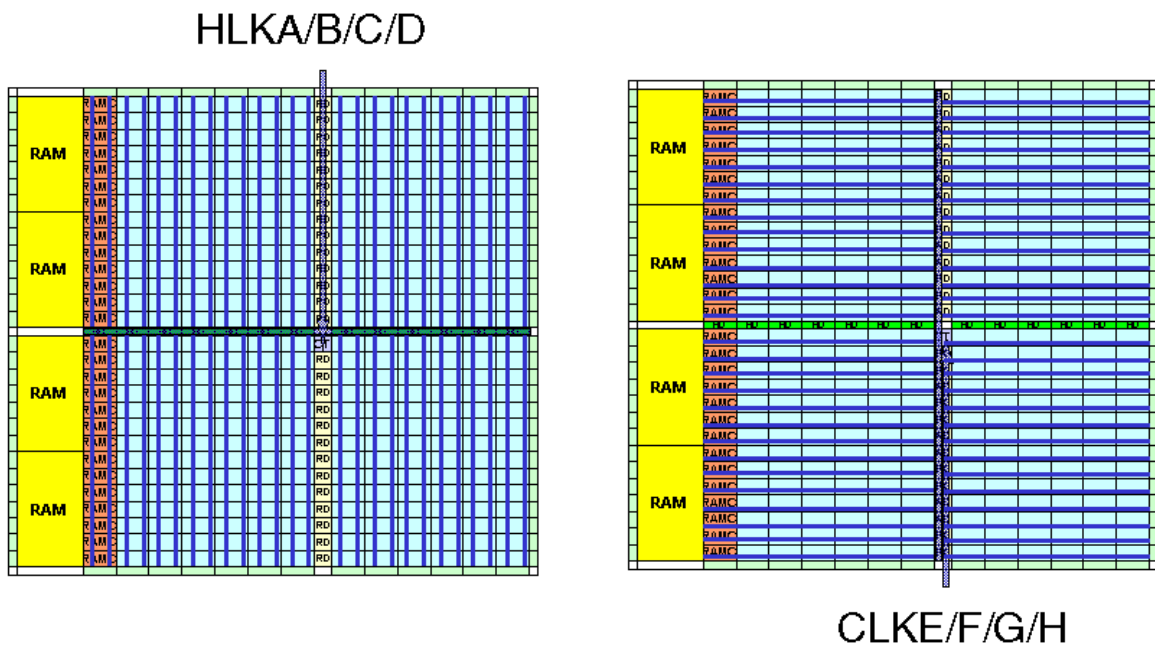


Figure 27 • HCLK and CLK Distribution within a Core Tile

The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

An unused input can be tied to ground for power savings.

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently. Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

An unused input can be tied to ground for power savings.

Thus, the AX architecture is capable of supporting a large number of local clocks – 24 HCLK segments (times four HCLKs) driving north-south and 28 CLK segments (times four CLKs) driving east-west per core tile. This capability will be supported in a later release of the design software.

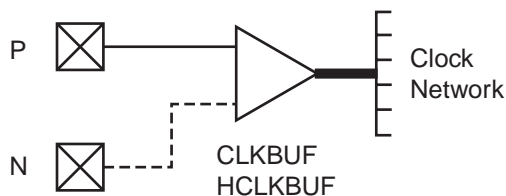
Actel's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but lower power as well. Future releases of Designer will give the user greater control over the use of these individual clock segments.

### Global Resource Access Macros

Global resources can be driven by one of three sources: an external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

#### CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF\_LVCMOS25, HCLKBUF\_LVDS, etc.) (Figure 28).



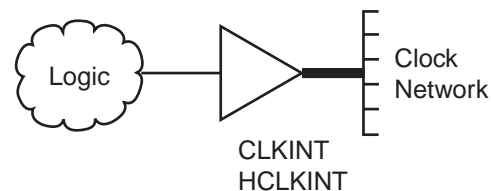
**Figure 28 • CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

#### CLKINT and HCLKINT

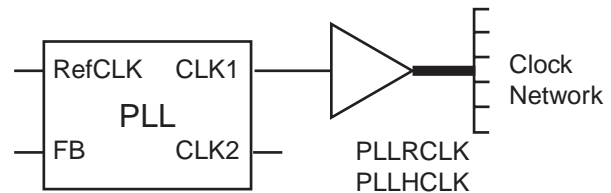
CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 29).



**Figure 29 • CLKINT and HCLKINT**

#### PLLCLK and PLLHCLK

PLLCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (Figure 30).



**Figure 30 • PLLCLK and PLLHCLK**

#### Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, etc.

In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE (Figure 31 on page 69).

There are two macros needed when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

#### PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

#### PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (Figure 32 on page 69).

Implementation Example:

Figure 33 shows a complex clock distribution example. The reference clock (RefCLK) of PLLF is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLF is being fed to the RefCLK input of PLLF. The CLK2

output of PLLF is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

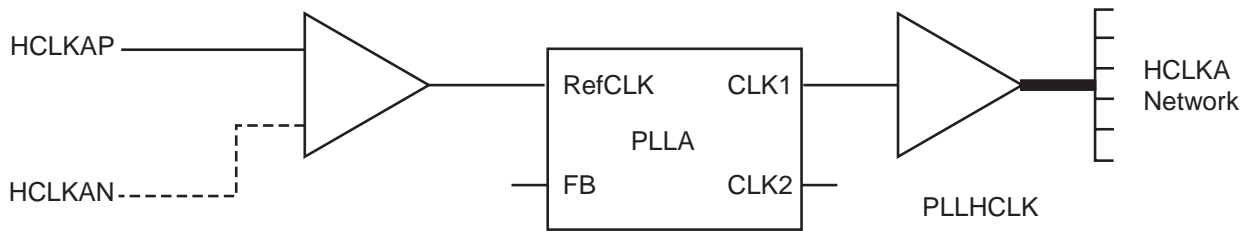


Figure 31 • Example of HCLKA driven from a PLL with External Clock Source

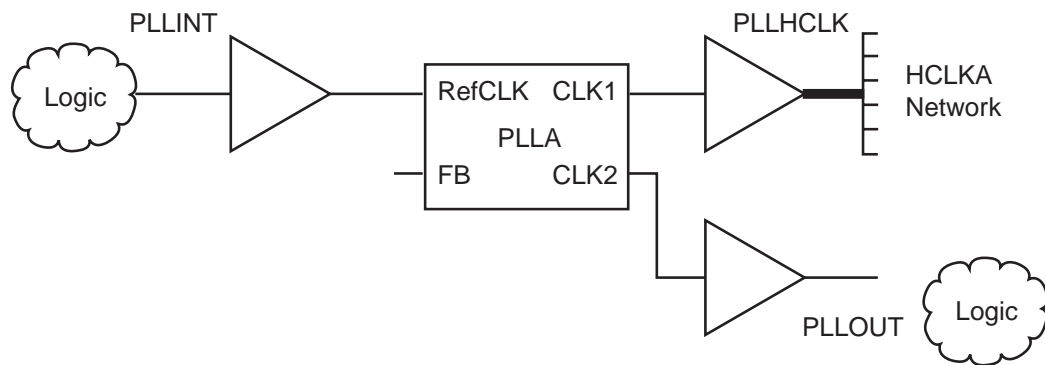


Figure 32 • Example of PLLINT and PLLOUT Usage

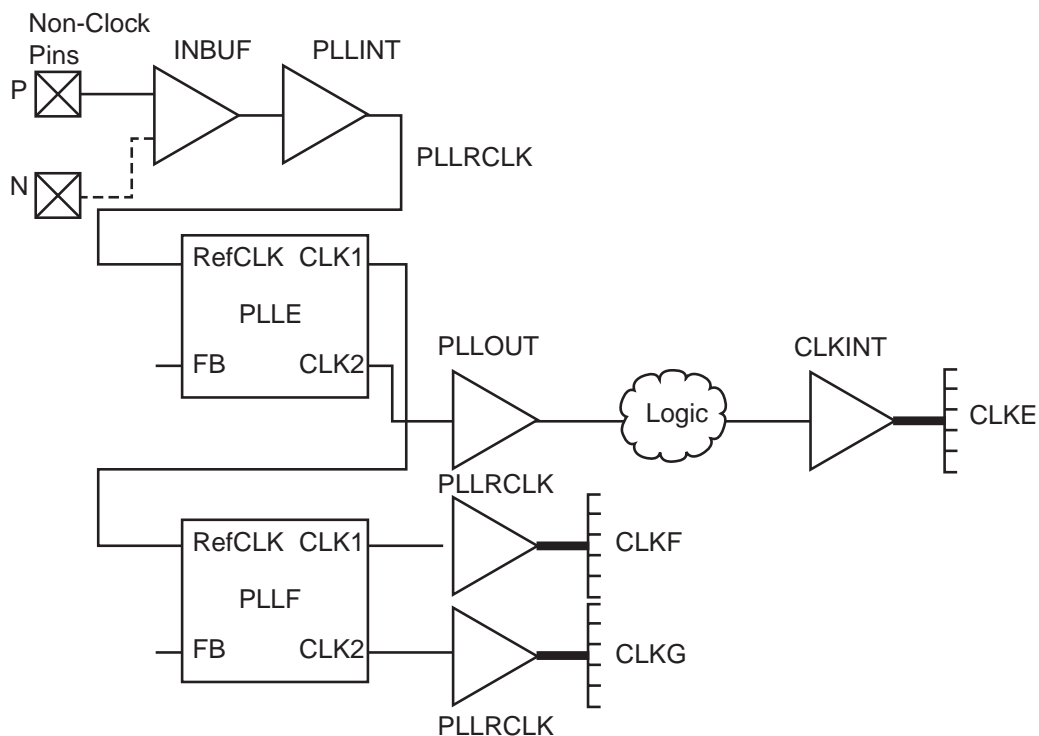


Figure 33 • Complex Clock Distribution Example

# Axcelerator Clock Management System

## Introduction

Each member of the Axcelerator family contains eight phase-locked loop (PLL) blocks which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range – 14 to 200 MHz
- Output Frequency Range – 20 MHz to 1 GHz
- Output Duty Cycle Range – 45% to 55%
- Maximum Long-Term Jitter – 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter – 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock) – 20 $\mu$ s

## Physical Implementation

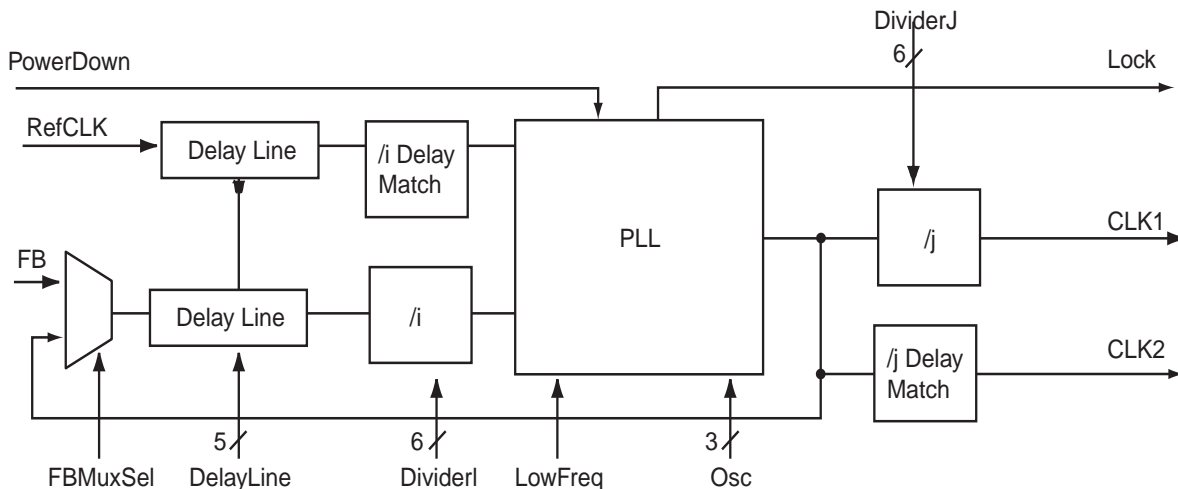
The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of

the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (e.g. PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (e.g. PLLE can drive CLKE).

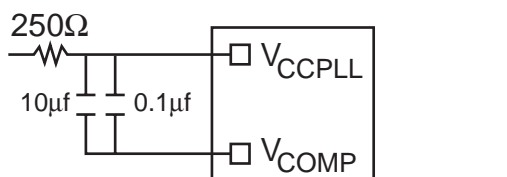
Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. [Figure 34](#) illustrates a PLL block diagram. The  $V_{CCPLL}$  pin should be connected to a 1.5V power supply through a 250 $\Omega$  resistor. Furthermore, 0.1 $\mu$ F and 10 $\mu$ F decoupling capacitors should be connected across the  $V_{CCPLL}$  and  $V_{CompPLL}$  pins. Note: The  $V_{CompPLL}$  pin should never be grounded ([Figure 35](#))!

The I/O pads associated with a PLL can also be configured for regular I/O functions except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the REFP pad can be configured as a differential pair, single-ended or voltage-referenced standard. The REFN pad can only be used as a differential pair with REFP.

The block marked “i Delay Match” is a fixed delay equal to that of the i divider. The “j Delay Match” block has the same function as its j divider counterpart.



**Figure 34 • PLL Block Diagram**



**Figure 35 • PLL Electrical Interface**

## Functional Description

Figure 34 on page 70 illustrates a block diagram of the PLL. The PLL contains two dividers, i and j, that allow frequency scaling of the clock signal:

- The i divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64, and the resultant frequency is available at the output of the PLL block.
- The j divider divides the PLL output by integer factors ranging from 1 to 64, and the divided clock is available at CLK1.
- The two dividers together can implement any combination of multiplication and division up to a maximum frequency of 1 GHz on CLK1. Both the CLK1 and CLK2 outputs have a fixed 50/50 duty cycle.

- The output frequencies of the two clocks are given by the following formulas ( $f_{REF}$  is the reference clock frequency):

$$f_{CLK1} = f_{REF} * (DividerI) / (DividerJ)$$

$$f_{CLK2} = f_{REF} * (DividerI)$$

- CLK2 provides the PLL output directly – without division

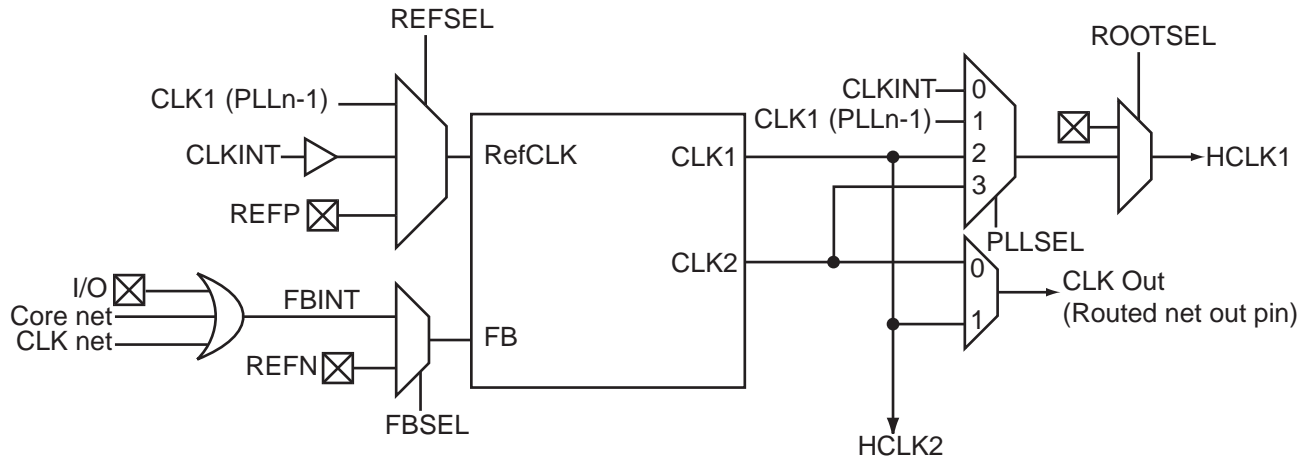
The input and output frequency ranges are selected by LowFreq and Osc(2:0), respectively. These functions are described in Table 11.

The delay lines shown in Figure 34 on page 70 are programmable. The feedback clock path can be delayed (using the 5 DelayLine bits) relative to the reference clock (or vice versa) up to 3.75 ns in increments of 250 ps. Table 11 illustrates the usage of these bits. The delay increments are independent of frequency, so this results in phase changes that vary with frequency. The delay value is highly dependent on  $V_{CC}$  and the speed grade.

**Table 11 • PLL Configuration Signals**

Pins	Type	Allowable Values	Function
LOWFREQ	Bit	0 1	RefCLK Input Frequency Range (MHz) 50 - 200 14 - 50
OSC2 - OSC0	Bit	XX0 001 011 101 111	CLK2 Output Frequency Range (MHz) 400 - 1000 200 - 400 100 - 200 50 - 100 20 - 50
DIVI5 - DIVI0	Integer	1 to 64	Clock Multiplication
DIVJ5 - DIVJ0	Integer	1 to 64	Clock Division
DELAYLINE4 - DELAYLINE0	Integer	-15 to +15	Clock Delay (positive or negative) in increments of 0.25ns

## Interface



### PLL Signals

Signal Name	Type	Function
RefCLK	Input	Reference clock for PLL.
FB	Input	Feedback port for PLL.
PowerDown	Input	When "low" powers down the PLL.
FBMuxSel	Input	Selects source of feedback path.
DividerI(5:0)	Input	Sets divide by value for feedback divider.
DividerJ(5:0)	Input	Sets divide by value for "CLK1" divider.
DelayLine(4:0)	Input	Sets delay value from -3.75 ns to +3.75 ns in 250ps increments, with the MSB being a sign bit.
Osc(2:0)	Input	Sets frequency range for PLL output.
LowFreq2:0)	Input	Set input frequency range.
Lock	Output	High value indicates PLL has locked.
CLK1	Output	PLL core output.
CLK2	Output	PLL core output.

#### RefCLK

Table 12 shows the different sources for the reference clock input (RefCLK) to the PLL. This is determined by the value of the two REFSEL bits. Please note that the REFSEL bits are not accessible to the user and are statically configured by the Designer software.

**Table 12 • RefCLK Input Connections**

REFSEL[1:0]	RefCLK Input
00	CLK1 output from an adjacent PLL
01	CLKINT net from the FPGA core
1x	The attached I/O pad

#### FB

The feedback input (FB) to the PLL is controlled by FBMuxSEL.



### ROOTSEL

The ROOTSEL signal, along with the two PLLSEL bits, select the Clock Tree Root (i.e. the driver of the HCLK or CLK network) between external or internal sources.

ROOTSEL	PLLSEL[1:0]	Clock Tree Root
0	XX	The attached I/O pad
1	00	CLKINT net from FPGA core
1	01	CLK1 of the adjacent PLL cell
1	10	CLK1 of the same PLL cell
1	11	CLK2 of the same PLL cell

### OUTSEL

The OUTSEL signal selects the routed net output from one of two PLL outputs:

- CLK1
- CLK2

### Lock

The Lock output signal indicates that the PLL has locked onto the incoming signal.

### Power Down

The PLL also includes an active-low power-down signal and consumes very little standby current in this mode.

## PLL Configurations

The following rules apply to the different PLL inputs and outputs:

### Reference Clock

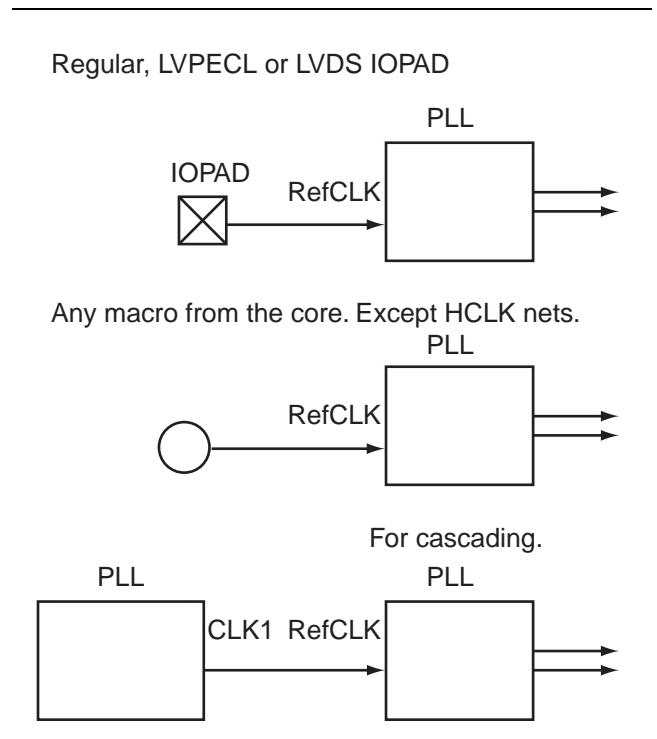
The RefCLK can be driven by (Figure 36):

1. Any net from the core via the CLKINT macro (except on HCLK net)
2. CLK1 of the adjacent PLL
3. REFP (single-ended or voltage-referenced)
4. REFP/REFN pair (differential modes like LVPECL or LVDS)

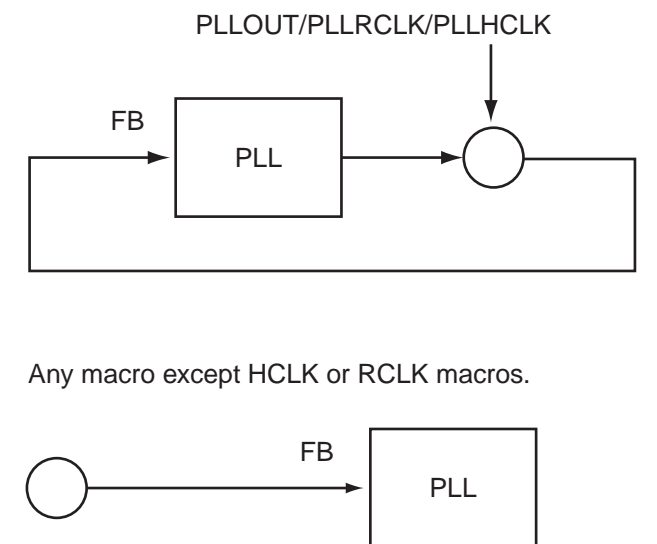
### Feedback Clock

The feedback clock can be driven by (Figure 37):

1. Any net from the core (except HCLK)
2. External REFP I/O pad from the adjacent PLL cell
3. An internal signal from the PLL block



**Figure 36 • Reference Clock Connections**



**Figure 37 • Feedback Clock Connections**

## CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLLs RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (Table 13).

**Table 13 • PLL General Connections Rules**

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

### Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same *type* of global resource (i.e. either HCLK or CLK).
- Only one can drive a routed net at any given time.

Table 14 and Table 15 specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (Note that HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (Figure 34 on page 70).

**Table 14 • North PLL Connections**

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable

**Table 14 • North PLL Connections (Continued)**

CLK1	CLK2
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

**Note:** Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g. CLK1 driving HCLK1, and HCLK2 is not supported).

**Table 15 • South PLL Connections**

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

**Note:** Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (e.g. CLK1 driving HCLK1, and HCLK2 is not supported).

## Special PLL Macros

Table 16 shows the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

**Table 16 • PLL Special Macros**

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLRCLK	Connects CLK1 or CLK2 to the CLK network.
PL LHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

## Electrical Specifications

Parameter	Value	Notes
<b>Frequency Ranges</b>		
Reference Frequency (min.)	14 MHz	Lowest input frequency
Reference Frequency (max.)	200 MHz	Highest input frequency
OSC Frequency (min.)	20 MHz	Lowest output frequency
OSC Frequency (max.)	1 GHz	Highest output frequency
<b>Jitter</b>		
Long-Term Jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-Term Jitter (max.)	100ps	High reference clock frequencies
Short-Term Jitter (max.)	50ps+1%	Percentage of output frequency
<b>Acquisition Time (lock) from Cold Start</b>		
Acquisition Time (max.)	400 cycles	Period of low reference clock frequencies
Acquisition Time (max.)	1.5 $\mu$ s	High reference clock frequencies
<b>Power Consumption</b>		
Analog Supply Current (low freq.)	200 $\mu$ A	Current at minimum oscillator frequency
Analog Supply Current (high freq.)	200 $\mu$ A	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 $\mu$ A/MHz	Current at maximum oscillator frequency, unloaded
Digital Supply Current (high freq.)	1 $\mu$ A/MHz	Frequency-dependent current
<b>Duty Cycle</b>		
Minimum Duty Cycle	45%	
Maximum Duty Cycle	55%	

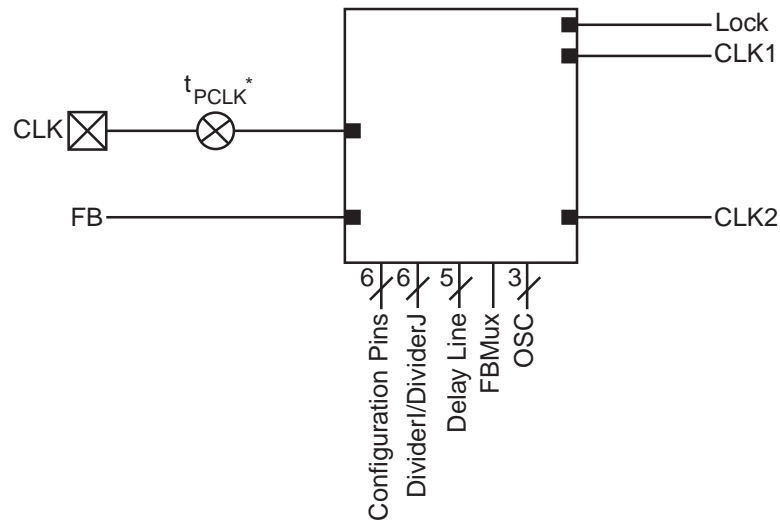
## User Flow

There are two methods of including a PLL in a design:

- The recommended method of using a PLL to create custom PLL blocks that can be instantiated in a design utilize ACTgen.
- The alternative is to instantiate one of the generic library primitives into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

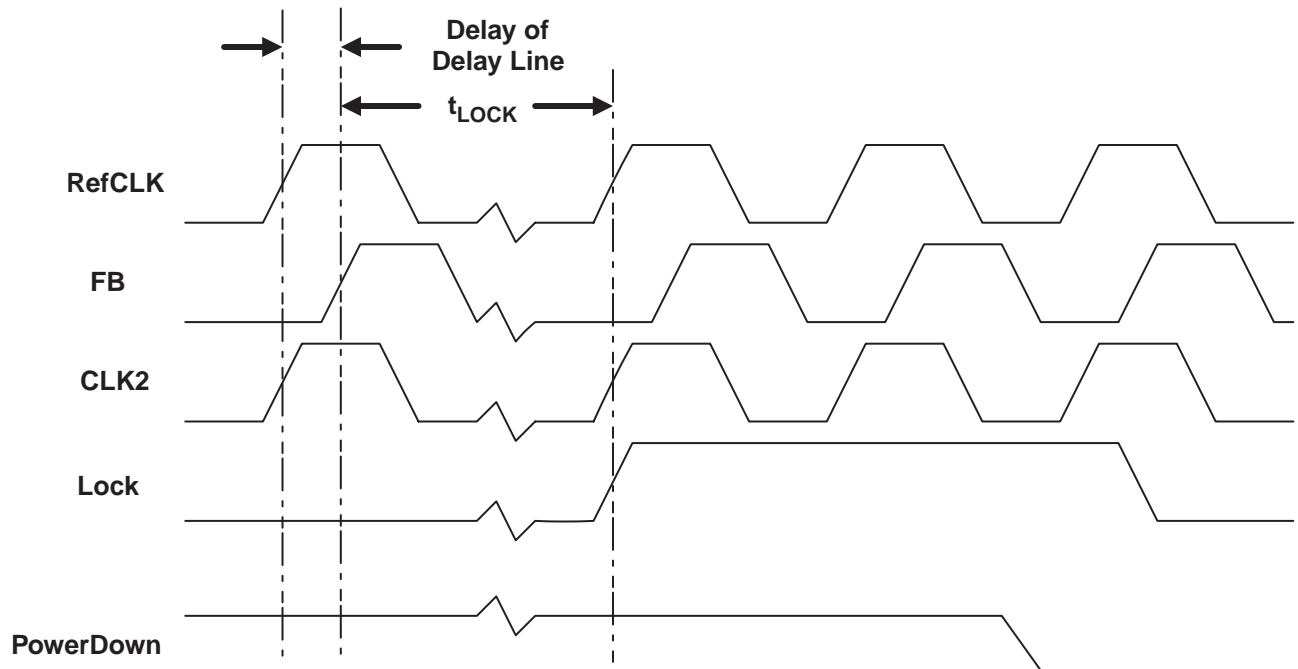
## Timing Characteristics

### PLL Model



**Note:**  $t_{PCLK}^*$  is the delay in the clock signal.

Timing Waveforms



Timing Characteristics

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>PLL</b>										
	RefCLK Low to High Pulse Width									ns
	RefCLK Drift Period (change in frequency with time)									ns
	CLK1 Period Jitter		0.18		0.18		0.18		0.18	ns
	CLK2 Period Jitter		0.18		0.18		0.18		0.18	ns
$t_{LOCK}$	Aquisition Time (lock)		1500		1500		1500		1500	ns
$t_{PCLK}$	Delay in the Clock Signal									

## Sample Implementations

### Frequency Synthesis

Figure 38 illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

Figure 39 uses both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

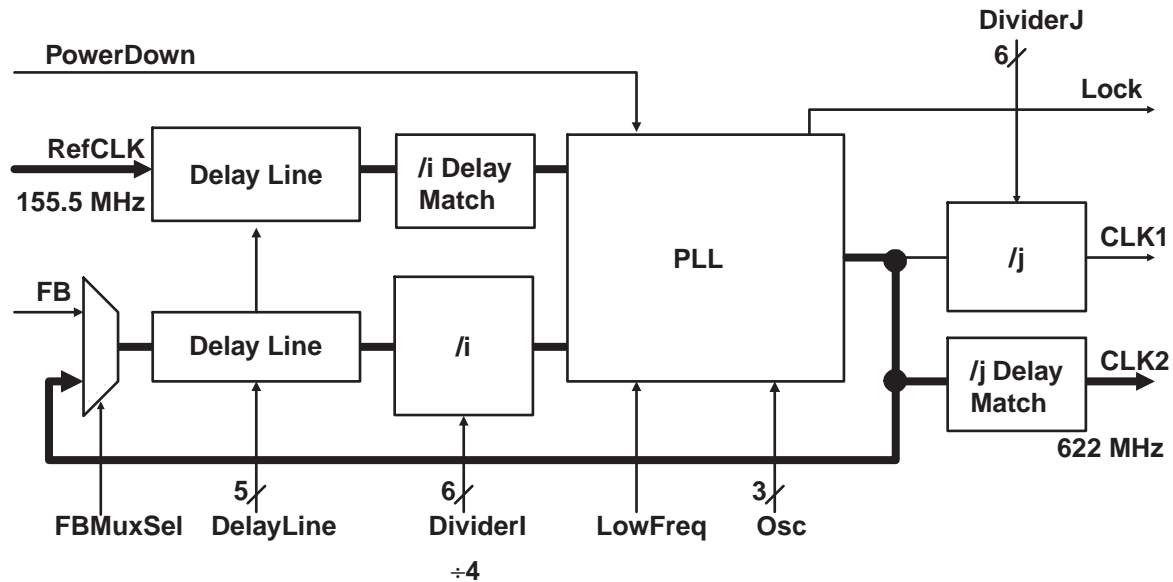


Figure 38 • Using the PLL 155.5 MHz In, 622 MHz Out

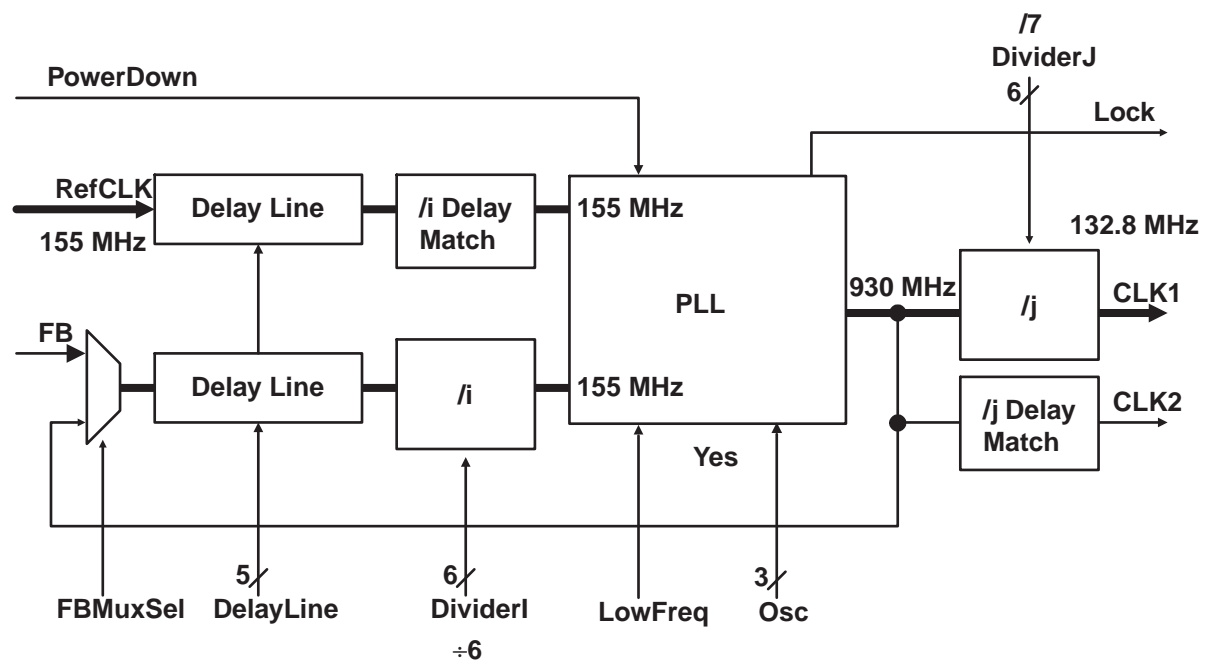


Figure 39 • Using the PLL 155 MHz In, 133 MHz Out

## Adjustable Clock Delay

Figure 40 illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference

clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

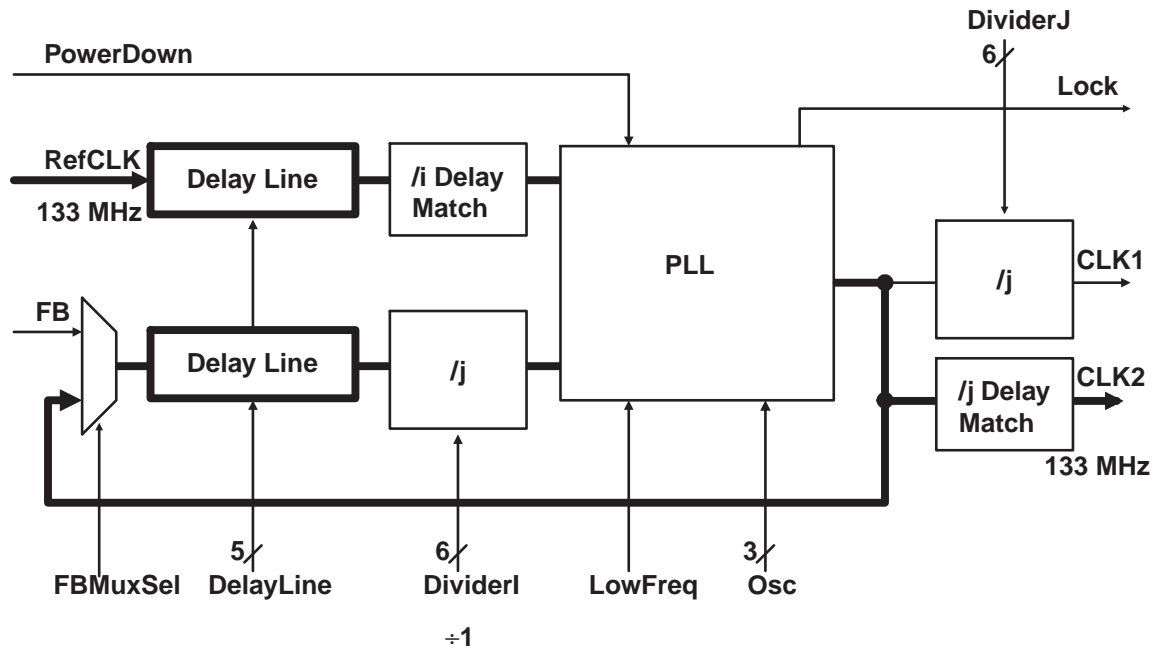
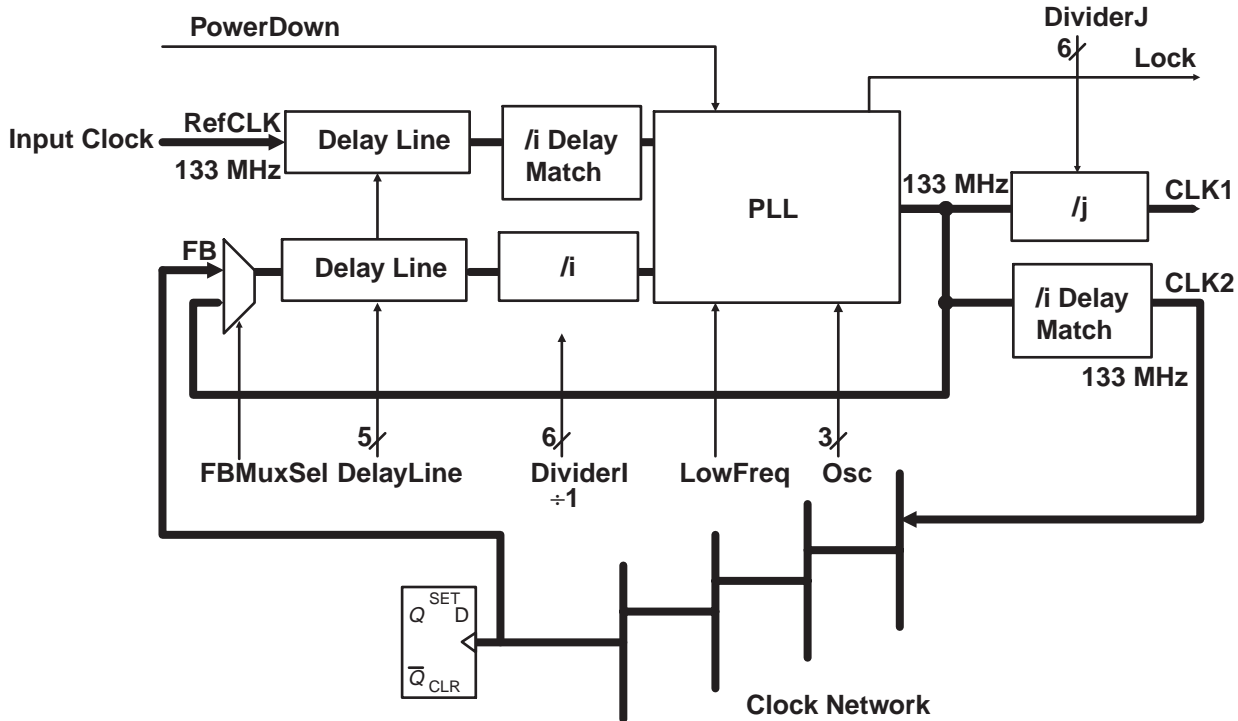


Figure 40 • Using the PLL Delaying the Reference Clock

## Clock Skew Minimization

Figure 41 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the "input" clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The

PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Accelerator Family PLL and Clock Management* application note for more information.



**Figure 41** • Using the PLL for Clock Deskewing



# PerPin FIFO and I/O FIFO Embedded Controller

## PerPin FIFO

### Introduction

The AX architecture provides a dedicated 64-bit PerPin FIFO in each I/O module (Figure 1 on page 22). The AX PerPin FIFO has separate read (RCLK) and write (WCLK) clocks. This enables crossing clock and phase domains.

The PerPin FIFO can buffer the input data, output data, or be bypassed. It can be individually controlled using core logic or by the dedicated I/O FIFO Embedded Controller, which is capable of controlling a set of PerPin FIFOs for bus applications. The I/O FIFO Embedded Controller does not consume any of the core logic cells and also gives better performance.

### Modes of Operation

There are two modes of operation for the PerPin FIFO:

1. **Single PerPin FIFO:** When used in this mode, the PerPin FIFO can be individually controlled; in which case the flag logic has to be built into the FPGA with the same control signals.
2. **Bus PerPin FIFO (i.e. FIFO Block):** Multiple I/Os (from 1 to 26) can be combined together to form a block. The block can be controlled via the I/O FIFO Embedded Controller.

### Functionality

The depth of the PerPin FIFO is 64 bits of input or output data. It has active-low clear, read enable, and write enable. The PerPin FIFO features synchronous read and write. There is a separate read clock and a separate write clock allowing these operations to be completely independent of each other. The RCLK and WCLK can be connected to any of the HCLKs, any of the CLKs, or internal logic (Figure 42).

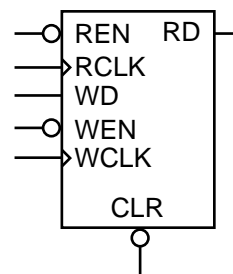


Figure 42 • PerPin FIFO Block Diagram

### PerPin FIFO Control Interface

The control signals for the PerPin FIFO are MUXed, as shown in Figure 43, to allow for the sourcing of the different modes of operation.

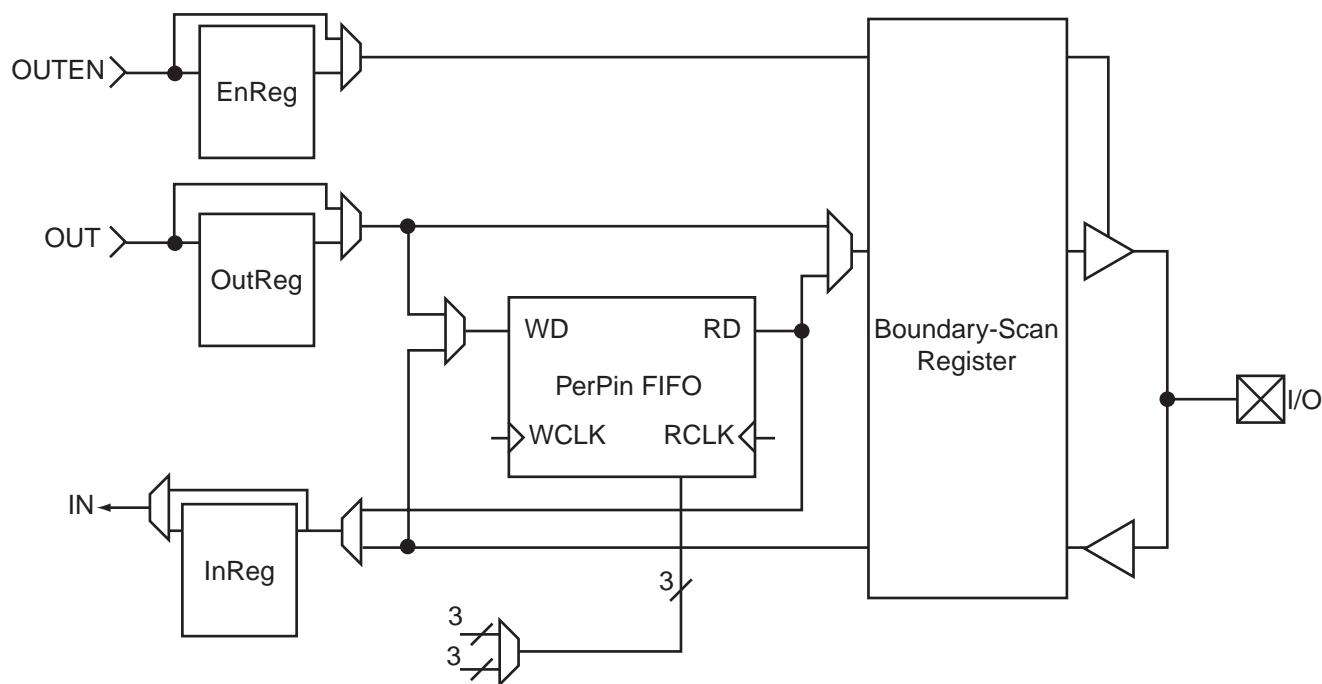


Figure 43 • PerPin FIFO Enable Control Interface

## PerPin FIFO Signal Description

Pin Name	Width	Function
CLR	1 bit	Clear input (active low). Asserting this signal clears the output data and resets the read and write addresses to FIFO memory to location 0.
RCLK	1 bit	Read clock input (rising-edge triggered).
WCLK	1 bit	Write clock input (rising-edge triggered).
REN	1 bit	Read enable input (active low). Asserting REN before the rising edge of RCLK outputs data at the current read address and then increments the read address.
WEN	1 bit	Write enable input (active low). Asserting WEN before the rising edge of WCLK writes data at the current write address and then increments the write address.
RD	1 bit	Read data.
WD	1 bit	Write data.

## I/O FIFO Embedded Controller

### Introduction

There are two I/O modules in each I/O Cluster ([Figure 1 on page 22](#)). There are two I/O FIFO Embedded Controllers per tile edge. The I/O FIFO Embedded Controller can be used when one or more I/Os are combined to form a FIFO Block. Combining adjacent I/Os for a particular I/O FIFO Embedded Controller is recommended.

The exact number of PerPin FIFOs controlled by a single I/O FIFO Embedded Controller depends on the die and package selected, the location on the chip, and the type of I/O buffers used. It can vary from 18 to 26. Furthermore, the PerPin FIFO of an unbonded pad cannot be used, and only one PerPin FIFO in an I/O Cluster is usable when differential pads are employed.

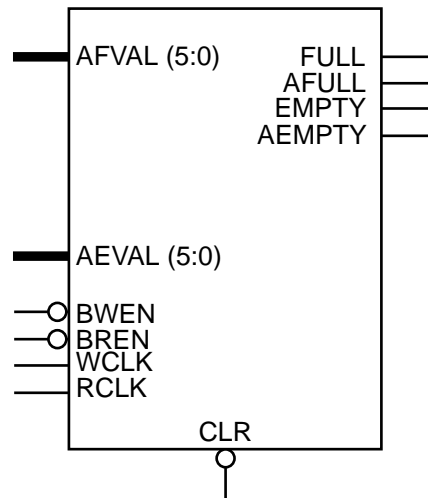
### Functionality

The I/O FIFO Embedded Controller can control several surrounding PerPin FIFOs for bus applications ([Figure 44](#)). It generates a full set of flags (EMPTY, FULL, AEMPTY, and AFULL) the same way they are generated in the RAM FIFO Controller. The user can set the almost empty and almost full threshold values.

The FIFO inhibits writing when the FULL flag is asserted and inhibits reading when the EMPTY flag is asserted.

### Interface

The I/O FIFO Embedded Controller and its surrounding PerPin FIFOs must be connected to the same clock signal. Note that the top and bottom I/O Clusters share two tile-wide CLK segments. Side I/O Clusters share one tile-wide HCLK segment (Refer to the [“Global Resources” section on page 62](#) for more information). All FIFOs associated with the Controller should have compatible technologies and should belong to the same bank. It is recommended that the user employs adjacent controllers to control their respective PerPin FIFOs.



**Figure 44 • I/O FIFO Embedded Controller Block Diagram**

The pin names and functions are described in Table 17.

**Table 17 • PerPin FIFO Embedded Controller**

Pin Name	Width	Function
CLR	1 bit	Active low clear input. Clears FULL and AFULL.
RCLK	1 bit	Rising edge triggered read clock input. When REN active, memory usage counter increments at active RCLK edge.
WCLK	1 bit	Rising edge triggered write clock input. When WEN active, memory usage counter incremented at active WCLK edge.
BREN	1 bit	PerPin FIFO block REN output. Used to drive REN input(s) of controlled PerPin FIFO(s).
BWEN	1 bit	PerPin FIFO block WEN output. Used to drive WEN input(s) of controlled PerPin FIFO(s).
AFVAL0 to AFVAL5	5 bits	AFULL threshold value inputs. All 6 bits used together to specify an absolute binary memory address in the range of 0 to 63.
AEVAL0 to AEVAL5	5 bits	AEMPTY threshold value inputs. All 6 bits used together to specify an absolute binary memory address in the range of 0 to 63.
FULL	1 bit	FIFO full output. It is set to logic "1" when all 64 bits of memory used.
AFULL	1 bit	FIFO AFULL output. It is set to logic "1" when amount of memory used reaches or exceeds AFVAL threshold.
EMPTY	1 bit	FIFO EMPTY output. It is set to logic "1" when amount of memory used drops to zero.
AEMPTY	1 bit	FIFO AEMPTY output. It is set to logic "1" when amount of memory used reaches or drops below AEVAL threshold.
REN	1 bit	Active low read enable input.
BCLR	1 bit	Active Low. PerPin FIFO block BCLR output. Used to drive BCLR input(s) of controlled PerPin FIFO(s).
WEN	1 bit	Active low write enable input.

## DDR\_FIFO

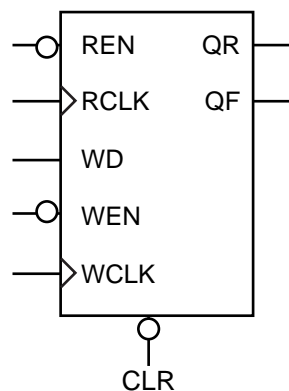
A DDR\_FIFO can also be created using the ACTgen macro builder. It can be connected to an input buffer (i.e. INBUF) implementing any I/O standard to allow double data rate FIFO functionality. Note that when DDR is used, the maximum number of PerPin FIFOs that can be controlled by a single I/O FIFO Embedded Controller ranges from 9 to 13. Also, when single-ended standards are used to implement DDR, only the p-input is used. When differential standards are used; however, both inputs (p and n) are employed.

Figure 45 illustrates the DDR\_FIFO interface, where the QR output is the output of the rising-edge-triggered PerPin FIFO, and the QF output is the output of the falling-edge-triggered PerPin FIFO.

## Building the PerPin FIFO and the Controller

To access the PerPin FIFO, FIFO-Block or the I/O FIFO Embedded Controller, the user must instantiate them in the netlist and then connect them to the I/Os. Actel's Designer software will then combine the PerPin FIFOs with the I/Os where appropriate.

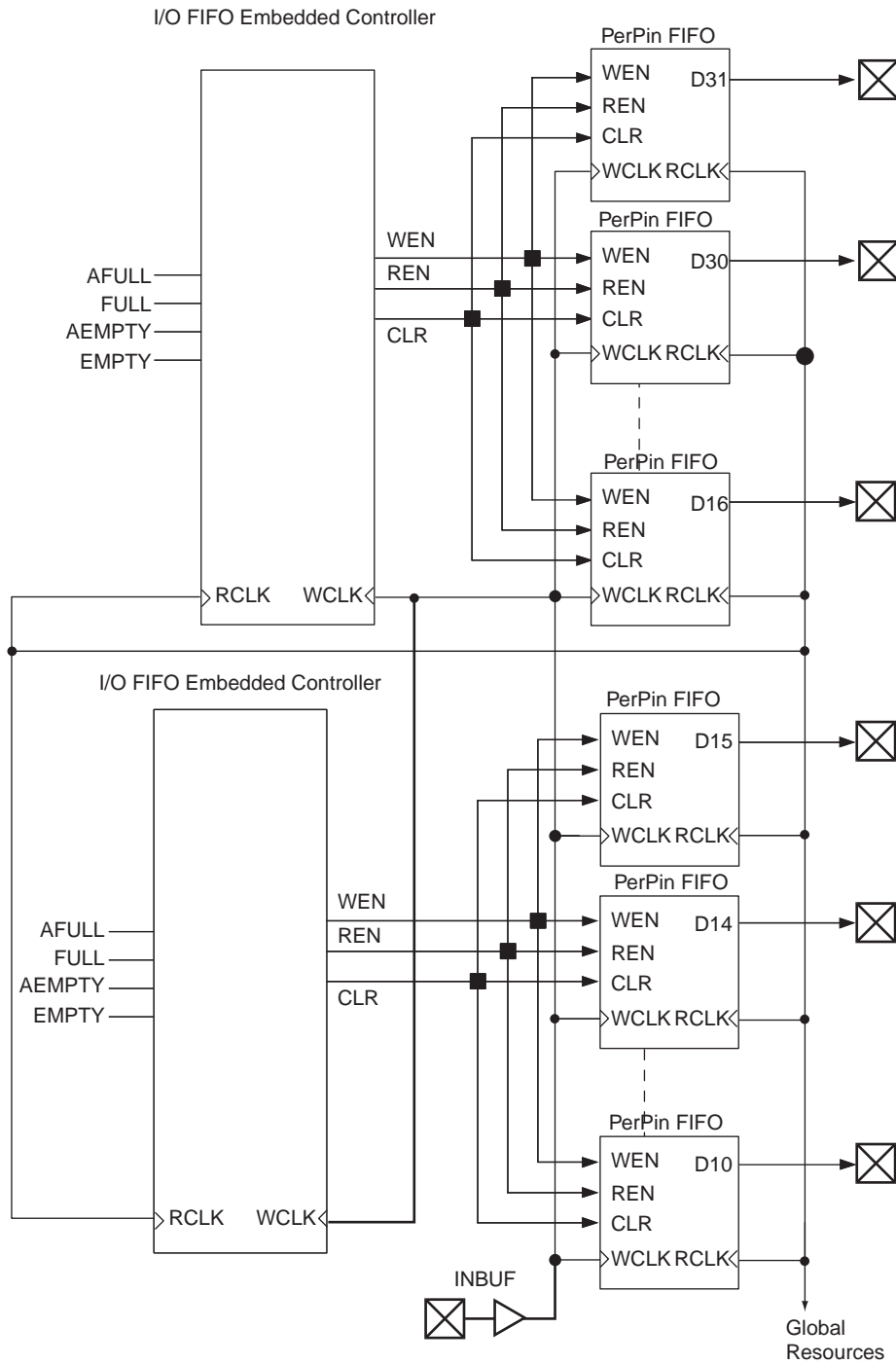
There are two ways that can be used to build the PerPin FIFO and the I/O FIFO Embedded Controller:



**Figure 45 • DDR FIFO Block Diagram**

1. The recommended method for configuring the PerPin FIFO and the I/O FIFO Embedded Controller is using Actel's macro builder, ACTgen. Please refer to the application note, *Using the Axcelerator PerPin FIFOs* for details on how to build the PerPin FIFO, the Bus PerPin FIFO (i.e. PerPin FIFO Block), and the I/O FIFO Embedded Controller.
2. The alternative to using ACTgen is to instantiate one or more of the PerPin FIFOs into either the schematic or the HDL netlist, connecting all inputs and outputs to the desired signals.

## Sample Implementation



**Note:** D= RD or WD.

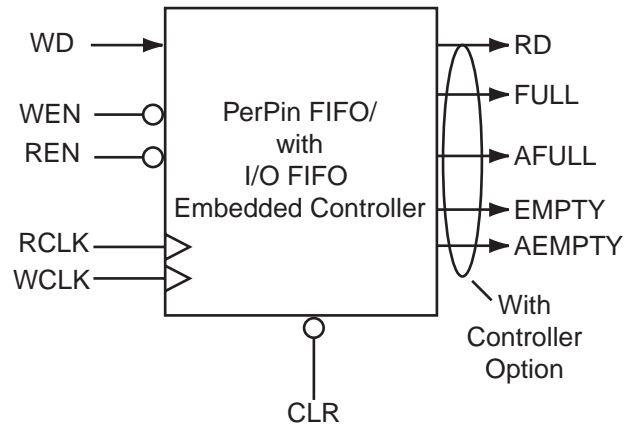
## Power-Up Behavior

The PerPin FIFO blocks reset on power-up.

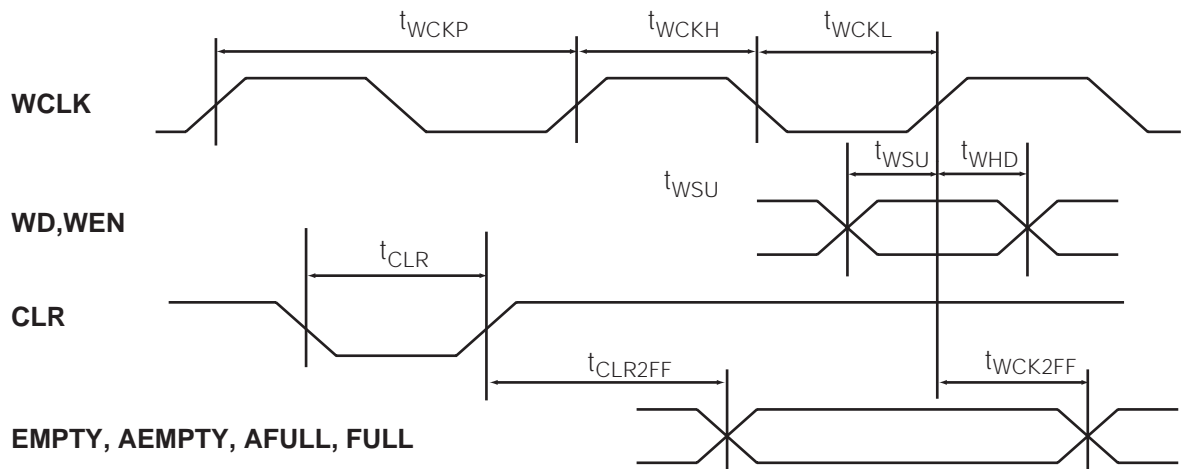
## Physical Implementation

### Timing Characteristics

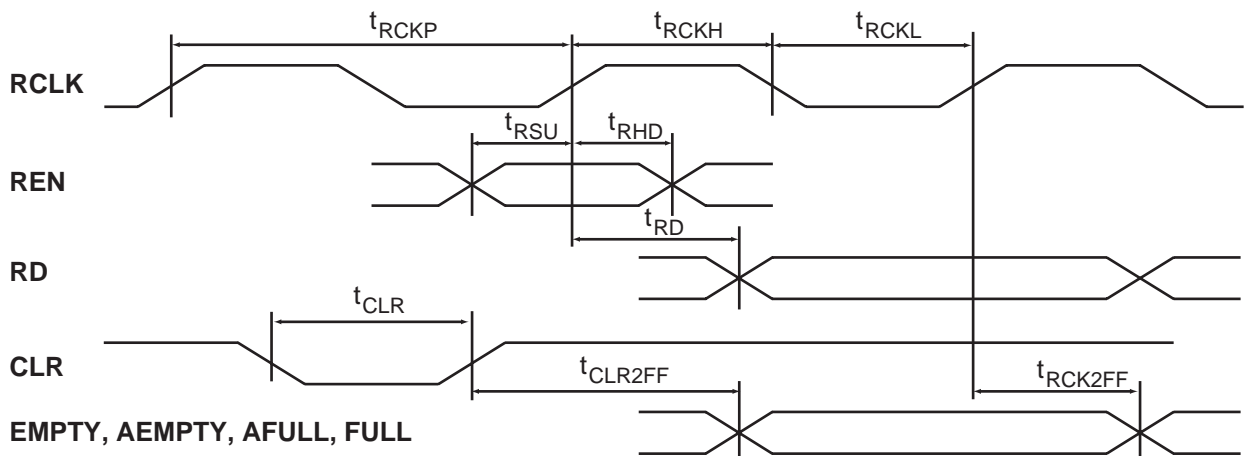
#### PerPin FIFO Model



PerPin FIFO with I/O FIFO Embedded Controller Write



PerPin FIFO with I/O FIFO Embedded Controller Read



Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>I/O FIFO Module Timing</b>										
$t_{WCKH}$	WCLK High									ns
$t_{WCKL}$	WCLK Low									ns
$t_{RCKH}$	RCLK High									ns
$t_{RCKL}$	RCLK Low									ns
$t_{RD}$	Read Time									ns
$t_{CLR}$	Clear Low									ns

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>PerPin FIFO Module Timing (Dynamic AF/AE with I/O FIFO Embedded Controller Mode)</b>										
$t_{WCKH}$	WCLK High									ns
$t_{WCKL}$	WCLK Low									ns
$t_{RCKH}$	RCLK High									ns
$t_{RCKL}$	RCLK Low									ns
$t_{RCK2RD1}$	Sequential Clock-to-Q									ns
$t_{CLR}$	Asynchronous Clear Low									ns
$t_{CLK}$	Clock Period									ns
$t_{CLR2FF}$	Asynchronous Clear -to-flag EMPTY/FULL		1.09		1.26		1.42		1.67	ns
$t_{CLR2FF}$	Asynchronous Clear -to-flag AEMPTY/AFULL		3.15		3.64		4.12		4.85	ns
$t_{CLK2FF}$	Clock-to-flag EMPTY/FULL		1.17		1.36		1.54		1.81	ns
$t_{CLK2FF}$	Clock-to-flag AEMPTY/AFULL		3.99		4.60		5.21		6.13	ns
$t_{EB2FF}$	Eval bits-to-flag AEMPTY/AFULL		2.84		3.28		3.71		4.37	ns

## Embedded Memory

The Axcelerator Family has extensive memory resources that can be used as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency less than or equal to 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The AX memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in [Figure 46](#).

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

**Table 18 • Memory Block WxD Options**

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

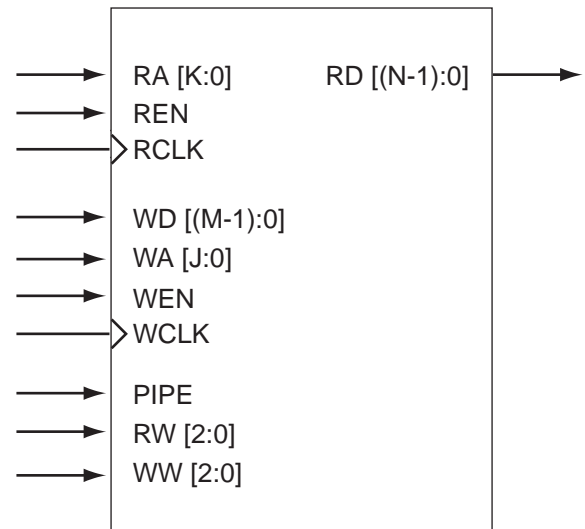
### Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

### RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The DxW different configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2, and 4kx1.



**Figure 46 • Axcelerator Memory Module**

### RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion ([Table 18](#)). Each block has independent read and write ports which enable simultaneous read and write operations.

The allowable RW and WW values are shown in [Table 19 on page 88](#).

When widths of 1, 2, and 4 are selected, the ninth bit is unused.

For example, when writing 9-bit values and reading 4-bit values, only the first 4 bits and the second 4 bits of each 9-bit value are addressable for read operations. The 9th bit is not accessible.

Conversely, when writing 4-bit values and reading 9-bit values, the 9th bit of a read operation will be undefined.

Note, that the RAM blocks employ little-endian byte order for read and write operations.

## RAM Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus. The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to 15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipe option to be on or off.

**Table 19 • Allowable RW and WW Values**

RW(2:0)	WW(2:0)	D x W
000	000	4kx1
001	001	2kx2
010	010	1kx4
011	011	512x9
100	100	256x18
101	101	128x36
11x	11x	reserved

## Modes of Operation

There are two read modes and one write mode:

- Read Non-pipelined (synchronous – one clock edge):

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read port clock active edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

- Read Pipelined (synchronous – two clock edges):

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting the PIPE to ON enables this mode.

- Write (synchronous – one clock edge):

On the write clock active edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements in the “[Timing Characteristics](#)” section on [page 89](#).

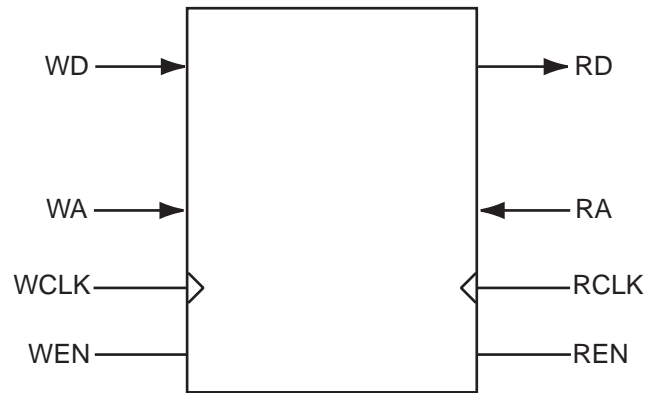
## RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port. The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation. This feature is disabled by programming the security fuse (See the “[Special Fuses](#)” section on [page 108](#)).

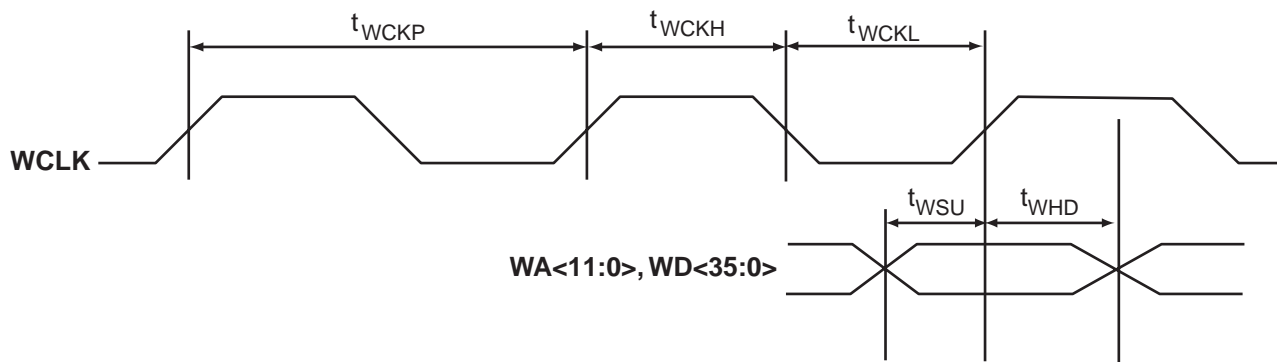


## Timing Characteristics

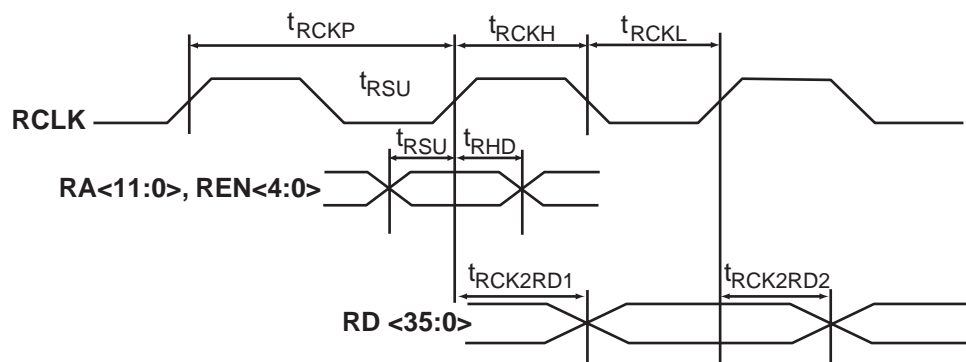
### SRAM Model



### RAM Write Timing Waveforms



### RAM Read Timing Waveforms



## One RAM Block

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>										
$t_{WDSU}$	Write Data Setup vs. WCLK		0.98		1.13		1.28		1.51	ns
$t_{WDHD}$	Write Data Hold vs. WCLK		0.20		0.20		0.20		0.20	ns
$t_{WADSU}$	Write Address Setup vs. WCLK		0.98		1.13		1.28		1.51	ns
$t_{WADHD}$	Write Address Hold vs. WCLK		0.20		0.20		0.20		0.20	ns
$t_{WENSU}$	Write Enable Setup vs. WCLK		0.98		1.13		1.28		1.51	ns
$t_{WENHD}$	Write Enable Hold vs. WCLK		0.20		0.20		0.20		0.20	ns
$t_{WCKH}$	WCLK Minimum High Pulse Width									ns
$t_{WCLK}$	WCLK Minimum Low Pulse Width									ns
$t_{WCKP}$	WCLK Minimum Period									ns
<b>Non-Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		0.73		0.84		0.95		1.12	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		0.73		0.84		0.95		1.12	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		2.07		2.39		2.71		3.18	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns
<b>Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		0.73		0.84		0.95		1.12	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		0.73		0.84		0.95		1.12	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		1.27		1.47		1.66		1.95	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns

## Two RAM Blocks are Cascaded

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>										
t <sub>WDSU</sub>	Write Data Setup vs. WCLK		1.27		1.47		1.66		1.95	ns
t <sub>WDHD</sub>	Write Data Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WADSU</sub>	Write Address Setup vs. WCLK		1.27		1.47		1.66		1.95	ns
t <sub>WADHD</sub>	Write Address Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WENSU</sub>	Write Enable Setup vs. WCLK		1.27		1.47		1.66		1.95	ns
t <sub>WENHD</sub>	Write Enable Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WCKH</sub>	WCLK Minimum High Pulse Width									ns
t <sub>WCLK</sub>	WCLK Minimum Low Pulse Width									ns
t <sub>WCKP</sub>	WCLK Minimum Period									ns
<b>Non-Pipelined Read Mode</b>										
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RCO</sub>	RCLK-To-OUT		2.16		2.49		2.82		3.32	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width									ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width									ns
t <sub>RCKP</sub>	RCLK Minimum Period									ns
<b>Pipelined Read Mode</b>										
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RCO</sub>	RCLK-To-OUT		1.37		1.58		1.79		2.11	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width									ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width									ns
t <sub>RCKP</sub>	RCLK Minimum Period									ns

## Four RAM Blocks are Cascaded

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>										
$t_{WDSU}$	Write Data Setup vs. WCLK		2.15		2.48		2.81		3.31	ns
$t_{WDHD}$	Write Data Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
$t_{WADSU}$	Write Address Setup vs. WCLK		2.15		2.48		2.81		3.31	ns
$t_{WADHD}$	Write Address Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
$t_{WENSU}$	Write Enable Setup vs. WCLK		2.15		2.48		2.81		3.31	ns
$t_{WENHD}$	Write Enable Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
$t_{WCKH}$	WCLK Minimum High Pulse Width									ns
$t_{WCLK}$	WCLK Minimum Low Pulse Width									ns
$t_{WCKP}$	WCLK Minimum Period									ns
<b>Non-Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		2.80		3.23		3.66		4.31	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		2.80		3.23		3.66		4.31	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		2.71		3.13		3.54		4.17	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns
<b>Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		2.80		3.23		3.66		4.31	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		2.80		3.23		3.66		4.31	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		2.26		2.61		2.96		3.48	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns

## Eight RAM Blocks are Cascaded

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>										
t <sub>WDSU</sub>	Write Data Setup vs. WCLK		5.25		6.06		6.87		8.08	ns
t <sub>WDHD</sub>	Write Data Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WADSU</sub>	Write Address Setup vs. WCLK		5.25		6.06		6.87		8.08	ns
t <sub>WADHD</sub>	Write Address Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WENSU</sub>	Write Enable Setup vs. WCLK		5.25		6.06		6.87		8.08	ns
t <sub>WENHD</sub>	Write Enable Hold vs. WCLK		0.00		0.00		0.00		0.00	ns
t <sub>WCKH</sub>	WCLK Minimum High Pulse Width									ns
t <sub>WCLK</sub>	WCLK Minimum Low Pulse Width									ns
t <sub>WCKP</sub>	WCLK Minimum Period									ns
<b>Non-Pipelined Read Mode</b>										
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		6.14		7.08		8.03		9.45	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		6.14		7.08		8.03		9.45	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RCO</sub>	RCLK-To-OUT		3.24		3.74		4.24		4.98	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width									ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width									ns
t <sub>RCKP</sub>	RCLK Minimum Period									ns
<b>Pipelined Read Mode</b>										
t <sub>RADSU</sub>	Read Address Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RADHD</sub>	Read Address Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RENSU</sub>	Read Enable Setup vs. RCLK		1.55		1.79		2.03		2.38	ns
t <sub>RENHD</sub>	Read Enable Hold vs. RCLK		0.00		0.00		0.00		0.00	ns
t <sub>RCO</sub>	RCLK-To-OUT		1.37		1.58		1.79		2.11	ns
t <sub>RCLKH</sub>	RCLK Minimum High Pulse Width									ns
t <sub>RCLKL</sub>	RCLK Minimum Low Pulse Width									ns
t <sub>RCKP</sub>	RCLK Minimum Period									ns

## Sixteen RAM Blocks are Cascaded

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

Parameter	Description	'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Mode</b>										
$t_{WDSU}$	Write Data Setup vs. WCLK		15.03		17.34		19.65		23.12	ns
$t_{WDHD}$	Write Data Hold vs. WCLK		0		0.00		0.00		0.00	ns
$t_{WADSU}$	Write Address Setup vs. WCLK		15.03		17.34		19.65		23.12	ns
$t_{WADHD}$	Write Address Hold vs. WCLK		0		0.00		0.00		0.00	ns
$t_{WENSU}$	Write Enable Setup vs. WCLK		15.03		17.34		19.65		23.12	ns
$t_{WENHD}$	Write Enable Hold vs. WCLK		0		0.00		0.00		0.00	ns
$t_{WCKH}$	WCLK Minimum High Pulse Width									ns
$t_{WCLK}$	WCLK Minimum Low Pulse Width									ns
$t_{WCKP}$	WCLK Minimum Period									ns
<b>Non-Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		16.47		19.00		21.54		25.34	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		16.47		19.00		21.54		25.34	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		12.27		14.16		16.05		18.88	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns
<b>Pipelined Read Mode</b>										
$t_{RADSU}$	Read Address Setup vs. RCLK		16.47		19.00		21.54		25.34	ns
$t_{RADHD}$	Read Address Hold vs. RCLK		0		0.00		0.00		0.00	ns
$t_{RENSU}$	Read Enable Setup vs. RCLK		16.47		19.00		21.54		25.34	ns
$t_{RENHD}$	Read Enable Hold vs. RCLK		0		0.00		0.00		0.00	ns
$t_{RCO}$	RCLK-To-OUT		11.55		13.33		15.10		17.77	ns
$t_{RCLKH}$	RCLK Minimum High Pulse Width									ns
$t_{RCLKL}$	RCLK Minimum Low Pulse Width									ns
$t_{RCKP}$	RCLK Minimum Period									ns

## FIFO

Every memory block has its own FIFO controller. Each FIFO block has a read port and a write port. Both ports are configurable in various size from 4kx1 to 128x36, similar to the RAM block size. Each port is fully synchronous.

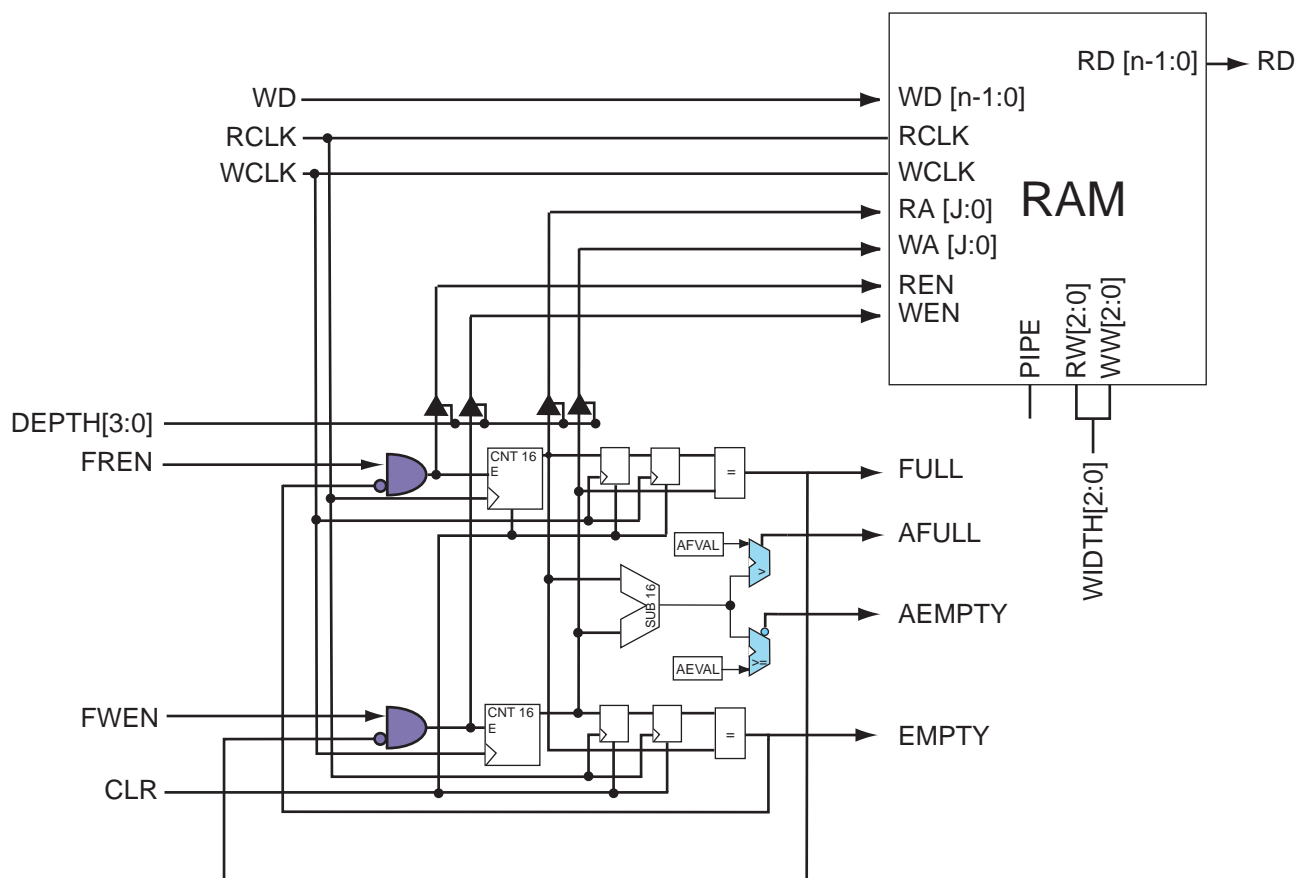
Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable almost empty (AEMPTY) and almost full (AFULL) flags as well as EMPTY and FULL flags ([Figure 47](#)):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.



**Figure 47** • Axcelerator RAM with Embedded FIFO Controller

## FIFO Flag Logic

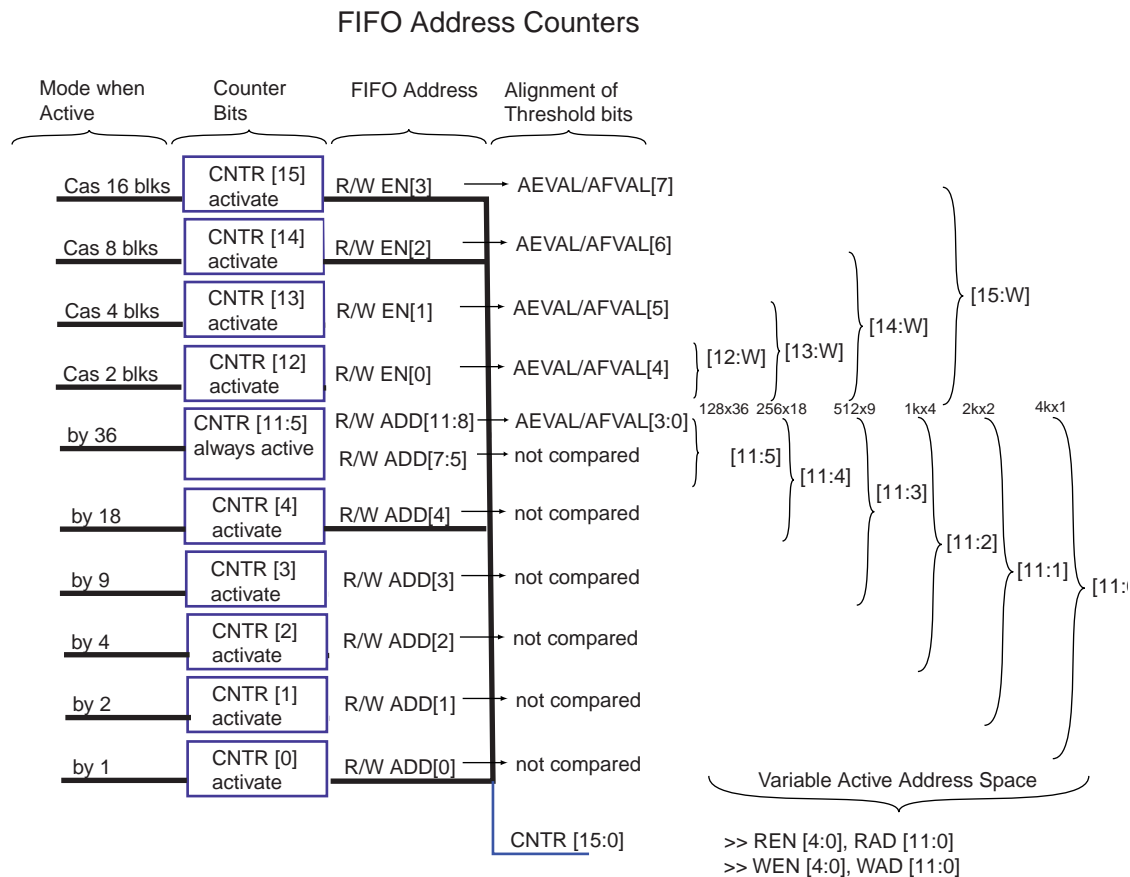
The FIFO is user configurable into various DEPTHS and WIDTHs. Figure 48 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, then bits 11 to 2

of the address will be used to specify locations within each RAM block, whereas bits 12 to 13 will be used to specify the RAM block.

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 20).



**Note:** Inactive counter bits are set to zero.

**Figure 48 • FIFO Address Counters**

**Table 20 • FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL bits	Inactive DIFF bits (set to 0)	DIFF comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] with AE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] with AE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] with AE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] with AE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] with AE/FVAL[7:0]



Figure 49 illustrates flag generation.

The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >= {AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000} >= DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 21).

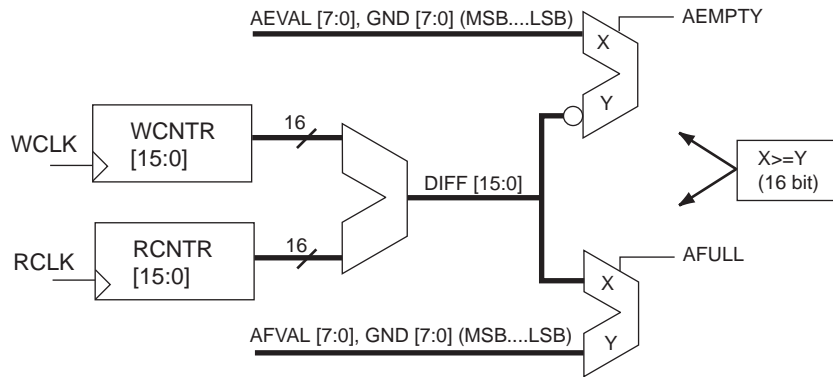


Figure 49 • ALMOST-EMPTY and ALMOST-FULL Logic

Table 21 • Number of Available Configuration Bits

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in the “Timing Characteristics” section on page 99.

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address RA, and the write address WA. The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 50). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 50).

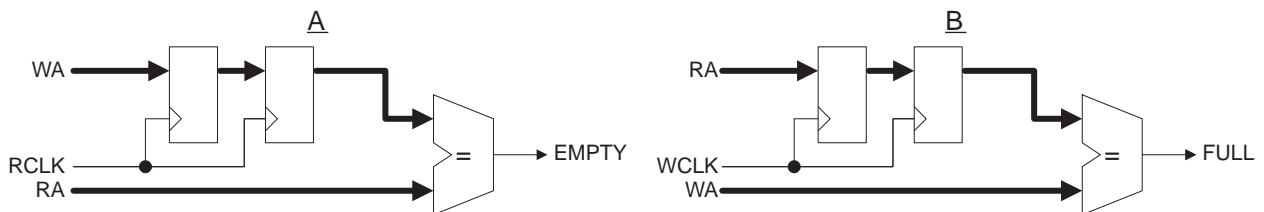


Figure 50 • Overflow and Underflow Control

## FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 22.

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 18 on page 87 describes the FIFO depth options for various data width and memory blocks. As with the RAM, when building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. Again, when using ACTgen, the user needs to only specify the depth and width of the RAM/FIFO blocks. ACTgen automatically configures these blocks to optimize performance.

## Interface

Figure 51 shows a logic block diagram of the Accelerator FIFO module.

## Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using ACTgen, the user only needs to specify the depth and width of the necessary FIFO blocks. ACTgen automatically configures these blocks to optimize performance.

## FIFO Signal Description

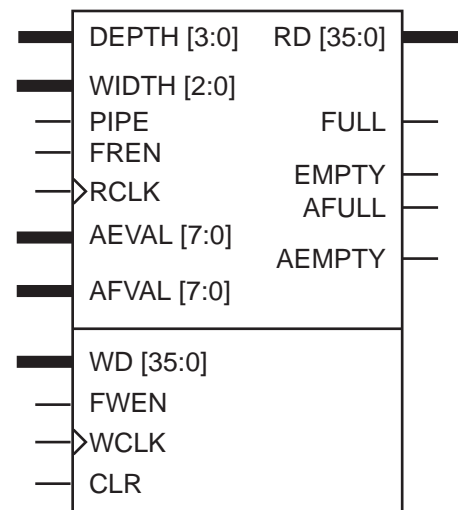
Signal	Direction	Description
WCLK	Input	Write clock (active either edge).
FWEN	Input	FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented.
WD[N-1:0]	Input	Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
FULL	Output	Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored.
AFULL	Output	Active high signal indicating that the FIFO is AFULL.
AFVAL	Input	8-bit input defining the AFULL value of the FIFO.
RCLK	Input	Read clock (active either edge).
FREN	Input	FIFO read enable.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
EMPTY	Output	Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored.
AEMPTY	Output	Active high signal indicating that the FIFO is AEMPTY.
AEVAL	Input	8-bit input defining the almost-empty value of the FIFO.
PIPE	Input	Sets the pipe option on or off.
CLR	Input	Active high clear input.
DEPTH	Input	Determines the depth of the FIFO and the number of FIFOs to be cascaded.
WIDTH	Input	Determines the width of the dataword / width of the FIFO, and the number of the FIFOs to be cascaded.

## Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection.

**Table 22 • FIFO Width Configurations**

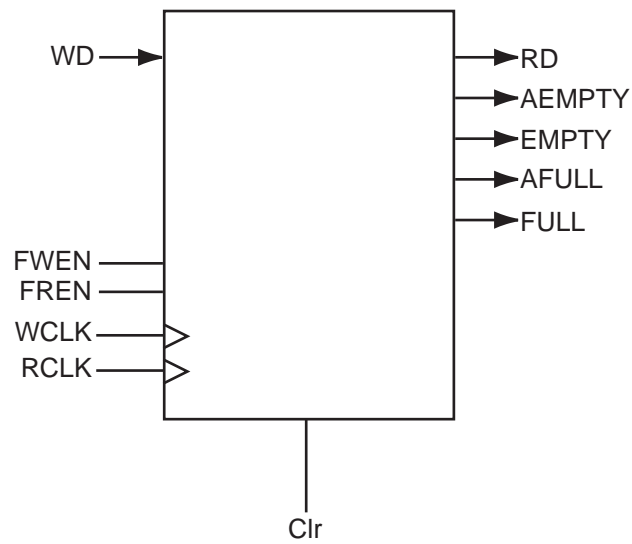
WIDTH(2:0)	WxD
000	1x4k
001	2x2k
010	4x1k
011	9x512
100	18x256
101	36x128
11x	reserved



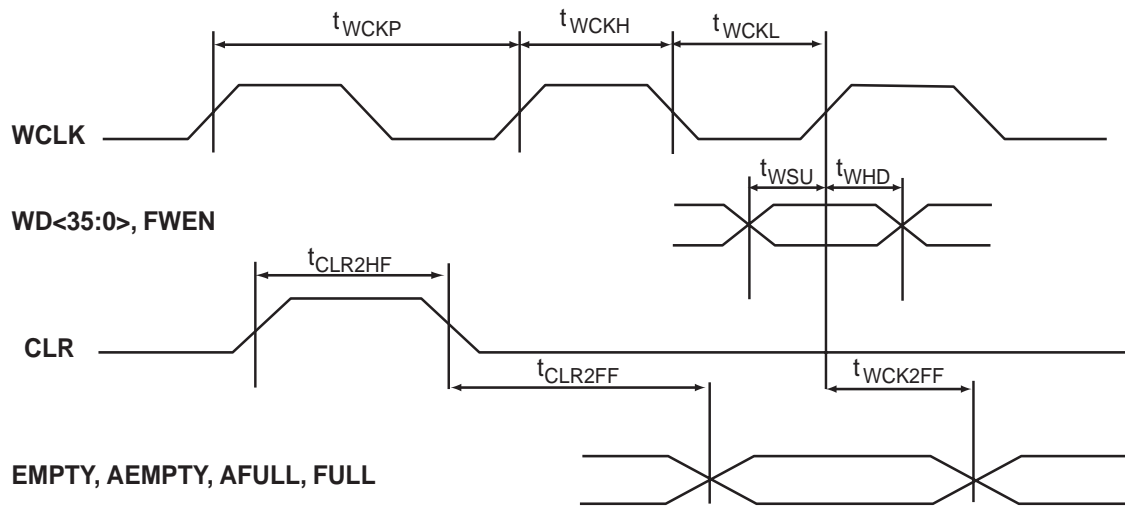
**Figure 51 • FIFO Block Diagram**

## Timing Characteristics

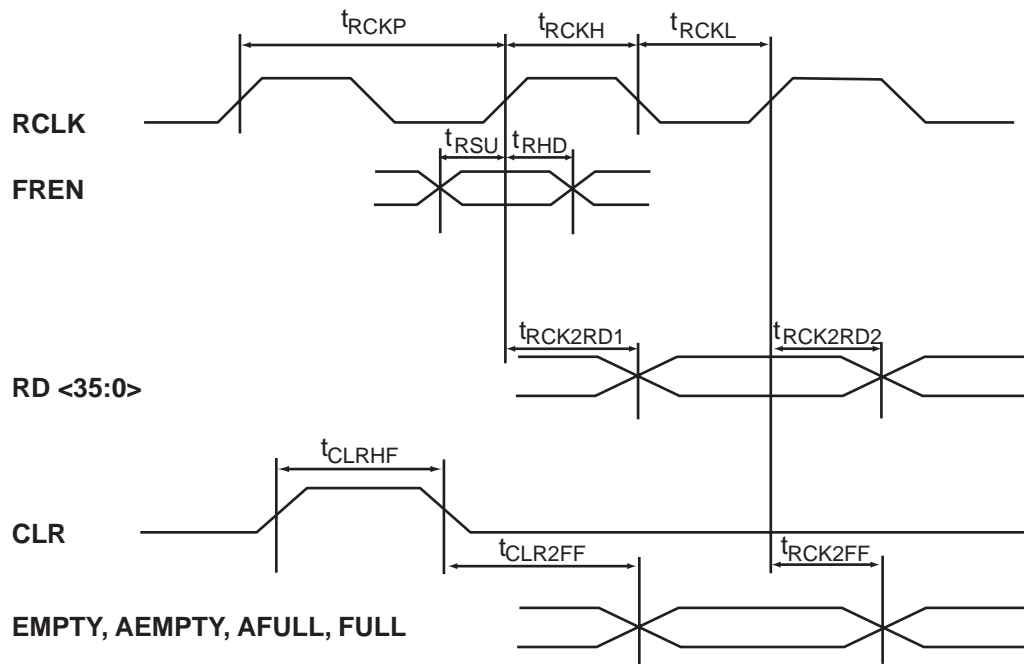
### FIFO Model



### FIFO Write Timing



## FIFO Read Timing



## One FIFO Block

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Non-pipelined)</b>										
t <sub>WSU</sub>	Write Setup									ns
t <sub>WHD</sub>	Write Hold									ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q									ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)									ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)									ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)									ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)									ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK $\uparrow$									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK $\uparrow$									ns
t <sub>RCK2RD2</sub>	Read Time									ns

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Pipelined)</b>										
t <sub>WSU</sub>	Write Setup	0.98	15.08	1.13	17.40	1.28	19.72	1.51	23.20	ns
t <sub>WHD</sub>	Write Hold		0.21		0.24		0.27		0.32	ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q	2.08	12.31	2.40	14.21	2.72	16.10	3.20	18.94	ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)		1.84		2.13		2.41		2.84	ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)		4.22		4.86		5.51		6.49	ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)		2.04		2.35		2.67		3.14	ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)		4.84		5.59		6.33		7.45	ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK $\uparrow$									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK $\uparrow$									ns
t <sub>RCK2RD2</sub>	Read Time									ns

## Two FIFO Blocks are Cascaded

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CC1} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Non-pipelined)</b>										
t <sub>WSU</sub>	Write Setup									ns
t <sub>WHD</sub>	Write Hold									ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q									ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)									ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)									ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)									ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)									ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK↑									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK↑									ns
t <sub>RCK2RD2</sub>	Read Time									ns

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CC1} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Pipelined)</b>										
t <sub>WSU</sub>	Write Setup	0.98	15.08	1.13	17.40	1.28	19.72	1.51	23.20	ns
t <sub>WHD</sub>	Write Hold		0.21		0.24		0.27		0.32	ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q	2.08	12.31	2.40	14.21	2.72	16.10	3.20	18.94	ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)		1.84		2.13		2.41		2.84	ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)		4.22		4.86		5.51		6.49	ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)		2.04		2.35		2.67		3.14	ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)		4.84		5.59		6.33		7.45	ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK↑									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK↑									ns
t <sub>RCK2RD2</sub>	Read Time									ns

## Four FIFO Blocks are Cascaded

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Non-pipelined)</b>										
t <sub>WSU</sub>	Write Setup									ns
t <sub>WHD</sub>	Write Hold									ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q									ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)									ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)									ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)									ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)									ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK <sup>↑</sup>									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK <sup>↑</sup>									ns
t <sub>RCK2RD2</sub>	Read Time									ns

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Pipelined)</b>										
t <sub>WSU</sub>	Write Setup	0.98	15.08	1.13	17.40	1.28	19.72	1.51	23.20	ns
t <sub>WHD</sub>	Write Hold		0.21		0.24		0.27		0.32	ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q	2.08	12.31	2.40	14.21	2.72	16.10	3.20	18.94	ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)		1.84		2.13		2.41		2.84	ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)		4.22		4.86		5.51		6.49	ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)		2.04		2.35		2.67		3.14	ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)		4.84		5.59		6.33		7.45	ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK <sup>↑</sup>									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK <sup>↑</sup>									ns
t <sub>RCK2RD2</sub>	Read Time									ns

## Eight FIFO Blocks are Cascaded

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CC1} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Non-pipelined)</b>										
$t_{WSU}$	Write Setup									ns
$t_{WHD}$	Write Hold									ns
$t_{WCKH}$	WCLK High									ns
$t_{WCKL}$	WCLK Low									ns
$t_{RSU}$	Read Setup									ns
$t_{RHD}$	Read Hold									ns
$t_{RCKH}$	RCLK High									ns
$t_{RCKL}$	RCLK Low									ns
$t_{RCK2RD1}$	Sequential Clock-to-Q									ns
$t_{CKP}$	Min CLK period									ns
$t_{CLRHF}$	Clear High									ns
$t_{CLR2FF}$	Clear-to-flag (EMPTY/FULL)									ns
$t_{CLR2FF}$	Clear-to-flag (AEMPTY/AFULL)									ns
$t_{CK2FF}$	Clock-to-flag (EMPTY/FULL)									ns
$t_{CK2PF}$	Clock-to-flag (AEMPTY/AFULL)									ns
$t_{ORDRCKH}$	Old Read data valid from RCLK $\uparrow$									ns
$t_{NRDRCKH}$	New Read data valid from RCLK $\uparrow$									ns
$t_{RCK2RD2}$	Read Time									ns

 Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CC1} = 3.0V$ ,  $T_J = 70^\circ C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Pipelined)</b>										
$t_{WSU}$	Write Setup	0.98	15.08	1.13	17.40	1.28	19.72	1.51	23.20	ns
$t_{WHD}$	Write Hold		0.21		0.24		0.27		0.32	ns
$t_{WCKH}$	WCLK High									ns
$t_{WCKL}$	WCLK Low									ns
$t_{RSU}$	Read Setup									ns
$t_{RHD}$	Read Hold									ns
$t_{RCKH}$	RCLK High									ns
$t_{RCKL}$	RCLK Low									ns
$t_{RCK2RD1}$	Sequential Clock-to-Q	2.08	12.31	2.40	14.21	2.72	16.10	3.20	18.94	ns
$t_{CKP}$	Min CLK period									ns
$t_{CLRHF}$	Clear High									ns
$t_{CLR2FF}$	Clear-to-flag (EMPTY/FULL)		1.84		2.13		2.41		2.84	ns
$t_{CLR2FF}$	Clear-to-flag (AEMPTY/AFULL)		4.22		4.86		5.51		6.49	ns
$t_{CK2FF}$	Clock-to-flag (EMPTY/FULL)		2.04		2.35		2.67		3.14	ns
$t_{CK2PF}$	Clock-to-flag (AEMPTY/AFULL)		4.84		5.59		6.33		7.45	ns
$t_{ORDRCKH}$	Old Read data valid from RCLK $\uparrow$									ns
$t_{NRDRCKH}$	New Read data valid from RCLK $\uparrow$									ns
$t_{RCK2RD2}$	Read Time									ns



## Sixteen FIFO Blocks are Cascaded

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Non-pipelined)</b>										
t <sub>WSU</sub>	Write Setup									ns
t <sub>WHD</sub>	Write Hold									ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q									ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)									ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)									ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)									ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)									ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK <sup>↑</sup>									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK <sup>↑</sup>									ns
t <sub>RCK2RD2</sub>	Read Time									ns

Worst-Case Commercial Conditions  $V_{CCA} = 1.425V$ ,  $V_{CCI} = 3.0V$ ,  $T_J = 70^{\circ}C$ 

		'-3' Speed		'-2' Speed		'-1' Speed		'Std' Speed		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
<b>FIFO Module Timing (Pipelined)</b>										
t <sub>WSU</sub>	Write Setup	0.98	15.08	1.13	17.40	1.28	19.72	1.51	23.20	ns
t <sub>WHD</sub>	Write Hold		0.21		0.24		0.27		0.32	ns
t <sub>WCKH</sub>	WCLK High									ns
t <sub>WCKL</sub>	WCLK Low									ns
t <sub>RSU</sub>	Read Setup									ns
t <sub>RHD</sub>	Read Hold									ns
t <sub>RCKH</sub>	RCLK High									ns
t <sub>RCKL</sub>	RCLK Low									ns
t <sub>RCK2RD1</sub>	Sequential Clock-to-Q	2.08	12.31	2.40	14.21	2.72	16.10	3.20	18.94	ns
t <sub>CKP</sub>	Min CLK period									ns
t <sub>CLRHF</sub>	Clear High									ns
t <sub>CLR2FF</sub>	Clear-to-flag (EMPTY/FULL)		1.84		2.13		2.41		2.84	ns
t <sub>CLR2FF</sub>	Clear-to-flag (AEMPTY/AFULL)		4.22		4.86		5.51		6.49	ns
t <sub>CK2FF</sub>	Clock-to-flag (EMPTY/FULL)		2.04		2.35		2.67		3.14	ns
t <sub>CK2PF</sub>	Clock-to-flag (AEMPTY/AFULL)		4.84		5.59		6.33		7.45	ns
t <sub>ORDRCKH</sub>	Old Read data valid from RCLK <sup>↑</sup>									ns
t <sub>NRDRCKH</sub>	New Read data valid from RCLK <sup>↑</sup>									ns
t <sub>RCK2RD2</sub>	Read Time									ns

## Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the ACTgen Macro Builder where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (please refer to Actel's *A Guide to ACTgen Macros* for more information)
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground

## Other Architectural Features

### Low Power Mode

The Axcelerator family devices can operate in a low power mode, in which all selected inputs and outputs with the Low Power feature enabled, will be tristated. The low power mode can be initiated by asserting the LP pin, which is grounded in normal operation. When leaving the low power mode, the logic states of all elements in the chip will be preserved.

To best reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "V<sub>PUMP</sub>" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V<sub>PUMP</sub> should be tied to GND. When the voltage level on V<sub>PUMP</sub> is set to 3.3V, the internal charge pump is turned off, and the V<sub>PUMP</sub> voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e. high drive, low output impedance, and good decoupling) should be used at V<sub>PUMP</sub>.

To allow running at very low frequency, some I/Os must be kept alive while disabling all the other inputs and tristating all outputs. Please note, if the I/O bank is not disabled, differential I/Os belonging to this I/O bank will still consume regular power, even when operating in the low power mode.

### JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the [Table 23](#).

**Table 23 • JTAG Instruction Code**

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload / Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
Reserved	All others
Bypass	11111

### Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS and TDI have on-chip pull-up resistors; while TRST has an optional on-chip pull-up resistor.

#### TRST

TRST (Test-Logic Reset) is an active-low asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1kΩ resistor.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a V<sub>CCA</sub> and/or V<sub>CCDA</sub> voltage drop.

#### TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift\_DR" state or "Shift\_IR" state. The least significant bit of the selected register (i.e. IR or DR) is clocked out to TDO first by the falling edge of TCK.

#### TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

#### Instruction Register (IR)

The IR has 5 bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data coming out of TDO during the "Shift-IR" will be "10111." If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO\_ERRORB," "PROBA\_ERRORB," and "PROBB\_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode Start-up Sequence, if the micro-probe has not been used, the "PROBA\_ERRORB" is used as a "Power-up done successfully" flag.

## Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follows:

### 1. IDCODE:

The IDCODE is a 32 bits hard coded JTAG Silicon Signature. It is a hard-wired device ID code, which contains the Actel identity, part number, and version number in a specific JTAG format.

### 2. USERCODE:

The USERCODE is a 32 bits programmable JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed.

### 3. Boundary-Scan Register (BSR):

Each I/O contains 3 Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.

### 4. Bypass Register (BYR):

This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

## Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

## Special Fuses

### Security

The Actel FuseLock advantage ensures that unauthorized users will not be able to read back the contents of an Actel antifuse FPGA. In addition to the inherent strengths of the architecture, special security fuses that prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making both invasive and more-subtle noninvasive attacks ineffective against Actel antifuse FPGAs.

Look for this symbol to ensure your valuable IP is secure.



For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

There are two fuses that are used to insure maximum security in Axcelerator devices:

- PFUS

The program fuse (PFUS) must be programmed. When programmed, the chip will be powered up in the user mode (following an internal circuit power up sequence: internal charge pump activated, I/Os enabled...etc.).

- SFUS

SFUS is a security fuse. When programmed, the Silicon Explorer II testing probes are disabled to inhibit chip diagnostic. Programming the security fuse will also disable SRAM initialization. All JTAG public instructions are still accessible by the user.

## Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe four nodes at a time without changing the placement and routing of the design and without using any additional resources. Highlighted nets in Silicon Explorer II can be accessed using Designer's Chip Edit in order to observe their real time values.

Silicon Explorer II's non-invasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

By eliminating multiple place-and-route program cycles the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that devices that have a single core tile, such as the AX125, only have two probe signals that can be observed). Each core tile can have up to two probe signals. To disallow probing, a security fuse in the silicon signature has to be

programmed (please see [Special Fuses](#) ).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a 9-Pin D-Sub connector ([Figure 11 on page 11](#)). Once the design has been placed and routed, and the Axcelerator device programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and another 14 channels are available to probe additional external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

## Programming

Device programming is supported through the Silicon Sculptor II, a single-site and multi-site device programmer for the PC. Silicon Sculptor II is a robust, compact device programmer. With stand-alone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. After being programmed, each fuse gets verified by Silicon Sculptor II to insure that its been programmed correctly. Furthermore, at the end of programming, there are integrity tests that are run to ensure no extra fuses were programmed. Not only does it test programmed and non-programmed fuses, Silicon Sculptor II also allows self-test to test its own hardware extensively.

Programming an Axcelerator device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

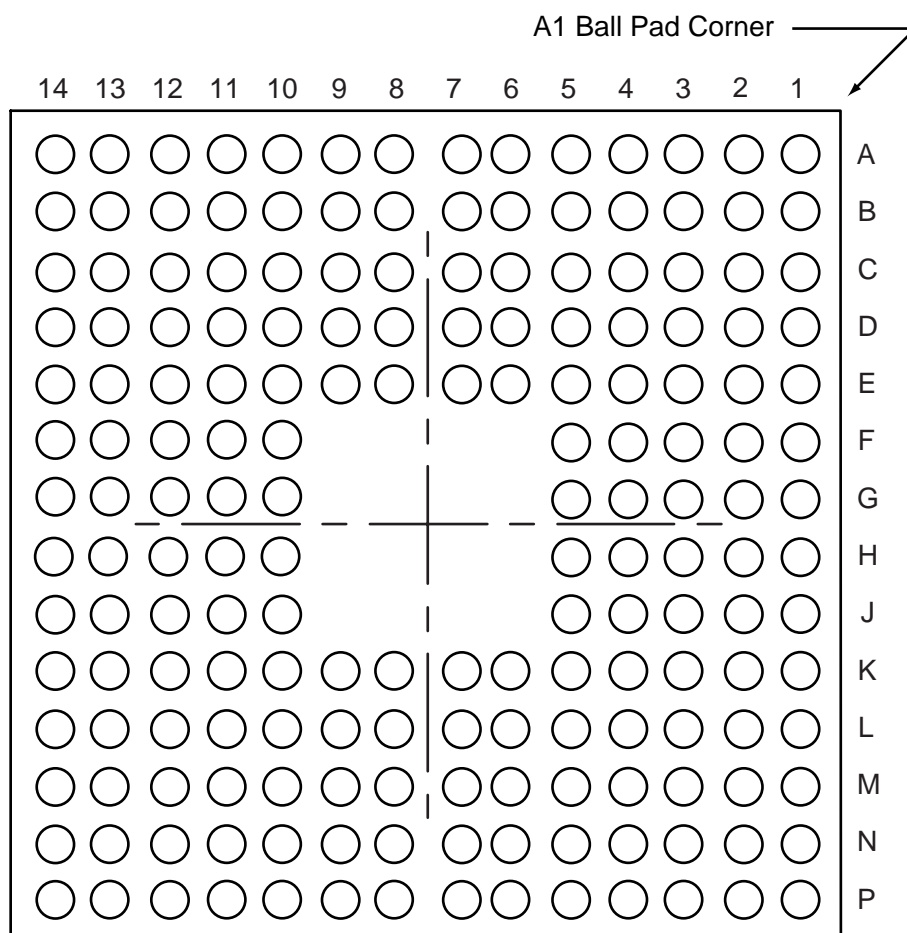
- Load the AFM file
- Select the device to be programmed
- Begin programming

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via In-House Programming from the factory.

For more details on programming the Axcelerator devices, please refer to the *Silicon Sculptor II User's Guide*.

# Package Pin Assignments

## 180-Pin CSP (Bottom View)



180-Pin CSP

AX125 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	B3
IO00PB0F0	A3
IO02NB0F0	B4
IO02PB0F0	A4
IO07NB0F0/HCLKAN	B5
IO07PB0F0/HCLKAP	A5
IO08NB0F0/HCLKBN	B7
IO08PB0F0/HCLKBP	B6
<b>Bank 1 - Block 1</b>	
IO09NB1F1/HCLKCN	C9
IO09PB1F1/HCLKCP	C8
IO10NB1F1/HCLKDN	A10
IO10PB1F1/HCLKDP	B10
IO11NB1F1	B11
IO11PB1F1	A11
IO15NB1F1	B12
IO15PB1F1	A12
IO17NB1F1	D12
IO17PB1F1	D11
<b>Bank 2 - Block 2</b>	
IO18NB2F2	C13
IO18PB2F2	C12
IO19NB2F2	C14
IO19PB2F2	B14
IO20NB2F2	D13
IO20PB2F2	D14
IO22NB2F2	F12
IO22PB2F2	E12
IO24NB2F2	E13
IO24PB2F2	E14
IO26NB2F2	F13
IO26PB2F2	F14
IO28NB2F2	G12
IO28PB2F2	G11
<b>Bank 3 - Block 3</b>	
IO30NB3F3	H13
IO30PB3F3	G13
IO32NB3F3	H11
IO32PB3F3	H12
IO34NB3F3	K14
IO34PB3F3	J14

180-Pin CSP

AX125 Function	Pin Number
IO36NB3F3	K13
IO36PB3F3	J13
IO38NB3F3	L13
IO38PB3F3	L14
IO40NB3F3	M13
IO40PB3F3	M14
IO41NB3F3	K12
IO41PB3F3	J12
<b>Bank 4 - Block 4</b>	
IO42NB4F4	P13
IO42PB4F4	N13
IO43NB4F4	L12
IO43PB4F4	M12
IO46NB4F4	P12
IO46PB4F4	N12
IO47NB4F4	N11
IO47PB4F4	P11
IO49NB4F4/CLKEN	M11
IO49PB4F4/CLKEP	M10
IO50NB4F4/CLKFN	N9
IO50PB4F4/CLKFP	P9
<b>Bank 5 - Block 5</b>	
IO51NB5F5/CLKGN	M7
IO51PB5F5/CLKGP	M8
IO52NB5F5/CLKHN	P5
IO52PB5F5/CLKHP	N5
IO53NB5F5	P4
IO53PB5F5	N4
IO55NB5F5	P3
IO55PB5F5	N3
IO56NB5F5	M4
IO56PB5F5	M5
IO57NB5F5	M2
IO57PB5F5	M3
IO59NB5F5	N2
IO59PB5F5	P2
<b>Bank 6 - Block 6</b>	
IO60NB6F6	M1
IO60PB6F6	N1
IO62NB6F6	K3
IO62PB6F6	L3
IO64NB6F6	L2

180-Pin CSP

AX125 Function	Pin Number
IO64PB6F6	L1
IO66NB6F6	K2
IO66PB6F6	K1
IO68NB6F6	H3
IO68PB6F6	J3
IO70NB6F6	G4
IO70PB6F6	H4
IO71NB6F6	J1
IO71PB6F6	J2
<b>Bank 7 - Block 7</b>	
IO72NB7F7	G2
IO72PB7F7	H2
IO74NB7F7	F3
IO74PB7F7	G3
IO76NB7F7	F1
IO76PB7F7	F2
IO78NB7F7	E1
IO78PB7F7	E2
IO79NB7F7	D2
IO79PB7F7	D1
IO83NB7F7	C1
IO83PB7F7	C2
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	B1
GND	A1
GND	A14
GND	A7
GND	A8
GND	E10
GND	E5
GND	E6
GND	E9
GND	F10
GND	F5
GND	G1
GND	G14
GND	H1
GND	H14
GND	J10
GND	J5
GND	K10
GND	K5

## 180-Pin CSP

AX125 Function	Pin Number
GND	K6
GND	K9
GND	N14
GND	P1
GND	P14
GND	P7
GND	P8
GND/LP	C3
PRA	D8
PRB	B8
PRC	N8
PRD	N7
TCK	C4
TDI	E3
TDO	C5
TMS	D4
TRST	B2
V <sub>CCA</sub>	E7
V <sub>CCA</sub>	G10
V <sub>CCA</sub>	H5
V <sub>CCA</sub>	K8
V <sub>CCPLA</sub>	C6
V <sub>CCPLB</sub>	C7
V <sub>CCPLC</sub>	A9
V <sub>CCPLD</sub>	C10
V <sub>CCPLE</sub>	N10
V <sub>CCPLF</sub>	L8
V <sub>CCPLG</sub>	P6
V <sub>CCPLH</sub>	M6
V <sub>CCDA</sub>	B13
V <sub>CCDA</sub>	D3
V <sub>CCDA</sub>	E8
V <sub>CCDA</sub>	G5
V <sub>CCDA</sub>	H10
V <sub>CCDA</sub>	K7
V <sub>CCDA</sub>	L11
V <sub>CCDA</sub>	L4
V <sub>CCIB0</sub>	D5
V <sub>CCIB0</sub>	D6
V <sub>CCIB1</sub>	D10
V <sub>CCIB1</sub>	D9
V <sub>CCIB2</sub>	E11

## 180-Pin CSP

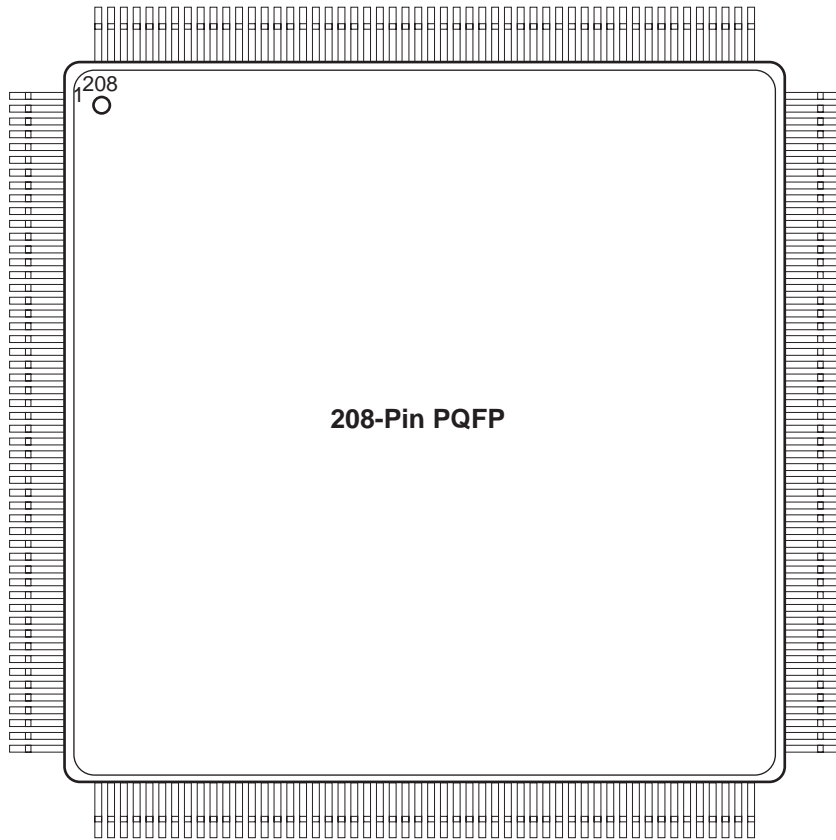
AX125 Function	Pin Number
V <sub>CCIB2</sub>	F11
V <sub>CCIB3</sub>	J11
V <sub>CCIB3</sub>	K11
V <sub>CCIB4</sub>	L10
V <sub>CCIB4</sub>	L9
V <sub>CCIB5</sub>	L5
V <sub>CCIB5</sub>	L6
V <sub>CCIB6</sub>	J4
V <sub>CCIB6</sub>	K4
V <sub>CCIB7</sub>	E4
V <sub>CCIB7</sub>	F4
V <sub>CCDA</sub>	A2
V <sub>COMPLA</sub>	A6
V <sub>COMPLB</sub>	D7
V <sub>COMPLC</sub>	B9
V <sub>COMPLD</sub>	C11
V <sub>COMPLE</sub>	P10
V <sub>COMPLF</sub>	M9
V <sub>COMPLG</sub>	N6
V <sub>COMPLH</sub>	L7
V <sub>PUMP</sub>	A13



## Package Pin Assignments (Continued)

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### 208-Pin PQFP



## 208-Pin PQFP

AX250 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
<b>Bank 1 - Block 1</b>	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
<b>Bank 2 - Block 2</b>	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
<b>Bank 3 - Block 3</b>	
IO45NB3F3	127

## 208-Pin PQFP

AX250 Function	Pin Number
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
<b>Bank 4 - Block 4</b>	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
<b>Bank 5 - Block 5</b>	
IO76NB5F5/CLKGN	76
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57

## 208-Pin PQFP

AX250 Function	Pin Number
IO89NB5F5	54
IO89PB5F5	55
<b>Bank 6 - Block 6</b>	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
<b>Bank 7 - Block 7</b>	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	1
V <sub>CCDA</sub>	26

208-Pin PQFP

AX250 Function	Pin Number
V <sub>CCDA</sub>	53
V <sub>CCDA</sub>	63
V <sub>CCDA</sub>	78
V <sub>CCDA</sub>	95
V <sub>CCDA</sub>	105
V <sub>CCDA</sub>	130
V <sub>CCDA</sub>	157
V <sub>CCDA</sub>	167
V <sub>CCDA</sub>	182
V <sub>CCDA</sub>	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79

208-Pin PQFP

AX250 Function	Pin Number
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
V <sub>CCA</sub>	2
V <sub>CCA</sub>	52
V <sub>CCA</sub>	156
V <sub>CCA</sub>	14
V <sub>CCA</sub>	38
V <sub>CCA</sub>	64
V <sub>CCA</sub>	93
V <sub>CCA</sub>	118
V <sub>CCA</sub>	142
V <sub>CCA</sub>	168
V <sub>CCA</sub>	195
V <sub>CCPLA</sub>	189
V <sub>CCPLB</sub>	187
V <sub>CCPLC</sub>	178
V <sub>CCPLD</sub>	176
V <sub>CCPLE</sub>	85
V <sub>CCPLF</sub>	83
V <sub>CCPLG</sub>	74
V <sub>CCPLH</sub>	72
V <sub>CCIB0</sub>	193
V <sub>CCIB0</sub>	200
V <sub>CCIB1</sub>	163
V <sub>CCIB1</sub>	172
V <sub>CCIB2</sub>	135
V <sub>CCIB2</sub>	149
V <sub>CCIB3</sub>	112
V <sub>CCIB3</sub>	124
V <sub>CCIB4</sub>	89
V <sub>CCIB4</sub>	98
V <sub>CCIB5</sub>	58
V <sub>CCIB5</sub>	68
V <sub>CCIB6</sub>	31
V <sub>CCIB6</sub>	45
V <sub>CCIB7</sub>	8
V <sub>CCIB7</sub>	20
V <sub>COMPLA</sub>	190
V <sub>COMPLB</sub>	188

208-Pin PQFP

AX250 Function	Pin Number
V <sub>COMPLC</sub>	179
V <sub>COMPLD</sub>	177
V <sub>COMPLE</sub>	86
V <sub>COMPLF</sub>	84
V <sub>COMPLG</sub>	75
V <sub>COMPLH</sub>	73
V <sub>PUMP</sub>	158

## 208-Pin PQFP

AX500 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
<b>Bank 0 - Block 1</b>	
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
<b>Bank 1 - Block 2</b>	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO24NB1F2	170
IO24PB1F2	171
<b>Bank 1 - Block 3</b>	
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
<b>Bank 2 - Block 4</b>	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
<b>Bank 2 - Block 5</b>	
IO57NB2F5	139
IO57PB3F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132
IO61PB2F5	134
IO62NB2F5	131

## 208-Pin PQFP

AX500 Function	Pin Number
IO62PB2F5	133
<b>Bank 3 - Block 6</b>	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
<b>Bank 3 - Block 7</b>	
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
<b>Bank 4 - Block 8</b>	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
<b>Bank 4 - Block 9</b>	
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
<b>Bank 5 - Block 10</b>	
IO105NB5F10/CLKGN	76
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67

## 208-Pin PQFP

AX500 Function	Pin Number
<b>Bank 5 - Block 11</b>	
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
<b>Bank 6 - Block 12</b>	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
<b>Bank 6 - Block 13</b>	
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
<b>Bank 7 - Block 14</b>	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
<b>Bank 7 - Block 15</b>	
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11

208-Pin PQFP

AX500 Function	Pin Number
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	1
V <sub>CCDA</sub>	2
V <sub>CCDA</sub>	26
V <sub>CCDA</sub>	52
V <sub>CCDA</sub>	53
V <sub>CCDA</sub>	63
V <sub>CCDA</sub>	78
V <sub>CCDA</sub>	95
V <sub>CCDA</sub>	105
V <sub>CCDA</sub>	130
V <sub>CCDA</sub>	156
V <sub>CCDA</sub>	157
V <sub>CCDA</sub>	167
V <sub>CCDA</sub>	182
V <sub>CCDA</sub>	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155

208-Pin PQFP

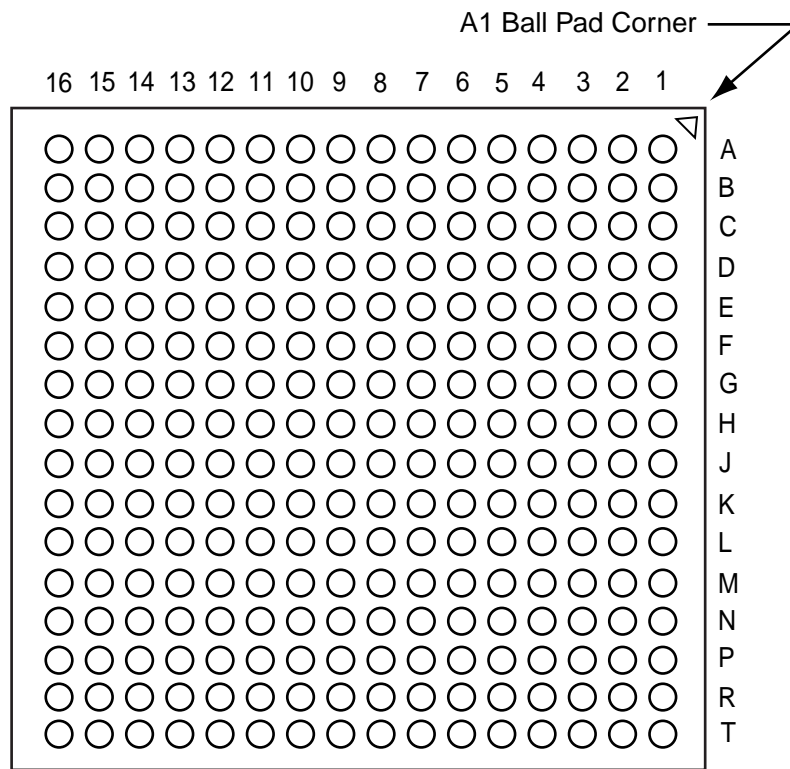
AX500 Function	Pin Number
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
V <sub>CCA</sub>	14
V <sub>CCA</sub>	38
V <sub>CCA</sub>	64
V <sub>CCA</sub>	93
V <sub>CCA</sub>	118
V <sub>CCA</sub>	142
V <sub>CCA</sub>	168
V <sub>CCA</sub>	195
V <sub>CCPLA</sub>	189
V <sub>CCPLB</sub>	187
V <sub>CCPLC</sub>	178
V <sub>CCPLD</sub>	176
V <sub>CCPLE</sub>	85
V <sub>CCPLF</sub>	83
V <sub>CCPLG</sub>	74
V <sub>CCPLH</sub>	72
V <sub>CCIB0</sub>	200
V <sub>CCIB0</sub>	193
V <sub>CCIB1</sub>	172
V <sub>CCIB1</sub>	163
V <sub>CCIB2</sub>	149
V <sub>CCIB2</sub>	135
V <sub>CCIB3</sub>	124
V <sub>CCIB3</sub>	112
V <sub>CCIB4</sub>	98
V <sub>CCIB4</sub>	89

208-Pin PQFP

AX500 Function	Pin Number
V <sub>CCIB5</sub>	68
V <sub>CCIB5</sub>	58
V <sub>CCIB6</sub>	45
V <sub>CCIB6</sub>	31
V <sub>CCIB7</sub>	20
V <sub>CCIB7</sub>	8
V <sub>COMPLA</sub>	190
V <sub>COMPLB</sub>	188
V <sub>COMPLC</sub>	179
V <sub>COMPLD</sub>	177
V <sub>COMPLE</sub>	86
V <sub>COMPLF</sub>	84
V <sub>COMPLG</sub>	75
V <sub>COMPLH</sub>	73
V <sub>PUMP</sub>	158

# Package Pin Assignments (Continued)

## 256-Pin FBGA (Bottom View)



## 256-Pin FBGA

AX125 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO04NB0F0	B6
IO04PB0F0	B5
IO06NB0F0	A6
IO06PB0F0	A5
IO07NB0F0/HCLKAN	B8
IO07PB0F0/HCLKAP	B7
IO08NB0F0/HCLKBN	A9
IO08PB0F0/HCLKBP	A8
<b>Bank 1 - Block 1</b>	
IO09NB1F1/HCLKCN	C10
IO09PB1F1/HCLKCP	C9
IO10NB1F1/HCLKDN	B11
IO10PB1F1/HCLKDP	B10
IO12NB1F1	A13
IO12PB1F1	A12
IO13NB1F1	B13
IO13PB1F1	B12
IO14NB1F1	C12
IO14PB1F1	C11
IO15NB1F1	A15
IO15PB1F1	B14
IO16NB1F1	C15
IO16PB1F1	C14
IO17NB1F1	D13
IO17PB1F1	D12
<b>Bank 2 - Block 2</b>	
IO18NB2F2	F13
IO18PB2F2	E13
IO19NB2F2	F14
IO19PB2F2	E14
IO20NB2F2	F15
IO20PB2F2	E15
IO21NB2F2	C16
IO21PB2F2	B16
IO22NB2F2	H13
IO22PB2F2	G13
IO23NB2F2	E16
IO23PB2F2	D16
IO25NB2F2	H15
IO25PB2F2	G15

## 256-Pin FBGA

AX125 Function	Pin Number
IO26NB2F2	H14
IO26PB2F2	G14
IO27NB2F2	G16
IO27PB2F2	F16
IO28NB2F2	K15
IO28PB2F2	K16
IO29NB2F2	J16
IO29PB2F2	H16
<b>Bank 3 - Block 3</b>	
IO30NB3F3	K13
IO30PB3F3	J13
IO31NB3F3	K14
IO31PB3F3	J14
IO33NB3F3	L15
IO33PB3F3	L16
IO35NB3F3	P16
IO35PB3F3	N16
IO36PB3F3	M16
IO37NB3F3	P15
IO37PB3F3	R16
IO39NB3F3	N15
IO39PB3F3	M15
IO40NB3F3	M13
IO40PB3F3	L13
IO41NB3F3	M14
IO41PB3F3	L14
<b>Bank 4 - Block 4</b>	
IO42NB4F4	N12
IO42PB4F4	N13
IO43NB4F4	T14
IO43PB4F4	R14
IO44PB4F4	T15
IO45NB4F4	R12
IO45PB4F4	R13
IO46NB4F4	P11
IO46PB4F4	P12
IO47PB4F4	T11
IO48NB4F4	T12
IO48PB4F4	T13
IO49NB4F4/CLKEN	R9
IO49PB4F4/CLKEP	R10
IO50NB4F4/CLKFN	T8
IO50PB4F4/CLKFP	T9
<b>Bank 5 - Block 5</b>	
IO51NB5F5/CLKGN	P7

## 256-Pin FBGA

AX125 Function	Pin Number
IO51PB5F5/CLKGP	P8
IO52NB5F5/CLKHN	R6
IO52PB5F5/CLKHP	R7
IO54NB5F5	T5
IO54PB5F5	T6
IO55NB5F5	P5
IO55PB5F5	P6
IO56NB5F5	T3
IO56PB5F5	T4
IO57NB5F5	R3
IO57PB5F5	R4
IO58NB5F5	R1
IO58PB5F5	T2
IO59NB5F5	N4
IO59PB5F5	N5
<b>Bank 6 - Block 6</b>	
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
<b>Bank 7 - Block 7</b>	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2

## 256-Pin FBGA

AX125 Function	Pin Number
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
<b>Dedicated I/O</b>	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15

## 256-Pin FBGA

AX125 Function	Pin Number
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6
VCCA	L10
VCCA	L7
VCCA	L8
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A2

## 256-Pin FBGA

AX125 Function	Pin Number
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14



## 256-Pin FBGA

AX250 Function	Pin Number
<b>Bank 0 -Block 0</b>	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO05NB0F0	B6
IO05PB0F0	B5
IO07NB0F0	A6
IO07PB0F0	A5
IO12NB0F0/HCLKAN	B8
IO12PB0F0/HCLKAP	B7
IO13NB0F0/HCLKBN	A9
IO13PB0F0/HCLKBP	A8
<b>Bank 1 -Block 1</b>	
IO14NB1F1/HCLKCN	C10
IO14PB1F1/HCLKCP	C9
IO15NB1F1/HCLKDN	B11
IO15PB1F1/HCLKDP	B10
IO17NB1F1	A13
IO17PB1F1	A12
IO19NB1F1	B13
IO19PB1F1	B12
IO21NB1F1	C12
IO21PB1F1	C11
IO23NB1F1	A15
IO23PB1F1	B14
IO26NB1F1	C15
IO26PB1F1	C14
IO27NB1F1	D13
IO27PB1F1	D12
<b>Bank 2 - Block 2</b>	
IO29NB2F2	F13
IO29PB2F2	E13
IO30NB2F2	F14
IO30PB2F2	E14
IO32NB2F2	C16
IO32PB2F2	B16
IO33NB2F2	F15
IO33PB2F2	E15
IO35NB2F2	H13
IO35PB2F2	G13
IO36NB2F2	E16
IO36PB2F2	D16
IO38NB2F2	H15
IO38PB2F2	G15

## 256-Pin FBGA

AX250 Function	Pin Number
IO39NB2F2	H14
IO39PB2F2	G14
IO40NB2F2	G16
IO40PB2F2	F16
IO43NB2F2	K15
IO43PB2F2	K16
IO44NB2F2	J16
IO44PB2F2	H16
<b>Bank 3 - Block 3</b>	
IO45NB3F3	K13
IO45PB3F3	J13
IO46NB3F3	K14
IO46PB3F3	J14
IO52NB3F3	L15
IO52PB3F3	L16
IO54NB3F3	P16
IO54PB3F3	N16
IO55PB3F3	M16
IO56NB3F3	P15
IO56PB3F3	R16
IO58NB3F3	N15
IO58PB3F3	M15
IO59NB3F3	M13
IO59PB3F3	L13
IO61NB3F3	M14
IO61PB3F3	L14
<b>Bank 4 - Block 4</b>	
IO62NB4F4	N12
IO62PB4F4	N13
IO63NB4F4	T14
IO63PB4F4	R14
IO66PB4F4	T15
IO67NB4F4	R12
IO67PB4F4	R13
IO69NB4F4	P11
IO69PB4F4	P12
IO70PB4F4	T11
IO73NB4F4	T12
IO73PB4F4	T13
IO74NB4F4/CLKEN	R9
IO74PB4F4/CLKEP	R10
IO75NB4F4/CLKFN	T8
IO75PB4F4/CLKFP	T9
<b>Bank 5 - Block 5</b>	
IO76NB5F5/CLKGN	P7

## 256-Pin FBGA

AX250 Function	Pin Number
IO76PB5F5/CLKGP	P8
IO77NB5F5/CLKHN	R6
IO77PB5F5/CLKHP	R7
IO79NB5F5	T5
IO79PB5F5	T6
IO81NB5F5	P5
IO81PB5F5	P6
IO83NB5F5	T3
IO83PB5F5	T4
IO85NB5F5	R3
IO85PB5F5	R4
IO88NB5F5	R1
IO88PB5F5	T2
IO89NB5F5	N4
IO89PB5F5	N5
<b>Bank 6 - Block 6</b>	
IO91NB6F6	L4
IO91PB6F6	M4
IO92NB6F6	L3
IO92PB6F6	M3
IO94NB6F6	P2
IO94PB6F6	N2
IO97NB6F6	J4
IO97PB6F6	K4
IO98NB6F6	N1
IO98PB6F6	P1
IO100NB6F6	L2
IO100PB6F6	M2
IO102NB6F6	L1
IO102PB6F6	M1
IO103NB6F6	J3
IO103PB6F6	K3
IO104NB6F6	J2
IO104PB6F6	K2
<b>Bank 7 - Block 7</b>	
IO107NB7F7	J1
IO107PB7F7	K1
IO108NB7F7	G2
IO108PB7F7	H2
IO111NB7F7	G3
IO111PB7F7	H3
IO112NB7F7	E1
IO112PB7F7	F1
IO113NB7F7	G1
IO114NB7F7	E2

## 256-Pin FBGA

AX250 Function	Pin Number
IO114PB7F7	F2
IO115NB7F7	G4
IO115PB7F7	H4
IO116NB7F7	C1
IO116PB7F7	D1
IO117NB7F7	C2
IO117PB7F7	B1
IO118NB7F7	D2
IO118PB7F7	D3
IO119NB7F7	E3
IO119PB7F7	F3
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15

## 256-Pin FBGA

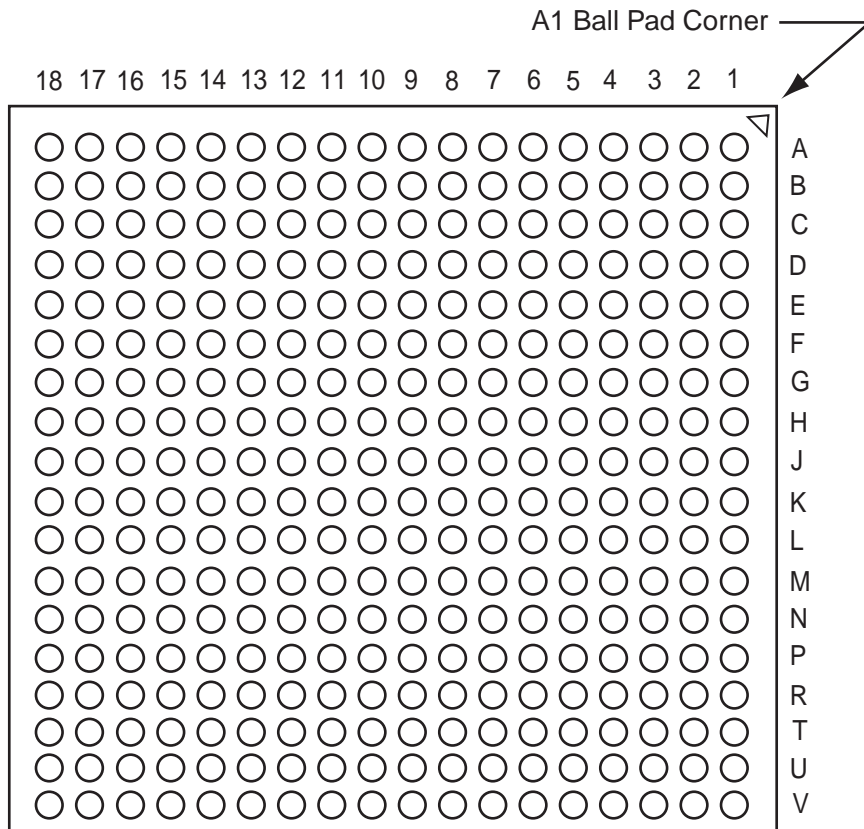
AX250 Function	Pin Number
GND	R2
GND	T1
GND	T16
GND/LP	D4
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4
TMS	C3
TRST	C5
V <sub>CCA</sub>	D14
V <sub>CCA</sub>	F10
V <sub>CCA</sub>	F4
V <sub>CCA</sub>	F7
V <sub>CCA</sub>	F8
V <sub>CCA</sub>	F9
V <sub>CCA</sub>	G11
V <sub>CCA</sub>	G6
V <sub>CCA</sub>	H11
V <sub>CCA</sub>	H6
V <sub>CCA</sub>	J11
V <sub>CCA</sub>	J6
V <sub>CCA</sub>	K11
V <sub>CCA</sub>	K6
V <sub>CCA</sub>	L10
V <sub>CCA</sub>	L7
V <sub>CCA</sub>	L8
V <sub>CCA</sub>	L9
V <sub>CCA</sub>	N3
V <sub>CCA</sub>	P14
V <sub>CCPLA</sub>	C7
V <sub>CCPLB</sub>	D6
V <sub>CCPLC</sub>	A10
V <sub>CCPLD</sub>	D10
V <sub>CCPLE</sub>	P10
V <sub>CCPLF</sub>	N11
V <sub>CCPLG</sub>	T7
V <sub>CCPLH</sub>	N7
V <sub>CCDA</sub>	A11
V <sub>CCDA</sub>	A2
V <sub>CCDA</sub>	C13
V <sub>CCDA</sub>	D9

## 256-Pin FBGA

AX250 Function	Pin Number
V <sub>CCDA</sub>	H1
V <sub>CCDA</sub>	J15
V <sub>CCDA</sub>	N14
V <sub>CCDA</sub>	N8
V <sub>CCDA</sub>	P4
V <sub>CCDA</sub>	R11
V <sub>CCDA</sub>	R5
V <sub>CCIB0</sub>	E6
V <sub>CCIB0</sub>	E7
V <sub>CCIB0</sub>	E8
V <sub>CCIB1</sub>	E10
V <sub>CCIB1</sub>	E11
V <sub>CCIB1</sub>	E9
V <sub>CCIB2</sub>	F12
V <sub>CCIB2</sub>	G12
V <sub>CCIB2</sub>	H12
V <sub>CCIB3</sub>	J12
V <sub>CCIB3</sub>	K12
V <sub>CCIB3</sub>	L12
V <sub>CCIB4</sub>	M10
V <sub>CCIB4</sub>	M11
V <sub>CCIB4</sub>	M9
V <sub>CCIB5</sub>	M6
V <sub>CCIB5</sub>	M7
V <sub>CCIB5</sub>	M8
V <sub>CCIB6</sub>	J5
V <sub>CCIB6</sub>	K5
V <sub>CCIB6</sub>	L5
V <sub>CCIB7</sub>	F5
V <sub>CCIB7</sub>	G5
V <sub>CCIB7</sub>	H5
V <sub>COMPLA</sub>	A7
V <sub>COMPLB</sub>	D7
V <sub>COMPLC</sub>	B9
V <sub>COMPLD</sub>	D11
V <sub>COMPLE</sub>	T10
V <sub>COMPLF</sub>	N10
V <sub>COMPLG</sub>	R8
V <sub>COMPLH</sub>	N6
V <sub>PUMP</sub>	A14

# Package Pin Assignments (Continued)

## 324-Pin FBGA



324-Pin FBGA

AX125 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	C5
IO00PB0F0	C4
IO01NB0F0	A3
IO01PB0F0	A2
IO02NB0F0	C7
IO02PB0F0	C6
IO03NB0F0	B5
IO03PB0F0	B4
IO04NB0F0	A5
IO04PB0F0	A4
IO05NB0F0	A7
IO05PB0F0	A6
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0/HCLKAN	C9
IO07PB0F0/HCLKAP	C8
IO08NB0F0/HCLKBN	B10
IO08PB0F0/HCLKBP	B9
<b>Bank 1 - Block 1</b>	
IO09NB1F1/HCLKCN	D11
IO09PB1F1/HCLKCP	D10
IO10NB1F1/HCLKDN	C12
IO10PB1F1/HCLKDP	C11
IO11NB1F1	A15
IO11PB1F1	A14
IO12NB1F1	B14
IO12PB1F1	B13
IO13NB1F1	A17
IO13PB1F1	A16
IO14NB1F1	D13
IO14PB1F1	D12
IO15NB1F1	C14
IO15PB1F1	C13
IO16NB1F1	B16
IO16PB1F1	C15
IO17NB1F1	E14
IO17PB1F1	E13
<b>Bank 2 - Block 2</b>	
IO18NB2F2	G14
IO18PB2F2	F14
IO19NB2F2	D16

324-Pin FBGA

AX125 Function	Pin Number
IO19PB2F2	D15
IO20NB2F2	C18
IO20PB2F2	B18
IO21NB2F2	D17
IO21PB2F2	C17
IO22NB2F2	F17
IO22PB2F2	E17
IO23NB2F2	G16
IO23PB2F2	F16
IO24NB2F2	E18
IO24PB2F2	D18
IO25NB2F2	G18
IO25PB2F2	F18
IO26NB2F2	H17
IO26PB2F2	G17
IO27NB2F2	J16
IO27PB2F2	H16
IO28NB2F2	J18
IO28PB2F2	H18
IO29NB2F2	K17
IO29PB2F2	J17
<b>Bank 3 - Block 3</b>	
IO30NB3F3	N18
IO30PB3F3	M18
IO31NB3F3	L18
IO31PB3F3	K18
IO32NB3F3	L16
IO32PB3F3	L17
IO33NB3F3	R18
IO33PB3F3	P18
IO34NB3F3	N15
IO34PB3F3	M15
IO35NB3F3	M16
IO35PB3F3	M17
IO36NB3F3	P16
IO36PB3F3	N16
IO37NB3F3	R17
IO37PB3F3	P17
IO38NB3F3	N14
IO38PB3F3	M14
IO39NB3F3	U18
IO39PB3F3	T18

324-Pin FBGA

AX125 Function	Pin Number
IO40NB3F3	R16
IO40PB3F3	T17
IO41NB3F3	P13
IO41PB3F3	P14
<b>Bank 4 - Block 4</b>	
IO42NB4F4	T13
IO42PB4F4	T14
IO43NB4F4	U15
IO43PB4F4	T15
IO44NB4F4	U13
IO44PB4F4	U14
IO45NB4F4	V15
IO45PB4F4	V16
IO46NB4F4	V13
IO46PB4F4	V14
IO47NB4F4	V12
IO47PB4F4	U12
IO48NB4F4	V10
IO48PB4F4	V11
IO49NB4F4/CLKEN	T10
IO49PB4F4/CLKEP	T11
IO50NB4F4/CLKFN	U9
IO50PB4F4/CLKFP	U10
<b>Bank 5 - Block 5</b>	
IO51NB5F5/CLKGN	R8
IO51PB5F5/CLKGP	R9
IO52NB5F5/CLKHN	T7
IO52PB5F5/CLKHP	T8
IO53NB5F5	U6
IO53PB5F5	U7
IO54NB5F5	V8
IO54PB5F5	V9
IO55NB5F5	V6
IO55PB5F5	V7
IO56NB5F5	U4
IO56PB5F5	U5
IO57NB5F5	T4
IO57PB5F5	T5
IO58NB5F5	V4
IO58PB5F5	V5
IO59NB5F5	V2
IO59PB5F5	V3

324-Pin FBGA

AX125 Function	Pin Number
<b>Bank 6 - Block 6</b>	
IO60NB6F6	P5
IO60PB6F6	P6
IO61NB6F6	T2
IO61PB6F6	U3
IO62NB6F6	T1
IO62PB6F6	U1
IO63NB6F6	P1
IO63PB6F6	R1
IO64NB6F6	R3
IO64PB6F6	P3
IO65NB6F6	P2
IO65PB6F6	R2
IO66NB6F6	M3
IO66PB6F6	N3
IO67NB6F6	M2
IO67PB6F6	N2
IO68NB6F6	M1
IO68PB6F6	N1
IO69NB6F6	K4
IO69PB6F6	L4
IO70NB6F6	K1
IO70PB6F6	L1
IO71NB6F6	K3
IO71PB6F6	L3
<b>Bank 7 - Block 7</b>	
IO72NB7F7	H4
IO72PB7F7	J4
IO73NB7F7	K2
IO73PB7F7	L2
IO74NB7F7	H2
IO74PB7F7	H1
IO75NB7F7	H3
IO75PB7F7	J3
IO76NB7F7	F2
IO76PB7F7	G2
IO77NB7F7	F1
IO77PB7F7	G1
IO78NB7F7	D2
IO78PB7F7	E2
IO79NB7F7	F3
IO79PB7F7	G3

324-Pin FBGA

AX125 Function	Pin Number
IO80NB7F7	E3
IO80PB7F7	E4
IO81NB7F7	D1
IO81PB7F7	E1
IO82NB7F7	D3
IO82PB7F7	C2
IO83NB7F7	B1
IO83PB7F7	C1
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	F5
GND	A1
GND	A18
GND	B17
GND	B2
GND	C16
GND	C3
GND	E16
GND	F13
GND	F6
GND	G12
GND	G7
GND	H10
GND	H11
GND	H8
GND	H9
GND	J10
GND	J11
GND	J8
GND	J9
GND	K10
GND	K11
GND	K8
GND	K9
GND	L10
GND	L11
GND	L8
GND	L9
GND	M12
GND	M7
GND	N13
GND	N6
GND	R14

324-Pin FBGA

AX125 Function	Pin Number
GND	R4
GND	T16
GND	T3
GND	U17
GND	U2
GND	V1
GND	V18
GND/LP	E5
NC	A10
NC	A11
NC	A12
NC	A13
NC	A8
NC	A9
NC	B12
NC	F15
NC	F4
NC	G15
NC	G4
NC	H14
NC	H15
NC	H5
NC	J1
NC	J14
NC	J15
NC	J5
NC	K14
NC	K15
NC	K5
NC	L14
NC	L15
NC	L5
NC	M4
NC	M5
NC	N17
NC	N4
NC	N5
NC	R12
NC	R13
NC	R6
NC	R7
NC	T12

## 324-Pin FBGA

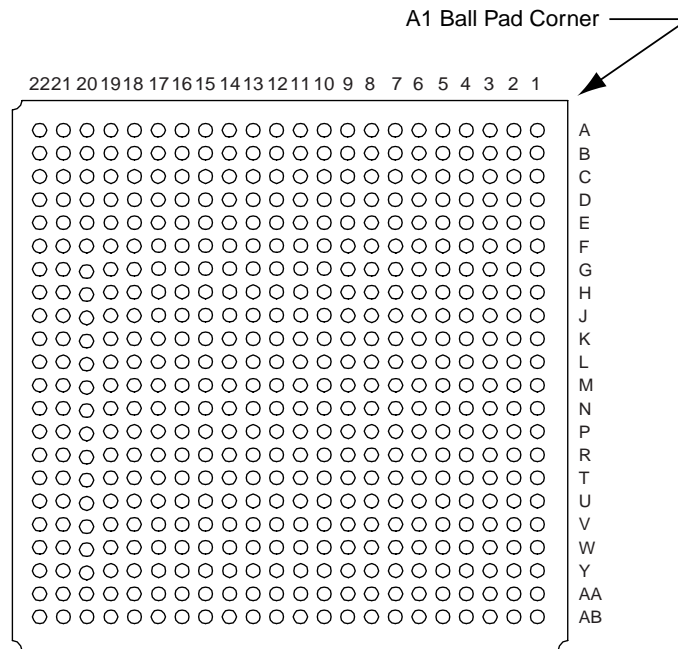
AX125 Function	Pin Number
NC	T6
NC	U16
NC	V17
PRA	E9
PRB	D9
PRC	P10
PRD	R10
TCK	E6
TDI	D7
TDO	D5
TMS	D4
TRST	D6
V <sub>CCA</sub>	E15
V <sub>CCA</sub>	G10
V <sub>CCA</sub>	G11
V <sub>CCA</sub>	G5
V <sub>CCA</sub>	G8
V <sub>CCA</sub>	G9
V <sub>CCA</sub>	H12
V <sub>CCA</sub>	H7
V <sub>CCA</sub>	J12
V <sub>CCA</sub>	J7
V <sub>CCA</sub>	K12
V <sub>CCA</sub>	K7
V <sub>CCA</sub>	L12
V <sub>CCA</sub>	L7
V <sub>CCA</sub>	M10
V <sub>CCA</sub>	M11
V <sub>CCA</sub>	M8
V <sub>CCA</sub>	M9
V <sub>CCA</sub>	P4
V <sub>CCA</sub>	R15
V <sub>CCCPLA</sub>	D8
V <sub>CCCPLB</sub>	E7
V <sub>CCCPLC</sub>	B11
V <sub>CCCPLD</sub>	E11
V <sub>CCCPL E</sub>	R11
V <sub>CCCPLF</sub>	P12
V <sub>CCCPLG</sub>	U8
V <sub>CCCPLH</sub>	P8
V <sub>CCDA</sub>	B3
V <sub>CCDA</sub>	D14

## 324-Pin FBGA

AX125 Function	Pin Number
V <sub>CCDA</sub>	E10
V <sub>CCDA</sub>	J2
V <sub>CCDA</sub>	K16
V <sub>CCDA</sub>	P15
V <sub>CCDA</sub>	P9
V <sub>CCDA</sub>	R5
V <sub>CCIB0</sub>	F7
V <sub>CCIB0</sub>	F8
V <sub>CCIB0</sub>	F9
V <sub>CCIB1</sub>	F10
V <sub>CCIB1</sub>	F11
V <sub>CCIB1</sub>	F12
V <sub>CCIB2</sub>	G13
V <sub>CCIB2</sub>	H13
V <sub>CCIB2</sub>	J13
V <sub>CCIB3</sub>	K13
V <sub>CCIB3</sub>	L13
V <sub>CCIB3</sub>	M13
V <sub>CCIB4</sub>	N10
V <sub>CCIB4</sub>	N11
V <sub>CCIB4</sub>	N12
V <sub>CCIB5</sub>	N7
V <sub>CCIB5</sub>	N8
V <sub>CCIB5</sub>	N9
V <sub>CCIB6</sub>	K6
V <sub>CCIB6</sub>	L6
V <sub>CCIB6</sub>	M6
V <sub>CCIB7</sub>	G6
V <sub>CCIB7</sub>	H6
V <sub>CCIB7</sub>	J6
V <sub>COMPLA</sub>	B8
V <sub>COMPLB</sub>	E8
V <sub>COMPLC</sub>	C10
V <sub>COMPLD</sub>	E12
V <sub>COMPLE</sub>	U11
V <sub>COMPLF</sub>	P11
V <sub>COMPLG</sub>	T9
V <sub>COMPLH</sub>	P7
V <sub>PUMP</sub>	B15

# Package Pin Assignments (Continued)

## 484-Pin FBGA (Bottom View)



## 484-Pin FBGA

AX500 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	E3
IO00PB0F0	D3
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	D7
IO03PB0F0	D6
IO04NB0F0	B5
IO04PB0F0	B4
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	A5
IO06PB0F0	A4
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	B7
IO08PB0F0	B6
IO10NB0F0	B9
IO10PB0F0	B8
IO11NB0F0	E9
IO11PB0F0	E8
<b>Bank 0 - Block 1</b>	
IO12NB0F1	D9
IO12PB0F1	D8
IO13NB0F1	C9
IO13PB0F1	C8
IO14NB0F1	A9
IO14PB0F1	A8
IO15NB0F1	B10
IO15PB0F1	A10
IO16NB0F1	B12
IO16PB0F1	B11
IO18NB0F1	C13
IO18PB0F1	C12
IO19NB0F1/HCLKAN	E11
IO19PB0F1/HCLKAP	E10
IO20NB0F1/HCLKBN	D12
IO20PB0F1/HCLKBP	D11
<b>Bank 1 - Block 2</b>	
IO21NB1F2/HCLKCN	F13

## 484-Pin FBGA

AX500 Function	Pin Number
IO21PB1F2/HCLKCP	F12
IO22NB1F2/HCLKDN	E14
IO22PB1F2/HCLKDP	E13
IO24NB1F2	A14
IO24PB1F2	A13
IO25NB1F2	B14
IO25PB1F2	B13
IO26NB1F2	C15
IO27NB1F2	A16
IO27PB1F2	A15
IO28NB1F2	B16
IO28PB1F2	B15
IO29NB1F2	D16
IO29PB1F2	D15
IO30NB1F2	A18
IO30PB1F2	A17
IO31NB1F2	F15
IO31PB1F2	F14
<b>Bank 1 - Block 3</b>	
IO32NB1F3	C17
IO32PB1F3	C16
IO33NB1F3	E16
IO33PB1F3	E15
IO34NB1F3	B18
IO34PB1F3	B17
IO35NB1F3	B19
IO35PB1F3	A19
IO36NB1F3	C19
IO36PB1F3	C18
IO37NB1F3	F18
IO37PB1F3	F17
IO38NB1F3	D18
IO38PB1F3	E17
IO39NB1F3	E21
IO39PB1F3	D21
IO40NB1F3	E20
IO40PB1F3	D20
IO41NB1F3	G16
IO41PB1F3	G15
<b>Bank 2 - Block 4</b>	
IO42NB2F4	F19
IO42PB2F4	E19

## 484-Pin FBGA

AX500 Function	Pin Number
IO43NB2F4	J16
IO43PB2F4	H16
IO44NB2F4	E22
IO44PB2F4	D22
IO45NB2F4	H19
IO45PB2F4	G19
IO46NB2F4	G22
IO46PB2F4	F22
IO47NB2F4	J17
IO47PB2F4	H17
IO48NB2F4	G20
IO48PB2F4	F20
IO49NB2F4	J18
IO49PB2F4	H18
IO50NB2F4	G21
IO50PB2F4	F21
IO51NB2F4	K19
IO51PB2F4	J19
<b>Bank 2 - Block 5</b>	
IO52NB2F5	J21
IO52PB2F5	H21
IO53NB2F5	J20
IO53PB2F5	H20
IO54NB2F5	J22
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
<b>Bank 3 - Block 6</b>	
IO63NB3F6	N16
IO63PB3F6	M16



## 484-Pin FBGA

AX500 Function	Pin Number
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20
IO72PB3F6	P20
IO73PB3F6	R19
<b>Bank 3 - Block 7</b>	
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
<b>Bank 4 - Block 8</b>	
IO84NB4F8	AB18

## 484-Pin FBGA

AX500 Function	Pin Number
IO84PB4F8	AB19
IO85NB4F8	T15
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
<b>Bank 4 - Block 9</b>	
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
<b>Bank 5 - Block 10</b>	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11

## 484-Pin FBGA

AX500 Function	Pin Number
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
<b>Bank 5 - Block 11</b>	
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
<b>Bank 6 - Block 12</b>	
IO126NB6F12	V2
IO126PB6F12	W2
IO127NB6F12	P7

## 484-Pin FBGA

AX500 Function	Pin Number
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
<b>Bank 6 - Block 13</b>	
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7
IO146NB6F13	M3
IO146PB6F13	N3
<b>Bank 7 - Block 14</b>	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1

## 484-Pin FBGA

AX500 Function	Pin Number
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
<b>Bank 7 - Block 15</b>	
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	H7
GND	A1

## 484-Pin FBGA

AX500 Function	Pin Number
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10

484-Pin FBGA

AX500 Function	Pin Number
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
V <sub>CCA</sub>	G17
V <sub>CCA</sub>	J10
V <sub>CCA</sub>	J11
V <sub>CCA</sub>	J12
V <sub>CCA</sub>	J13
V <sub>CCA</sub>	J7
V <sub>CCA</sub>	K14

484-Pin FBGA

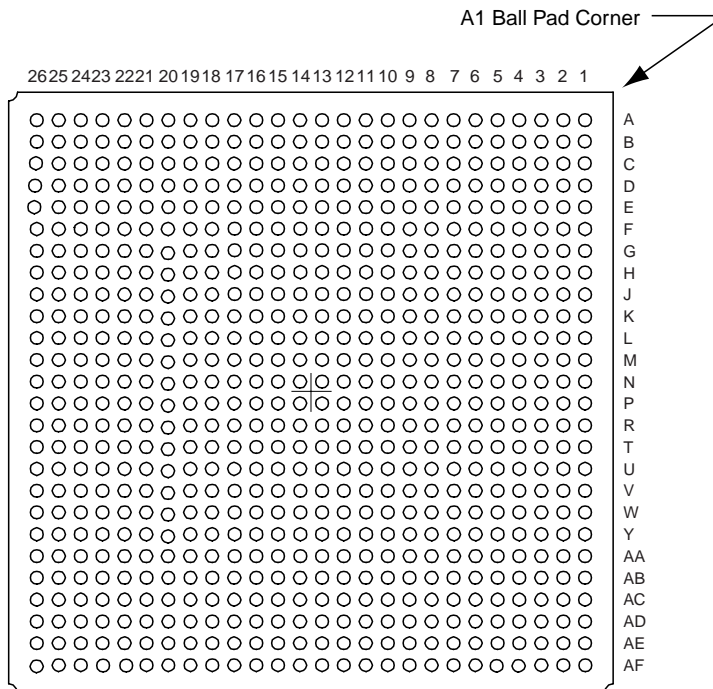
AX500 Function	Pin Number
V <sub>CCA</sub>	K9
V <sub>CCA</sub>	L14
V <sub>CCA</sub>	L9
V <sub>CCA</sub>	M14
V <sub>CCA</sub>	M9
V <sub>CCA</sub>	N14
V <sub>CCA</sub>	N9
V <sub>CCA</sub>	P10
V <sub>CCA</sub>	P11
V <sub>CCA</sub>	P12
V <sub>CCA</sub>	P13
V <sub>CCA</sub>	T6
V <sub>CCA</sub>	U17
V <sub>CCPLA</sub>	F10
V <sub>CCPLB</sub>	G9
V <sub>CCPLC</sub>	D13
V <sub>CCPLD</sub>	G13
V <sub>CCPLE</sub>	U13
V <sub>CCPLF</sub>	T14
V <sub>CCPLG</sub>	W10
V <sub>CCPLH</sub>	T10
V <sub>CCDA</sub>	D14
V <sub>CCDA</sub>	D5
V <sub>CCDA</sub>	F16
V <sub>CCDA</sub>	G12
V <sub>CCDA</sub>	L4
V <sub>CCDA</sub>	M18
V <sub>CCDA</sub>	T11
V <sub>CCDA</sub>	T17
V <sub>CCDA</sub>	U7
V <sub>CCDA</sub>	V14
V <sub>CCDA</sub>	V8
V <sub>CCIB0</sub>	A3
V <sub>CCIB0</sub>	B3
V <sub>CCIB0</sub>	H10
V <sub>CCIB0</sub>	H11
V <sub>CCIB0</sub>	H9
V <sub>CCIB1</sub>	A20
V <sub>CCIB1</sub>	B20
V <sub>CCIB1</sub>	H12
V <sub>CCIB1</sub>	H13
V <sub>CCIB1</sub>	H14

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AX500 Function	Pin Number
V <sub>CCIB2</sub>	C21
V <sub>CCIB2</sub>	C22
V <sub>CCIB2</sub>	J15
V <sub>CCIB2</sub>	K15
V <sub>CCIB2</sub>	L15
V <sub>CCIB3</sub>	M15
V <sub>CCIB3</sub>	N15
V <sub>CCIB3</sub>	P15
V <sub>CCIB3</sub>	Y21
V <sub>CCIB3</sub>	Y22
V <sub>CCIB4</sub>	AA20
V <sub>CCIB4</sub>	AB20
V <sub>CCIB4</sub>	R12
V <sub>CCIB4</sub>	R13
V <sub>CCIB4</sub>	R14
V <sub>CCIB5</sub>	AA3
V <sub>CCIB5</sub>	AB3
V <sub>CCIB5</sub>	R10
V <sub>CCIB5</sub>	R11
V <sub>CCIB5</sub>	R9
V <sub>CCIB6</sub>	M8
V <sub>CCIB6</sub>	N8
V <sub>CCIB6</sub>	P8
V <sub>CCIB6</sub>	Y1
V <sub>CCIB6</sub>	Y2
V <sub>CCIB7</sub>	C1
V <sub>CCIB7</sub>	C2
V <sub>CCIB7</sub>	J8
V <sub>CCIB7</sub>	K8
V <sub>CCIB7</sub>	L8
V <sub>COMPLA</sub>	D10
V <sub>COMPLB</sub>	G10
V <sub>COMPLC</sub>	E12
V <sub>COMPLD</sub>	G14
V <sub>COMPLE</sub>	W13
V <sub>COMPLF</sub>	T13
V <sub>COMPLG</sub>	V11
V <sub>COMPLH</sub>	T9
V <sub>PUMP</sub>	D17

# Package Pin Assignments (Continued)

## 676-Pin FBGA (Bottom View)



## 676-Pin FBGA

AX500 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
<b>Bank 0 - Block 1</b>	
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12

## 676-Pin FBGA

AX500 Function	Pin Number
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
<b>Bank 1 - Block 2</b>	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
<b>Bank 1 - Block 3</b>	
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20

## 676-Pin FBGA

AX500 Function	Pin Number
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
<b>Bank 2 - Block 4</b>	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25
IO51NB2F4	L20
IO51PB2F4	L21
<b>Bank 2 - Block 5</b>	
IO52NB2F5	K26
IO52PB2F5	J26
IO53NB2F5	L23
IO53PB2F5	L22
IO54NB2F5	L24
IO54PB2F5	K24
IO55NB2F5	M20
IO55PB2F5	M21
IO56NB2F5	L26
IO56PB2F5	L25
IO57NB2F5	M23
IO57PB2F5	M22
IO58NB2F5	M26
IO58PB2F5	M25
IO59NB2F5	N22
IO59PB2F5	N23

## 676-Pin FBGA

AX500 Function	Pin Number
IO60NB2F5	N24
IO60PB2F5	M24
IO61NB2F5	N20
IO61PB2F5	N21
IO62NB2F5	P25
IO62PB2F5	N25
<b>Bank 3 - Block 6</b>	
IO63NB3F6	T26
IO63PB3F6	R26
IO64NB3F6	R24
IO64PB3F6	P24
IO65NB3F6	P20
IO65PB3F6	P21
IO66NB3F6	T25
IO66PB3F6	R25
IO67NB3F6	T23
IO67PB3F6	R23
IO68NB3F6	V26
IO68PB3F6	U26
IO69NB3F6	V25
IO69PB3F6	U25
IO70NB3F6	Y25
IO70PB3F6	W25
IO71NB3F6	W24
IO71PB3F6	V24
IO72NB3F6	V23
IO72PB3F6	U23
IO73NB3F6	T21
IO73PB3F6	T20
<b>Bank 3 - Block 7</b>	
IO74NB3F7	AA26
IO74PB3F7	Y26
IO75NB3F7	AA24
IO75PB3F7	Y24
IO76NB3F7	Y23
IO76PB3F7	W23
IO77NB3F7	V21
IO77PB3F7	U21
IO78NB3F7	AB25
IO78PB3F7	AA25
IO79NB3F7	AC26
IO79PB3F7	AB26

## 676-Pin FBGA

AX500 Function	Pin Number
IO80NB3F7	AC24
IO80PB3F7	AB24
IO81NB3F7	AB23
IO81PB3F7	AA23
IO82NB3F7	AA22
IO82PB3F7	Y22
IO83NB3F7	AE26
IO83PB3F7	AD26
<b>Bank 4 - Block 8</b>	
IO84NB4F8	AB21
IO84PB4F8	AA21
IO85NB4F8	AE23
IO85PB4F8	AE24
IO86NB4F8	AC21
IO86PB4F8	AC22
IO87NB4F8	AF22
IO87PB4F8	AF23
IO88NB4F8	AD22
IO88PB4F8	AD23
IO89NB4F8	AC19
IO89PB4F8	AC20
IO90NB4F8	AE21
IO90PB4F8	AE22
IO91NB4F8	AA17
IO91PB4F8	AA18
IO92NB4F8	AD20
IO92PB4F8	AD21
IO93NB4F8	AF20
IO93PB4F8	AF21
<b>Bank 4 - Block 9</b>	
IO94NB4F9	AE19
IO94PB4F9	AE20
IO95NB4F9	AC17
IO95PB4F9	AC18
IO96NB4F9	AD18
IO96PB4F9	AD19
IO97NB4F9	AA16
IO97PB4F9	Y16
IO98NB4F9	AE17
IO98PB4F9	AE18
IO99NB4F9	AC16
IO99PB4F9	AB16

## 676-Pin FBGA

AX500 Function	Pin Number
IO100NB4F9	AF17
IO100PB4F9	AF18
IO101NB4F9	AA15
IO101PB4F9	Y15
IO102NB4F9	AC15
IO102PB4F9	AB15
IO103NB4F9/CLKEN	AE16
IO103PB4F9/CLKEP	AF16
IO104NB4F9/CLKFN	AE14
IO104PB4F9/CLKFP	AE15
<b>Bank 5 - Block 10</b>	
IO105NB5F10/CLKGN	AE12
IO105PB5F10/CLKGP	AE13
IO106NB5F10/CLKHN	AE11
IO106PB5F10/CLKHP	AF11
IO107NB5F10	Y12
IO107PB5F10	AA13
IO108NB5F10	AC12
IO108PB5F10	AB12
IO109NB5F10	AC10
IO109PB5F10	AC11
IO110NB5F10	AF9
IO110PB5F10	AF10
IO111NB5F10	Y11
IO111PB5F10	AA12
IO112NB5F10	AE9
IO112PB5F10	AE10
IO113NB5F10	AC9
IO113PB5F10	AD9
<b>Bank 5 - Block 11</b>	
IO114NB5F11	AF6
IO114PB5F11	AF7
IO115NB5F11	AA10
IO115PB5F11	AB10
IO116NB5F11	AE7
IO116PB5F11	AE8
IO117NB5F11	AD7
IO117PB5F11	AD8
IO118NB5F11	AC7
IO118PB5F11	AC8
IO119NB5F11	AD6
IO119PB5F11	AE6

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AX500 Function	Pin Number
IO120NB5F11	AE5
IO120PB5F11	AF5
IO121NB5F11	AF4
IO121PB5F11	AE4
IO122NB5F11	AC5
IO122PB5F11	AC6
IO123NB5F11	AD4
IO123PB5F11	AD5
IO124NB5F11	AB6
IO124PB5F11	AB7
IO125NB5F11	AE3
IO125PB5F11	AF3
<b>Bank 6 - Block 12</b>	
IO126NB6F12	AB3
IO126PB6F12	AC3
IO127NB6F12	AA2
IO127PB6F12	AB2
IO128NB6F12	AC2
IO128PB6F12	AD2
IO129NB6F12	Y1
IO129PB6F12	AA1
IO130NB6F12	Y3
IO130PB6F12	AA3
IO131NB6F12	U6
IO131PB6F12	V6
IO132NB6F12	W2
IO132PB6F12	Y2
IO133NB6F12	V4
IO133PB6F12	W4
IO134NB6F12	V3
IO134PB6F12	W3
IO135NB6F12	V1
IO135PB6F12	V2
<b>Bank 6 - Block 13</b>	
IO136NB6F13	U4
IO136PB6F13	U5
IO137NB6F13	T6
IO137PB6F13	T7
IO138NB6F13	T5
IO138PB6F13	T4
IO139NB6F13	R6
IO139PB6F13	R7

676-Pin FBGA

AX500 Function	Pin Number
IO140NB6F13	T3
IO140PB6F13	U3
IO141NB6F13	U1
IO141PB6F13	U2
IO142NB6F13	R2
IO142PB6F13	T2
IO143NB6F13	P3
IO143PB6F13	R3
IO144NB6F13	P5
IO144PB6F13	P4
IO145NB6F13	P6
IO145PB6F13	P7
IO146NB6F13	R1
IO146PB6F13	T1
<b>Bank 7 - Block 14</b>	
IO147NB7F14	N6
IO147PB7F14	N7
IO148NB7F14	N5
IO148PB7F14	N4
IO149NB7F14	N2
IO149PB7F14	N3
IO150NB7F14	L1
IO150PB7F14	M1
IO151NB7F14	M2
IO151PB7F14	M3
IO152NB7F14	M5
IO152PB7F14	M4
IO153NB7F14	M7
IO153PB7F14	M6
IO154NB7F14	K2
IO154PB7F14	L2
IO155NB7F14	K3
IO155PB7F14	L3
IO156NB7F14	L5
IO156PB7F14	L4
IO157NB7F14	L6
IO157PB7F14	L7
<b>Bank 7 - Block 15</b>	
IO158NB7F15	J1
IO158PB7F15	K1
IO159NB7F15	J4
IO159PB7F15	K4

676-Pin FBGA

AX500 Function	Pin Number
IO160NB7F15	H2
IO160PB7F15	J2
IO161NB7F15	K6
IO161PB7F15	K5
IO162NB7F15	H3
IO162PB7F15	J3
IO163NB7F15	G2
IO163PB7F15	G1
IO164NB7F15	G4
IO164PB7F15	H4
IO165NB7F15	F3
IO165PB7F15	G3
IO166NB7F15	E2
IO166PB7F15	F2
IO167NB7F15	F5
IO167PB7F15	G5
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	B1
GND	A1
NC	A11
GND	A13
GND	A14
GND	A19
NC	A21
NC	A22
NC	A24
NC	A25
GND	A26
GND	A8
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18

## 676-Pin FBGA

AX500 Function	Pin Number
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
GND	AC23
NC	AC25
GND	AC4
NC	AD1
NC	AD11
NC	AD16
GND	AD24
NC	AD25
GND	AD3
NC	AE1
NC	AE2
NC	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF2
GND	AF25
GND	AF26
GND	AF8
NC	B11
GND	B2
NC	B24
GND	B25
GND	B26
NC	B4
NC	C16
GND	C24
GND	C3
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18

## 676-Pin FBGA

AX500 Function	Pin Number
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
GND	G20
NC	G21
NC	G22
GND	G7
GND	H1
GND	H19
NC	H21
NC	H22
NC	H23
GND	H26
NC	H5
NC	H6
GND	H8
GND	J18
NC	J5
NC	J6
GND	J9
GND	K10
GND	K11
GND	K12

## 676-Pin FBGA

AX500 Function	Pin Number
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
NC	P22
GND	P26



676-Pin FBGA

AX500 Function	Pin Number
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
NC	R20
NC	R21
NC	R22
NC	R4
NC	R5
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
NC	T22
NC	T24
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
NC	U22
NC	U24
GND	V18
NC	V22
NC	V5
GND	V9
GND	W1
GND	W19
NC	W21
NC	W22
GND	W26

676-Pin FBGA

AX500 Function	Pin Number
NC	W5
NC	W6
GND	W8
GND	Y20
NC	Y21
NC	Y4
NC	Y5
NC	Y6
GND	Y7
GND/LP	C2
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
V <sub>CCA</sub>	J10
V <sub>CCA</sub>	J11
V <sub>CCA</sub>	J12
V <sub>CCA</sub>	J13
V <sub>CCA</sub>	J14
V <sub>CCA</sub>	J15
V <sub>CCA</sub>	J16
V <sub>CCA</sub>	J17
V <sub>CCA</sub>	K18
V <sub>CCA</sub>	K9
V <sub>CCA</sub>	L18
V <sub>CCA</sub>	L9
V <sub>CCA</sub>	M18
V <sub>CCA</sub>	M9
V <sub>CCA</sub>	N18
V <sub>CCA</sub>	N9
V <sub>CCA</sub>	P18
V <sub>CCA</sub>	P9
V <sub>CCA</sub>	R18
V <sub>CCA</sub>	R9
V <sub>CCA</sub>	T18
V <sub>CCA</sub>	T9
V <sub>CCA</sub>	U18

676-Pin FBGA

AX500 Function	Pin Number
V <sub>CCA</sub>	U9
V <sub>CCA</sub>	V10
V <sub>CCA</sub>	V11
V <sub>CCA</sub>	V12
V <sub>CCA</sub>	V13
V <sub>CCA</sub>	V14
V <sub>CCA</sub>	V15
V <sub>CCA</sub>	V16
V <sub>CCA</sub>	V17
V <sub>CCPLA</sub>	E12
V <sub>CCPLB</sub>	F13
V <sub>CCPLC</sub>	E15
V <sub>CCPLD</sub>	G14
V <sub>CCPLE</sub>	AF15
V <sub>CCPLF</sub>	AA14
V <sub>CCPLG</sub>	AF12
V <sub>CCPLH</sub>	AB13
V <sub>CCDA</sub>	AB22
V <sub>CCDA</sub>	AB4
V <sub>CCDA</sub>	AB5
V <sub>CCDA</sub>	AD10
V <sub>CCDA</sub>	AD13
V <sub>CCDA</sub>	AF24
V <sub>CCDA</sub>	C1
V <sub>CCDA</sub>	C26
V <sub>CCDA</sub>	D24
V <sub>CCDA</sub>	E14
V <sub>CCDA</sub>	P2
V <sub>CCDA</sub>	P23
V <sub>CCIB0</sub>	G10
V <sub>CCIB0</sub>	G8
V <sub>CCIB0</sub>	G9
V <sub>CCIB0</sub>	H10
V <sub>CCIB0</sub>	H11
V <sub>CCIB0</sub>	H12
V <sub>CCIB0</sub>	H13
V <sub>CCIB0</sub>	H9
V <sub>CCIB1</sub>	G17
V <sub>CCIB1</sub>	G18
V <sub>CCIB1</sub>	G19
V <sub>CCIB1</sub>	H14
V <sub>CCIB1</sub>	H15

## 676-Pin FBGA

AX500 Function	Pin Number
V <sub>CCI</sub> B1	H16
V <sub>CCI</sub> B1	H17
V <sub>CCI</sub> B1	H18
V <sub>CCI</sub> B2	H20
V <sub>CCI</sub> B2	J19
V <sub>CCI</sub> B2	J20
V <sub>CCI</sub> B2	K19
V <sub>CCI</sub> B2	K20
V <sub>CCI</sub> B2	L19
V <sub>CCI</sub> B2	M19
V <sub>CCI</sub> B2	N19
V <sub>CCI</sub> B3	P19
V <sub>CCI</sub> B3	R19
V <sub>CCI</sub> B3	T19
V <sub>CCI</sub> B3	U19
V <sub>CCI</sub> B3	U20
V <sub>CCI</sub> B3	V19
V <sub>CCI</sub> B3	V20
V <sub>CCI</sub> B3	W20
V <sub>CCI</sub> B4	W14
V <sub>CCI</sub> B4	W15
V <sub>CCI</sub> B4	W16
V <sub>CCI</sub> B4	W17
V <sub>CCI</sub> B4	W18
V <sub>CCI</sub> B4	Y17
V <sub>CCI</sub> B4	Y18
V <sub>CCI</sub> B4	Y19
V <sub>CCI</sub> B5	W10
V <sub>CCI</sub> B5	W11
V <sub>CCI</sub> B5	W12
V <sub>CCI</sub> B5	W13
V <sub>CCI</sub> B5	W9
V <sub>CCI</sub> B5	Y10
V <sub>CCI</sub> B5	Y8
V <sub>CCI</sub> B5	Y9
V <sub>CCI</sub> B6	P8
V <sub>CCI</sub> B6	R8
V <sub>CCI</sub> B6	T8
V <sub>CCI</sub> B6	U7
V <sub>CCI</sub> B6	U8
V <sub>CCI</sub> B6	V7
V <sub>CCI</sub> B6	V8

## 676-Pin FBGA

AX500 Function	Pin Number
V <sub>CCI</sub> B6	W7
V <sub>CCI</sub> B7	H7
V <sub>CCI</sub> B7	J7
V <sub>CCI</sub> B7	J8
V <sub>CCI</sub> B7	K7
V <sub>CCI</sub> B7	K8
V <sub>CCI</sub> B7	L8
V <sub>CCI</sub> B7	M8
V <sub>CCI</sub> B7	N8
V <sub>CCDA</sub>	A3
V <sub>COMPLA</sub>	D12
V <sub>COMPLB</sub>	G13
V <sub>COMPLC</sub>	D15
V <sub>COMPLD</sub>	F14
V <sub>CCDA</sub>	AD15
V <sub>COMPLE</sub>	AD17
V <sub>COMPLF</sub>	AB14
V <sub>COMPLG</sub>	AD12
V <sub>COMPLH</sub>	Y13
V <sub>CCDA</sub>	B17
V <sub>PUMP</sub>	E22

## 676-Pin FBGA

AX1000 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
<b>Bank 0 - Block 1</b>	
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10
IO21PB0F1	C10
<b>Bank 0 - Block 2</b>	
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11

## 676-Pin FBGA

AX1000 Function	Pin Number
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
<b>Bank 1 - Block 3</b>	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
<b>Bank 1 - Block 4</b>	
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20

## 676-Pin FBGA

AX1000 Function	Pin Number
IO52PB1F4	C20
<b>Bank 1 - Block 5</b>	
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
<b>Bank 2 - Block 6</b>	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26
IO73PB2F6	D26
<b>Bank 2 - Block 7</b>	

## 676-Pin FBGA

AX1000 Function	Pin Number
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
<b>Bank 2 - Block 8</b>	
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
<b>Bank 3 - Block 9</b>	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24

## 676-Pin FBGA

AX1000 Function	Pin Number
IO100NB3F9	R22
IO100PB3F9	P22
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
<b>Bank 3 - Block 10</b>	
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
<b>Bank 3 - Block 11</b>	
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24

## 676-Pin FBGA

AX1000 Function	Pin Number
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
<b>Bank 4 - Block 12</b>	
IO129NB4F12	AB21
IO129PB4F12	AA21
IO131NB4F12	AD22
IO131PB4F12	AD23
IO132NB4F12	AE23
IO132PB4F12	AE24
IO133NB4F12	AB20
IO133PB4F12	AA20
IO134NB4F12	AC21
IO134PB4F12	AC22
IO135NB4F12	AF22
IO135PB4F12	AF23
IO137NB4F12	AB19
IO137PB4F12	AA19
<b>Bank 4 - Block 13</b>	
IO139NB4F13	AC19
IO139PB4F13	AC20
IO140NB4F13	AE21
IO140PB4F13	AE22
IO141NB4F13	AD20
IO141PB4F13	AD21
IO143NB4F13	AB17
IO143PB4F13	AB18
IO144NB4F13	AE19
IO144PB4F13	AE20
IO145NB4F13	AC17
IO145PB4F13	AC18
IO146NB4F13	AD18
IO146PB4F13	AD19

## 676-Pin FBGA

AX1000 Function	Pin Number
IO147NB4F13	AA17
IO147PB4F13	AA18
IO148NB4F13	AF20
IO148PB4F13	AF21
IO149NB4F13	AA16
IO149PB4F13	Y16
IO151NB4F13	AC16
IO151PB4F13	AB16
<b>Bank 4 - Block 14</b>	
IO153NB4F14	AE17
IO153PB4F14	AE18
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AA15
IO155PB4F14	Y15
IO157NB4F14	AC15
IO157PB4F14	AB15
IO159NB4F14/CLKEN	AE16
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AE14
IO160PB4F14/CLKFP	AE15
<b>Bank 5 - Block 15</b>	
IO161NB5F15/CLKGN	AE12
IO161PB5F15/CLKGP	AE13
IO162NB5F15/CLKHN	AE11
IO162PB5F15/CLKHP	AF11
IO163NB5F15	AC12
IO163PB5F15	AB12
IO165NB5F15	Y12
IO165PB5F15	AA13
IO167NB5F15	Y11
IO167PB5F15	AA12
IO168NB5F15	AF9
IO168PB5F15	AF10
IO169NB5F15	AB11
IO169PB5F15	AA11
<b>Bank 5 - Block 16</b>	
IO171NB5F16	AE9
IO171PB5F16	AE10
IO173NB5F16	AC10
IO173PB5F16	AC11
IO174NB5F16	AE7

## 676-Pin FBGA

AX1000 Function	Pin Number
IO174PB5F16	AE8
IO175NB5F16	AC9
IO175PB5F16	AD9
IO176NB5F16	AF6
IO176PB5F16	AF7
IO177NB5F16	AA10
IO177PB5F16	AB10
IO179NB5F16	AD7
IO179PB5F16	AD8
IO180NB5F16	AC7
IO180PB5F16	AC8
<b>Bank 5 - Block 17</b>	
IO181NB5F17	AA9
IO181PB5F17	AB9
IO183NB5F17	AD6
IO183PB5F17	AE6
IO184NB5F17	AE5
IO184PB5F17	AF5
IO185NB5F17	AA8
IO185PB5F17	AB8
IO187NB5F17	AC5
IO187PB5F17	AC6
IO188NB5F17	AD4
IO188PB5F17	AD5
IO189NB5F17	AB6
IO189PB5F17	AB7
IO190NB5F17	AF4
IO190PB5F17	AE4
IO191NB5F17	AE3
IO191PB5F17	AF3
IO192NB5F17	AA6
IO192PB5F17	AA7
<b>Bank 6 - Block 18</b>	
IO193NB6F18	Y5
IO193PB6F18	AA5
IO194NB6F18	AB3
IO194PB6F18	AC3
IO195NB6F18	Y4
IO195PB6F18	AA4
IO196NB6F18	AC2
IO196PB6F18	AD2
IO197NB6F18	W6

## 676-Pin FBGA

AX1000 Function	Pin Number
IO197PB6F18	Y6
IO198NB6F18	AD1
IO198PB6F18	AE1
IO199NB6F18	AA2
IO199PB6F18	AB2
IO200NB6F18	Y3
IO200PB6F18	AA3
IO201NB6F18	V5
IO201PB6F18	W5
IO202NB6F18	AB1
IO202PB6F18	AC1
<b>Bank 6 - Block 19</b>	
IO203NB6F19	V4
IO203PB6F19	W4
IO204NB6F19	V3
IO204PB6F19	W3
IO205NB6F19	U6
IO205PB6F19	V6
IO206NB6F19	W2
IO206PB6F19	Y2
IO207NB6F19	U4
IO207PB6F19	U5
IO208NB6F19	Y1
IO208PB6F19	AA1
IO209NB6F19	T6
IO209PB6F19	T7
IO211NB6F19	T3
IO211PB6F19	U3
IO212NB6F19	V1
IO212PB6F19	V2
IO213NB6F19	T5
IO213PB6F19	T4
<b>Bank 6 - Block 20</b>	
IO214NB6F20	U1
IO214PB6F20	U2
IO215NB6F20	R6
IO215PB6F20	R7
IO217NB6F20	R5
IO217PB6F20	R4
IO218NB6F20	R2
IO218PB6F20	T2
IO219NB6F20	P3

## 676-Pin FBGA

AX1000 Function	Pin Number
IO219PB6F20	R3
IO220NB6F20	R1
IO220PB6F20	T1
IO221NB6F20	P6
IO221PB6F20	P7
IO223NB6F20	P5
IO223PB6F20	P4
<b>Bank 7 - Block 21</b>	
IO225NB7F21	N5
IO225PB7F21	N4
IO226NB7F21	N2
IO226PB7F21	N3
IO227NB7F21	N6
IO227PB7F21	N7
IO229NB7F21	M7
IO229PB7F21	M6
IO231NB7F21	M5
IO231PB7F21	M4
IO232NB7F21	L1
IO232PB7F21	M1
IO233NB7F21	M2
IO233PB7F21	M3
IO235NB7F21	K2
IO235PB7F21	L2
<b>Bank 7 - Block 22</b>	
IO236NB7F22	L5
IO236PB7F22	L4
IO237NB7F22	L6
IO237PB7F22	L7
IO238NB7F22	K3
IO238PB7F22	L3
IO240NB7F22	J1
IO240PB7F22	K1
IO241NB7F22	K6
IO241PB7F22	K5
IO242NB7F22	H2
IO242PB7F22	J2
IO243NB7F22	J4
IO243PB7F22	K4
IO244NB7F22	H3
IO244PB7F22	J3
IO245NB7F22	G2

## 676-Pin FBGA

AX1000 Function	Pin Number
IO245PB7F22	G1
<b>Bank 7 - Block 23</b>	
IO247NB7F23	J6
IO247PB7F23	J5
IO248NB7F23	E1
IO248PB7F23	F1
IO249NB7F23	E2
IO249PB7F23	F2
IO250NB7F23	G4
IO250PB7F23	H4
IO251NB7F23	F3
IO251PB7F23	G3
IO253NB7F23	H6
IO253PB7F23	H5
IO254NB7F23	D2
IO254PB7F23	D1
IO255NB7F23	E4
IO255PB7F23	F4
IO256NB7F23	D3
IO256PB7F23	E3
IO257NB7F23	F5
IO257PB7F23	G5
<b>Dedicated I/O</b>	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2

## 676-Pin FBGA

AX1000 Function	Pin Number
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14

## 676-Pin FBGA

AX1000 Function	Pin Number
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19

## 676-Pin FBGA

AX1000 Function	Pin Number
GND	W26
GND	W8
GND	Y20
GND	Y7
LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25
NC	D13
NC	D14
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18

## 676-Pin FBGA

AX1000 Function	Pin Number
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCCDA	A11
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD11
VCCDA	AD13
VCCDA	AD16
VCCDA	AD17
VCCDA	B1
VCCDA	B11
VCCDA	B17
VCCDA	C16
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23
VCCI <sub>B0</sub>	G10
VCCI <sub>B0</sub>	G8

## 676-Pin FBGA

AX1000 Function	Pin Number
V <sub>CC</sub> I <sub>B0</sub>	G9
V <sub>CC</sub> I <sub>B0</sub>	H10
V <sub>CC</sub> I <sub>B0</sub>	H11
V <sub>CC</sub> I <sub>B0</sub>	H12
V <sub>CC</sub> I <sub>B0</sub>	H13
V <sub>CC</sub> I <sub>B0</sub>	H9
V <sub>CC</sub> I <sub>B1</sub>	G17
V <sub>CC</sub> I <sub>B1</sub>	G18
V <sub>CC</sub> I <sub>B1</sub>	G19
V <sub>CC</sub> I <sub>B1</sub>	H14
V <sub>CC</sub> I <sub>B1</sub>	H15
V <sub>CC</sub> I <sub>B1</sub>	H16
V <sub>CC</sub> I <sub>B1</sub>	H17
V <sub>CC</sub> I <sub>B1</sub>	H18
V <sub>CC</sub> I <sub>B2</sub>	H20
V <sub>CC</sub> I <sub>B2</sub>	J19
V <sub>CC</sub> I <sub>B2</sub>	J20
V <sub>CC</sub> I <sub>B2</sub>	K19
V <sub>CC</sub> I <sub>B2</sub>	K20
V <sub>CC</sub> I <sub>B2</sub>	L19
V <sub>CC</sub> I <sub>B2</sub>	M19
V <sub>CC</sub> I <sub>B2</sub>	N19
V <sub>CC</sub> I <sub>B3</sub>	P19
V <sub>CC</sub> I <sub>B3</sub>	R19
V <sub>CC</sub> I <sub>B3</sub>	T19
V <sub>CC</sub> I <sub>B3</sub>	U19
V <sub>CC</sub> I <sub>B3</sub>	U20
V <sub>CC</sub> I <sub>B3</sub>	V19
V <sub>CC</sub> I <sub>B3</sub>	V20
V <sub>CC</sub> I <sub>B3</sub>	W20
V <sub>CC</sub> I <sub>B4</sub>	W14
V <sub>CC</sub> I <sub>B4</sub>	W15
V <sub>CC</sub> I <sub>B4</sub>	W16
V <sub>CC</sub> I <sub>B4</sub>	W17
V <sub>CC</sub> I <sub>B4</sub>	W18
V <sub>CC</sub> I <sub>B4</sub>	Y17
V <sub>CC</sub> I <sub>B4</sub>	Y18
V <sub>CC</sub> I <sub>B4</sub>	Y19
V <sub>CC</sub> I <sub>B5</sub>	W10
V <sub>CC</sub> I <sub>B5</sub>	W11
V <sub>CC</sub> I <sub>B5</sub>	W12
V <sub>CC</sub> I <sub>B5</sub>	W13

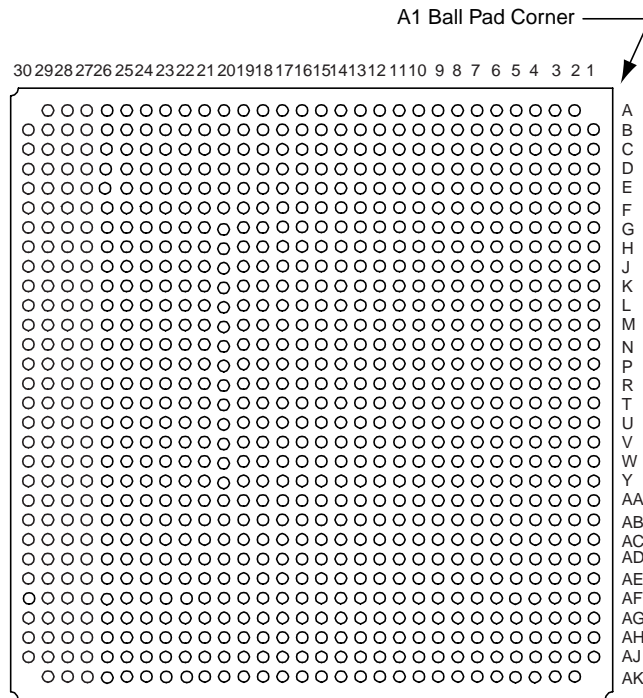
## 676-Pin FBGA

AX1000 Function	Pin Number
V <sub>CC</sub> I <sub>B5</sub>	W9
V <sub>CC</sub> I <sub>B5</sub>	Y10
V <sub>CC</sub> I <sub>B5</sub>	Y8
V <sub>CC</sub> I <sub>B5</sub>	Y9
V <sub>CC</sub> I <sub>B6</sub>	P8
V <sub>CC</sub> I <sub>B6</sub>	R8
V <sub>CC</sub> I <sub>B6</sub>	T8
V <sub>CC</sub> I <sub>B6</sub>	U7
V <sub>CC</sub> I <sub>B6</sub>	U8
V <sub>CC</sub> I <sub>B6</sub>	V7
V <sub>CC</sub> I <sub>B6</sub>	V8
V <sub>CC</sub> I <sub>B6</sub>	W7
V <sub>CC</sub> I <sub>B7</sub>	H7
V <sub>CC</sub> I <sub>B7</sub>	J7
V <sub>CC</sub> I <sub>B7</sub>	J8
V <sub>CC</sub> I <sub>B7</sub>	K7
V <sub>CC</sub> I <sub>B7</sub>	K8
V <sub>CC</sub> I <sub>B7</sub>	L8
V <sub>CC</sub> I <sub>B7</sub>	M8
V <sub>CC</sub> I <sub>B7</sub>	N8
V <sub>COMPLA</sub>	D12
V <sub>COMPLB</sub>	G13
V <sub>COMPLC</sub>	D15
V <sub>COMPLD</sub>	F14
V <sub>COMPLE</sub>	AD15
V <sub>COMPLF</sub>	AB14
V <sub>COMPLG</sub>	AD12
V <sub>COMPLH</sub>	Y13
V <sub>PUMP</sub>	E22



# Package Pin Assignments (Continued)

## 896-Pin FBGA (Bottom View)



## 896-Pin FBGA

AX1000 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	D6
IO00PB0F0	E6
IO01NB0F0	A5
IO01PB0F0	B5
IO02NB0F0	G9
IO02PB0F0	G8
IO03NB0F0	F8
IO03PB0F0	F7
IO04NB0F0	D7
IO04PB0F0	E7
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	H9
IO06PB0F0	H8
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	E9
IO08PB0F0	F9
IO09NB0F0	A7
IO09PB0F0	B7
IO10NB0F0	H10
IO10PB0F0	G10
IO11NB0F0	C9
IO11PB0F0	C8
<b>Bank 0 - Block 1</b>	
IO12NB0F1	E10
IO12PB0F1	F10
IO13NB0F1	D10
IO13PB0F1	D9
IO14NB0F1	F11
IO14PB0F1	G11
IO15NB0F1	A10
IO15PB0F1	A9
IO16NB0F1	H12
IO16PB0F1	H11
IO17NB0F1	B11
IO17PB0F1	B10
IO18NB0F1	D11
IO18PB0F1	E11
IO19NB0F1	C12
IO19PB0F1	C11

## 896-Pin FBGA

AX1000 Function	Pin Number
IO20NB0F1	F12
IO20PB0F1	G12
IO21NB0F1	D12
IO21PB0F1	E12
<b>Bank 0 - Block 2</b>	
IO22NB0F2	H13
IO22PB0F2	J13
IO23NB0F2	A12
IO23PB0F2	A11
IO24NB0F2	F13
IO24PB0F2	G13
IO25NB0F2	B13
IO25PB0F2	B12
IO26NB0F2	E14
IO26PB0F2	E13
IO27NB0F2	B14
IO27PB0F2	A14
IO28NB0F2	H14
IO28PB0F2	J14
IO29NB0F2	B15
IO29PB0F2	A15
IO30NB0F2/HCLKAN	C14
IO30PB0F2/HCLKAP	D14
IO31NB0F2/HCLKBN	E15
IO31PB0F2/HCLKBP	D15
<b>Bank 1 - Block 3</b>	
IO32NB1F3/HCLKCN	E17
IO32PB1F3/HCLKCP	E16
IO33NB1F3/HCLKDN	C17
IO33PB1F3/HCLKDP	D17
IO34NB1F3	A17
IO34PB1F3	B17
IO35NB1F3	D18
IO35PB1F3	C18
IO36NB1F3	H17
IO36PB1F3	J17
IO37NB1F3	B19
IO37PB1F3	A19
IO38NB1F3	H18
IO38PB1F3	J18
IO39NB1F3	B20
IO39PB1F3	A20

## 896-Pin FBGA

AX1000 Function	Pin Number
IO40NB1F3	C20
IO40PB1F3	C19
<b>Bank 1 - Block 4</b>	
IO41NB1F4	E20
IO41PB1F4	E19
IO42NB1F4	F18
IO42PB1F4	G18
IO43NB1F4	A22
IO43PB1F4	A21
IO44NB1F4	F20
IO44PB1F4	F19
IO45NB1F4	D21
IO45PB1F4	D20
IO46NB1F4	D22
IO46PB1F4	C22
IO47NB1F4	A25
IO47PB1F4	A24
IO48NB1F4	H19
IO48PB1F4	G19
IO49NB1F4	C24
IO49PB1F4	C23
IO50NB1F4	G20
IO50PB1F4	H20
IO51NB1F4	F21
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
<b>Bank 1 - Block 5</b>	
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26

## 896-Pin FBGA

AX1000 Function	Pin Number
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
<b>Bank 2 - Block 6</b>	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
<b>Bank 2 - Block 7</b>	
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29

## 896-Pin FBGA

AX1000 Function	Pin Number
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
<b>Bank 2 - Block 8</b>	
IO85NB2F8	M29
IO85PB2F8	L29
IO86NB2F8	N28
IO86PB2F8	N27
IO87NB2F8	P29
IO87PB2F8	P30
IO88NB2F8	P25
IO88PB2F8	P24
IO89NB2F8	P28
IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
<b>Bank 3 - Block 9</b>	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26

## 896-Pin FBGA

AX1000 Function	Pin Number
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22
IO103NB3F9	V27
IO103PB3F9	U27
IO104NB3F9	W29
IO104PB3F9	V29
IO105NB3F9	Y28
IO105PB3F9	W28
IO106NB3F9	V25
IO106PB3F9	U25
<b>Bank 3 - Block 10</b>	
IO107NB3F10	W26
IO107PB3F10	V26
IO108NB3F10	W24
IO108PB3F10	V24
IO109NB3F10	Y27
IO109PB3F10	W27
IO110NB3F10	V23
IO110PB3F10	V22
IO111NB3F10	AA29
IO111PB3F10	Y29
IO112NB3F10	Y25
IO112PB3F10	W25
IO113NB3F10	AB27
IO113PB3F10	AA27
IO114NB3F10	Y23
IO114PB3F10	W23
IO115NB3F10	AA26
IO115PB3F10	Y26
IO116NB3F10	AC28
IO116PB3F10	AB28
IO117NB3F10	AE29
IO117PB3F10	AD29
<b>Bank 3 - Block 11</b>	
IO118NB3F11	AE28
IO118PB3F11	AD28
IO119NB3F11	AD27
IO119PB3F11	AC27

## 896-Pin FBGA

AX1000 Function	Pin Number
IO120NB3F11	AA24
IO120PB3F11	Y24
IO121NB3F11	AB25
IO121PB3F11	AA25
IO122NB3F11	AC26
IO122PB3F11	AB26
IO123NB3F11	AG28
IO123PB3F11	AF28
IO124NB3F11	AB23
IO124PB3F11	AA23
IO125NB3F11	AF27
IO125PB3F11	AE27
IO126NB3F11	AD25
IO126PB3F11	AC25
IO127NB3F11	AE26
IO127PB3F11	AD26
IO128NB3F11	AC24
IO128PB3F11	AB24
<b>Bank 4 - Block 12</b>	
IO129NB4F12	AD23
IO129PB4F12	AC23
IO130NB4F12	AK26
IO130PB4F12	AK27
IO131NB4F12	AF24
IO131PB4F12	AF25
IO132NB4F12	AG25
IO132PB4F12	AG26
IO133NB4F12	AD22
IO133PB4F12	AC22
IO134NB4F12	AE23
IO134PB4F12	AE24
IO135NB4F12	AH24
IO135PB4F12	AH25
IO136NB4F12	AJ25
IO136PB4F12	AJ26
IO137NB4F12	AD21
IO137PB4F12	AC21
IO138NB4F12	AK24
IO138PB4F12	AK25
<b>Bank 4 - Block 13</b>	
IO139NB4F13	AE21
IO139PB4F13	AE22

## 896-Pin FBGA

AX1000 Function	Pin Number
IO140NB4F13	AG23
IO140PB4F13	AG24
IO141NB4F13	AF22
IO141PB4F13	AF23
IO142NB4F13	AJ23
IO142PB4F13	AJ24
IO143NB4F13	AD19
IO143PB4F13	AD20
IO144NB4F13	AG21
IO144PB4F13	AG22
IO145NB4F13	AE19
IO145PB4F13	AE20
IO146NB4F13	AF20
IO146PB4F13	AF21
IO147NB4F13	AC19
IO147PB4F13	AC20
IO148NB4F13	AH22
IO148PB4F13	AH23
IO149NB4F13	AC18
IO149PB4F13	AB18
IO150NB4F13	AK21
IO150PB4F13	AJ21
IO151NB4F13	AE18
IO151PB4F13	AD18
<b>Bank 4 - Block 14</b>	
IO152NB4F14	AJ20
IO152PB4F14	AK20
IO153NB4F14	AG19
IO153PB4F14	AG20
IO154NB4F14	AH19
IO154PB4F14	AH20
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16

## 896-Pin FBGA

AX1000 Function	Pin Number
IO160PB4F14/CLKFP	AG17
<b>Bank 5 - Block 15</b>	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
<b>Bank 5 - Block 16</b>	
IO171NB5F16	AG11
IO171PB5F16	AG12
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9

## 896-Pin FBGA

AX1000 Function	Pin Number
IO180PB5F16	AE10
<b>Bank 5 - Block 17</b>	
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
<b>Bank 6 - Block 18</b>	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5

## 896-Pin FBGA

AX1000 Function	Pin Number
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3
IO202PB6F18	AE3
<b>Bank 6 - Block 19</b>	
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4
IO206PB6F19	AB4
IO207NB6F19	W6
IO207PB6F19	W7
IO208NB6F19	AB3
IO208PB6F19	AC3
IO209NB6F19	V8
IO209PB6F19	V9
IO210NB6F19	AA2
IO210PB6F19	AA1
IO211NB6F19	V5
IO211PB6F19	W5
IO212NB6F19	Y3
IO212PB6F19	Y4
IO213NB6F19	V7
IO213PB6F19	V6
<b>Bank 6 - Block 20</b>	
IO214NB6F20	W3
IO214PB6F20	W4
IO215NB6F20	U8
IO215PB6F20	U9
IO216NB6F20	W1
IO216PB6F20	W2
IO217NB6F20	U7
IO217PB6F20	U6
IO218NB6F20	U4
IO218PB6F20	V4
IO219NB6F20	T5
IO219PB6F20	U5
IO220NB6F20	U3

## 896-Pin FBGA

AX1000 Function	Pin Number
IO220PB6F20	V3
IO221NB6F20	T8
IO221PB6F20	T9
IO222NB6F20	U2
IO222PB6F20	V2
IO223NB6F20	T7
IO223PB6F20	T6
IO224NB6F20	R2
IO224PB6F20	T2
<b>Bank 7 - Block 21</b>	
IO225NB7F21	R7
IO225PB7F21	R6
IO226NB7F21	R4
IO226PB7F21	R5
IO227NB7F21	R8
IO227PB7F21	R9
IO228NB7F21	P1
IO228PB7F21	R1
IO229NB7F21	P9
IO229PB7F21	P8
IO230NB7F21	N2
IO230PB7F21	P2
IO231NB7F21	P7
IO231PB7F21	P6
IO232NB7F21	N3
IO232PB7F21	P3
IO233NB7F21	P4
IO233PB7F21	P5
IO234NB7F21	L1
IO234PB7F21	M1
IO235NB7F21	M4
IO235PB7F21	N4
<b>Bank 7 - Block 22</b>	
IO236NB7F22	N7
IO236PB7F22	N6
IO237NB7F22	N8
IO237PB7F22	N9
IO238NB7F22	M5
IO238PB7F22	N5
IO239NB7F22	L2
IO239PB7F22	M2
IO240NB7F22	L3

## 896-Pin FBGA

AX1000 Function	Pin Number
IO240PB7F22	M3
IO241NB7F22	M8
IO241PB7F22	M7
IO242NB7F22	K4
IO242PB7F22	L4
IO243NB7F22	L6
IO243PB7F22	M6
IO244NB7F22	K5
IO244PB7F22	L5
IO245NB7F22	J4
IO245PB7F22	J3
IO246NB7F22	G2
IO246PB7F22	H2
<b>Bank 7 - Block 23</b>	
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	G3
IO248PB7F23	H3
IO249NB7F23	G4
IO249PB7F23	H4
IO250NB7F23	J6
IO250PB7F23	K6
IO251NB7F23	H5
IO251PB7F23	J5
IO252NB7F23	F2
IO252PB7F23	F1
IO253NB7F23	K8
IO253PB7F23	K7
IO254NB7F23	F4
IO254PB7F23	F3
IO255NB7F23	G6
IO255PB7F23	H6
IO256NB7F23	F5
IO256PB7F23	G5
IO257NB7F23	H7
IO257PB7F23	J7
<b>Dedicated I/O</b>	
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29

## 896-Pin FBGA

AX1000 Function	Pin Number
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10

## 896-Pin FBGA

AX1000 Function	Pin Number
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13

896-Pin FBGA

AX1000 Function	Pin Number
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18

896-Pin FBGA

AX1000 Function	Pin Number
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	Y11
GND	Y20
LP	E4
NC	A16
NC	A26
NC	A4
NC	A6
NC	AA30
NC	AB1
NC	AB30
NC	AC2
NC	AC29
NC	AD1
NC	AD2
NC	AD30
NC	AE1
NC	AE15
NC	AE16
NC	AE2
NC	AE30
NC	AF1
NC	AF2
NC	AF29
NC	AF30
NC	AG1
NC	AG2
NC	AG29
NC	AG30
NC	AH27
NC	AH4
NC	AJ14
NC	AJ15

896-Pin FBGA

AX1000 Function	Pin Number
NC	AJ16
NC	AJ27
NC	AJ4
NC	AK14
NC	AK15
NC	AK16
NC	AK17
NC	AK22
NC	AK4
NC	AK5
NC	B16
NC	B18
NC	B21
NC	B23
NC	B26
NC	B4
NC	B6
NC	B8
NC	C27
NC	D1
NC	D2
NC	D29
NC	D30
NC	E1
NC	E2
NC	E29
NC	E30
NC	F15
NC	F16
NC	F29
NC	F30
NC	G1
NC	G29
NC	G30
NC	H29
NC	J1
NC	J30
NC	K1
NC	K2
NC	L30
NC	M30
NC	N29

## 896-Pin FBGA

AX1000 Function	Pin Number
NC	T1
NC	U1
NC	W30
NC	Y1
NC	Y2
NC	Y30
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
V <sub>CCA</sub>	AD6
V <sub>CCA</sub>	AH26
V <sub>CCA</sub>	E28
V <sub>CCA</sub>	E3
V <sub>CCA</sub>	L12
V <sub>CCA</sub>	L13
V <sub>CCA</sub>	L14
V <sub>CCA</sub>	L15
V <sub>CCA</sub>	L16
V <sub>CCA</sub>	L17
V <sub>CCA</sub>	L18
V <sub>CCA</sub>	L19
V <sub>CCA</sub>	M11
V <sub>CCA</sub>	M20
V <sub>CCA</sub>	N11
V <sub>CCA</sub>	N20
V <sub>CCA</sub>	P11
V <sub>CCA</sub>	P20
V <sub>CCA</sub>	R11
V <sub>CCA</sub>	R20
V <sub>CCA</sub>	T11
V <sub>CCA</sub>	T20
V <sub>CCA</sub>	U11
V <sub>CCA</sub>	U20
V <sub>CCA</sub>	V11
V <sub>CCA</sub>	V20
V <sub>CCA</sub>	W11

## 896-Pin FBGA

AX1000 Function	Pin Number
V <sub>CCA</sub>	W20
V <sub>CCA</sub>	Y12
V <sub>CCA</sub>	Y13
V <sub>CCA</sub>	Y14
V <sub>CCA</sub>	Y15
V <sub>CCA</sub>	Y16
V <sub>CCA</sub>	Y17
V <sub>CCA</sub>	Y18
V <sub>CCA</sub>	Y19
V <sub>CCPLA</sub>	G14
V <sub>CCPLB</sub>	H15
V <sub>CCPLC</sub>	G17
V <sub>CCPLD</sub>	J16
V <sub>CCPLE</sub>	AH17
V <sub>CCPLF</sub>	AC16
V <sub>CCPLG</sub>	AH14
V <sub>CCPLH</sub>	AD15
V <sub>CCDA</sub>	AD24
V <sub>CCDA</sub>	AD7
V <sub>CCDA</sub>	AF12
V <sub>CCDA</sub>	AF13
V <sub>CCDA</sub>	AF15
V <sub>CCDA</sub>	AF18
V <sub>CCDA</sub>	AF19
V <sub>CCDA</sub>	C13
V <sub>CCDA</sub>	C5
V <sub>CCDA</sub>	D13
V <sub>CCDA</sub>	D19
V <sub>CCDA</sub>	D3
V <sub>CCDA</sub>	E18
V <sub>CCDA</sub>	F26
V <sub>CCDA</sub>	G16
V <sub>CCDA</sub>	T25
V <sub>CCDA</sub>	T4
V <sub>CCIB0</sub>	A3
V <sub>CCIB0</sub>	B3
V <sub>CCIB0</sub>	J10
V <sub>CCIB0</sub>	J11
V <sub>CCIB0</sub>	J12
V <sub>CCIB0</sub>	K11
V <sub>CCIB0</sub>	K12
V <sub>CCIB0</sub>	K13

## 896-Pin FBGA

AX1000 Function	Pin Number
V <sub>CCIB0</sub>	K14
V <sub>CCIB0</sub>	K15
V <sub>CCIB1</sub>	A28
V <sub>CCIB1</sub>	B28
V <sub>CCIB1</sub>	J19
V <sub>CCIB1</sub>	J20
V <sub>CCIB1</sub>	J21
V <sub>CCIB1</sub>	K16
V <sub>CCIB1</sub>	K17
V <sub>CCIB1</sub>	K18
V <sub>CCIB1</sub>	K19
V <sub>CCIB1</sub>	K20
V <sub>CCIB2</sub>	C29
V <sub>CCIB2</sub>	C30
V <sub>CCIB2</sub>	K22
V <sub>CCIB2</sub>	L21
V <sub>CCIB2</sub>	L22
V <sub>CCIB2</sub>	M21
V <sub>CCIB2</sub>	M22
V <sub>CCIB2</sub>	N21
V <sub>CCIB2</sub>	P21
V <sub>CCIB2</sub>	R21
V <sub>CCIB3</sub>	AA22
V <sub>CCIB3</sub>	AH29
V <sub>CCIB3</sub>	AH30
V <sub>CCIB3</sub>	T21
V <sub>CCIB3</sub>	U21
V <sub>CCIB3</sub>	V21
V <sub>CCIB3</sub>	W21
V <sub>CCIB3</sub>	W22
V <sub>CCIB3</sub>	Y21
V <sub>CCIB3</sub>	Y22
V <sub>CCIB4</sub>	AA16
V <sub>CCIB4</sub>	AA17
V <sub>CCIB4</sub>	AA18
V <sub>CCIB4</sub>	AA19
V <sub>CCIB4</sub>	AA20
V <sub>CCIB4</sub>	AB19
V <sub>CCIB4</sub>	AB20
V <sub>CCIB4</sub>	AB21
V <sub>CCIB4</sub>	AJ28
V <sub>CCIB4</sub>	AK28



## 896-Pin FBGA

AX1000 Function	Pin Number
V <sub>CC</sub> I B5	AA11
V <sub>CC</sub> I B5	AA12
V <sub>CC</sub> I B5	AA13
V <sub>CC</sub> I B5	AA14
V <sub>CC</sub> I B5	AA15
V <sub>CC</sub> I B5	AB10
V <sub>CC</sub> I B5	AB11
V <sub>CC</sub> I B5	AB12
V <sub>CC</sub> I B5	AJ3
V <sub>CC</sub> I B5	AK3
V <sub>CC</sub> I B6	AA9
V <sub>CC</sub> I B6	AH1
V <sub>CC</sub> I B6	AH2
V <sub>CC</sub> I B6	T10
V <sub>CC</sub> I B6	U10
V <sub>CC</sub> I B6	V10
V <sub>CC</sub> I B6	W10
V <sub>CC</sub> I B6	W9
V <sub>CC</sub> I B6	Y10
V <sub>CC</sub> I B6	Y9
V <sub>CC</sub> I B7	C1
V <sub>CC</sub> I B7	C2
V <sub>CC</sub> I B7	K9
V <sub>CC</sub> I B7	L10
V <sub>CC</sub> I B7	L9
V <sub>CC</sub> I B7	M10
V <sub>CC</sub> I B7	M9
V <sub>CC</sub> I B7	N10
V <sub>CC</sub> I B7	P10
V <sub>CC</sub> I B7	R10
V <sub>COMPLA</sub>	F14
V <sub>COMPLB</sub>	J15
V <sub>COMPLC</sub>	F17
V <sub>COMPLD</sub>	H16
V <sub>COMPLE</sub>	AF17
V <sub>COMPLF</sub>	AD16
V <sub>COMPLG</sub>	AF14
V <sub>COMPLH</sub>	AB15
V <sub>PUMP</sub>	G24

## 896-Pin FBGA

AX2000 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
<b>Bank 0 - Block 1</b>	
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
<b>Bank 0 - Block 2</b>	

## 896-Pin FBGA

AX2000 Function	Pin Number
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
<b>Bank 0 - Block 3</b>	
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15
<b>Bank 1 - Block 4</b>	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17

## 896-Pin FBGA

AX2000 Function	Pin Number
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
<b>Bank 1 - Block 5</b>	
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
<b>Bank 1 - Block 6</b>	
IO65NB1F6	G20
IO65PB1F6	H20
IO66NB1F6	B23
IO66PB1F6	B21
IO67NB1F6	H21
IO67PB1F6	G21
IO68NB1F6	D22
IO68PB1F6	C22
IO69NB1F6	A25
IO69PB1F6	A24
IO70NB1F6	F22
IO70PB1F6	E22
IO71NB1F6	F21
IO71PB1F6	E21
IO73NB1F6	C24
IO73PB1F6	C23
IO74NB1F6	D24

## 896-Pin FBGA

AX2000 Function	Pin Number
IO74PB1F6	D23
IO75NB1F6	H23
IO75PB1F6	H22
<b>Bank 1 - Block 7</b>	
IO76NB1F7	B25
IO76PB1F7	B24
IO78NB1F7	B26
IO78PB1F7	A26
IO79NB1F7	F23
IO79PB1F7	E23
IO80NB1F7	D25
IO80PB1F7	C25
IO81NB1F7	G23
IO81PB1F7	G22
IO82NB1F7	B27
IO82PB1F7	A27
IO83NB1F7	F24
IO83PB1F7	E24
IO84NB1F7	D26
IO84PB1F7	C26
IO85NB1F7	F25
IO85PB1F7	E25
<b>Bank 2 - Block 8</b>	
IO86NB2F8	G26
IO86PB2F8	G25
IO87NB2F8	K23
IO87PB2F8	J23
IO88NB2F8	J24
IO88PB2F8	H24
IO89NB2F8	E29
IO89PB2F8	D29
IO90NB2F8	F27
IO90PB2F8	E27
IO91NB2F8	H26
IO91PB2F8	H25
IO92NB2F8	G28
IO92PB2F8	F28
IO93NB2F8	J26
IO93PB2F8	J25
IO94NB2F8	H27
IO94PB2F8	G27
IO95NB2F8	H29

## 896-Pin FBGA

AX2000 Function	Pin Number
IO95PB2F8	G29
<b>Bank 2 - Block 9</b>	
IO96NB2F9	G30
IO96PB2F9	F30
IO97NB2F9	K25
IO97PB2F9	K24
IO98NB2F9	J28
IO98PB2F9	H28
IO99NB2F9	L23
IO99PB2F9	L24
IO100NB2F9	K27
IO100PB2F9	J27
IO101PB2F9	J30
IO102NB2F9	E30
IO102PB2F9	D30
IO103NB2F9	L26
IO103PB2F9	K26
IO104NB2F9	F29
IO105NB2F9	M25
IO105PB2F9	L25
IO106NB2F9	K30
IO106PB2F9	K29
<b>Bank 2 - Block 10</b>	
IO107NB2F10	M23
IO107PB2F10	M24
IO109NB2F10	M27
IO109PB2F10	L27
IO110NB2F10	M28
IO110PB2F10	L28
IO111NB2F10	N22
IO111PB2F10	N23
IO112NB2F10	M29
IO112PB2F10	L29
IO113NB2F10	N26
IO113PB2F10	M26
IO114NB2F10	M30
IO114PB2F10	L30
IO115NB2F10	N28
IO115PB2F10	N27
IO117NB2F10	N25
IO117PB2F10	N24
<b>Bank 2 - Block 11</b>	

## 896-Pin FBGA

AX2000 Function	Pin Number
IO118NB2F11	N29
IO119NB2F11	P22
IO119PB2F11	P23
IO121NB2F11	P25
IO121PB2F11	P24
IO122NB2F11	P28
IO122PB2F11	P27
IO123NB2F11	R26
IO123PB2F11	P26
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
<b>Bank 3 - Block 12</b>	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
<b>Bank 3 - Block 13</b>	
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29

## 896-Pin FBGA

AX2000 Function	Pin Number
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
<b>Bank 3 - Block 14</b>	
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
<b>Bank 3 - Block 15</b>	
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27
IO163NB3F15	AC26
IO163PB3F15	AB26

## 896-Pin FBGA

AX2000 Function	Pin Number
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23
IO170PB3F15	AA23
<b>Bank 4 - Block 16</b>	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23
IO180PB4F16	AG24
<b>Bank 4 - Block 17</b>	
IO181NB4F17	AK24
IO181PB4F17	AK25
IO182NB4F17	AD22
IO182PB4F17	AC22
IO183NB4F17	AF22
IO183PB4F17	AF23
IO184NB4F17	AE21

## 896-Pin FBGA

AX2000 Function	Pin Number
IO184PB4F17	AE22
IO185NB4F17	AJ23
IO185PB4F17	AJ24
IO187NB4F17	AH22
IO187PB4F17	AH23
IO188NB4F17	AD21
IO188PB4F17	AC21
IO189PB4F17	AK22
IO190NB4F17	AF20
IO190PB4F17	AF21
IO191NB4F17	AG21
IO191PB4F17	AG22
IO192NB4F17	AE19
IO192PB4F17	AE20
<b>Bank 4 - Block 18</b>	
IO195NB4F18	AK21
IO195PB4F18	AJ21
IO196NB4F18	AD19
IO196PB4F18	AD20
IO197NB4F18	AJ20
IO197PB4F18	AK20
IO198NB4F18	AC19
IO198PB4F18	AC20
IO199NB4F18	AG19
IO199PB4F18	AG20
IO200NB4F18	AH19
IO200PB4F18	AH20
IO201NB4F18	AK19
IO201PB4F18	AJ19
IO202NB4F18	AC18
IO202PB4F18	AB18
<b>Bank 4 - Block 19</b>	
IO206NB4F19	AE18
IO206PB4F19	AD18
IO207NB4F19	AJ17
IO207PB4F19	AJ18
IO208NB4F19	AE17
IO208PB4F19	AD17
IO209NB4F19	AK17
IO210NB4F19	AC17
IO210PB4F19	AB17
IO211NB4F19	AJ16

## 896-Pin FBGA

AX2000 Function	Pin Number
IO211PB4F19	AK16
IO212NB4F19/CLKEN	AG18
IO212PB4F19/CLKEP	AH18
IO213NB4F19/CLKFN	AG16
IO213PB4F19/CLKFP	AG17
<b>Bank 5 - Block 20</b>	
IO214NB5F20/CLKGN	AG14
IO214PB5F20/CLKGP	AG15
IO215NB5F20/CLKHN	AG13
IO215PB5F20/CLKHP	AH13
IO216NB5F20	AB14
IO216PB5F20	AC15
IO217NB5F20	AK15
IO217PB5F20	AJ15
IO218NB5F20	AE14
IO218PB5F20	AD14
IO219NB5F20	AK14
IO219PB5F20	AJ14
IO222NB5F20	AB13
IO222PB5F20	AC14
<b>Bank 5 - Block 21</b>	
IO223NB5F21	AJ12
IO223PB5F21	AJ13
IO225NB5F21	AH11
IO225PB5F21	AH12
IO226NB5F21	AC13
IO226PB5F21	AD13
IO227NB5F21	AE12
IO227PB5F21	AE13
IO228NB5F21	AG11
IO228PB5F21	AG12
IO229NB5F21	AK11
IO229PB5F21	AK12
IO230NB5F21	AC12
IO230PB5F21	AD12
IO232NB5F21	AE11
IO232PB5F21	AF11
IO233NB5F21	AJ10
IO233PB5F21	AJ11
IO234NB5F21	AC11
IO234PB5F21	AD11
<b>Bank 5 - Block 22</b>	

## 896-Pin FBGA

AX2000 Function	Pin Number
IO236NB5F22	AK9
IO236PB5F22	AK10
IO237NB5F22	AG9
IO237PB5F22	AG10
IO238NB5F22	AF9
IO238PB5F22	AF10
IO239NB5F22	AH8
IO239PB5F22	AH9
IO240NB5F22	AC10
IO240PB5F22	AD10
IO242NB5F22	AE9
IO242PB5F22	AE10
IO243NB5F22	AJ7
IO243PB5F22	AJ8
IO244NB5F22	AK6
IO244PB5F22	AK7
<b>Bank 5 - Block 23</b>	
IO245NB5F23	AF8
IO245PB5F23	AG8
IO246NB5F23	AD8
IO246PB5F23	AD9
IO247NB5F23	AG7
IO247PB5F23	AH7
IO248NB5F23	AK5
IO249NB5F23	AJ5
IO249PB5F23	AJ6
IO250NB5F23	AC8
IO250PB5F23	AC9
IO251NB5F23	AH6
IO251PB5F23	AG6
IO252NB5F23	AF6
IO252PB5F23	AF7
IO253NB5F23	AG2
IO253PB5F23	AG1
IO254NB5F23	AE7
IO254PB5F23	AE8
IO255NB5F23	AG5
IO255PB5F23	AH5
IO256NB5F23	AJ4
IO256PB5F23	AK4
<b>Bank 6 - Block 24</b>	
IO257NB6F24	AE4

## 896-Pin FBGA

AX2000 Function	Pin Number
IO257PB6F24	AF4
IO258NB6F24	AB7
IO258PB6F24	AC7
IO259NB6F24	AD5
IO259PB6F24	AE5
IO260NB6F24	AF1
IO260PB6F24	AF2
IO261NB6F24	AF3
IO261PB6F24	AG3
IO262NB6F24	AC4
IO262PB6F24	AD4
IO263NB6F24	AD3
IO263PB6F24	AE3
IO264NB6F24	AB6
IO264PB6F24	AC6
IO265NB6F24	AD1
IO265PB6F24	AE1
IO266NB6F24	AA8
IO266PB6F24	AB8
<b>Bank 6 - Block 25</b>	
IO267NB6F25	AB5
IO267PB6F25	AC5
IO268NB6F25	AB3
IO268PB6F25	AC3
IO269NB6F25	AC2
IO269PB6F25	AD2
IO270NB6F25	Y7
IO270PB6F25	AA7
IO271NB6F25	AA4
IO271PB6F25	AB4
IO272NB6F25	Y6
IO272PB6F25	AA6
IO273NB6F25	AB1
IO273PB6F25	AE2
IO274NB6F25	W8
IO274PB6F25	Y8
IO275NB6F25	Y5
IO275PB6F25	AA5
IO277NB6F25	AA2
IO277PB6F25	AA1
<b>Bank 6 - Block 26</b>	
IO278NB6F26	W6

## 896-Pin FBGA

AX2000 Function	Pin Number
IO278PB6F26	W7
IO279NB6F26	Y3
IO279PB6F26	Y4
IO280NB6F26	V8
IO280PB6F26	V9
IO281NB6F26	Y1
IO281PB6F26	Y2
IO282NB6F26	V5
IO282PB6F26	W5
IO284NB6F26	V7
IO284PB6F26	V6
IO285NB6F26	W3
IO285PB6F26	W4
IO286NB6F26	U8
IO286PB6F26	U9
IO287NB6F26	W1
IO287PB6F26	W2
IO288NB6F26	U7
IO288PB6F26	U6
<b>Bank 6 - Block 27</b>	
IO290NB6F27	U4
IO290PB6F27	V4
IO291NB6F27	U3
IO291PB6F27	V3
IO292NB6F27	T5
IO292PB6F27	U5
IO293NB6F27	U2
IO293PB6F27	V2
IO294NB6F27	T8
IO294PB6F27	T9
IO296NB6F27	T1
IO296PB6F27	U1
IO298NB6F27	T7
IO298PB6F27	T6
IO299NB6F27	R2
IO299PB6F27	T2
<b>Bank 7 - Block 28</b>	
IO300NB7F28	R8
IO300PB7F28	R9
IO302NB7F28	R4
IO302PB7F28	R5
IO303NB7F28	P1

## 896-Pin FBGA

AX2000 Function	Pin Number
IO303PB7F28	R1
IO304NB7F28	R7
IO304PB7F28	R6
IO306NB7F28	N2
IO306PB7F28	P2
IO307NB7F28	N3
IO307PB7F28	P3
IO308NB7F28	P9
IO308PB7F28	P8
IO309NB7F28	P4
IO309PB7F28	P5
<b>Bank 7 - Block 29</b>	
IO310NB7F29	P7
IO310PB7F29	P6
IO311NB7F29	L1
IO311PB7F29	M1
IO312NB7F29	M5
IO312PB7F29	N5
IO313NB7F29	M4
IO313PB7F29	N4
IO315NB7F29	L2
IO315PB7F29	M2
IO316NB7F29	N7
IO316PB7F29	N6
IO317NB7F29	L3
IO317PB7F29	M3
IO318NB7F29	N8
IO318PB7F29	N9
IO320NB7F29	L6
IO320PB7F29	M6
<b>Bank 7 - Block 30</b>	
IO321NB7F30	K4
IO321PB7F30	L4
IO322NB7F30	M8
IO322PB7F30	M7
IO323NB7F30	J1
IO323PB7F30	K1
IO324NB7F30	K5
IO324PB7F30	L5
IO326NB7F30	G1
IO326PB7F30	K2
IO327NB7F30	J4

## 896-Pin FBGA

AX2000 Function	Pin Number
IO327PB7F30	J3
IO328NB7F30	L8
IO328PB7F30	L7
IO329NB7F30	G2
IO329PB7F30	H2
IO330NB7F30	G3
IO330PB7F30	H3
IO331NB7F30	K8
IO331PB7F30	K7
<b>Bank 7 - Block 31</b>	
IO332NB7F31	J6
IO332PB7F31	K6
IO333NB7F31	D1
IO333PB7F31	D2
IO334NB7F31	G4
IO334PB7F31	H4
IO335NB7F31	F2
IO335PB7F31	F1
IO336NB7F31	H5
IO336PB7F31	J5
IO337NB7F31	E2
IO337PB7F31	E1
IO338NB7F31	H7
IO338PB7F31	J7
IO339NB7F31	F4
IO339PB7F31	F3
IO340NB7F31	F5
IO340PB7F31	G5
IO341NB7F31	G6
IO341PB7F31	H6
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	D3
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3

## 896-Pin FBGA

AX2000 Function	Pin Number
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3

## 896-Pin FBGA

AX2000 Function	Pin Number
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18

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AX2000 Function	Pin Number
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14

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AX2000 Function	Pin Number
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
V <sub>CCA</sub>	AD6
V <sub>CCA</sub>	AH26
V <sub>CCA</sub>	E28
V <sub>CCA</sub>	E3
V <sub>CCA</sub>	L12
V <sub>CCA</sub>	L13
V <sub>CCA</sub>	L14
V <sub>CCA</sub>	L15
V <sub>CCA</sub>	L16
V <sub>CCA</sub>	L17
V <sub>CCA</sub>	L18
V <sub>CCA</sub>	L19
V <sub>CCA</sub>	M11
V <sub>CCA</sub>	M20
V <sub>CCA</sub>	N11
V <sub>CCA</sub>	N20
V <sub>CCA</sub>	P11
V <sub>CCA</sub>	P20
V <sub>CCA</sub>	R11
V <sub>CCA</sub>	R20
V <sub>CCA</sub>	T11
V <sub>CCA</sub>	T20
V <sub>CCA</sub>	U11
V <sub>CCA</sub>	U20
V <sub>CCA</sub>	V11

896-Pin FBGA

AX2000 Function	Pin Number
V <sub>CCA</sub>	V20
V <sub>CCA</sub>	W11
V <sub>CCA</sub>	W20
V <sub>CCA</sub>	Y12
V <sub>CCA</sub>	Y13
V <sub>CCA</sub>	Y14
V <sub>CCA</sub>	Y15
V <sub>CCA</sub>	Y16
V <sub>CCA</sub>	Y17
V <sub>CCA</sub>	Y18
V <sub>CCA</sub>	Y19
V <sub>CCPLA</sub>	G14
V <sub>CCPLB</sub>	H15
V <sub>CCPLC</sub>	G17
V <sub>CCPLD</sub>	J16
V <sub>CCPLE</sub>	AH17
V <sub>CCPLF</sub>	AC16
V <sub>CCPLG</sub>	AH14
V <sub>CCPLH</sub>	AD15
V <sub>CCDA</sub>	AD24
V <sub>CCDA</sub>	AD7
V <sub>CCDA</sub>	AE15
V <sub>CCDA</sub>	AE16
V <sub>CCDA</sub>	AF12
V <sub>CCDA</sub>	AF13
V <sub>CCDA</sub>	AF15
V <sub>CCDA</sub>	AF18
V <sub>CCDA</sub>	AF19
V <sub>CCDA</sub>	AH27
V <sub>CCDA</sub>	AH4
V <sub>CCDA</sub>	C13
V <sub>CCDA</sub>	C27
V <sub>CCDA</sub>	C5
V <sub>CCDA</sub>	D13
V <sub>CCDA</sub>	D19
V <sub>CCDA</sub>	E18
V <sub>CCDA</sub>	F15
V <sub>CCDA</sub>	F16
V <sub>CCDA</sub>	F26
V <sub>CCDA</sub>	G16
V <sub>CCDA</sub>	T25
V <sub>CCDA</sub>	T4

## 896-Pin FBGA

AX2000 Function	Pin Number
V <sub>CC</sub> I <sub>B0</sub>	A3
V <sub>CC</sub> I <sub>B0</sub>	B3
V <sub>CC</sub> I <sub>B0</sub>	J10
V <sub>CC</sub> I <sub>B0</sub>	J11
V <sub>CC</sub> I <sub>B0</sub>	J12
V <sub>CC</sub> I <sub>B0</sub>	K11
V <sub>CC</sub> I <sub>B0</sub>	K12
V <sub>CC</sub> I <sub>B0</sub>	K13
V <sub>CC</sub> I <sub>B0</sub>	K14
V <sub>CC</sub> I <sub>B0</sub>	K15
V <sub>CC</sub> I <sub>B1</sub>	A28
V <sub>CC</sub> I <sub>B1</sub>	B28
V <sub>CC</sub> I <sub>B1</sub>	J19
V <sub>CC</sub> I <sub>B1</sub>	J20
V <sub>CC</sub> I <sub>B1</sub>	J21
V <sub>CC</sub> I <sub>B1</sub>	K16
V <sub>CC</sub> I <sub>B1</sub>	K17
V <sub>CC</sub> I <sub>B1</sub>	K18
V <sub>CC</sub> I <sub>B1</sub>	K19
V <sub>CC</sub> I <sub>B1</sub>	K20
V <sub>CC</sub> I <sub>B2</sub>	C29
V <sub>CC</sub> I <sub>B2</sub>	C30
V <sub>CC</sub> I <sub>B2</sub>	K22
V <sub>CC</sub> I <sub>B2</sub>	L21
V <sub>CC</sub> I <sub>B2</sub>	L22
V <sub>CC</sub> I <sub>B2</sub>	M21
V <sub>CC</sub> I <sub>B2</sub>	M22
V <sub>CC</sub> I <sub>B2</sub>	N21
V <sub>CC</sub> I <sub>B2</sub>	P21
V <sub>CC</sub> I <sub>B2</sub>	R21
V <sub>CC</sub> I <sub>B3</sub>	AA22
V <sub>CC</sub> I <sub>B3</sub>	AH29
V <sub>CC</sub> I <sub>B3</sub>	AH30
V <sub>CC</sub> I <sub>B3</sub>	T21
V <sub>CC</sub> I <sub>B3</sub>	U21
V <sub>CC</sub> I <sub>B3</sub>	V21
V <sub>CC</sub> I <sub>B3</sub>	W21
V <sub>CC</sub> I <sub>B3</sub>	W22
V <sub>CC</sub> I <sub>B3</sub>	Y21
V <sub>CC</sub> I <sub>B3</sub>	Y22
V <sub>CC</sub> I <sub>B4</sub>	AA16
V <sub>CC</sub> I <sub>B4</sub>	AA17

## 896-Pin FBGA

AX2000 Function	Pin Number
V <sub>CC</sub> I <sub>B4</sub>	AA18
V <sub>CC</sub> I <sub>B4</sub>	AA19
V <sub>CC</sub> I <sub>B4</sub>	AA20
V <sub>CC</sub> I <sub>B4</sub>	AB19
V <sub>CC</sub> I <sub>B4</sub>	AB20
V <sub>CC</sub> I <sub>B4</sub>	AB21
V <sub>CC</sub> I <sub>B4</sub>	AJ28
V <sub>CC</sub> I <sub>B5</sub>	AK28
V <sub>CC</sub> I <sub>B5</sub>	AA11
V <sub>CC</sub> I <sub>B5</sub>	AA12
V <sub>CC</sub> I <sub>B5</sub>	AA13
V <sub>CC</sub> I <sub>B5</sub>	AA14
V <sub>CC</sub> I <sub>B5</sub>	AA15
V <sub>CC</sub> I <sub>B5</sub>	AB10
V <sub>CC</sub> I <sub>B5</sub>	AB11
V <sub>CC</sub> I <sub>B5</sub>	AB12
V <sub>CC</sub> I <sub>B5</sub>	AJ3
V <sub>CC</sub> I <sub>B5</sub>	AK3
V <sub>CC</sub> I <sub>B6</sub>	AA9
V <sub>CC</sub> I <sub>B6</sub>	AH1
V <sub>CC</sub> I <sub>B6</sub>	AH2
V <sub>CC</sub> I <sub>B6</sub>	T10
V <sub>CC</sub> I <sub>B6</sub>	U10
V <sub>CC</sub> I <sub>B6</sub>	V10
V <sub>CC</sub> I <sub>B6</sub>	W10
V <sub>CC</sub> I <sub>B6</sub>	W9
V <sub>CC</sub> I <sub>B6</sub>	Y10
V <sub>CC</sub> I <sub>B6</sub>	Y9
V <sub>CC</sub> I <sub>B7</sub>	C1
V <sub>CC</sub> I <sub>B7</sub>	C2
V <sub>CC</sub> I <sub>B7</sub>	K9
V <sub>CC</sub> I <sub>B7</sub>	L10
V <sub>CC</sub> I <sub>B7</sub>	L9
V <sub>CC</sub> I <sub>B7</sub>	M10
V <sub>CC</sub> I <sub>B7</sub>	M9
V <sub>CC</sub> I <sub>B7</sub>	N10
V <sub>CC</sub> I <sub>B7</sub>	P10
V <sub>CC</sub> I <sub>B7</sub>	R10
V <sub>COMPLA</sub>	F14
V <sub>COMPLB</sub>	J15
V <sub>COMPLC</sub>	F17
V <sub>COMPLD</sub>	H16

## 896-Pin FBGA

AX2000 Function	Pin Number
V <sub>COMPLE</sub>	AF17
V <sub>COMPLF</sub>	AD16
V <sub>COMPLG</sub>	AF14
V <sub>COMPLH</sub>	AB15
V <sub>PUMP</sub>	G24





## 1152-Pin FBGA

AX2000 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	D6
IO00PB0F0	C6
IO01NB0F0	H10
IO01PB0F0	H9
IO02NB0F0	F8
IO02PB0F0	G8
IO03NB0F0	A6
IO03PB0F0	B6
IO04NB0F0	C7
IO04PB0F0	D7
IO05NB0F0	K10
IO05PB0F0	J10
IO06NB0F0	F9
IO06PB0F0	G9
IO07NB0F0	F10
IO07PB0F0	G10
IO08NB0F0	E9
IO08PB0F0	E8
IO09NB0F0	J11
IO09PB0F0	K11
IO10NB0F0	C8
IO10PB0F0	D8
IO11NB0F0	K12
IO11PB0F0	J12
<b>Bank 0 - Block 1</b>	
IO12NB0F1	G11
IO12PB0F1	H11
IO13NB0F1	G12
IO13PB0F1	H12
IO14NB0F1	A7
IO14PB0F1	B7
IO15NB0F1	H13
IO15PB0F1	J13
IO16NB0F1	C9
IO16PB0F1	D9
IO17NB0F1	F12
IO17PB0F1	F11
IO18NB0F1	E11
IO18PB0F1	E10
IO19NB0F1	F13
IO19PB0F1	G13

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO20NB0F1	A10
IO20PB0F1	A9
IO21NB0F1	K14
IO21PB0F1	K13
<b>Bank 0 - Block 2</b>	
IO22NB0F2	B11
IO22PB0F2	B10
IO23NB0F2	C12
IO23PB0F2	C11
IO24NB0F2	A12
IO24PB0F2	A11
IO25NB0F2	H14
IO25PB0F2	J14
IO26NB0F2	D13
IO26PB0F2	D12
IO27NB0F2	F14
IO27PB0F2	G14
IO28NB0F2	E14
IO28PB0F2	E13
IO29NB0F2	B13
IO29PB0F2	B12
IO30NB0F2	C14
IO30PB0F2	C13
IO31NB0F2	H15
IO31PB0F2	J15
IO32NB0F2	A14
IO32PB0F2	B14
IO33NB0F2	K15
IO33PB0F2	L15
<b>Bank 0 - Block 3</b>	
IO34NB0F3	D15
IO34PB0F3	D14
IO35NB0F3	A15
IO35PB0F3	B15
IO36NB0F3	B16
IO36PB0F3	A16
IO37NB0F3	G16
IO37PB0F3	G15
IO38NB0F3	D16
IO38PB0F3	C16
IO39NB0F3	K16
IO39PB0F3	L16

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO40NB0F3	D17
IO40PB0F3	C17
IO41NB0F3/HCLKAN	E16
IO41PB0F3/HCLKAP	F16
IO42NB0F3/HCLKBN	G17
IO42PB0F3/HCLKBP	F17
<b>Bank 1 - Block 4</b>	
IO43NB1F4/HCLKCN	G19
IO43PB1F4/HCLKCP	G18
IO44NB1F4/HCLKDN	E19
IO44PB1F4/HCLKDP	F19
IO45NB1F4	C18
IO45PB1F4	D18
IO46NB1F4	A18
IO46PB1F4	B18
IO47NB1F4	K19
IO47PB1F4	L19
IO48NB1F4	C19
IO48PB1F4	D19
IO49NB1F4	K20
IO49PB1F4	L20
IO50NB1F4	A19
IO50PB1F4	B19
IO51NB1F4	H20
IO51PB1F4	J20
IO52NB1F4	B20
IO52PB1F4	A20
IO53NB1F4	F20
IO53PB1F4	E20
<b>Bank 1 - Block 5</b>	
IO54NB1F5	B21
IO54PB1F5	A21
IO55NB1F5	K21
IO55PB1F5	J21
IO56NB1F5	D21
IO56PB1F5	C21
IO57NB1F5	G22
IO57PB1F5	G21
IO58NB1F5	E22
IO58PB1F5	E21
IO59NB1F5	D22
IO59PB1F5	C22

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO60NB1F5	B23
IO60PB1F5	A23
IO61NB1F5	H22
IO61PB1F5	H21
IO62NB1F5	C24
IO62PB1F5	C23
IO63NB1F5	F23
IO63PB1F5	F22
<b>Bank 1 - Block 6</b>	
IO64NB1F6	B24
IO64PB1F6	A24
IO65NB1F6	J22
IO65PB1F6	K22
IO66NB1F6	B25
IO66PB1F6	A25
IO67NB1F6	K23
IO67PB1F6	J23
IO68NB1F6	F24
IO68PB1F6	E24
IO69NB1F6	C27
IO69PB1F6	C26
IO70NB1F6	H24
IO70PB1F6	G24
IO71NB1F6	H23
IO71PB1F6	G23
IO72NB1F6	B28
IO72PB1F6	A28
IO73NB1F6	E26
IO73PB1F6	E25
IO74NB1F6	F26
IO74PB1F6	F25
IO75NB1F6	K25
IO75PB1F6	K24
<b>Bank 1 - Block 7</b>	
IO76NB1F7	D27
IO76PB1F7	D26
IO77NB1F7	B29
IO77PB1F7	A29
IO78NB1F7	D28
IO78PB1F7	C28
IO79NB1F7	H25
IO79PB1F7	G25

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO80NB1F7	F27
IO80PB1F7	E27
IO81NB1F7	J25
IO81PB1F7	J24
IO82NB1F7	D29
IO82PB1F7	C29
IO83NB1F7	H26
IO83PB1F7	G26
IO84NB1F7	F28
IO84PB1F7	E28
IO85NB1F7	H27
IO85PB1F7	G27
<b>Bank 2 - Block 8</b>	
IO86NB2F8	J28
IO86PB2F8	J27
IO87NB2F8	M25
IO87PB2F8	L25
IO88NB2F8	L26
IO88PB2F8	K26
IO89NB2F8	G31
IO89PB2F8	F31
IO90NB2F8	H29
IO90PB2F8	G29
IO91NB2F8	K28
IO91PB2F8	K27
IO92NB2F8	J30
IO92PB2F8	H30
IO93NB2F8	L28
IO93PB2F8	L27
IO94NB2F8	K29
IO94PB2F8	J29
IO95NB2F8	K31
IO95PB2F8	J31
<b>Bank 2 - Block 9</b>	
IO96NB2F9	J32
IO96PB2F9	H32
IO97NB2F9	M27
IO97PB2F9	M26
IO98NB2F9	L30
IO98PB2F9	K30
IO99NB2F9	N25
IO99PB2F9	N26

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO100NB2F9	M29
IO100PB2F9	L29
IO101NB2F9	L33
IO101PB2F9	L32
IO102NB2F9	K34
IO102PB2F9	K33
IO103NB2F9	N28
IO103PB2F9	M28
IO104NB2F9	M34
IO104PB2F9	L34
IO105NB2F9	P27
IO105PB2F9	N27
IO106NB2F9	M32
IO106PB2F9	M31
<b>Bank 2 - Block 10</b>	
IO107NB2F10	P25
IO107PB2F10	P26
IO108NB2F10	N33
IO108PB2F10	M33
IO109NB2F10	P29
IO109PB2F10	N29
IO110NB2F10	P30
IO110PB2F10	N30
IO111NB2F10	R24
IO111PB2F10	R25
IO112NB2F10	P31
IO112PB2F10	N31
IO113NB2F10	R28
IO113PB2F10	P28
IO114NB2F10	P32
IO114PB2F10	N32
IO115NB2F10	R30
IO115PB2F10	R29
IO116NB2F10	P34
IO116PB2F10	P33
IO117NB2F10	R27
IO117PB2F10	R26
<b>Bank 2 - Block 11</b>	
IO118NB2F11	R34
IO118PB2F11	R33
IO119NB2F11	T24
IO119PB2F11	T25

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO120NB2F11	T33
IO120PB2F11	T34
IO121NB2F11	T27
IO121PB2F11	T26
IO122NB2F11	T30
IO122PB2F11	T29
IO123NB2F11	U28
IO123PB2F11	T28
IO124NB2F11	T31
IO124PB2F11	T32
IO125NB2F11	U24
IO125PB2F11	U25
IO126NB2F11	U33
IO126PB2F11	U34
IO127NB2F11	U26
IO127PB2F11	U27
IO128NB2F11	U31
IO128PB2F11	U32
<b>Bank 3 - Block 12</b>	
IO129NB3F12	V29
IO129PB3F12	U29
IO130NB3F12	V31
IO130PB3F12	V32
IO131NB3F12	V24
IO131PB3F12	V25
IO132NB3F12	W28
IO132PB3F12	V28
IO133NB3F12	W26
IO133PB3F12	V26
IO134NB3F12	W33
IO134PB3F12	V33
IO135NB3F12	W25
IO135PB3F12	W24
IO136NB3F12	W31
IO136PB3F12	W32
IO137NB3F12	Y30
IO137PB3F12	W30
IO138NB3F12	Y29
IO138PB3F12	W29
<b>Bank 3 - Block 13</b>	
IO139NB3F13	Y27
IO139PB3F13	W27

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO140NB3F13	AA33
IO140PB3F13	Y33
IO141NB3F13	Y25
IO141PB3F13	Y24
IO142NB3F13	AA31
IO142PB3F13	Y31
IO143NB3F13	AA28
IO143PB3F13	Y28
IO144NB3F13	AA34
IO144PB3F13	Y34
IO145NB3F13	AA26
IO145PB3F13	Y26
IO146NB3F13	AA29
IO146PB3F13	AA30
IO147NB3F13	AB30
IO147PB3F13	AB29
IO148NB3F13	AB32
IO148PB3F13	AA32
IO149NB3F13	AB27
IO149PB3F13	AA27
<b>Bank 3 - Block 14</b>	
IO150NB3F14	AC31
IO150PB3F14	AB31
IO151NB3F14	AD33
IO151PB3F14	AC33
IO152NB3F14	AC28
IO152PB3F14	AB28
IO153NB3F14	AB25
IO153PB3F14	AA25
IO154NB3F14	AD32
IO154PB3F14	AC32
IO155NB3F14	AD29
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO160PB3F14	AF32
<b>Bank 3 - Block 15</b>	
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
<b>Bank 4 - Block 16</b>	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO180PB4F16	AJ26
<b>Bank 4 - Block 17</b>	
IO181NB4F17	AM26
IO181PB4F17	AM27
IO182NB4F17	AF24
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
<b>Bank 4 - Block 18</b>	
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO200PB4F18	AK22
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
<b>Bank 4 - Block 19</b>	
IO203NB4F19	AN21
IO203PB4F19	AP21
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19
IO207PB4F19	AL20
IO208NB4F19	AG19
IO208PB4F19	AF19
IO209NB4F19	AN18
IO209PB4F19	AP18
IO210NB4F19	AE19
IO210PB4F19	AD19
IO211NB4F19	AL18
IO211PB4F19	AM18
IO212NB4F19/CLKEN	AJ20
IO212PB4F19/CLKEP	AK20
IO213NB4F19/CLKFN	AJ18
IO213PB4F19/CLKFP	AJ19
<b>Bank 5 - Block 20</b>	
IO214NB5F20/CLKGN	AJ16
IO214PB5F20/CLKGP	AJ17
IO215NB5F20/CLKHN	AJ15
IO215PB5F20/CLKHP	AK15
IO216NB5F20	AD16
IO216PB5F20	AE17
IO217NB5F20	AM17
IO217PB5F20	AL17
IO218NB5F20	AG16
IO218PB5F20	AF16
IO219NB5F20	AM16
IO219PB5F20	AL16
IO220NB5F20	AP16

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO220PB5F20	AN16
IO221NB5F20	AN15
IO221PB5F20	AP15
IO222NB5F20	AD15
IO222PB5F20	AE16
<b>Bank 5 - Block 21</b>	
IO223NB5F21	AL14
IO223PB5F21	AL15
IO224NB5F21	AN14
IO224PB5F21	AP14
IO225NB5F21	AK13
IO225PB5F21	AK14
IO226NB5F21	AE15
IO226PB5F21	AF15
IO227NB5F21	AG14
IO227PB5F21	AG15
IO228NB5F21	AJ13
IO228PB5F21	AJ14
IO229NB5F21	AM13
IO229PB5F21	AM14
IO230NB5F21	AE14
IO230PB5F21	AF14
IO231NB5F21	AN12
IO231PB5F21	AP12
IO232NB5F21	AG13
IO232PB5F21	AH13
IO233NB5F21	AL12
IO233PB5F21	AL13
IO234NB5F21	AE13
IO234PB5F21	AF13
<b>Bank 5 - Block 22</b>	
IO235NB5F22	AN11
IO235PB5F22	AP11
IO236NB5F22	AM11
IO236PB5F22	AM12
IO237NB5F22	AJ11
IO237PB5F22	AJ12
IO238NB5F22	AH11
IO238PB5F22	AH12
IO239NB5F22	AK10
IO239PB5F22	AK11
IO240NB5F22	AE12

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO240PB5F22	AF12
IO241NB5F22	AN10
IO241PB5F22	AP10
IO242NB5F22	AG11
IO242PB5F22	AG12
IO243NB5F22	AL9
IO243PB5F22	AL10
IO244NB5F22	AM8
IO244PB5F22	AM9
<b>Bank 5 - Block 23</b>	
IO245NB5F23	AH10
IO245PB5F23	AJ10
IO246NB5F23	AF10
IO246PB5F23	AF11
IO247NB5F23	AJ9
IO247PB5F23	AK9
IO248NB5F23	AN7
IO248PB5F23	AP7
IO249NB5F23	AL7
IO249PB5F23	AL8
IO250NB5F23	AE10
IO250PB5F23	AE11
IO251NB5F23	AK8
IO251PB5F23	AJ8
IO252NB5F23	AH8
IO252PB5F23	AH9
IO253NB5F23	AN6
IO253PB5F23	AP6
IO254NB5F23	AG9
IO254PB5F23	AG10
IO255NB5F23	AJ7
IO255PB5F23	AK7
IO256NB5F23	AL6
IO256PB5F23	AM6
<b>Bank 6 - Block 24</b>	
IO257NB6F24	AG6
IO257PB6F24	AH6
IO258NB6F24	AD9
IO258PB6F24	AE9
IO259NB6F24	AF7
IO259PB6F24	AG7
IO260NB6F24	AH3

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO260PB6F24	AH4
IO261NB6F24	AH5
IO261PB6F24	AJ5
IO262NB6F24	AE6
IO262PB6F24	AF6
IO263NB6F24	AF5
IO263PB6F24	AG5
IO264NB6F24	AD8
IO264PB6F24	AE8
IO265NB6F24	AF3
IO265PB6F24	AG3
IO266NB6F24	AC10
IO266PB6F24	AD10
<b>Bank 6 - Block 25</b>	
IO267NB6F25	AD7
IO267PB6F25	AE7
IO268NB6F25	AD5
IO268PB6F25	AE5
IO269NB6F25	AE4
IO269PB6F25	AF4
IO270NB6F25	AB9
IO270PB6F25	AC9
IO271NB6F25	AC6
IO271PB6F25	AD6
IO272NB6F25	AB8
IO272PB6F25	AC8
IO273NB6F25	AE1
IO273PB6F25	AE2
IO274NB6F25	AA10
IO274PB6F25	AB10
IO275NB6F25	AB7
IO275PB6F25	AC7
IO276NB6F25	AD1
IO276PB6F25	AD2
IO277NB6F25	AC4
IO277PB6F25	AC3
<b>Bank 6 - Block 26</b>	
IO278NB6F26	AA8
IO278PB6F26	AA9
IO279NB6F26	AB5
IO279PB6F26	AB6
IO280NB6F26	Y10

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO280PB6F26	Y11
IO281NB6F26	AB3
IO281PB6F26	AB4
IO282NB6F26	Y7
IO282PB6F26	AA7
IO283NB6F26	AC2
IO283PB6F26	AC1
IO284NB6F26	Y9
IO284PB6F26	Y8
IO285NB6F26	AA5
IO285PB6F26	AA6
IO286NB6F26	W10
IO286PB6F26	W11
IO287NB6F26	AA3
IO287PB6F26	AA4
IO288NB6F26	W9
IO288PB6F26	W8
<b>Bank 6 - Block 27</b>	
IO289NB6F27	AA1
IO289PB6F27	AA2
IO290NB6F27	W6
IO290PB6F27	Y6
IO291NB6F27	W5
IO291PB6F27	Y5
IO292NB6F27	V7
IO292PB6F27	W7
IO293NB6F27	W4
IO293PB6F27	Y4
IO294NB6F27	V10
IO294PB6F27	V11
IO295NB6F27	Y1
IO295PB6F27	Y2
IO296NB6F27	W1
IO296PB6F27	W2
IO297NB6F27	V1
IO297PB6F27	V2
IO298NB6F27	V9
IO298PB6F27	V8
IO299NB6F27	U4
IO299PB6F27	V4
<b>Bank 7 - Block 28</b>	
IO300NB7F28	U10

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO300PB7F28	U11
IO301NB7F28	U2
IO301PB7F28	U1
IO302NB7F28	U6
IO302PB7F28	U7
IO303NB7F28	T3
IO303PB7F28	U3
IO304NB7F28	U9
IO304PB7F28	U8
IO305NB7F28	R2
IO305PB7F28	R1
IO306NB7F28	R4
IO306PB7F28	T4
IO307NB7F28	R5
IO307PB7F28	T5
IO308NB7F28	T11
IO308PB7F28	T10
IO309NB7F28	T6
IO309PB7F28	T7
<b>Bank 7 - Block 29</b>	
IO310NB7F29	T9
IO310PB7F29	T8
IO311NB7F29	N3
IO311PB7F29	P3
IO312NB7F29	P7
IO312PB7F29	R7
IO313NB7F29	P6
IO313PB7F29	R6
IO314NB7F29	M2
IO314PB7F29	N2
IO315NB7F29	N4
IO315PB7F29	P4
IO316NB7F29	R9
IO316PB7F29	R8
IO317NB7F29	N5
IO317PB7F29	P5
IO318NB7F29	R10
IO318PB7F29	R11
IO319NB7F29	L2
IO319PB7F29	L1
IO320NB7F29	N8
IO320PB7F29	P8

## 1152-Pin FBGA

AX2000 Function	Pin Number
<b>Bank 7 - Block 30</b>	
IO321NB7F30	M6
IO321PB7F30	N6
IO322NB7F30	P10
IO322PB7F30	P9
IO323NB7F30	L3
IO323PB7F30	M3
IO324NB7F30	M7
IO324PB7F30	N7
IO325NB7F30	K2
IO325PB7F30	K1
IO326NB7F30	G2
IO326PB7F30	H2
IO327NB7F30	L6
IO327PB7F30	L5
IO328NB7F30	N10
IO328PB7F30	N9
IO329NB7F30	J4
IO329PB7F30	K4
IO330NB7F30	J5
IO330PB7F30	K5
IO331NB7F30	M10
IO331PB7F30	M9
<b>Bank 7 - Block 31</b>	
IO332NB7F31	L8
IO332PB7F31	M8
IO333NB7F31	F2
IO333PB7F31	F1
IO334NB7F31	J6
IO334PB7F31	K6
IO335NB7F31	H4
IO335PB7F31	H3
IO336NB7F31	K7
IO336PB7F31	L7
IO337NB7F31	G4
IO337PB7F31	G3
IO338NB7F31	K9
IO338PB7F31	L9
IO339NB7F31	H6
IO339PB7F31	H5
IO340NB7F31	H7
IO340PB7F31	J7

## 1152-Pin FBGA

AX2000 Function	Pin Number
IO341NB7F31	J8
IO341PB7F31	K8
<b>Dedicated I/O</b>	
V <sub>CCDA</sub>	F5
GND	A13
GND	A2
GND	A22
GND	A27
GND	A3
GND	A31
GND	A32
GND	A33
GND	A4
GND	A8
GND	AA14
GND	AA15
GND	AA16
GND	AA17
GND	AA18
GND	AA19
GND	AA20
GND	AA21
GND	AB1
GND	AB13
GND	AB22
GND	AB34
GND	AC12
GND	AC23
GND	AC30
GND	AC5
GND	AD11
GND	AD24
GND	AD31
GND	AD4
GND	AE3
GND	AE32
GND	AF2
GND	AF33
GND	AG1
GND	AG27
GND	AG34
GND	AG8

## 1152-Pin FBGA

AX2000 Function	Pin Number
GND	AH28
GND	AH7
GND	AJ29
GND	AJ6
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33
GND	AN34
GND	AN4
GND	AN9

## 1152-Pin FBGA

AX2000 Function	Pin Number
GND	AP13
GND	AP2
GND	AP22
GND	AP27
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4
GND	D1
GND	D11
GND	D2
GND	D24
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34
GND	D4

## 1152-Pin FBGA

AX2000 Function	Pin Number
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5
GND	N1
GND	N13
GND	N22
GND	N34
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	P20
GND	P21
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18



1152-Pin FBGA

AX2000 Function	Pin Number
GND	R19
GND	R20
GND	R21
GND	R3
GND	R32
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T20
GND	T21
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U20
GND	U21
GND	U30
GND	U5
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V20
GND	V21
GND	V30
GND	V5
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	W20
GND	W21
GND	Y14

1152-Pin FBGA

AX2000 Function	Pin Number
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y3
GND	Y32
LP	G6
NC	A17
NC	A26
NC	AB2
NC	AB33
NC	AC34
NC	AD3
NC	AD34
NC	AE31
NC	AE33
NC	AE34
NC	AF1
NC	AF34
NC	AG2
NC	AG4
NC	AH1
NC	AH2
NC	AH31
NC	AH32
NC	AH34
NC	AJ1
NC	AJ2
NC	AJ3
NC	AJ31
NC	AJ32
NC	AJ33
NC	AJ34
NC	AJ4
NC	AL29
NC	AM19
NC	AM7
NC	AN13
NC	AN17

1152-Pin FBGA

AX2000 Function	Pin Number
NC	AN25
NC	AN27
NC	AN8
NC	AP17
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H31
NC	H33
NC	J1
NC	J3
NC	J34
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17
PRB	F18
PRC	AD18
PRD	AH18

## 1152-Pin FBGA

AX2000 Function	Pin Number
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
V <sub>CCA</sub>	AA13
V <sub>CCA</sub>	AA22
V <sub>CCA</sub>	AB14
V <sub>CCA</sub>	AB15
V <sub>CCA</sub>	AB16
V <sub>CCA</sub>	AB17
V <sub>CCA</sub>	AB18
V <sub>CCA</sub>	AB19
V <sub>CCA</sub>	AB20
V <sub>CCA</sub>	AB21
V <sub>CCA</sub>	AF8
V <sub>CCA</sub>	AK28
V <sub>CCA</sub>	G30
V <sub>CCA</sub>	G5
V <sub>CCA</sub>	N14
V <sub>CCA</sub>	N15
V <sub>CCA</sub>	N16
V <sub>CCA</sub>	N17
V <sub>CCA</sub>	N18
V <sub>CCA</sub>	N19
V <sub>CCA</sub>	N20
V <sub>CCA</sub>	N21
V <sub>CCA</sub>	P13
V <sub>CCA</sub>	P22
V <sub>CCA</sub>	R13
V <sub>CCA</sub>	R22
V <sub>CCA</sub>	T13
V <sub>CCA</sub>	T22
V <sub>CCA</sub>	U13
V <sub>CCA</sub>	U22
V <sub>CCA</sub>	V13
V <sub>CCA</sub>	V22
V <sub>CCA</sub>	W13
V <sub>CCA</sub>	W22
V <sub>CCA</sub>	Y13
V <sub>CCA</sub>	Y22
V <sub>CCPLA</sub>	J16

## 1152-Pin FBGA

AX2000 Function	Pin Number
V <sub>CCPLB</sub>	K17
V <sub>CCPLC</sub>	J19
V <sub>CCPLD</sub>	L18
V <sub>CCPLE</sub>	AK19
V <sub>CCPLF</sub>	AE18
V <sub>CCPLG</sub>	AK16
V <sub>CCPLH</sub>	AF17
V <sub>CCDA</sub>	AF26
V <sub>CCDA</sub>	AF9
V <sub>CCDA</sub>	AG17
V <sub>CCDA</sub>	AG18
V <sub>CCDA</sub>	AH14
V <sub>CCDA</sub>	AH15
V <sub>CCDA</sub>	AH17
V <sub>CCDA</sub>	AH20
V <sub>CCDA</sub>	AH21
V <sub>CCDA</sub>	AK29
V <sub>CCDA</sub>	AK6
V <sub>CCDA</sub>	E15
V <sub>CCDA</sub>	E29
V <sub>CCDA</sub>	E7
V <sub>CCDA</sub>	F15
V <sub>CCDA</sub>	F21
V <sub>CCDA</sub>	G20
V <sub>CCDA</sub>	H17
V <sub>CCDA</sub>	H18
V <sub>CCDA</sub>	H28
V <sub>CCDA</sub>	J18
V <sub>CCDA</sub>	V27
V <sub>CCDA</sub>	V6
V <sub>CCIB0</sub>	A5
V <sub>CCIB0</sub>	B5
V <sub>CCIB0</sub>	C5
V <sub>CCIB0</sub>	D5
V <sub>CCIB0</sub>	L12
V <sub>CCIB0</sub>	L13
V <sub>CCIB0</sub>	L14
V <sub>CCIB0</sub>	M13
V <sub>CCIB0</sub>	M14
V <sub>CCIB0</sub>	M15
V <sub>CCIB0</sub>	M16
V <sub>CCIB0</sub>	M17

## 1152-Pin FBGA

AX2000 Function	Pin Number
V <sub>CCIB1</sub>	A30
V <sub>CCIB1</sub>	B30
V <sub>CCIB1</sub>	C30
V <sub>CCIB1</sub>	D30
V <sub>CCIB1</sub>	L21
V <sub>CCIB1</sub>	L22
V <sub>CCIB1</sub>	L23
V <sub>CCIB1</sub>	M18
V <sub>CCIB1</sub>	M19
V <sub>CCIB1</sub>	M20
V <sub>CCIB1</sub>	M21
V <sub>CCIB1</sub>	M22
V <sub>CCIB2</sub>	E31
V <sub>CCIB2</sub>	E32
V <sub>CCIB2</sub>	E33
V <sub>CCIB2</sub>	E34
V <sub>CCIB2</sub>	M24
V <sub>CCIB2</sub>	N23
V <sub>CCIB2</sub>	N24
V <sub>CCIB2</sub>	P23
V <sub>CCIB2</sub>	P24
V <sub>CCIB2</sub>	R23
V <sub>CCIB2</sub>	T23
V <sub>CCIB2</sub>	U23
V <sub>CCIB3</sub>	AA23
V <sub>CCIB3</sub>	AA24
V <sub>CCIB3</sub>	AB23
V <sub>CCIB3</sub>	AB24
V <sub>CCIB3</sub>	AC24
V <sub>CCIB3</sub>	AK31
V <sub>CCIB3</sub>	AK32
V <sub>CCIB3</sub>	AK33
V <sub>CCIB3</sub>	AK34
V <sub>CCIB3</sub>	V23
V <sub>CCIB3</sub>	W23
V <sub>CCIB3</sub>	Y23
V <sub>CCIB4</sub>	AC18
V <sub>CCIB4</sub>	AC19
V <sub>CCIB4</sub>	AC20
V <sub>CCIB4</sub>	AC21
V <sub>CCIB4</sub>	AC22
V <sub>CCIB4</sub>	AD21

## 1152-Pin FBGA

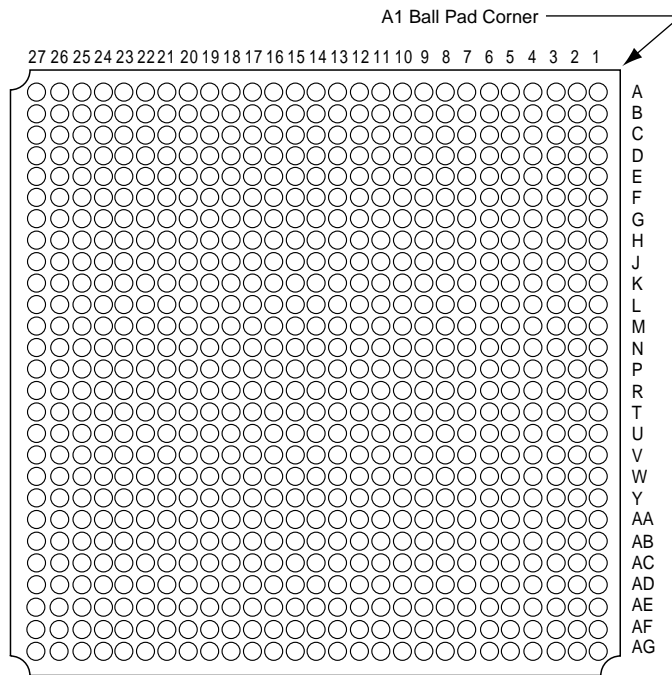
AX2000 Function	Pin Number
V <sub>CCI</sub> B4	AD22
V <sub>CCI</sub> B4	AD23
V <sub>CCI</sub> B4	AL30
V <sub>CCI</sub> B4	AM30
V <sub>CCI</sub> B4	AN30
V <sub>CCI</sub> B4	AP30
V <sub>CCI</sub> B5	AC13
V <sub>CCI</sub> B5	AC14
V <sub>CCI</sub> B5	AC15
V <sub>CCI</sub> B5	AC16
V <sub>CCI</sub> B5	AC17
V <sub>CCI</sub> B5	AD12
V <sub>CCI</sub> B5	AD13
V <sub>CCI</sub> B5	AD14
V <sub>CCI</sub> B5	AL5
V <sub>CCI</sub> B5	AM5
V <sub>CCI</sub> B5	AN5
V <sub>CCI</sub> B5	AP5
V <sub>CCI</sub> B6	AA11
V <sub>CCI</sub> B6	AA12
V <sub>CCI</sub> B6	AB11
V <sub>CCI</sub> B6	AB12
V <sub>CCI</sub> B6	AC11
V <sub>CCI</sub> B6	AK1
V <sub>CCI</sub> B6	AK2
V <sub>CCI</sub> B6	AK3
V <sub>CCI</sub> B6	AK4
V <sub>CCI</sub> B6	V12
V <sub>CCI</sub> B6	W12
V <sub>CCI</sub> B6	Y12
V <sub>CCI</sub> B7	E1
V <sub>CCI</sub> B7	E2
V <sub>CCI</sub> B7	E3
V <sub>CCI</sub> B7	E4
V <sub>CCI</sub> B7	M11
V <sub>CCI</sub> B7	N11
V <sub>CCI</sub> B7	N12
V <sub>CCI</sub> B7	P11
V <sub>CCI</sub> B7	P12
V <sub>CCI</sub> B7	R12
V <sub>CCI</sub> B7	T12
V <sub>CCI</sub> B7	U12

## 1152-Pin FBGA

AX2000 Function	Pin Number
V <sub>COMPLA</sub>	H16
V <sub>COMPLB</sub>	L17
V <sub>COMPLC</sub>	H19
V <sub>COMPLD</sub>	K18
V <sub>COMPLE</sub>	AH19
V <sub>COMPLF</sub>	AF18
V <sub>COMPLG</sub>	AH16
V <sub>COMPLH</sub>	AD17
V <sub>PUMP</sub>	J26

# Package Pin Assignments (Continued)

## 729-Pin PBGA (Bottom View)



## 729-Pin PBGA

AX1000 Function	Pin Number
<b>Bank 0 - Block 0</b>	
IO00NB0F0	E6
IO00PB0F0	F6
IO01NB0F0	G8
IO01PB0F0	G7
IO02NB0F0	D7
IO02PB0F0	E7
IO03NB0F0	D5
IO03PB0F0	E5
IO04NB0F0	G9
IO04PB0F0	H9
IO05NB0F0	E8
IO05PB0F0	F8
IO06NB0F0	C6
IO06PB0F0	D6
IO07NB0F0	B5
IO07PB0F0	C5
IO08NB0F0	A6
IO08PB0F0	A5
IO09NB0F0	E9
IO09PB0F0	F9
IO10NB0F0	G10
IO10PB0F0	H10
IO11NB0F0	B7
IO11PB0F0	B6
<b>Bank 0 - Block 1</b>	
IO12NB0F1	C8
IO12PB0F1	C7
IO13NB0F1	E10
IO13PB0F1	F10
IO14NB0F1	G11
IO14PB0F1	H11
IO15NB0F1	D9
IO15PB0F1	D8
IO16NB0F1	A8
IO16PB0F1	A7
IO17NB0F1	B9
IO17PB0F1	B8
IO18NB0F1	C10
IO18PB0F1	C9
IO19NB0F1	E11
IO19PB0F1	F11

## 729-Pin PBGA

AX1000 Function	Pin Number
IO20NB0F1	G12
IO20PB0F1	H12
IO21NB0F1	D11
IO21PB0F1	D10
<b>Bank 0 - Block 2</b>	
IO22NB0F2	A10
IO22PB0F2	A9
IO23NB0F2	B11
IO23PB0F2	B10
IO24NB0F2	G13
IO24PB0F2	H13
IO25NB0F2	C12
IO25PB0F2	C11
IO26NB0F2	E12
IO26PB0F2	D12
IO27NB0F2	E13
IO27PB0F2	F13
IO28NB0F2	G14
IO28PB0F2	H14
IO29NB0F2	A12
IO29PB0F2	B12
IO30NB0F2/HCLKAN	C13
IO30PB0F2/HCLKAP	D13
IO31NB0F2/HCLKBN	F14
IO31PB0F2/HCLKBP	E14
<b>Bank 1 - Block 3</b>	
IO32NB1F3/HCLKCN	C14
IO32PB1F3/HCLKCP	B14
IO33NB1F3/HCLKDN	D16
IO33PB1F3/HCLKDP	D15
IO34NB1F3	B16
IO34PB1F3	A16
IO35NB1F3	E15
IO35PB1F3	F15
IO36NB1F3	H15
IO36PB1F3	G15
IO37NB1F3	C17
IO37PB1F3	C16
IO38NB1F3	B18
IO38PB1F3	B17
IO39NB1F3	A18
IO39PB1F3	A17

## 729-Pin PBGA

AX1000 Function	Pin Number
IO40NB1F3	H16
IO40PB1F3	G16
<b>Bank 1 - Block 4</b>	
IO41NB1F4	B19
IO41PB1F4	A19
IO42NB1F4	C19
IO42PB1F4	C18
IO43NB1F4	D18
IO43PB1F4	D17
IO44NB1F4	H17
IO44PB1F4	G17
IO45NB1F4	F17
IO45PB1F4	E17
IO46NB1F4	B20
IO46PB1F4	A20
IO47NB1F4	C21
IO47PB1F4	C20
IO48NB1F4	H18
IO48PB1F4	G18
IO49NB1F4	F18
IO49PB1F4	E18
IO50NB1F4	D20
IO50PB1F4	D19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	B22
IO52PB1F4	B21
IO53NB1F4	F19
IO53PB1F4	E19
<b>Bank 1 - Block 5</b>	
IO54NB1F5	F20
IO54PB1F5	E20
IO55NB1F5	E21
IO55PB1F5	D21
IO56NB1F5	H19
IO56PB1F5	G19
IO57NB1F5	D22
IO57PB1F5	C22
IO58NB1F5	B23
IO58PB1F5	A23
IO59NB1F5	D23
IO59PB1F5	C23

## 729-Pin PBGA

AX1000 Function	Pin Number
IO60NB1F5	G21
IO60PB1F5	G20
IO61NB1F5	E23
IO61PB1F5	E22
IO62NB1F5	F22
IO62PB1F5	F21
IO63NB1F5	H20
IO63PB1F5	J19
<b>Bank 2 - Block 6</b>	
IO64NB2F6	J21
IO64PB2F6	H21
IO65NB2F6	F24
IO65PB2F6	F23
IO66NB2F6	F26
IO66PB2F6	F25
IO67NB2F6	E26
IO67PB2F6	E25
IO68NB2F6	J22
IO68PB2F6	H22
IO69NB2F6	G24
IO69PB2F6	G23
IO70NB2F6	K20
IO70PB2F6	J20
IO71NB2F6	G26
IO71PB2F6	G25
IO72NB2F6	J24
IO72PB2F6	J23
IO73NB2F6	H24
IO73PB2F6	H23
<b>Bank 2 - Block 7</b>	
IO74NB2F7	L21
IO74PB2F7	K21
IO75NB2F7	G27
IO75PB2F7	F27
IO76NB2F7	K23
IO76PB2F7	K22
IO77NB2F7	H26
IO77PB2F7	H25
IO78NB2F7	K25
IO78PB2F7	K24
IO79NB2F7	J26
IO79PB2F7	J25

## 729-Pin PBGA

AX1000 Function	Pin Number
IO80NB2F7	M20
IO80PB2F7	L20
IO81NB2F7	J27
IO81PB2F7	H27
IO82NB2F7	L23
IO82PB2F7	L22
IO83NB2F7	L25
IO83PB2F7	L24
IO84NB2F7	N21
IO84PB2F7	M21
<b>Bank 2 - Block 8</b>	
IO85NB2F8	K27
IO85PB2F8	K26
IO86NB2F8	M23
IO86PB2F8	M22
IO87NB2F8	M25
IO87PB2F8	M24
IO88NB2F8	L27
IO88PB2F8	L26
IO89NB2F8	M27
IO89PB2F8	M26
IO90NB2F8	N23
IO90PB2F8	N22
IO91NB2F8	N25
IO91PB2F8	N24
IO92NB2F8	N27
IO92PB2F8	N26
IO93NB2F8	P26
IO93PB2F8	P27
IO94NB2F8	N19
IO94PB2F8	N20
IO95NB2F8	P23
IO95PB2F8	P22
<b>Bank 3 - Block 9</b>	
IO96NB3F9	P25
IO96PB3F9	P24
IO97NB3F9	R26
IO97PB3F9	R27
IO98NB3F9	P21
IO98PB3F9	P20
IO99NB3F9	R24
IO99PB3F9	R25

## 729-Pin PBGA

AX1000 Function	Pin Number
IO100NB3F9	T26
IO100PB3F9	T27
IO101NB3F9	T24
IO101PB3F9	T25
IO102NB3F9	R20
IO102PB3F9	R21
IO103NB3F9	R23
IO103PB3F9	R22
IO104NB3F9	U26
IO104PB3F9	U27
IO105NB3F9	U24
IO105PB3F9	U25
IO106NB3F9	R19
IO106PB3F9	P19
<b>Bank 3 - Block 10</b>	
IO107NB3F10	V26
IO107PB3F10	V27
IO108NB3F10	T23
IO108PB3F10	T22
IO109NB3F10	V24
IO109PB3F10	V25
IO110NB3F10	T20
IO110PB3F10	T21
IO111NB3F10	W26
IO111PB3F10	W27
IO112NB3F10	U22
IO112PB3F10	U23
IO113NB3F10	Y26
IO113PB3F10	Y27
IO114NB3F10	U20
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	W25
IO116NB3F10	V22
IO116PB3F10	V23
IO117NB3F10	Y24
IO117PB3F10	Y25
<b>Bank 3 - Block 11</b>	
IO118NB3F11	V20
IO118PB3F11	V21
IO119NB3F11	AA26
IO119PB3F11	AA27

## 729-Pin PBGA

AX1000 Function	Pin Number
IO120NB3F11	W22
IO120PB3F11	W23
IO121NB3F11	AA24
IO121PB3F11	AA25
IO122NB3F11	W20
IO122PB3F11	W21
IO123NB3F11	AB26
IO123PB3F11	AB27
IO124NB3F11	Y22
IO124PB3F11	Y23
IO125NB3F11	AB24
IO125PB3F11	AB25
IO126NB3F11	AA22
IO126PB3F11	AA23
IO127NB3F11	AC26
IO127PB3F11	AC27
IO128NB3F11	Y20
IO128PB3F11	W19
<b>Bank 4 - Block 12</b>	
IO129NB4F12	AA20
IO129PB4F12	Y21
IO130NB4F12	AB22
IO130PB4F12	AB23
IO131NB4F12	AC22
IO131PB4F12	AC23
IO132NB4F12	AD23
IO132PB4F12	AD24
IO133NB4F12	AF23
IO133PB4F12	AE23
IO134NB4F12	AC21
IO134PB4F12	AB21
IO135NB4F12	AC20
IO135PB4F12	AB20
IO136NB4F12	AD21
IO136PB4F12	AD22
IO137NB4F12	Y19
IO137PB4F12	AA19
IO138NB4F12	AE21
IO138PB4F12	AE22
<b>Bank 4 - Block 13</b>	
IO139NB4F13	AF21
IO139PB4F13	AF22

## 729-Pin PBGA

AX1000 Function	Pin Number
IO140NB4F13	AG22
IO140PB4F13	AG23
IO141NB4F13	Y18
IO141PB4F13	AA18
IO142NB4F13	AE20
IO142PB4F13	AD20
IO143NB4F13	AG20
IO143PB4F13	AG21
IO144NB4F13	AC19
IO144PB4F13	AB19
IO145NB4F13	AD18
IO145PB4F13	AD19
IO146NB4F13	AC18
IO146PB4F13	AB18
IO147NB4F13	Y17
IO147PB4F13	AA17
IO148NB4F13	AF19
IO148PB4F13	AF20
IO149NB4F13	AC17
IO149PB4F13	AB17
IO150NB4F13	AE18
IO150PB4F13	AE19
IO151NB4F13	AA16
IO151PB4F13	Y16
<b>Bank 4 - Block 14</b>	
IO152NB4F14	AG18
IO152PB4F14	AG19
IO153NB4F14	AC16
IO153PB4F14	AB16
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AB15
IO155PB4F14	AC15
IO156NB4F14	AE16
IO156PB4F14	AE17
IO157NB4F14	Y15
IO157PB4F14	AA15
IO158NB4F14	AG16
IO158PB4F14	AG17
IO159NB4F14/CLKEN	AF15
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AD14

## 729-Pin PBGA

AX1000 Function	Pin Number
IO160PB4F14/CLKFP	AD15
<b>Bank 5 - Block 15</b>	
IO161NB5F15/CLKGN	AE14
IO161PB5F15/CLKGP	AE15
IO162NB5F15/CLKHN	AC13
IO162PB5F15/CLKHP	AD13
IO163NB5F15	Y14
IO163PB5F15	AA14
IO164NB5F15	AE13
IO164PB5F15	AF13
IO165NB5F15	AF12
IO165PB5F15	AG12
IO166NB5F15	AD12
IO166PB5F15	AE12
IO167NB5F15	Y13
IO167PB5F15	AA13
IO168NB5F15	AD11
IO168PB5F15	AE11
IO169NB5F15	AG11
IO169PB5F15	AF11
IO170NB5F15	AB11
IO170PB5F15	AC11
<b>Bank 5 - Block 16</b>	
IO171NB5F16	AF10
IO171PB5F16	AG10
IO172NB5F16	AD10
IO172PB5F16	AE10
IO173NB5F16	Y12
IO173PB5F16	AA12
IO174NB5F16	AB10
IO174PB5F16	AC10
IO175NB5F16	AF9
IO175PB5F16	AG9
IO176NB5F16	AD9
IO176PB5F16	AE9
IO177NB5F16	Y11
IO177PB5F16	AA11
IO178NB5F16	AF8
IO178PB5F16	AG8
IO179NB5F16	AD8
IO179PB5F16	AE8
IO180NB5F16	AB9

## 729-Pin PBGA

AX1000 Function	Pin Number
IO180PB5F16	AC9
<b>Bank 5 - Block 17</b>	
IO181NB5F17	Y10
IO181PB5F17	AA10
IO182NB5F17	AF7
IO182PB5F17	AG7
IO183NB5F17	AD7
IO183PB5F17	AE7
IO184NB5F17	AC7
IO184PB5F17	AC8
IO185NB5F17	AF6
IO185PB5F17	AG6
IO186NB5F17	AB7
IO186PB5F17	AB8
IO187NB5F17	Y9
IO187PB5F17	AA9
IO188NB5F17	AD6
IO188PB5F17	AE6
IO189NB5F17	AB6
IO189PB5F17	AC6
IO190NB5F17	AF5
IO190PB5F17	AG5
IO191NB5F17	AA6
IO191PB5F17	AA7
IO192NB5F17	Y8
IO192PB5F17	AA8
<b>Bank 6 - Block 18</b>	
IO193NB6F18	W8
IO193PB6F18	Y7
IO194NB6F18	AB5
IO194PB6F18	AC5
IO195NB6F18	AC2
IO195PB6F18	AC3
IO196NB6F18	AC4
IO196PB6F18	AD4
IO197NB6F18	Y5
IO197PB6F18	Y6
IO198NB6F18	AB3
IO198PB6F18	AB4
IO199NB6F18	V7
IO199PB6F18	W7
IO200NB6F18	AA4

## 729-Pin PBGA

AX1000 Function	Pin Number
IO200PB6F18	AA5
IO201NB6F18	W5
IO201PB6F18	W6
IO202NB6F18	AB1
IO202PB6F18	AC1
<b>Bank 6 - Block 19</b>	
IO203NB6F19	Y3
IO203PB6F19	AA3
IO204NB6F19	AA2
IO204PB6F19	AB2
IO205NB6F19	U8
IO205PB6F19	V8
IO206NB6F19	V5
IO206PB6F19	V6
IO207NB6F19	Y1
IO207PB6F19	AA1
IO208NB6F19	W4
IO208PB6F19	Y4
IO209NB6F19	T7
IO209PB6F19	U7
IO210NB6F19	W2
IO210PB6F19	Y2
IO211NB6F19	U5
IO211PB6F19	U6
IO212NB6F19	V3
IO212PB6F19	W3
IO213NB6F19	R9
IO213PB6F19	T8
<b>Bank 6 - Block 20</b>	
IO214NB6F20	U4
IO214PB6F20	V4
IO215NB6F20	T5
IO215PB6F20	T6
IO216NB6F20	V1
IO216PB6F20	W1
IO217NB6F20	R7
IO217PB6F20	R8
IO218NB6F20	U2
IO218PB6F20	V2
IO219NB6F20	T1
IO219PB6F20	U1
IO220NB6F20	R5

## 729-Pin PBGA

AX1000 Function	Pin Number
IO220PB6F20	R6
IO221NB6F20	T3
IO221PB6F20	T4
IO222NB6F20	R2
IO222PB6F20	T2
IO223NB6F20	P8
IO223PB6F20	P9
IO224NB6F20	R3
IO224PB6F20	R4
<b>Bank 7 - Block 21</b>	
IO225NB7F21	P1
IO225PB7F21	R1
IO226NB7F21	P3
IO226PB7F21	P2
IO227NB7F21	N7
IO227PB7F21	P7
IO228NB7F21	P5
IO228PB7F21	P4
IO229NB7F21	N2
IO229PB7F21	N1
IO230NB7F21	N6
IO230PB7F21	P6
IO231NB7F21	N9
IO231PB7F21	N8
IO232NB7F21	N4
IO232PB7F21	N3
IO233NB7F21	M2
IO233PB7F21	M1
IO234NB7F21	M4
IO234PB7F21	M3
IO235NB7F21	M5
IO235PB7F21	N5
<b>Bank 7 - Block 22</b>	
IO236NB7F22	L2
IO236PB7F22	L1
IO237NB7F22	L4
IO237PB7F22	L3
IO238NB7F22	L6
IO238PB7F22	M6
IO239NB7F22	M8
IO239PB7F22	M7
IO240NB7F22	K2



## 729-Pin PBGA

AX1000 Function	Pin Number
IO240PB7F22	K1
IO241NB7F22	K4
IO241PB7F22	K3
IO242NB7F22	K5
IO242PB7F22	L5
IO243NB7F22	J2
IO243PB7F22	J1
IO244NB7F22	J4
IO244PB7F22	J3
IO245NB7F22	H2
IO245PB7F22	H1
IO246NB7F22	H4
IO246PB7F22	H3
<b>Bank 7 - Block 23</b>	
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	J6
IO248PB7F23	K6
IO249NB7F23	H5
IO249PB7F23	J5
IO250NB7F23	G2
IO250PB7F23	G1
IO251NB7F23	K8
IO251PB7F23	K7
IO252NB7F23	G4
IO252PB7F23	G3
IO253NB7F23	F2
IO253PB7F23	F1
IO254NB7F23	G6
IO254PB7F23	H6
IO255NB7F23	F5
IO255PB7F23	G5
IO256NB7F23	F3
IO256PB7F23	F4
IO257NB7F23	H7
IO257PB7F23	J7
<b>Dedicated I/O</b>	
GND	A1
GND	A2
GND	A25
GND	A26
GND	A27

## 729-Pin PBGA

AX1000 Function	Pin Number
GND	A3
GND	AC24
GND	AE1
GND	AE2
GND	AE25
GND	AE26
GND	AE27
GND	AE3
GND	AE5
GND	AF1
GND	AF2
GND	AF25
GND	AF26
GND	AF27
GND	AF3
GND	AG1
GND	AG2
GND	AG25
GND	AG26
GND	AG27
GND	AG3
GND	B1
GND	B2
GND	B25
GND	B26
GND	B27
GND	B3
GND	C1
GND	C2
GND	C25
GND	C26
GND	C27
GND	C3
GND	E27
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M11

## 729-Pin PBGA

AX1000 Function	Pin Number
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
LP	J8

## 729-Pin PBGA

AX1000 Function	Pin Number
NC	U3
PRA	J14
PRB	D14
PRC	V14
PRD	AB14
TCK	E4
TDI	D4
TDO	J9
TMS	H8
TRST	E3
V <sub>CCA</sub>	AA21
V <sub>CCA</sub>	AD5
V <sub>CCA</sub>	E1
V <sub>CCA</sub>	G22
V <sub>CCA</sub>	K10
V <sub>CCA</sub>	K11
V <sub>CCA</sub>	K17
V <sub>CCA</sub>	K18
V <sub>CCA</sub>	L10
V <sub>CCA</sub>	L18
V <sub>CCA</sub>	U10
V <sub>CCA</sub>	U18
V <sub>CCA</sub>	V10
V <sub>CCA</sub>	V11
V <sub>CCA</sub>	V17
V <sub>CCA</sub>	V18
V <sub>CCPLA</sub>	A13
V <sub>CCPLB</sub>	J13
V <sub>CCPLC</sub>	B15
V <sub>CCPLD</sub>	C15
V <sub>CCPLE</sub>	AG14
V <sub>CCPLF</sub>	AF14
V <sub>CCPLG</sub>	AB13
V <sub>CCPLH</sub>	AG13
V <sub>CCDA</sub>	A11
V <sub>CCDA</sub>	AB12
V <sub>CCDA</sub>	AC12
V <sub>CCDA</sub>	AC25
V <sub>CCDA</sub>	AD16
V <sub>CCDA</sub>	AD17
V <sub>CCDA</sub>	E16
V <sub>CCDA</sub>	E2

## 729-Pin PBGA

AX1000 Function	Pin Number
V <sub>CCDA</sub>	E24
V <sub>CCDA</sub>	F12
V <sub>CCDA</sub>	F16
V <sub>CCDA</sub>	F7
V <sub>CCDA</sub>	K14
V <sub>CCDA</sub>	P10
V <sub>CCDA</sub>	P18
V <sub>CCDA</sub>	W14
V <sub>CCDA</sub>	W9
V <sub>CCIB0</sub>	A4
V <sub>CCIB0</sub>	B4
V <sub>CCIB0</sub>	C4
V <sub>CCIB0</sub>	J10
V <sub>CCIB0</sub>	J11
V <sub>CCIB0</sub>	J12
V <sub>CCIB0</sub>	K12
V <sub>CCIB0</sub>	K13
V <sub>CCIB1</sub>	A24
V <sub>CCIB1</sub>	B24
V <sub>CCIB1</sub>	C24
V <sub>CCIB1</sub>	J16
V <sub>CCIB1</sub>	J17
V <sub>CCIB1</sub>	J18
V <sub>CCIB1</sub>	K15
V <sub>CCIB1</sub>	K16
V <sub>CCIB2</sub>	D25
V <sub>CCIB2</sub>	D26
V <sub>CCIB2</sub>	D27
V <sub>CCIB2</sub>	K19
V <sub>CCIB2</sub>	L19
V <sub>CCIB2</sub>	M18
V <sub>CCIB2</sub>	M19
V <sub>CCIB2</sub>	N18
V <sub>CCIB3</sub>	AD25
V <sub>CCIB3</sub>	AD26
V <sub>CCIB3</sub>	AD27
V <sub>CCIB3</sub>	R18
V <sub>CCIB3</sub>	T18
V <sub>CCIB3</sub>	T19
V <sub>CCIB3</sub>	U19
V <sub>CCIB3</sub>	V19
V <sub>CCIB4</sub>	AE24

## 729-Pin PBGA

AX1000 Function	Pin Number
V <sub>CCIB4</sub>	AF24
V <sub>CCIB4</sub>	AG24
V <sub>CCIB4</sub>	V15
V <sub>CCIB4</sub>	V16
V <sub>CCIB4</sub>	W16
V <sub>CCIB4</sub>	W17
V <sub>CCIB4</sub>	W18
V <sub>CCIB5</sub>	AE4
V <sub>CCIB5</sub>	AF4
V <sub>CCIB5</sub>	AG4
V <sub>CCIB5</sub>	V12
V <sub>CCIB5</sub>	V13
V <sub>CCIB5</sub>	W10
V <sub>CCIB5</sub>	W11
V <sub>CCIB5</sub>	W12
V <sub>CCIB6</sub>	AD1
V <sub>CCIB6</sub>	AD2
V <sub>CCIB6</sub>	AD3
V <sub>CCIB6</sub>	R10
V <sub>CCIB6</sub>	T10
V <sub>CCIB6</sub>	T9
V <sub>CCIB6</sub>	U9
V <sub>CCIB6</sub>	V9
V <sub>CCIB7</sub>	D1
V <sub>CCIB7</sub>	D2
V <sub>CCIB7</sub>	D3
V <sub>CCIB7</sub>	K9
V <sub>CCIB7</sub>	L9
V <sub>CCIB7</sub>	M10
V <sub>CCIB7</sub>	M9
V <sub>CCIB7</sub>	N10
V <sub>COMPLA</sub>	B13
V <sub>COMPLB</sub>	A14
V <sub>COMPLC</sub>	A15
V <sub>COMPLD</sub>	J15
V <sub>COMPLE</sub>	AG15
V <sub>COMPLF</sub>	W15
V <sub>COMPLG</sub>	AC14
V <sub>COMPLH</sub>	W13
V <sub>PUMP</sub>	D24

## List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (Advanced v1.5)	Page
Advanced v1.4	"Standby Power" table on page 14 was updated.	page 14
	The figure in the "I/O Specifications" section on page 18 was updated.	page 18
	Figure 35 on page 70 was updated.	page 70
	The "Timing Waveforms" figure on page 77 was updated.	page 77
Advanced v1.3	In the "208-Pin PQFP" table on page 114, pin 196 was missing, but it has been added in this version with a function of GND.	page 114
	The following pins in the "484-Pin FBGA" table on page 128 for AX500 have changed. Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC.	page 128
	The "676-Pin FBGA" table on page 133, has been updated.	page 133
Advanced v1.2	The "Device Resources" table on page 2 was updated for the CS180.	page 2
	The "Programmable Interconnect Element" section on page 3 and Figure 2 on page 4 are new.	page 3 and page 4
	The "180-Pin CSP" table on page 111 is new	page 111
	The "208-Pin PQFP" table on page 116 for the AX500 has been updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136	page 116
Advanced v1.1	The "Axcelerator Family Product Profile" table on page 1 was updated.	page 1
	The Ordering Information Table, Product Plan Table, and "Device Resources" table on page 2 were updated.	page 2
	Figure 3 on page 5 was updated.	page 5
	The "Design Environment" section on page 10 was updated.	page 10
	Figure 10 on page 11 is new.	page 11
	The "Standby Power" table on page 14 was updated.	page 14
	The "Package Thermal Characteristics" table on page 17 was updated.	page 17
	The figure on page 18 was updated.	page 18
	Table 5 on page 21 was updated.	page 21
	The "Timing Model" figure on page 27 was updated.	page 27
	The Timing Characteristics tables from page 32 to page 64 were updated.	page 32 to page 64
	The "Global Resource Distribution" section on page 65 was updated.	page 65
	The Timing Characteristics tables from page 89 to page 105 were updated.	page 89 to page 105
	The "208-Pin PQFP" tables on page 114 are new.	page 114
The "256-Pin FBGA" table on page 119 are new.	page 119	
The "324-Pin FBGA" section on page 123 is new.	page 123	

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Web-only." The definition of these categories are as follows:

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The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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<http://www.actel.com>

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** (408) 739-1010

**Fax:** (408) 739-1540

**Actel Europe Ltd.**

Dunlop House, Riverside Way  
Camberley, Surrey GU15 3YL  
United Kingdom

**Tel:** +44 (0)1276 401450

**Fax:** +44 (0)1276 401490

**Actel Japan**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Tel:** +81 03-3445-7671

**Fax:** +81 03-3445-7668

**Actel Hong Kong**

39th Floor  
One Pacific Place  
88 Queensway  
Admiralty, Hong Kong  
Tel: 852-22735712