FLEXTRONICS
Semiconductor

# 0.35µ Gate Arrays

## Description

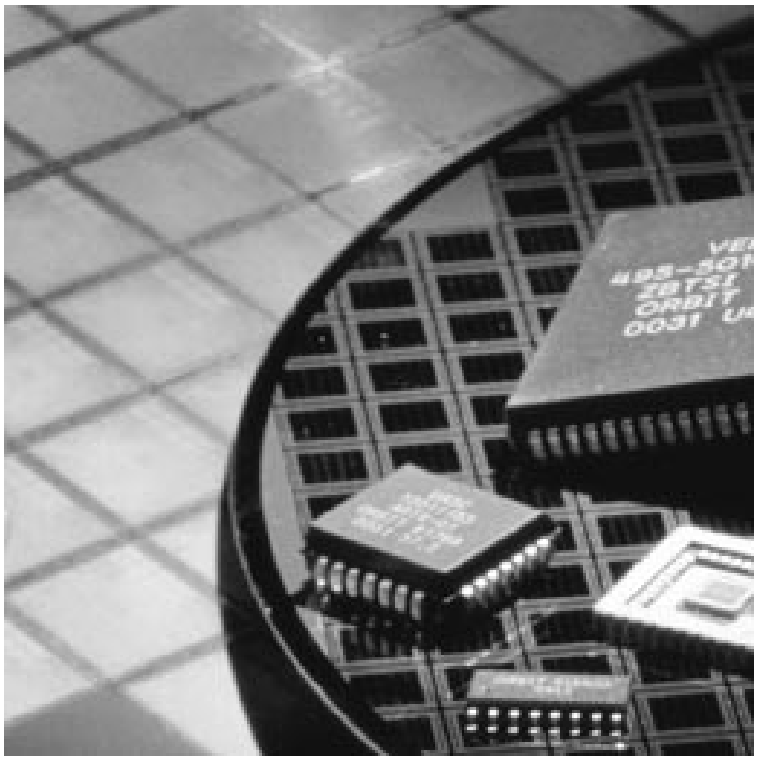
Flextronics Semiconductor's 0.35µ family of gate arrays provides retargeting solutions for FPGA and Gate Array conversions.

The Encore!*Plus* program is a retargeting service featuring direct replacement of FPGAs, PLDs, and ASICs, including other Gate Arrays, using Flextronics Semiconductor's 0.35µ Gate Array technology. In most cases no new tools are required to take advantage of this service. Encore!*Plus* offers low-NRE, fast-turnaround cycle times and flexible manufacturing.

Flextronics Semiconductor's gate arrays use a sea-of-gates architecture with a novel gate design which allows high utilization while minimizing the effect of interconnect capacitance on circuit performance. Since gate arrays are personalized with the last few processing masks, a fast response time to customer orders can be made, allowing the customer more options in circuit definition.

These gate arrays offer significant flexibility in pin definition. Contrary to designing with FPGAs, the customer can define any pin to be any signal function or power supply. The Encore!*Plus* program allows customers to redefine any pin's electrical parameters. Customers may select their choice of pin characteristics, such as output drive levels, slew rate control, different input switching points and hysteresis.

All prototypes are not only fully tested prior to shipment, but are assembled in the production package on the production line. This allows the customer to use prototypes as if they were production parts.



## Features

- **Five array sizes:**
  24,000 to 2M gates
  68 to 680 pads
- **3.3 volt operation**
- **Flexible pin assignments**
- **Conversion from FPGAs, PLDs, and ASICs, (including other gate arrays)**
- **Low power dissipation**
- **High gate utilization**
- **Sea-of-Gates architecture**
- **Functional logic equivalent guaranteed**

## Flextronics Semiconductor's 0.35µ Gate Array Family

The 0.35µ gate array family currently consists of five arrays, and new arrays can be added as the need arises. **Table 1** provides examples of the current arrays, their size and the number of pins.

These gate arrays have been designed with a maximum number of power and I/O pads. This allows Flextronics Semiconductor to offer the most cost-effective array size, especially in those cases where the design is limited by the number of I/O connections, rather than by the number of gates.

### Table 1. Flextronics Semiconductor's 0.35µ Gate Arrays

| Name | Gates | Typ. Used Gates[1] | # of Pins |
|---|---|---|---|
| Base_68 | 29,900 | 24,000 | 68 |
| Base_100 | 66,300 | 53,000 | 100 |
| Base_208 | 318,000 | 160,000 | 208 |
| Base_320 | 524,000 | 420,000 | 320 |
| Base_680 | 2,400,000 | 2,000,000 | 680 |

*Note: 1. Actual gate utilization is design-dependent.*

## Pin Assignment

Flextronics Semiconductor's gate arrays have been designed so that any pin may be assigned any input/output (I/O) function, including power and ground. This flexibility allows gate arrays to match any existing pinout, creating an exact replacement for either FPGAs, PLDs, or ASICs, (including gate arrays).

The internal power supply busses are designed to prevent any output switching transients from affecting the internal logic.

## I/O Capability

The gate array family I/O buffers are designed so that only the guard-banded, output drive transistors and the pull-up/pull-down transistors are dedicated to a specific pin. All of the output control logic and the input level translators are built from internal array transistors. Since these internal transistors are not dedicated to a specific buffer, a number of different I/O functions may be created.

Input buffers may be designed to work with either CMOS or TTL levels. In either case, a Schmitt trigger can be added, and there is also an optional pull-up or pull-down resistor.

Outputs vary by strength. Output strengths from 2 mA to 24 mA may be specified individually for each pin. Higher currents may be obtained by paralleling I/O pads.

The control logic for the outputs allows an output to be continuous, tristate or open-drain. Slew rate control is added on all outputs whose strength is in excess of 8 mA. Flextronics Semiconductor's gate array family also supports open-drain outputs with a dynamic precharge for extra system speed.

Any output may be combined with any input to create a bi-directional I/O buffer with a choice of characteristics.

## Power Pins

Flextronics Semiconductor's gate arrays have been designed to act as a replacement for many existing gate arrays and FPGAs. This means that the internal power busses are designed to be strong enough to support other vendors' rules on the number of supply pins necessary to support a given number and strength of outputs.

For new designs, the number of power pins required is a trade-off between the number of pins available and the ability of the PC board to provide a clean, low-inductance supply.

Flextronics Semiconductor can skew simultaneous switching outputs upon request. We also add slew rate controls to all high-power outputs to minimize the peak currents associated with output switching.

Flextronics Semiconductor recommends replacing some or all no-connect pins with supply pins, as a means of increasing the amount of margin within the design.

## Special Requests

Flextronics Semiconductor's gate arrays are made up of uncommitted transistors, and there are no arbitrary limits as to how these transistors may be used. We will create specific functions upon request.

Flextronics Semiconductor can provide circuitry to support PCI, JTAG, crystal oscillators, RC oscillators, current mirrors, etc. and the libraries include a variety of synthesizable cores.

## Design Conversions

For netlist conversions, Flextronics Semiconductor supports multiple formats and industry-standard tools.

To convert a customer's design, Flextronics Semiconductor needs a netlist of the circuit, vectors and a pinout. Additional information, such as the timing of a critical path, may be supplied if such a path needs additional evaluation.

## Netlists

A netlist defines the logic to be implemented in the gate array. While most gate-level formats are acceptable to the Encore!*Plus* program, the netlist must be in ASCII format. Most binary netlists are proprietary and undocumented, which prevents Flextronics Semiconductor from translating them. Examples of acceptable netlist formats include:

| | |
|---|---|
| XNF | (Xilinx) |
| EDIF | (Altera, others) |
| ADL | (Actel) |
| LDL | (LSI Logic) |
| TDL | (Toshiba) |
| QDF | (QuickLogic) |
| Wire File | (ViewLogic) |

## Simulations

Flextronics Semiconductor prefers simulations at 1 MHz are supplied by the customer. In the event that simulations are not available, assistance in the development of simulation vectors can be provided.

Flextronics Semiconductor provides a service to enhance test vectors using methods such as ATPG and SCAN.

Flextronics Semiconductor uses the customer's vectors to confirm that the design has been correctly converted into the Flextronics Semiconductor format, and to develop the production test vectors.

Using low-speed simulations makes it easier to verify the functionality of the logic. High-speed simulations, particularly with FPGAs, often produce vectors with signals which take more than one clock cycle to propagate to the output. Such vectors make it difficult to verify a correct design conversion. Flextronics Semiconductor will evaluate and confirm higher speed simulations upon request.

The preferred format for simulations is to show every signal pin in a table, with the simulation output in a "Print-On-Change" format. This supplies significant information to Flextronics Semiconductor engineering about the expected device performance. **Table 2** shows a Print-on-Change format for an exclusive-OR (XOR) gate.

### Table 2. Print-On-Change Format (XOR)

| Time | A | B | O |
|---|---|---|---|
| 0 ns | 0 | 0 | 0 |
| 50 ns | 0 | 1 | 0 |
| 52 ns | 0 | 1 | 1 |
| 100 ns | 1 | 0 | 1 |
| 150 ns | 1 | 1 | 1 |
| 153 ns | 1 | 1 | 0 |

## Pin List

Flextronics Semiconductor requires a listing of pin numbers, pin names and the function and/or specifications for the input and output pins. This list should include any special characteristics that the pin must have, such as TTL-level input or open-drain output. The pin list also provides customers with a means to modify the I/O characteristics normally associated with FPGA netlists. The default is to use the I/Os specified by the original FPGA manufacturer. By referencing different specifications in the pin file, the customer can obtain any desired I/O characteristics. **Table 3** lists some typical pinout specifications

### Table 3. Pinout Specifications

| Pin | Name | Specification |
|---|---|---|
| 1 | CLK | Input - TTL |
| 2 | IOR | Input - TTL |
| 3 | IOW | Input - TTL |
| 4 | PS3 | Input - CMOS w/10K pull-up resistor |
| 5 | CS | Input - CMOS w/10K pull-up resistor |
| 6 | VDD | Supply |
| 7 | DATA0 | Bidirectional - 12 mA |
| 8 | VSS | Supply |
| 9 | RMS | Input - TTL |
| 10 | DATA1 | Bidirectional - 12 mA |
| 11 | — | No Connect |
| 12 | VSS | Supply |
| 13 | OSC#IN | Input - TTL |
| 14 | OSC#OUT | Output - 6 mA |
| 15 | OSCBUF | Output - 6 mA |
| 16 | VDD | Supply |

## Implementing Designs

Flextronics Semiconductor's approach is based on the concept of transferring a design implemented in a given technology to Flextronics Semiconductor gate arrays. We perform the conversion and execute a number of checks on the design.

Flextronics Semiconductor provides production-ready ASICs. Customers can design a true ASIC while benefiting from all FPGA advantages (quick turnaround of prototypes, fast time to market, low NRE, no volume commitment) without the associated penalties (high cost, routing, pin and footprint constraints, and limited package selections).

A customer can first synthesize the netlist into an FPGA to validate the design concept, then synthesize to Flextronics Semiconductor gates to obtain:

- Significantly lower cost
- No risk
- Access to arrays with up to 2.4M gates
- Low NRE and quick turns
- Access to analog cells

Flextronics Semiconductor will support customers with these application issues:

- Optimize synthesis results (smallest silicon area, best timing)
- HDL simulation
- Static Timing analysis (pre- and post-layout)
- Pin configuration (ground-bounce issues)

The Flextronics Semiconductor design engineer converts the customer's netlist into the Encore!*Plus* format. The procedure varies, depending upon the type and source of the netlist. Flextronics Semiconductor uses a collection of proprietary and commercially available translators.

An appropriate cross reference library is used to generate the converted netlist. This library reflects all the primitives used by the customer in terms of Flextronics Semiconductor primitives.

After the netlist has been converted, Flextronics Semiconductor runs a design analysis program which determines the size of the circuit and looks for loading violations. Any violations discovered are fixed by either increasing the strength of the signal driver or by buffering the signal.

Particular attention is paid to the clock structure. The preferred clock organization is a single clock which goes to all flip flops. In this case, Flextronics Semiconductor designs a special clock driver that is matched to the load.

Timing-driven layout automatically compensates for variations in loading and balances the clock tree. Clock skew is rechecked during the "five corner" simulation runs.

Our designer converts the simulation output into an input stimulus for Flextronics Semiconductor's internal simulator.

## Initial Verification

Using a typical library, the Flextronics Semiconductor design engineer runs a simulation on the converted netlist and compares the results to the customer-supplied simulation. Usually, the results match. If they do not, the engineer determines the reason and works with the customer for an acceptable solution. A common cause for mismatches is race conditions introduced during the conversion process.

## Design Checks

Once Flextronics Semiconductor has verified that the design has been correctly converted, a series of checks is done. Principal among these checks is a "five corner" simulation. This consists of a set of five simulation runs, each run with a different timing library. These libraries cover the traditional best, typical, and worst case conditions. They also cover the cases of best rise times combined with the worst fall times, and the worst rise times combined with the best fall times. These last two cases are especially severe, and will generally cause a circuit failure if there is any weakness in the design.

In each of these simulations, Flextronics Semiconductor checks the setup and hold times for every flop in the circuit.

## Flextronics Semiconductor's Gate Array Packaging

The small size of Flextronics Semiconductor's gate arrays allows considerable flexibility in choosing a package. This is particularly relevant when dealing with an FPGA conversion, in that the large FPGA die size frequently limits package availability.

As a general rule, any commercially available package may be used with the gate array family, subject only to the requirement that the gate array must fit in the package cavity.

The customer may select either the original package type or an alternate one. Frequently, FPGA conversions can be implemented in a smaller package which can present considerable savings, both in board space and in unit cost.

**Table 4** is a partial list of package styles which are supported by Flextronics Semiconductor. Please contact us for your packaging specification and for various lead-length options.

### Table 4. Commonly Used Packages

| Package [1] | Pins | Max. Base Size |
|---|---|---|
| PLCC | 28 | Base_100 |
| PLCC | 44 | Base_100 |
| PLCC | 68 | Base_100 |
| PLCC | 84 | Base_100 |
| QFP | 100 | Base_100 |
| QFP | 144 | Base_208 |
| QFP | 160 | Base_208 |
| QFP | 208 | Base_680 |
| QFP | 240 | Base_680 |
| BGA | 225 | Base_680 |
| BGA | 352 | Base_ 680 |
| BGA | 432 | Base_680 |
| BGA | 672 | Base_680 |

*Note: 1. These are examples of commonly used packages. Virtually any commercially available package may be used.*

## Marking

The default marking scheme uses five lines of 16 characters each. The first three are defined by the customer. The last two lines are Flextronics Semiconductor's part number and the date code, indicating when the packaging was done.

Parts may also be marked with customer-supplied graphics. For your particular needs, please consult the factory.

## Absolute Ratings

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | -0.3 to 4.0 | V |
| Input Voltage | $V_{IN}$ | $V_{DD}$ +0.3 | V |
| Input Current | $I_{IN}$ | 10 | µA |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | +3 to 3.6 | V |
| Operating Temperature[1] | | | |
| Commercial | $T_A$ | 0 to +70 | °C |
| Industrial | $T_A$ | -40 to +85 | °C |
| Junction Temperature | $T_J$ | <150 | °C |

*Note: 1. Ambient temperature.*

## DC Characteristics ($V_{DD}$ = +3 V ± 5%)

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Voltage Input LOW | CMOS | | 0.3 ($V_{DD}$) | V |
| | | TTL | | 0.8 | V |
| $V_{IH}$ | Voltage Input HIGH | CMOS | 0.7 ($V_{DD}$) | | V |
| | | TTL | 2.0 | | V |
| $I_{IN}$ | Input Current | CMOS $V_{IN}$ = $V_{SS}$, $V_{DD}$ | -10 | 10 | µA |
| | | TTL $V_{IN}$ = $V_{SS}$, $V_{DD}$ | -10 | 10 | µA |
| $V_{OH}$ | Voltage Output HIGH | $I_{OH}$ = Rated current | 2.4 | | V |
| $V_{OL}$ | Voltage Output LOW | $I_{OL}$ = Rated current | | 0.4 | V |
| $I_{OZ}$ | TriState Output Leakage | $V_{OH}$ = $V_{SS}$ or $V_{DD}$ | -10 | 10 | µA |



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