

0.18μ Standard Cell

Application

Flextronics Semiconductor's 0.18μ Standard Cell product suite offer designers the best optimization for performance, low power, and system cost. Applications benefiting from these features are telecom, networking, portable datacom, and consumer applications. The product suite is well equipped for design teams who intend to migrate from advanced FPGA to full system on chip ASIC as well as system architects who need to prototype with an ASIC. Production is "all about results" utilizing Flextronics manufacturing supply chain muscle to execute cycle-time and cost performance.

Description

Deep sub-micron CMOS silicon utilizing a 0.15μ effective gate length capable of up to 250 MHz operation and 21M logic gates.

Low power 1.8 volt core operation with 0.06 μW/gate/MHz power dissipation.

Dense, fast SRAM, ROM, and Multi-port Register File compilers and instances.

Low noise 3.3 v and 3.3 v / 5.0 v tolerant I/O library designed for minimum die size / performance utilizing staggered, in-line, and flip-chip configurations. Complete pad sets tested for 4000 volts ESD and 300 ma latchup.

Process	
Core Voltage	1.8 V
I/O Voltage	3.3 V operation 5.0 V tolerant
Poly/Metal Density	1P6M (90K gates/mm ²)
Power Dissipation	0.06 μW/gate/MHz

Features

Standard Cells	Over 500+ cell engineered for optimum synthesis and high routability.
I/O Functions	350+ CMOS/TTL functions with multiple drive strengths (2 ma to 24 ma) 3.3 v and 5 v tolerant with built in level shifters. The 5 v tolerant function requires no external bias pin.
Application Specific I/O	PCI, SSTL, HSTL, USB, LVDS Clock driver, crystal oscillator, analog input, power, ground, and spacer cells for SoC compatibility.
SRAM / 1P	Single port SRAM compiler is a high density, high performance solution for embedded applications. Six transistor bordered bit cells achieve reduced die area while maintaining low tooling (mask) cost. The compiler maintains multi-bank architecture with capacity up to 1 Mbit.
SRAM / DP	High density dual port SRAM compiler offers a high performance solution with the highest density for embedded memory applications. Eight transistor bordered bit cells achieve minimum die area while maintaining low tooling (mask) cost. The compiler maintains multi-bank architecture with capacity up to 1 Mbit.

Features (continued)	
SRAM / 2P	Register compiled high performance two port memory solution for embedded applications. Best solution for register files, buffer memories, fall-through FIFO, palette RAM, and tag RAM. Capacity to compile very wide words up to 144 bits for address matching and virtual address. Low overhead of decode-logic and sense amplifiers minimize required die area.
ROM	Read Only Memory compiler is a high density, fully diffused ROM solution targeted for embedded applications that require program store. The bit cells are optimized to offer very high density and low power. Configurations up to 1 Mbit are available. Metal programmable versions are also available on a custom basis.
PLL	Compiler based technology that allows system designers to choose the center frequency, duty cycle, and create a customized PLL. Fully modular and embedded in the I/O pad ring with no area overhead to the core – eliminates manual wiring of analog power supply or additional band-gaps / external components.
Frequency Synthesizer	Sophisticated frequency synthesizer targeted for applications such as pixel (dot clock) generation for use as a video master and non-integer clock multiplication for high-speed networking application. Cascaded PLL architecture for precision and phase jitter stability. Fully modular and embedded in the I/O pad ring with no area overhead to the core – eliminates manual wiring of analog power supply or additional band-gaps / external components.

Design Kit Support	
EDA views	Verilog views with best case and worse case timing and power data VHDL views with best case and worse case timing and power data Synopsys views with best case and worse case timing and power data
Data Books	Typical timing & power data sheet for each cell Logic Data Book (typical case:25degrees C/1.8V) Inline I/O Cell Data Book (typical case:25degrees C/3.3V) Staggered I/O Cell Data Book (typical case:25degrees C/3.3V)

Our design kits include a broad selection of embedded semiconductor intellectual property components including standard cell logic, standard I/O, specialty I/O interfaces, memory, and PLL options. System on chip options include embedded RISC processors, buss standards, connectivity standards, high speed serial I/O, cryptology, and applied FEC applications. Please contact us regarding your specific requirements.

OFFICES WORLDWIDE

NORTH AMERICA

169 West Java Drive
Sunnyvale, CA 94089
Phone: (408) 744 1800
Fax: (408) 747 1263

5 Revere Dr #200
Northbrook, IL 60062
Phone: (847) 509-5870
Fax: (847) 509-5872

100 Cummings Ctr., Suite 323A
Beverly, MA 01915
Phone: (978) 921 0131
Fax: (978) 922 6965

1093 Commerce Park Dr. Ste.300
Oak Ridge, TN 37830
Phone: (865) 482 4616
Fax: (865) 482 8939

ASIA-PACIFIC

13/F. Hale Weal Industrial Bldg.
22-28 Tai Chung Road
Tsuen Wan, **Hong Kong**
Phone: (+852) 2276 1335
Fax: (+852) 2429 2768

EUROPE

3-5 North Street
Leatherhead, Surrey
KT22 7AX **England**
Phone: (+44) 1 372 363 222
Fax: (+44) 1372 363 444

1 Lev-Pesach St.
Ofek 1 Bldg. North Industrial Park
Lod 71293 **Israel**
Phone: (+972) 8 927 5555
Fax: (+972) 8 927 5552

Postbus 135
5520 AC Eersel
The Netherlands
Phone: (+31) 497 550 351
Fax: (+31) 497 550 353

Fabrikorvagen 8, Box 1203
SE-131 27 Nacka Strand
Sweden
Phone: (+46) 8 601 3771
Fax: (+46) 8 601 3775

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